ne state network

get reg. net.

oup

left_A3 left_A4 left_B1 left_B2 left_B3 left_B4 left_Burn1 left_Burn2 left_Burn3 left_Burn4 left_C1 left_C2 left_C3 left_C4 left_C5 left_C6 left_D1 left_D2 left_D3 left_D4 left_D5 left_E1 left_E2 left_E3 left_E4 right_A1 right_A2 right_A3 right_A4 right_B1 right_B2 right_B3 right_B4 right_Burn1 right_Burn2 right_Burn3 right_Burn4 right_Burn5 right_C1 right_C2 right_C3 right_C4 right_C5 right_C6 right_C7 right_C8 right_D1 right_D2 right_D3 right_D4 right_D5 right_D6 right_E1 right_E2 right_E3 right_E4 right_E5 right_F1 right_F2 right_F3 right_F4 right_F5 right_F6 right_G1 right_G2 right_G3 right_G4 right_H1 right_H2 right_H3 right_H4 right_I1 right_I2 right_I3 right_I4 right_I5 right_I6 right_J1 right_J2 right_J3 right_J4 right_J5 right_K1 right_K2 right_K3 right_K4 right_L1 right_L2 right_L3 right_L4 right_L5 right_L6 right_L7 right_L8 right_M1 right_M2 right_M3 right_M4 right_M5 right_N1 right_N2 right_N3 right_N4 right_N5 right_N6 right_O1 right_O2 right_O3 right_O4 right_O5 right_O6 Target

time

B

1e+04

Backbone module reg. net.

name

A1 A2 A3 A4 A5 A6 A7 B1 B10 B2 B3 B4 B5 B6 B7 B8 B9 left_A1 left_A2 left_A3 left_A4 left_B1 left_B2 left_B3 left_B4 left_Burn1 left_Burn2 left_Burn3 left_Burn4 left_C1 left_C2 left_C3 left_C4 left_C5 left_C6 left_D1 left_D2 left_D3 left_D4 left_D5 left_E1 left_E2 left_E3 left_E4 right_A1 right_A2 right_A3 right_A4 right_B1 right_B2 right_B3 right_B4 right_Burn1 right_Burn2 right_Burn3 right_Burn4 right_Burn5 right_C1 right_C2 right_C3 right_C4 right_C5 right_C6 right_C7 right_C8 right_D1 right_D2 right_D3 right_D4 right_D5 right_D6 right_E1 right_E2 right_E3 right_E4 right_E5 right_F1 right_F2 right_F3 right_F4 right_F5 right_F6 right_G1 right_G2 right_G3 right_G4 right_H1 right_H2 right_H3 right_H4 right_I1 right_I2 right_I3 right_I4 right_I5 right_I6 right_J1 right_J2 right_J3 right_J4 right_J5 right_K1 right_K2 right_K3 right_K4 right_K5 right_L1 right_L2 right_L3 right_L4 right_L5 right_L6 right_L7 right_L8 right_M1 right_M2 right_M3 right_M4 right_M5 right_N1 right_N2 right_N3 right_N4 right_N5 right_N6 right_O1 right_O2 right_O3 right_O4 right_O5 right_O6

C

TRUE

TF reg. net.

Module group

A1 A2 A3 A4 A5 A6 A7 B1 B10 B2 B3 B4 B5 B6 B7 B8 B9 left_A1 left_A2 left_A3 left_A4 left_B1 left_B2 left_B3 left_B4 left_Burn1 left_Burn2 left_Burn3 left_Burn4 left_C1 left_C2 left_C3 left_C4 left_C5 left_C6 left_D1 left_D2 left_D3 left_D4 left_D5 left_E1 left_E2 left_E3 left_E4 right_A1 right_A2 right_A3 right_A4 right_B1 right_B2 right_B3 right_B4 right_Burn1 right_Burn2 right_Burn3 right_Burn4 right_Burn5 right_C1 right_C2 right_C3 right_C4 right_C5 right_C6 right_C7 right_C8 right_D1 right_D2 right_D3 right_D4 right_D5 right_D6 right_E1 right_E2 right_E3 right_E4 right_E5 right_F1 right_F2 right_F3 right_F4 right_F5 right_F6 right_G1 right_G2 right_G3 right_G4 right_H1 right_H2 right_H3 right_H4 right_I1 right_I2 right_I3 right_I4 right_I5

E

Gold + simulations

edge

left_sA_left_sB left_sB_left_sC left_sC_left_sD left_sC_left_sE left_sD_left_sEndD left_sE_left_sEndE right_sA_right_sB right_sB_right_sC right_sC_right_sD right_sC_right_sE right_sC_right_sF right_sD_right_sI right_sD_right_sJ right_sE_right_sEndE right_sF_right_sG right_sF_right_sH right_sG_right_sEndG right_sH_right_sEndH right_sI_right_sK right_sI_right_sL right_sJ_right_sEndJ right_sK_right_sEndK right_sL_right_sM right_sL_right_sN right_sL_right_sO right_sM_right_sEndM right_sN_right_sEndN right_sO_right_sEndO

0.50 0.25 0.00 −0.25 −0.50

comp_2

comp_1

F

Simulations to gold mapping

edge

left_sA−>left_sB left_sB−>left_sC left_sC−>left_sD left_sC−>left_sE left_sD−>left_sEndD left_sE−>left_sEndE right_sA−>right_sB right_sB−>right_sC right_sC−>right_sD right_sC−>right_sE right_sC−>right_sF right_sD−>right_sI right_sD−>right_sJ right_sE−>right_sEndE right_sF−>right_sG right_sF−>right_sH right_sG−>right_sEndG right_sH−>right_sEndH right_sI−>right_sK right_sI−>right_sL right_sJ−>right_sEndJ right_sK−>right_sEndK right_sL−>right_sM right_sL−>right_sN right_sL−>right_sO right_sM−>right_sEndM right_sN−>right_sEndN right_sO−>right_sEndO

0.50 0.25 0.00 −0.25 −0.50

comp_2

comp_1

H

Gold pre−mRNA expression over time

module_id

A1 A2 A3 A4 A5 A6 A7 B1 B10 B2 B3 B4 B5 B6 B7 B8 B9 left_A1 left_A2 left_A3 left_A4 left_B1 left_B2 left_B3 left_B4 left_Burn1 left_Burn2 left_Burn3 left_Burn4 left_C1 left_C2 left_C3 left_C4 left_C5 left_C6 left_D1 left_D2 left_D3 left_D4 left_D5 left_E1 left_E2 left_E3 left_E4 right_A1 right_A2 right_A3 right_A4 right_B1 right_B2 right_B3 right_B4 right_Burn1 right_Burn2 right_Burn3 right_Burn4 right_Burn5 right_C1 right_C2 right_C3 right_C4 right_C5 right_C6 right_C7 right_C8 right_D1 right_D2 right_D3 right_D4 right_D5 right_D6 right_E1 right_E2 right_E3 right_E4 right_E5 right_F1 right_F2 right_F3 right_F4 right_F5 right_F6 right_G1 right_G2 right_G3 right_G4 right_H1 right_H2 right_H3 right_H4 right_I1 right_I2 right_I3 right_I4 right_I5 right_I6 right_J1 right_J2 right_J3 right_J4 right_J5 right_K1 right_K2 right_K3 right_K4 right_L1 right_L2 right_L3 right_L4 right_L5 right_L6 right_L7 right_L8 right_M1 right_M2 right_M3 right_M4 right_M5 right_N1 right_N2 right_N3 right_N4 right_N5 right_N6 right_O1 right_O2 right_O3 right_O4 right_O5 right_O6

value

sim_time

I

Simulation 1 pre−mRNA expression over time

module_id

A1 A2 A3 A4 A5 A6 A7 B1 B10 B2 B3 B4 B5 B6 B7 B8 B9 left_A1 left_A2 left_A3 left_A4 left_B1 left_B2 left_B3 left_B4 left_Burn1 left_Burn2 left_Burn3 left_Burn4 left_C1 left_C2 left_C3 left_C4 left_C5 left_C6 left_D1 left_D2 left_D3 left_D4 left_D5 left_E1 left_E2 left_E3 left_E4 right_A1 right_A2 right_A3 right_A4 right_B1 right_B2 right_B3 right_B4 right_Burn1 right_Burn2 right_Burn3 right_Burn4 right_Burn5 right_C1 right_C2 right_C3 right_C4 right_C5 right_C6 right_C7 right_C8 right_D1 right_D2 right_D3 right_D4 right_D5 right_D6 right_E1 right_E2 right_E3 right_E4 right_E5 right_F1 right_F2 right_F3 right_F4 right_F5 right_F6 right_G1 right_G2 right_G3 right_G4 right_H1 right_H2 right_H3 right_H4 right_I1 right_I2 right_I3 right_I4 right_I5

30 20 10 0

value

sim_time