Tobore Peter Egbikuadje

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PROFILE

Dedicated electrical engineer with a strong passion for digital design and verification. Proficient in Verilog, SystemVerilog, and C programming, with extensive hands-on experience developing FPGA designs and creating testbenches using Universal Verification Methodology (UVM). Committed to continuous learning, results-driven execution, and effective cross-functional collaboration.

WORK EXPERIENCE

Junior FPGA Designer at Fidus Systems Inc. (Ottawa, ON) **September 2022 - May 2023**

- Debugged and validated 30+ VHDL design files in a large-scale project, creating custom testbenches and automating simulations in QuestaSim, ensuring 100% functional correctness through top-down debug analysis
- Developed constrained-random SystemVerilog testbenches using UVM to verify 3+ IPs (Ethernet, AXI, UART), covering edge cases and achieving 100% functional and code coverage, which helped identify and resolve 20+ design bugs during simulation
- Automated design flow using Bash and TCL scripts, reducing project setup time by over 30% and minimizing manual errors across multiple project iterations
- Created a Python script to parse 50+ XML configuration files, dynamically extracting variable content from 3 external files, automating data handling and improving processing efficiency by over 70%
- Collaborated within a cross-functional team of 10+ engineers to enhance and improve client product functionality across hardware and software domains
- Managed version control with Git, tracked tasks and bugs using Jira and documented/reviewed project details in Confluence to enhance team collaboration and maintain project clarity
- All tasks were executed in a Linux environment, leveraging command-line tools and scripting to streamline development workflows

Engineering Intern at PWB Interconnect Solutions (Ottawa, ON) **May 2020 - August 2020**

- Programmed embedded microcontrollers in C to automate stress testing of 4 client products, enabling continuous monitoring, data analysis, and early detection of failure points to ensure product reliability
- Performed oscilloscope-based diagnostics and signal validation during test phases
- Developed documentation, user guides, and training manuals to support hardware and software product development

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PROJECTS

Capstone and Academic Project (Ottawa, ON)

Pacman Neural Network Game **September 2023 - June 2024**

- Converted a MATLAB-designed Spiking Neural Network into efficient Verilog code for FPGA implementation with real-time control of a Pacman game using Xilinx Vivado
- Implemented a USB-UART bridge in Verilog with a Python script using the pyserial library, achieving stable bi-directional PC-to-FPGA data transfer at 9600 baud for uninterrupted real-time gameplay
- Created testbenches for 5+ Verilog modules and debugged simulation behaviour in Vivado, achieving 100% functional correctness and documenting the design process in a comprehensive report
- Optimized the communication protocol to reduce the round-trip latency by 40% to 250 ms, simulating the average human reaction time

Egg Timer System **September 2021 - December 2021**

- Designed and implemented an FPGA-based egg timer system in Verilog using Xilinx Vivado, incorporating button-based and switch-based controls, a 7-segment display, an auditory alert mechanism and LED indicators for status updates
- Manually assigned FPGA pin constraints and verified functionality with timing-driven simulation and testbenches

Personal Projects (Ottawa, ON)

AXI4-Lite Slave Design & Verification **May 2025 – June 2025**

- Designed a protocol-compliant AXI4-Lite slave register block in SystemVerilog with address decoding and edge case handling
- Built a complete UVM testbench with driver, monitor, scoreboard, assertions, and coverage model; achieved 100% functional/code coverage during simulation using Xcelium
- Verified edge cases, such as invalid address access and response logic using directed and constrained-random tests

Asynchronous FIFO Design and Verification **May 2025**

- Designed a parameterized asynchronous FIFO in SystemVerilog, handling safe data transfer across two independently clocked domains
- Developed a complete UVM verification environment from scratch, including testbench architecture, agent, sequencer, driver, monitor, scoreboard, sequences, and environment
- Wrote directed and constrained-random test sequences to validate corner cases including overflow and underflow
- Integrated assertions and functional coverage to ensure design correctness and coverage completeness
- Simulated and debugged using Cadence Xcelium; achieved 100% functional and code coverage

Pong Game **September 2024 - December 2024**

- Developed an FPGA-based Pong game in Verilog using Xilinx Vivado, with 100% real-time pixel rendering at 60 FPS for smooth ball and paddle motion on a 640×480 VGA display using the Nexys4 DDR board
- Implemented VGA signal generation for 640×480 resolution output, integrating timing controllers and sync pulse generators to drive accurate frame rendering on a connected monitor
- Designed finite state machines (FSMs) for game logic, paddle control via push buttons, collision detection, and a scoring system with a reset function for gameplay management
- Created functional testbenches and mapped video I/O signals using a constraint file to physical FPGA I/O pins

Bank Management System **March 2022 – May 2022**

- Created a C-based console bank management system with registration, passcode login, and key features like deposit, withdrawal, balance check, account information update, and fund transfers
- Implemented persistent data storage using file I/O with structured data management through structs, enabling organized and efficient handling of user accounts

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EDUCATION

Carleton University (Ottawa, ON)

Bachelor of Electrical Engineering with High Distinction (CGPA: 11/12) **September 2019 - June 2024**

- Recognized on the Dean's Honour List for academic excellence (2020, 2021, 2022, 2024)

TECHNICAL SKILLS

Programming Languages: Verilog, SystemVerilog, VHDL, C, TCL, Bash, Python, MATLAB, Java
Verification: Universal Verification Methodology (UVM), Assertion-Based Verification (ABV)
Tools: Modelsim, Questasim, Vivado, Virtuoso, Xcelium
Collaboration: Git, Jira, Confluence
Protocols & Standards: Ethernet (1G/10G/25G/100G), I2C, SPI, UART, PCIe, SDI, AXI4(-Lite), VGA, SDI

ACHIEVEMENTS

- TLS Outstanding Teaching Assistant Award Nomination at Carleton University (2023/2024)
- Placed third in the Electrical Engineering Poster Fair at Carleton University (2023/2024)