Peter Egbikuadje

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PROFILE

Dedicated electrical engineer with a strong passion for digital design and verification. Skilled in Verilog/SystemVerilog, UVM, and FPGA development with hands-on experience in complex hardware-software projects. Committed to continuous learning, results-driven execution, and cross-functional collaboration.

EXPERIENCE WORK

Junior FPGA Designer at Fidus Systems Inc. (Ottawa, ON) **September 2022 - May 2023**

- Debugged and validated VHDL designs by creating testbenches and automating simulations in Questasim, ensuring functional correctness and timing closure
- Developed Bash and TCL scripts in Linux to automate design flows, reducing synthesis-to-bitstream generation time by ~30% and minimizing manual errors across multiple project iterations
- Developed a Python script to parse XML configuration files and dynamically extract referenced variable content from external files, automating data handling and improving processing efficiency
- Collaborated within a large, diverse team, working alongside professionals with varying skill sets to enhance and improve the functionality of clients' products
- Managed version control with Git, tracked tasks and bugs using Jira and documented/reviewed project details in Confluence to enhance team collaboration and maintain project clarity

Engineering Intern at PWB Interconnect Solutions (Ottawa, ON) **May 2020 - August 2020**

- Programmed embedded microcontrollers using C to automate stress testing of client products, enabling continuous monitoring, data analysis, and early detection of failure points to ensure product reliability
- Performed oscilloscope-based diagnostics and signal validation during test phases
- Developed documentation, user guides, and training manuals to support hardware and software product development

PROJECTS

Capstone and Academic Projects (Ottawa, ON)

Pacman Neural Network Game **September 2023 - June 2024**

- Converted a MATLAB-designed Spiking Neural Network into efficient Verilog code for FPGA implementation with real-time control of a Pacman game using Xilinx Vivado
- Implemented a USB-UART bridge in Verilog with a Python-based communication script leveraging the PySerial library, enabling bi-directional PC-to-FPGA communication for real-time gameplay
- Created testbenches for all Verilog modules and debugged simulation behavior in Vivado while documenting the design process in a comprehensive report
- Optimized the communication protocol to reduce the round-trip latency to 250 ms, simulating human reaction time

Egg Timer System **September 2021 - December 2021**

- Designed and implemented an FPGA-based egg timer system in Verilog using Xilinx Vivado, incorporating button-based and switch-based controls, a 7-segment display, an auditory alert mechanism and LED indicators for status updates
- Manually assigned FPGA pin constraints and verified functionality with timing-driven simulation and testbenches

Personal Projects (Ottawa, ON)

AXI4-Lite Slave Design & Verification **May 2025 – June 2025**

- Designed a protocol-compliant AXI4-Lite slave register block in SystemVerilog with address decoding and edge case handling
- Built a complete UVM testbench with driver, monitor, scoreboard, assertions, and coverage model; achieved 100% functional/code coverage using Xcelium
- Verified edge cases such as invalid address access and response logic using directed and constrained-

random tests

Pong Game **September 2024 - December 2024**

- Developed an FPGA-based implementation of the classic Pong game in Verilog using Xilinx Vivado, featuring real-time ball and paddle movement rendered via pixel-based VGA display logic on the Nexys4 DDR board
- Implemented VGA signal generation for 640×480 resolution output, integrating timing controllers and sync pulse generators to drive accurate frame rendering on a connected monitor
- Designed finite state machines (FSMs) for game logic, paddle control via push buttons, collision detection, and a scoring system with a reset function for gameplay management
- Created functional testbenches and mapped video/I/O signals using constraint files to physical FPGA I/Os

Bank Management System **March 2022 – May 2022**

- Created a C-based console bank management system with registration, passcode login, and key features like deposit, withdrawal, balance check, account information update, and fund transfers
- Implemented persistent data storage using file I/O with structured data management through structs, enabling organized and efficient handling of user accounts

EDUCATION

Carleton University (Ottawa, ON)

Bachelor of Electrical Engineering with High Distinction (CGPA: 11/12) **September 2019 - June 2024**

- Recognized on the Dean's Honour List for academic excellence (2020, 2021, 2022, 2024)

TECHNICAL SKILLS

Programming Languages: Verilog, SystemVerilog, VHDL, C, TCL, Bash, Python, MATLAB, Java
Verification: UVM, ABV
Tools: Modelsim, Questasim, Vivado, Virtuoso, Xcelium
Collaboration: Git, Jira, Confluence
Protocols & Standards: Ethernet (1G/10G/25G/100G), I2C, SPI, UART, PCIe, SDI, AXI4(-Lite)

CERTIFICATIONS

- SystemVerilog for Design and Verification – Cadence Design Systems, May 2025
- SystemVerilog Accelerated Verification with UVM – Cadence Design Systems, May 2025

ACHIEVEMENTS

- TLS Outstanding Teaching Assistant Award Nomination at Carleton University (2023/2024)
- Placed third place in the Electrical Engineering Poster Fair at Carleton University (2023/2024)