Peter Egbikuadje

A-428 Sunnyside Ave, Ottawa, Canada
(204)-915-6470 | peteregbiks@gmail.com

WORK EXPERIENCE

Junior FPGA Designer *Ottawa, ON*
Fidus Systems Inc. *September 2022 – May 2023*

- Developed Bash and Tcl scripts to automate FPGA project workflows, including environment setup, synthesis, simulation, and bitstream generation, optimizing development efficiency.
- Debugged and validated VHDL designs by creating testbenches and automating simulations in Questasim, ensuring functional correctness and reliability. Developed Python scripts for automated modification of VDHL design structures.
- Managed version control with Git, tracked tasks and bugs using Jira, and documented project details in Confluence to enhance team collaboration and maintain project clarity.
- Collaborated within a large, diverse team, working alongside professionals with varying skill sets to enhance and improve the functionality of a client's product.

Engineering Intern *Ottawa, ON*
PWB Interconnect Solutions *May 2020 - August 2020*

- Developed documentation, user guides, and training manuals to support hardware and software product development, while also creating user interfaces based on client and engineering specifications.
- Programmed embedded microcontrollers in C to automate testing of integrated systems and performed data analysis in Excel to evaluate test results.

RELEVANT PROJECTS

Pacman Spiking Neural Network Capstone Project *Ottawa, ON*
Carleton University *September 2023 – April 2024*

- Designed and implemented an FPGA-based Spiking Neural Network (SNN) using Xilinx Vivado and Verilog to control a Pacman game, translating biological neural behaviors into efficient hardware for real-time processing.
- Developed a USB-UART interface using Xilinx Vivado and a Python script with PySerial library to enable seamless serial data transmission between the FPGA and PC.
- Tested and debugged FPGA modules by creating Verilog testbenches, ensuring reliable communication and functionality, and documented the design process in a comprehensive report.
- Optimized the communication protocol to reduce the round-trip data transfer time to 250 ms, simulating human reaction time.

Bouncing DVD Video Replica *Ottawa, ON*
Personal *May 2023 – July 2023*

- Designed and implemented an FPGA-based bouncing DVD logo replica concept with a VGA interface, integrating a custom SMPTE color bar background for accurate color generation and synchronization.
- Optimized animation performance and VGA signal timing, ensuring smooth motion and stable video output.

Egg Timer System *Ottawa, ON*
Carleton University *November 2021 – December 2021*

- Designed and implemented an FPGA-based egg timer system using Xilinx Vivado and Verilog, incorporating button-based controls, a 7-segment display, an auditory alert mechanism and LED indicators for user interaction.
- Configured the constraints file to map each input and output to the corresponding FPGA pins, and thoroughly tested the design to ensure accurate timing, proper state transitions, and reliable functionality.

EXTRACURRICULAR ACTIVITIES

Teaching Assistant (Calculus & Linear Algebra) *Ottawa, ON*
Carleton University *September 2023 – April 2024*

- Collaborated with the professor to set up the classroom, distribute materials, and ensure an inclusive learning environment, making accommodations for students with disabilities. Graded assignments and provided constructive feedback to improve student understanding.
- Offered one-on-one support during office hours, clarifying misconceptions, guiding students through problem-solving steps, and providing explanations to deepen knowledge of the course. Created supplementary problems to reinforce key concepts.

TECHNICAL SKILLS

- Programming/Scripting Languages: Verilog, Python, C, Tcl, Bash, Matlab, and Java.
- Tools & Technologies: Xilinx Vivado, Visual Studio, Git, Linux CLI, FPGA, and Questasim.

EDUCATION

Carleton University *(Ottawa, ON)* *September 2019 – July 2024*

- Bachelor of Engineering in Electrical Engineering *CGPA: 11/12 (92%) – High Distinction*