TFE4146 - Semiconductor Devices - Fall 2023

Problem Set 7

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Contents

Problem 1

Figure 1 shows the high frequency capacitance vs. voltage ($C-V$ characteristics) of an n-channel MOSFET, made from p-type Si substrate with a dopant concentration of $N_a = 5 \cdot 10^{15}$ cm^{-3} and use of n$^+$-polysilicon gate electrode. The thickness of the oxide in the gate area is $d_{ox} = 100$Å, and the effective interface charge $Q_i = 4 \cdot 10^{10} q \left[\text{Ccm}^{-2}\right]$. Assume room temperature: $T = 295$ K.

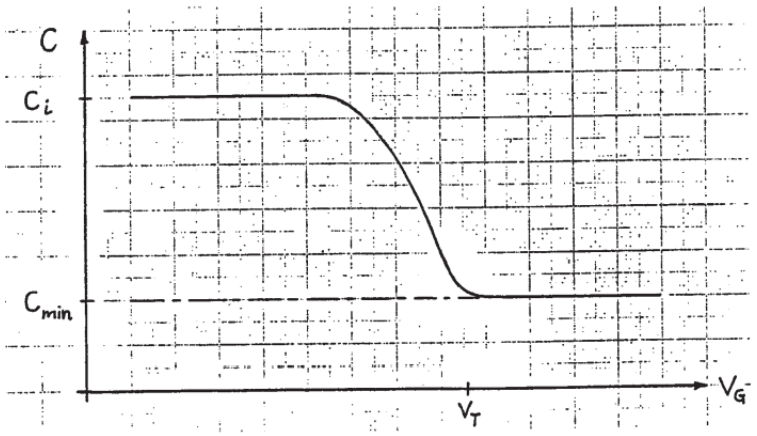

Figure 1: High frequency capacitance vs. voltage of an n-channel MOSFET

a) A MOSFET of this kind has two contributions to the capacitance: C_i and C_s. Describe the mechanisms behind these two contributions, draw an equivalent circuit diagram for the MOS capacitance and find an expression for C_{min} expressed by C_i and $C_s = C_{d,\text{min}}$ (assuming that the component at hand is biased in strong inversion).

We start by describing the to capacitance:

- The insulator capacitance C_i:

  This capacitance is given by $C_i = \frac{\epsilon_i}{d}$ where ϵ_i is the permittivity of the insulator, while d is the insulator thickness. This capacitance is associated woth the metal-oxide part of the mos structure. It behaves a lot like a parallel-plate capacitor as the oxide layer functions as the dielectric, and the capacitance is determined by the permittivity of the oxide material and the thickness of the oxide layer.

- The voltage-dependent semiconductor capacitance C_s:

  This capacitance is given by $C_s = \frac{qQ}{qV} = \frac{dQ_s}{d\phi_s}$ where Q_s is the space charge density per unit area and ϕ_s is the surface potential. This capacitance arise from the formation of a

space-charge region withing the semiconductor when a voltage is applied. For less negative voltage the accumulation of electrons at the surface makes the semiconductor surface becomes depleted and a depletion-layer capacitance us added in series with C_i

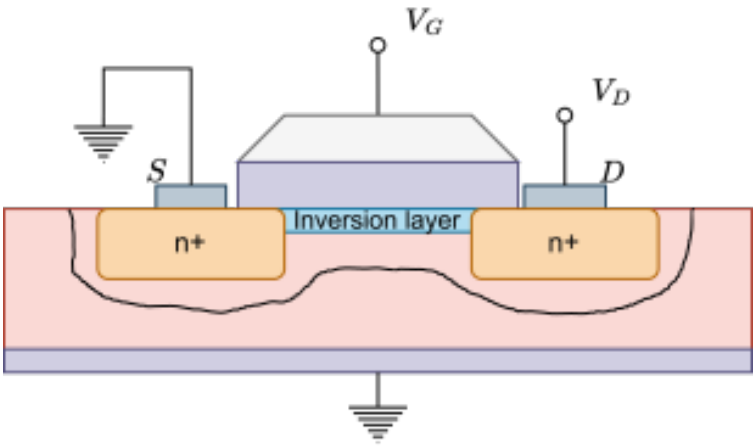

Figure 2: Circuit diagram for the MOS capacitance

The minimum MOS capacitance C_{min} is given by

$$C_{min} = \frac{C_i C_{d,min}}{C_i + C_{d,min}}$$

as $C_s = C_{d,min}$ we get

$$C_{min} = \frac{C_i C_s}{C_i + C_s}$$

b) Determine a numerical value for the capacitance of the MOS structure at hand operating at a negative gate voltage $(V_G \ll V_T)$ and positive gate voltage $(V_G \gg V_T)$, respectively.

For the case $(V_G \ll V_T)$:

$$C = C_i = \frac{\epsilon_i}{d}$$

as the relative permittivity ϵ_r for silicon dioxide is 3.9 and permittivity of free space $\epsilon_0 = 8.85 \cdot 10^{-14} \frac{F}{cm}$ this gives us:

$$C = \frac{3.9 \cdot 8.85 \cdot 10^{-14}}{10^{-6}} = 3.4515 \cdot 10^{-7}$$

For the case ($V_G \gg V_T$):

$$C = C_{min} = \frac{C_i C_s}{C_i + C_s}$$

where $C_s = \frac{\epsilon_s}{W_m}$. We start by calculating W_m

$$W_m = 2 \left[\frac{\epsilon_s \phi_F}{q N_a} \right]^{1/2}$$

where ϕ_F is given by

$$\phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i} = \frac{1.38 \cdot 10^{-23} \cdot 295}{1.6 \cdot 10^{-19}} \ln \frac{5 \cdot 10^{15}}{1.5 \cdot 10^{10}} = 0.324eV$$

this gives

$$W_m = 2 \left[\frac{11.68 \cdot 8.85 \cdot 10^{-14} \cdot 0.324}{1.6 \cdot 10^{-19} \cdot 5 \cdot 10^{15}} \right]^{1/2} = 4.1 \cdot 10^{-5} cm$$

$$\Rightarrow C_s = \frac{11.68 \cdot 8.85 \cdot 10^{-14}}{4.1 \cdot 10^{-5}} = 2.52 \cdot 10^{-8}$$

and we end up with

$$C = \frac{3.4515 \cdot 10^{-7} \cdot 2.52 \cdot 10^{-8}}{3.4515 \cdot 10^{-7} + 2.52 \cdot 10^{-8}} = 2.35 \cdot 10^{-8} \frac{F}{cm^2}$$

c) Draw a sketch that shows how the $C - V$ characteristics in the figure above changes for low frequencies (typical $\sim 1 - 100$ Hz), and explain the reason for this characteristic change in the $C - V$ characteristics.

Given:

- Intrinsic charge carrier density for Si : $n_i = 1.5 \cdot 10^{10}$ cm^{-3}

- Relative dielectric permittivity for Si : $\varepsilon_r = 11.8$
- Relative dielectric permittivity for SiO_2 : $\varepsilon_r = 3.9$

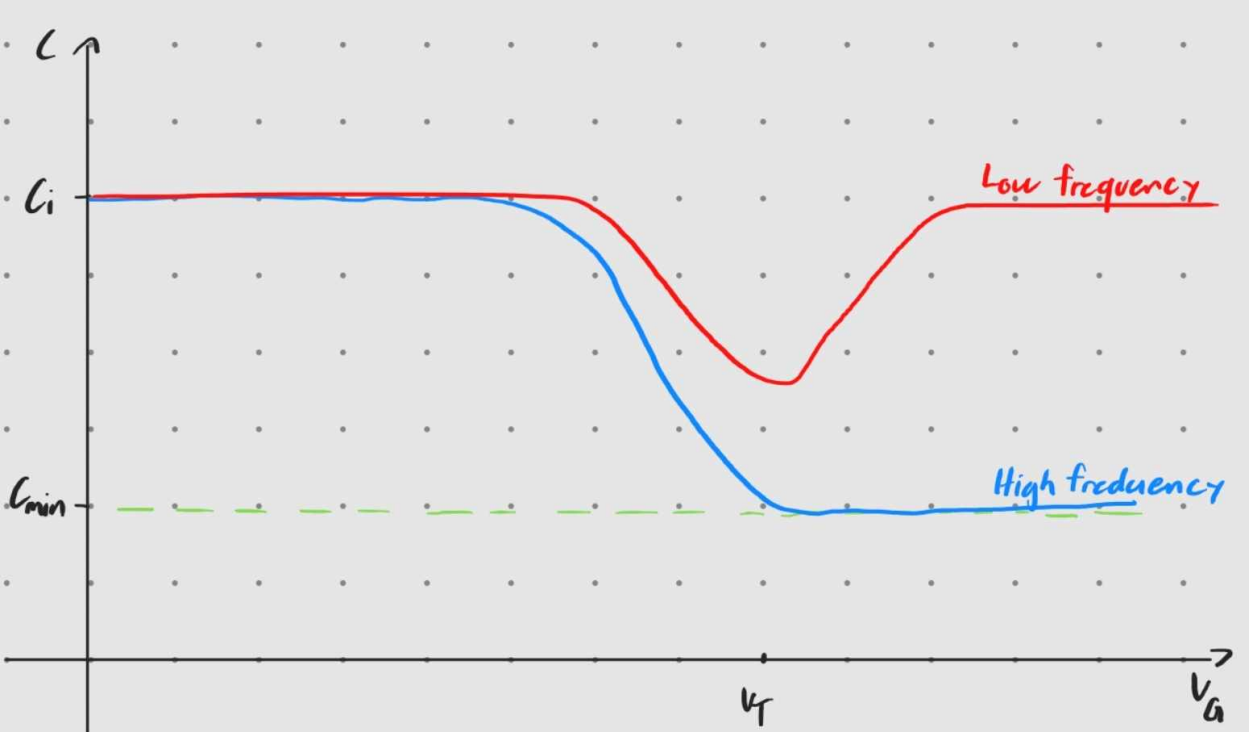

Figure 3: Sketch of the C - V characteristic.

Problem 2

In this problem we go through the derivation of the most basic mathematical models for the I-V characteristic of a MOSFET. We will first derive the model valid in the triode region and use this to find an expression valid in the saturation (active) region.

a) Draw a cross-section of an NMOS transistor (p-type substrate). Sketch the inversion layer and depletion region when $V_G > V_T, V_S = 0$ and $V_D = 0$.

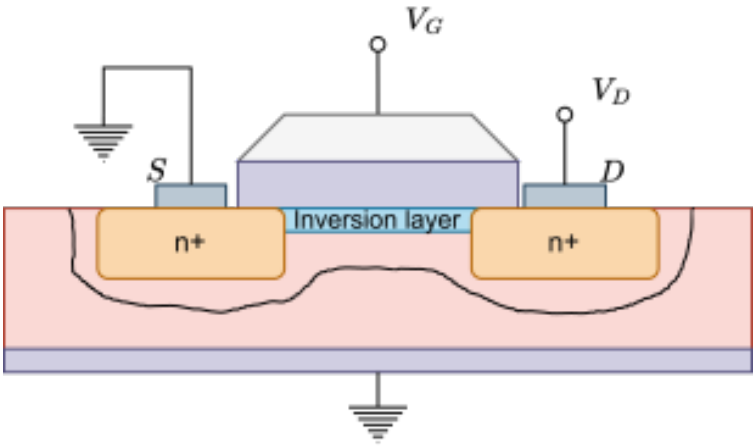

Figure 4: cross-section of an NMOS transistor

b) The contributions of the applied gate-voltage is given by

$$V_G = V_{FB} - \frac{Q_s}{C_i} + \phi_s = V_{FB} - \frac{Q_n + Q_d}{C_i} + \phi_s, \tag{1}$$

where V_{FB} is the flat-band voltage, Q_s is the total amount of induced charge in the semiconductor per area, C_i is the insulator (oxide) capacitance per area, and ϕ_s is the potential at interface between the semiconductor and the insulator. The induced charge Q_s consists of two contributions, the mobile inversion charge Q_n and the fixed charge in the depletion region Q_d.

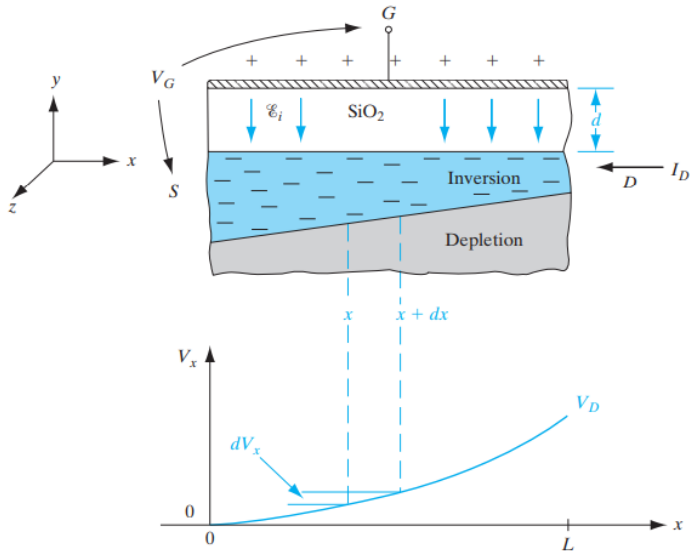

Figure 5: The inverted channel of an NMOS transistor. Figure 6-26 in Streetman.

Consider figure 5. When $V_D > 0$, the surface potential $\phi_s(x)$, and hence the inversion charge $Q_n(x)$, will no longer be constant throughout the channel, but depend on the potential V_x. Let $0 < V_D < (V_G - V_T)$ and use equation 1 to show that

$$Q_n(x) = -C_i\,(V_G - V_T - V_x) \tag{2}$$

when the variations of Q_d with respect to V_x is neglected. Discuss the validity of this assumption. Would the variations in Q_d increase or decrease the Q_n ?

Rewriting equation 1

$$Q_n = V_{FB}C_i - Q_d + \phi_s C_i - V_G C_i \tag{3}$$

$$= -C_i\left[V_G - \left(V_{FB} + \phi_s - \frac{Q_d}{C_i}\right)\right] \tag{4}$$

At threshold, the term in brackets can be written as $V_G - V_T$, but with a voltage V_D applied, there is a voltage rise V_x from the source to each point x in the channel.

$$Q_n = -C_i\left[V_G - V_{FB} - 2\phi_F - V_x - \frac{1}{C_i}\sqrt{2q\epsilon_s N_a\,(2\phi_F + V_x)}\right] \tag{5}$$

as we neglect the variations of Q_d with respect to V_x the equation gets simoplified to

$$Q_n(x) = -C_i\,(V_G - V_T - V_x) \tag{6}$$

c) The drain current I_D is given by

$$I_D = ZQ_n(x)\bar{\mu}_n \mathrm{E}_x(x), \tag{7}$$

where Z is the width of the gate, $\bar{\mu}_n$ is the surface electron mobility and

$$\mathrm{E}_x(x) = -\frac{dV_x}{dx} \tag{8}$$

is the component of the E-field in the x-direction. Use equations 2 and 8 to show that the drain current in this region is given by

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)\, V_D - \frac{1}{2}V_D^2\right]$$

at point x we have

$$I_D dx = \overline{\mu_n} Z |Q_n(x)| dV_x \tag{9}$$

If we integrate from source to drain,

$$\int_0^L I_D dx = \bar{\mu}_n Z C_i \int_0^{V_D} (V_G - V_T - V_x)\, dV_x$$

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)\, V_D - \frac{1}{2}V_D^2\right]$$

d) Sketch the inversion layer and depletion region in the transistor when the drain-voltage is increased such that $V_D = (V_G - V_T)$.

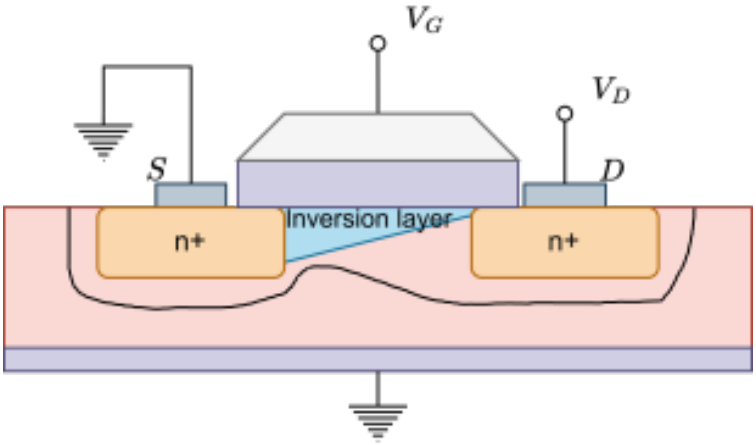

Figure 6: The inversion layer and depletion region in the transistor when the drain-voltage is increased such that $V_D = (V_G - V_T)$.

e) The square-law model is the simplest (useful) model describing the drain current of a MOSFET operating in saturation and strong inversion. This model assumes I_D to be independent of V_D when $V_G > V_T$ and $V_D > (V_G - V_T)$. Use this assumption to show that this saturation current is given by

$$I_D(\text{ sat. }) = \frac{1}{2}\bar{\mu}_n C_i \frac{Z}{L}(V_G - V_T)^2 .$$

the saturation condition is approximately given by

$$V_D(sat.) \cong V_G - V_T$$

If we substitute this approximation into we get

$$I_D \text{ (sat.)} \cong \frac{1}{2}\bar{\mu}_n \mathrm{C}_i \frac{Z}{L}(V_G - V_T)^2$$

f) Explain why I_D may be approximated as independent of V_D in the saturation region. Explain some of the physical effects we neglect and discuss the validity of this approximation for different values of L and V_D.

As the drain voltage is increased, the coltage acros the oxide decreqases near the drain, and Q_n becomes smaller. This results in the channel being pinched off at the drain end, and the current saturates.

The charge Q_d is often assumed constant and its variation with respect to the channel voltage V_x is neglected. This is valid as when a MOSFET is in a strong inversion ($V_G > V_T$), the mobile inversion charge Q_n is much larger than the depletion charge Q_d.

We can approximate L for longer channel length(?)