TFE4146 - Semiconductor Devices - Fall 2023

Problem Set 7

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Contents

Problem 1

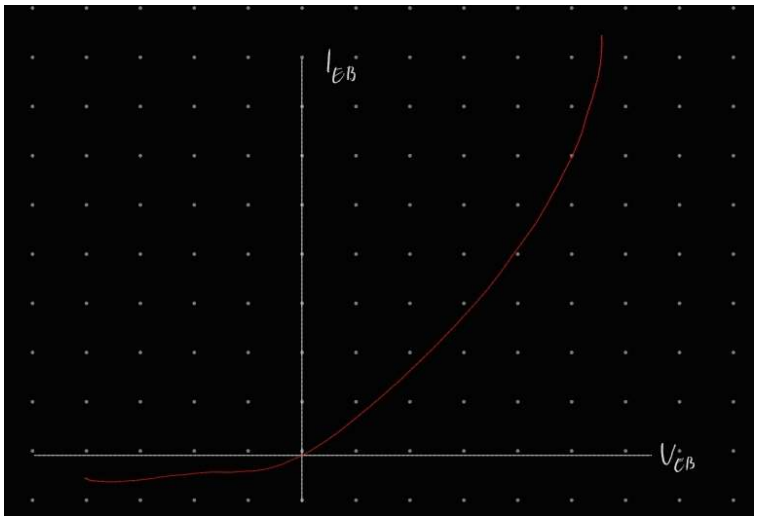
The component in figure 1 consists of an n-type semiconductor with uniform doping and ohmic contacts at the ends (top/bottom) and sharp (abrupt) $p^+ - n$ junctions with ohmic contacts at the edges. The length of the p^+ regions is L and the istance between these region is marked by d.

a) Assume that the terminals E-C and B-D are connected, and that $\mathrm{d} >> L_p$[1].

i) What standard semiconductor device does the figure represent under these conditions?

This is a pn junction

ii) Sketch the current I_{EB} as a function of applied voltage V_{EB} between the connected terminal pairs E-C and B-D



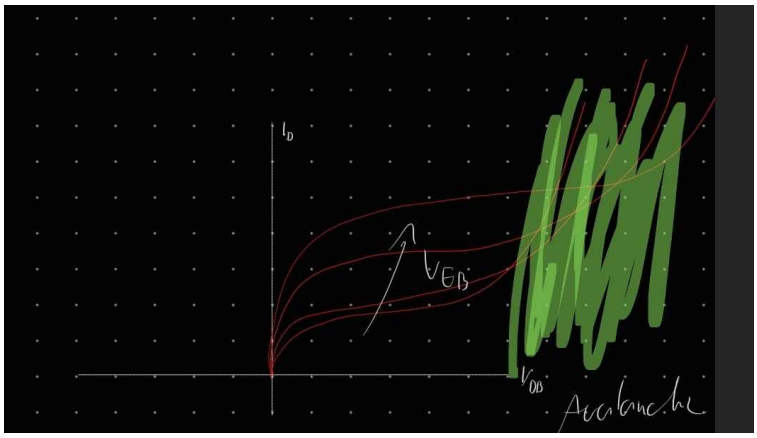
b) Assume now that only the terminals E-C are connected. Assume bias voltage $\mathrm{V}_{BD} > 0$ and $\mathrm{V}_{EB} < 0$.

i) What standard semiconductor device does the figure represent under these conditions?

JFET

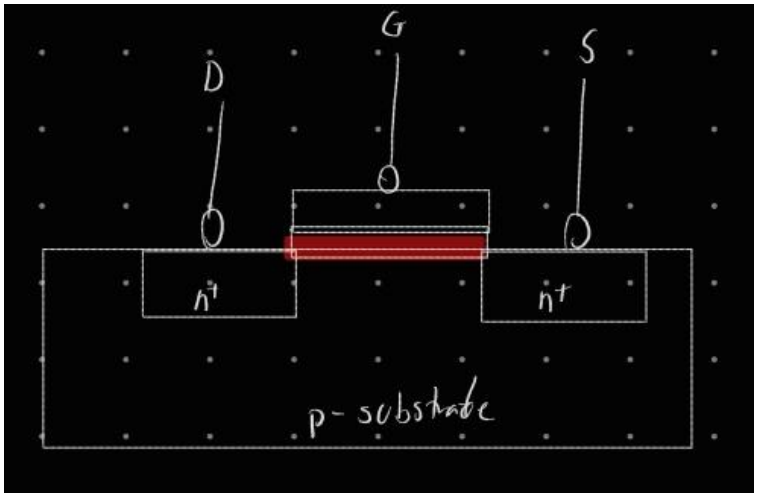
ii) Sketch the current I_D as a function of the applied voltage V_{DB} for different levels of V_{EB}

iii) Indicate in the sketched I-V characteristics the effect of avalanche breakdown in the two $p^+ - n$ junctions.



Problem 2

Draw a simple schematic of a MOSFET with n^+wells in a p-type substrate. The gate electrode is made of n^+-polysilicon and is separated from the substrate by a thin SiO_2 layer. Draw the corresponding band diagram from source to drain in the two scenarios



i) No gate Voltage

ii) $V_G > V_T$

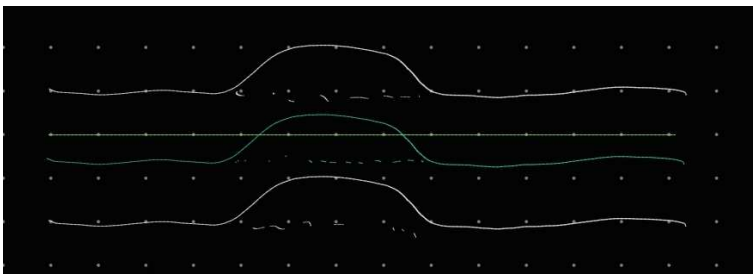


Figure 1: stippled is when $V_G > V_T$

Problem 3 - Narrow base diode