TFE 4152 Design of Integrated Circuits

Exercise 2

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Contents

Problem 1

From the problem text, we are given this information:

Table 1: NMOS Transistor Parameters in 180 nm Technology

Parameter	Unit/Equation	Value
V_{eff}	V	0.2
V_{Drain}	V	0.2
V_{Source}	V	0
W	μm	0.5
L	μm	0.2
T	K	293
μC_{OX}	$\frac{\mu\text{A}}{\text{V}^2}$	270
V_{t0}	V	0.45
$\lambda \cdot L$	$\frac{\mu\text{m}}{\text{V}}$	0.08
C_{OX}	$\frac{\text{fF}}{\mu\text{m}^2}$	8.5
t_{OX}	nm	5
n	–	1.6
θ	$\frac{1}{\text{V}}$	1.7
m	–	1.6
$\frac{C_{OV}}{W} = L_{OV}C_{OX}$	$\frac{\text{fF}}{\mu\text{m}}$	0.35
$\frac{C_{db}}{W} \approx \frac{C_{sb}}{W}$	$\frac{\text{fF}}{\mu\text{m}}$	0.5

a) What can you say about the region of operation for the transistor, based on the description above?

The region of operation where $\text{V}_{\text{DS}} > \text{V}_{\text{DS-sat}}$, the drain current is in is independend of V_{DS} and is called the active region:

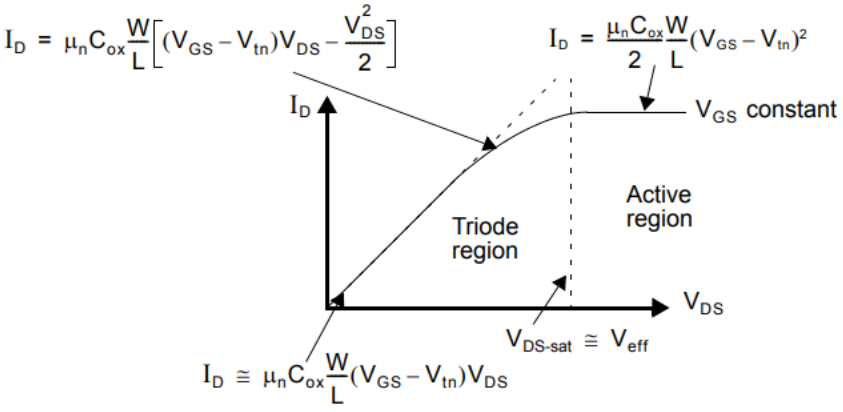


Figure 1: The I_D versus V_{DS} curve for an ideal MOS transistor. For $V_{DS} > V_{DS\text{-sat}}$, I_D is approximately constant.

Based on the paramters in the table and figure above we can say that the region of operation is when $V_{DS} > 0.2V$ as $V_{DS\text{-sat}}$ is given by

$$V_{DS\text{-sat}} = V_{GS} - V_{tn} = V_{eff}$$

b) Consider a similar case as described above. except that V_{DS} is increased by 50mV. Can you estimate the resulting drain current, I_{DS}?

From figure 1, we can se that the current I_D changes marginaly in the active region when V_DS increases, therfore the resulting drain current can be estimated to be

$$I_D = \frac{2.7 \cdot 10^{-4}}{2}\frac{5 \cdot 10^{-5}}{2 \cdot 10^{-5}}(0.2)^2 = 13.5\mu A$$

c) Estimate the maximum value for V_{eff} given that you would avoid mobility degradation for this transistor.

Due to mobility degadation, increases in V_{eff} beyond $\frac{1}{2\theta}$:

- fail to provide significant increases in small-signal transconductance,
- reduce the available signal swing limited by the fixed supply voltages, and
- reduce transistor intrinsic gain A_i dramatically

Therefore the maximum value for V_{eff} given that i would avoid mobility degradation for this transistor is

$$V_{\text{eff}} < \frac{1}{2 \cdot 1.7}$$
$$V_{\text{eff}} < \frac{5}{17} V$$

d) Calculate the small signal output resistance for the transistor when it's operating in the active region, and square-law behaviour holds.

We can use this equation

$$r_o = \frac{1}{\lambda \cdot I_D}$$

to find the small signal output resistance using the current I_D found in b)

$$r_o = \frac{1}{0.4\frac{1}{V} \cdot 13.5\mu A} = 185.2k\Omega$$

e) What would be the small-signal output resistance if the W/L ratio was kept, and the gate length multiplied by 3?

By keeping the W/L ratio, we know that the current I_D will stay the same,

$$\Lambda = \frac{0.08}{0.6} = \frac{2}{15}\frac{1}{V}$$

This gives us

$$r_o = \frac{1}{\frac{2}{15}\frac{1}{V} \cdot 13.5\mu A} = 555.6k\Omega$$

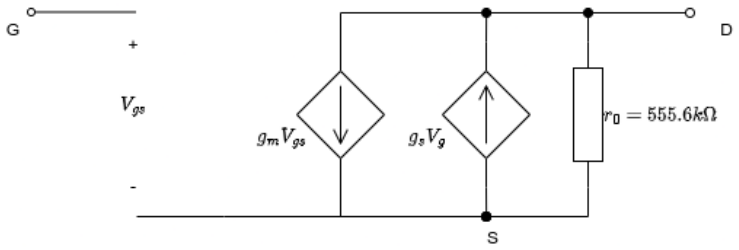
f) Calculate the small-signal transconductance, g_m, for the transistor under the conditions relevant for problem b), above.

The small-signal transconductance, g_m is given by

$$\frac{2I_D}{V_{eff}} = \mu_n C_{ox} \frac{W}{L} V_{eff}$$

$$g_m = \frac{2I_D}{V_{eff}} = \frac{2 \cdot 13.5\mu A}{0.2V} = 1.35 \cdot 10^{-4}$$

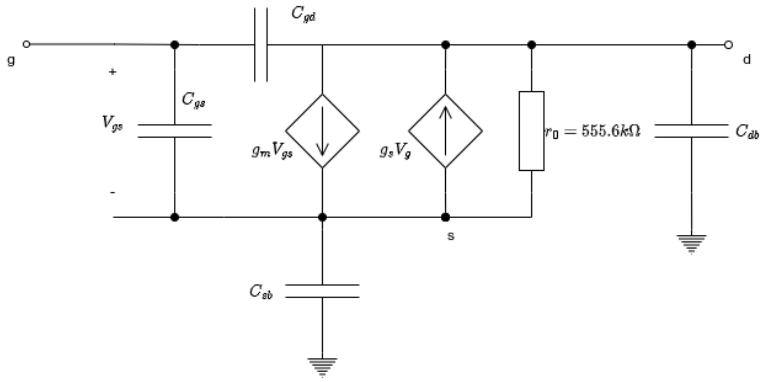
g) Indicate roughly the value for g_s and draw the low-frequency small-signal schematics for the transistor in the active region, and include relevant values based on what you have been asked to find, this far. Use r_{out} from 1 d)**.**



h) Problem 1 c) relates to mobility degradation for relatively high values of V_{DS}. Can you point to any other potential problems that could emerge from high V_{DS} voltages, especially for the shortest gate-lengths?

In shorter gate lengths, the carrier velocity in the channel can saturate at lower V_DS due to the high electric field, affecting the transistor's performance and linearity.

i) Make a sketch of the small-signal diagram from 1g), where you include the parasitic capacitances.



j) Consider the layout in Figure 2 in CJM and an implementation in the 0.8μm process from Table 1.5 in CJM for your calculations, and Let C_{js} have a value of nfF in your expression. Find an expression for the smallsignal capacitance between the source and bulk nodes.

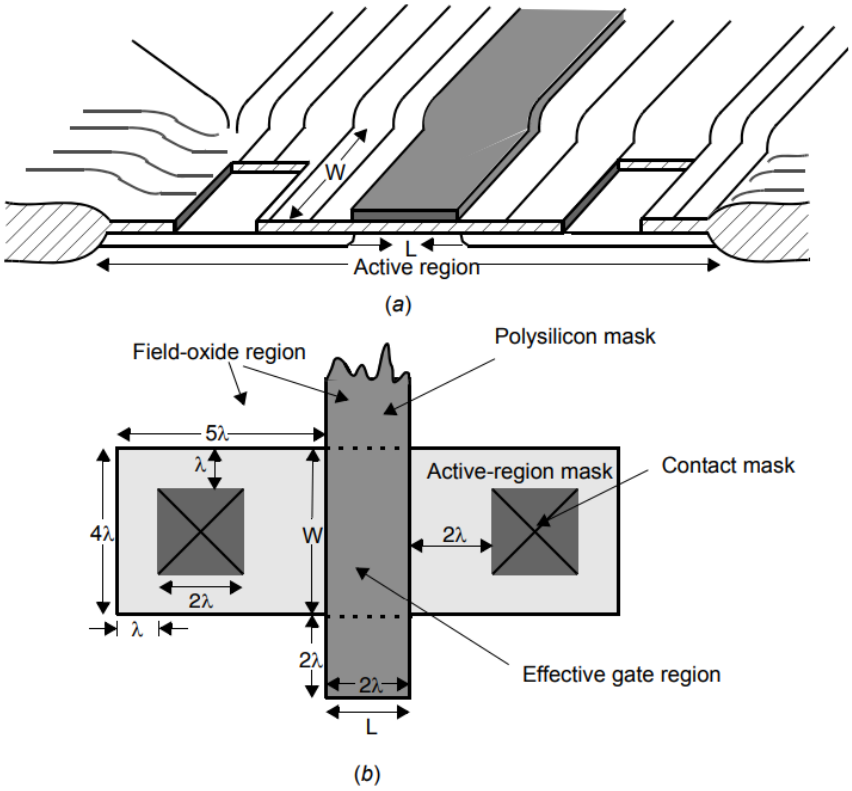


Figure 2: (a) A simplified view of a partially finished transistor and (b) the corresponding layout of the active, polysilicon, and contact masks.

Table 2: 0.8 μm Technology Parameters

Technology	**NMOS**	**PMOS**
$\mu C_{ox}\left(\mu A/V^2\right)$	92	30
$V_{t0}(V)$	0.80	-0.90
$\lambda \cdot L(\mu m/V)$	0.12	0.08
$C_{ox}\left(fF/\mu m^2\right)$	1.8	1.8
$t_{ox}(nm)$	18	18
n	1.5	1.5
$\theta(1/V)$	0.06	0.135
m	1.0	1.0
$C_{ov}/W = L_{ov}C_{ox}$ (fF/μm)	0.20	0.20
$C_{db}/W \approx C_{sb}/W$ (fF/μm)	0.50	0.80

C_{sb} is given by

$$C_{sb} = (A_s + A_{ch})\, C_{js}$$
$$C_{sb} = \left(\lambda^2 + W \cdot L\right) nfF$$

where A_s is the area of the source junction, A_{ch} is the area of the channel (i.e., WL) and C_{js} is the depletion capacitance of the source junction, given by

$$C_{js} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{sB}}{\Phi_0}}}$$

k) Estimate the minimum V_{GS} required for this NMOS transistor to be in the active region.

From 1a) we have that the region of operation is when $V_{DS} > V_{GS} - V_t$. As we dont have $V_{DS(min)}$, I assume that it is a lot smaler than $V_{GS} - V_t$. Therefore i would estimate the minimum V_{GS} required for this NMOS transistor to be in the active region is $0.08V$.

l) Circuits may in some cases operate with a supply voltage below the absolute values of both the pmos and nmos threshold voltages. Could you explain about when this could be beneficial for analog or digital circuits, or both?

From figure 1 we can se that the curve is quite linear at first, this can work as a amplifier in a analog circuit. This gives us controll of the current in the circuit.

Problem 2

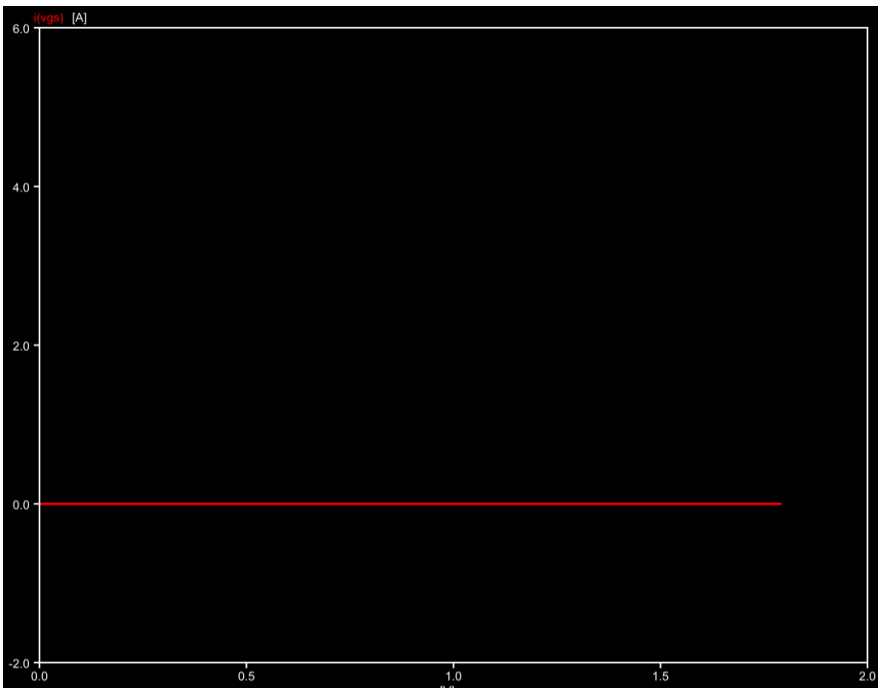


Figure 3: I_D vs V_{GS}

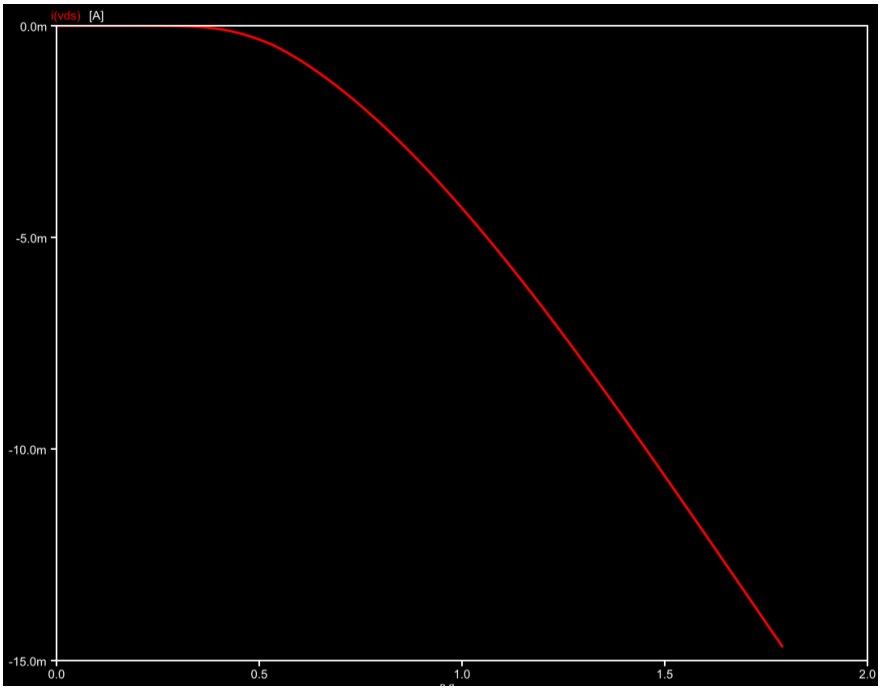


Figure 4: I_D vs V_{DS}

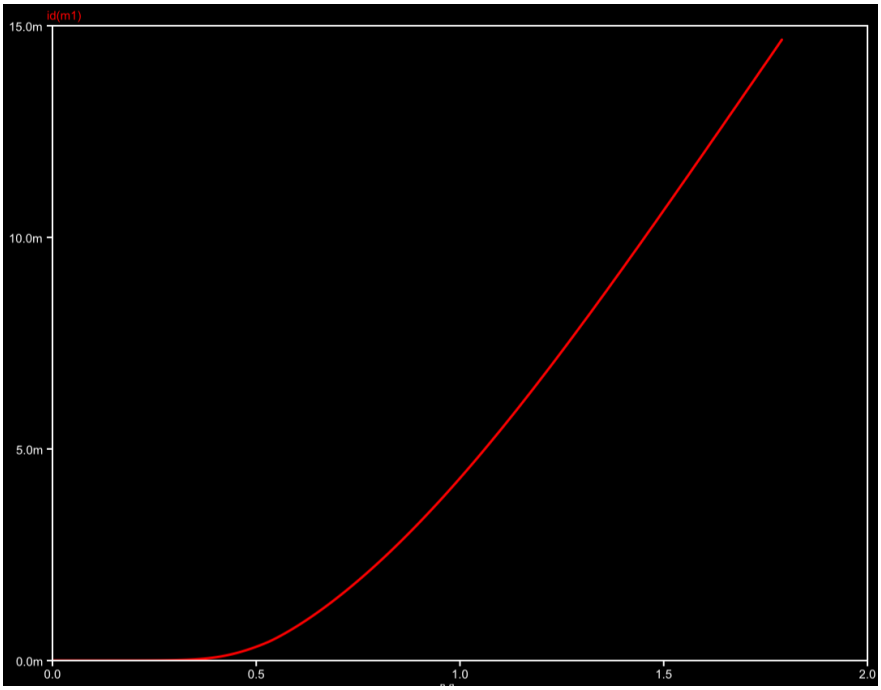


Figure 5: Drain current

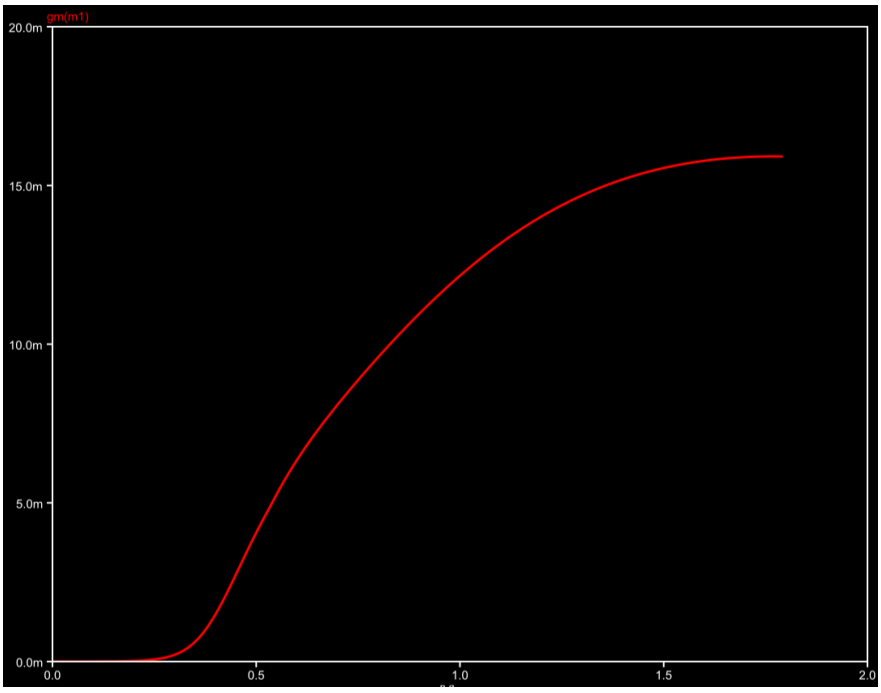


Figure 6: transconductance

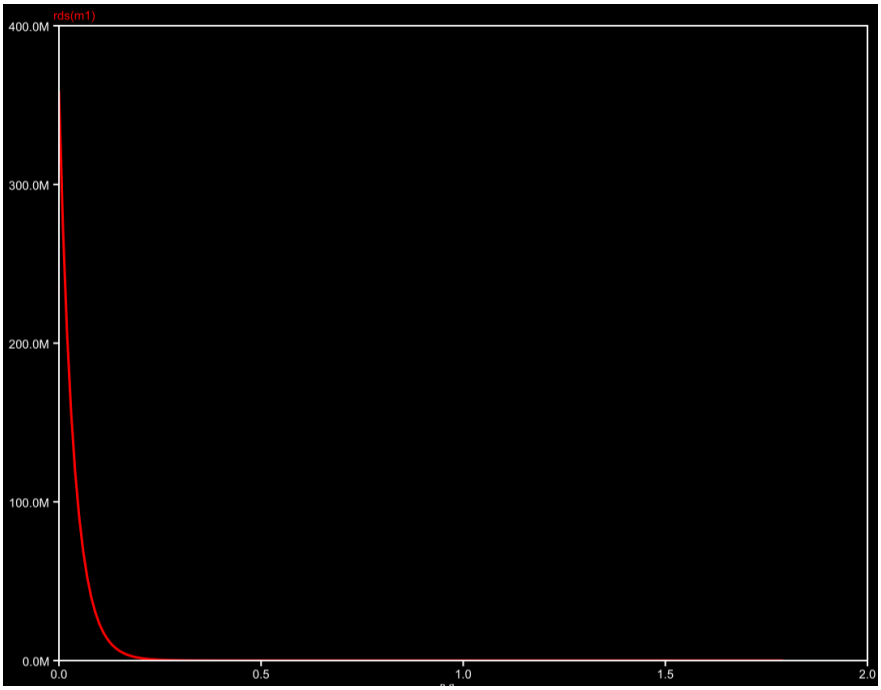


Figure 7: small signal output resistance

Listing 1: NMOS SPICE Netlist

```
* NMOS Characteristics
.include /home/peter/Software/aimspice/p18_cmos_models_ff.inc

* Defining NMOS transistor
M1 drain gate 0 0 NMOS L=0.5u W=50u

* Defining voltage sources
Vgs GATE 0 DC 0.9V
Vds DRAIN 0 DC 1.8V

.dc Vgs 0 1.8 0.01
.plot dc I(Vgs)
.plot dc I(Vds)
.plot dc id(M1)
.plot dc gm(M1)
.plot dc rds(M1)
.end
```

Problem 3

Statistical variation of device parameters on a wafer predicts a Gaussian distribution with variance $\sigma^2(\Delta P) = \frac{(A_p)^2}{WL} + (S_p)^2 D^2$, where ΔP is the difference in some device parameter P, D is the distance between two devices, and W and L their dimensions. A_p and S_p are constants, usually obtained from measurements. The standard deviation is the square root of the variance. Among the most important random variations in most analog circuits result in V_t mismatch. Figure 8 shows a differential pair. For such a circuit, it is important that transistors $Q1$ and $Q2$ are identical. Assume that the transistors in Figure 1 are closely spaced, so that the area dependent term in the above equation dominates. Given that $W = 2\mu$m and $L = 0.7\mu$m for the 2 transistors in Figure 1, what could be done to WL if you had to reduce the standard deviation of the V_t mismatch to 25% ?

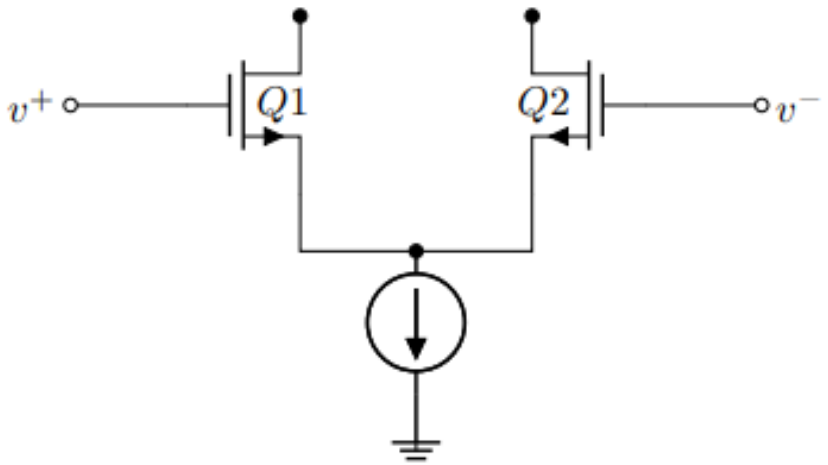


Figure 8: Differential pair.

Standart deviation given the information above is

$$\sigma(\Delta P) = \sqrt{\frac{(A_p)^2}{WL}}$$
$$\sigma(\Delta P) = \frac{(A_p)}{\sqrt{WL}}$$

If we reduce the standard deviation to 25% then we must increase W and or L

$$25\%\sigma(\Delta P) = \frac{(A_p)}{\sqrt{WL} \cdot 4}$$
$$25\%\sigma(\Delta P) = \frac{(A_p)}{\sqrt{2WL}}$$

To reduce the standard deciation of the V_t mismatch to 25% i can increase W to $4\mu m$ or L to $1.4\mu m$.

Problem 4

This problem includes elements from a chip layout where the PMOS transistors are found within the pink rectangle in the layout in Figure 9. The substrate is assumed to be of p-type and standard bulk CMOS technology is used. Can you draw the transistor schematics for a circuit that the layout illustrated in Figure 9 could represent?

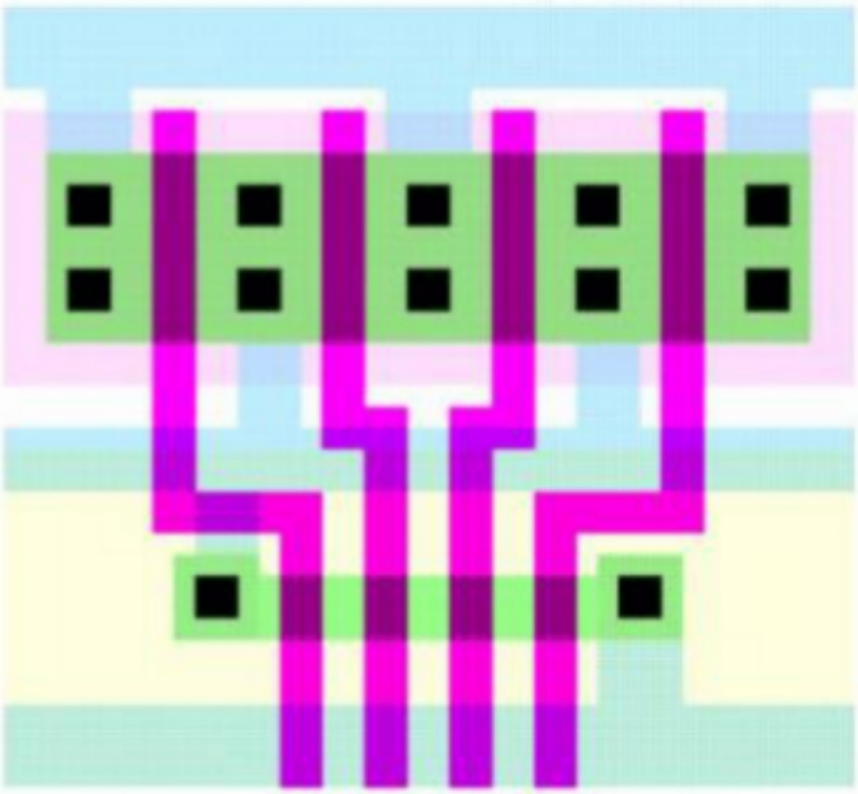
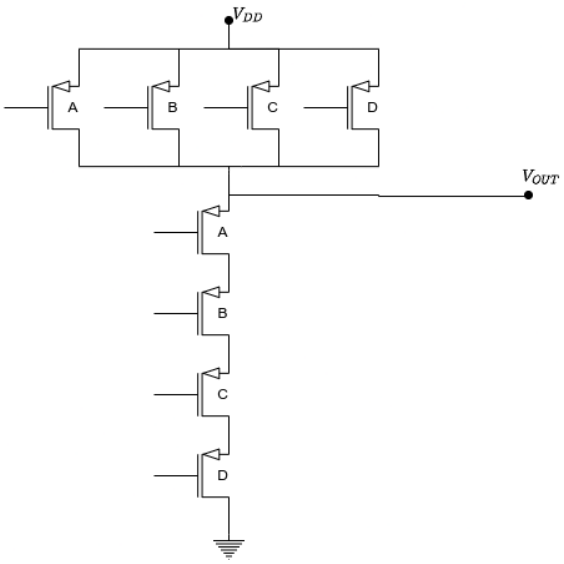


Figure 9: Layout representing a logic function implemented in CMOS.


V_{DD}
A
B
C
D
V_{OUT}
A
B
C
D