TFE 4152 Design of Integrated Circuits

Exercise 1

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Problem 1

A pn-junction has a donor concentration of $N_D = 10^{25} \frac{electrons}{m^3}$ and an acceptor concentration of $N_A = 5 \times 10^{22} \frac{holes}{m^3}$ at a temperature of $289K$. Assume that $n_i = 1.1 \times 10^{16} \frac{carriers}{m^3}$ at room temperature. What is the built-in junction potential Φ_0?

The built-in voltage of an open-circuit pn junction is:

$$\Phi_0 = V_T \ln\left(\frac{N_A N_D}{N_i^2}\right) \tag{1}$$

$$V_T = \frac{kT}{q} \tag{2}$$

Where T is the temperature in degrees Kelvin ($\cong 300^o K$) at room temperature, k is the Boltzmann's constant $1.38 \times 10^{-23} JK^{-1}$, and q is hte charge of an electron ($1.602 \times 10^{-19} C$). At room temperature, $V_T \approx 26mV$

In this problem $N_A = 5 \times 10^{22} \frac{holes}{m^3}$, $N_D = 10^{25} \frac{electrons}{m^3}$, $n_i = 1.1 \times 10^{16} \frac{carriers}{m^3}$ and $T = 289K$. By using equation 1 and 2 we get:

$$V_T = \frac{1.38 \times 10^{-23} JK^{-1} \times 289K}{1.602 \times 10^{-19} C} = 0.025V \tag{3}$$

and

$$\Phi_0 = 0.025V \ln\left(\frac{5 \times 10^{22} \frac{holes}{m^3} \times 10^{25} \frac{electrons}{m^3}}{(1.1 \times 10^{16} \frac{carriers}{m^3})^2}\right) = 0.899V \tag{4}$$

The built-in junction potential $\Phi_0 = 899mV$

Problem 2

A piece of Silicon is doped with arsenic at a concentration of $4 \times 10^2 5 \frac{atoms}{m^3}$

a) Is the material n-type or p-type?

This material is called n-type dopants since the free carriers resulting from their use have negative vharge.

b) The temperature is $300K$ and the intrinsic carrier concentration n_i at this temperature is $1.1 \times 10^1 6 \frac{carriers}{m^3}$. Estimate the carrier concentrations.

Since we have an n-type impurity used, the total number of negative carriers or electrons is almost the same as the doping concentration, and is much greater than the number of free electrons in intrinsic silicon. In other words,

$$n_n = N_D$$

where n_n denotes the free-electron concentration in n-type material and N_D is the doping concentration. We can therefore estimate that the carrier concentration will be approximately $4 \times 10^{25} \frac{atoms}{m^3}$

c) Estimate the electron and hole concentrations in the same material at a temperature of $322K$.

The number of carriers approximately doubles for every 11^oC increase in temperature.

Therefore we will get that the electron and hole concentrationw in the same material at a temperature of $322K$ is equal total to

$$4 \times 10^{25} \frac{atoms}{m^3} \times 2^2 = 1.6 \times 10^{25} \frac{atoms}{m^3}$$

d) How does a change in temperature change the conductivity σ of:

1. Intrinsic silicon?

An increased tempeature will increase the conductivity, while a decreased temperature will have the opposite result.

2. Extrinsic (heavily doped) silicon?

   With the extrinsic silicon the the carrier concentration will increace linear at low temperatures, and then increase exponentialy at high temperatures as the ammount of holes/electrons is given by:

$$p_n = \frac{n_i^2}{N_D}$$
$$n_p = \frac{n_i^2}{N_A}$$

   The higher the carrier concentration, the higher the conductivity will be.

Problem 3

The pn-junction in Figure 1 was fabricated using a $100\mu m \times 100\mu m$ mask. The pnjunction is backward biased with a 5 V voltage source, as is shown in the Figure 1. Due to thermal generation, 3.2×10^7 new electron-hole pairs are generated each second in the depletion region of the diode.

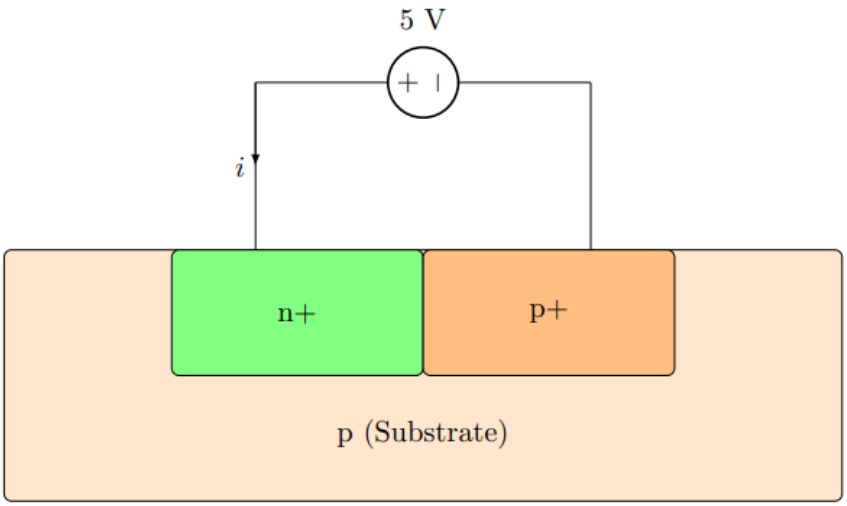

Figure 1: A pn-junction in a p-type substrate is reverse biased with a 5 V voltage source.

a) How much reverse leakage current will flow in the diode? (HINT: The charge of an electron is $q = 1.6 \times 10^{-19} C$)

We wan use the formula

$$I = q \times n \times A$$

Where I is the current, q is the charge of electron, n is the number of electropn-hole pairs generated per second and A is the cross-sectional area of the diode. Given that 3.2×10^7 new electron-hole pairs are generated each second in the depletion region of the diode, this equals to

$$I = 1.6 \times 10^{-19} C \times 3.2 \times 10^7 s^{-1} \times 100\mu m \times 100\mu m = 5.12 \times 10^{-20} A$$

b) Does this current depend on the reverse bias voltage? Why?

This current does not depend on the reverse bias voltage as the current is determined by the the thermal generation, which is primarily affected by the temperature.

c) Does this current increase or decrease if the temperature increases? Why?

As answered in problem 3b) the current is affected by the increase or decrease of the temperature, this is because the number of carriers approximately doubles for every 11^oC increase in temperature. This means that a increased temperature will result in an increased thermal generation.

d) Next to this diode, another similar diode was fabricated using a $200\mu m \times 200\mu m$ mask. How much is the reverse leakage current in this diode, if the temperature and the bias voltage are the same as with the $200\mu m \times 200\mu m$ diode?

Using the same equation as in problem 3a) we get

$$I = 1.6 \times 10^{-19}C \times 3.2 \times 10^{7}s^{-1} \times 200\mu m \times 200\mu m = 2.048 \times 10^{-19}A$$

Problem 4

This problem will simulate a diode using AIM-spice. All simulations should be performed at room temperature (27^o).

a) Describe the circuit of Figure 1 in AIM-Spice using the diode model 'DBSBdiode.mod' found on blackboard. The model files found on blackboard models a $100\mu m \times 100\mu m$ diode

Problem 5

A pn-junction has donor and acceptor concentrations of $N_D = 2.5 \times 10^{18} cm^{-3}$ and $N_A = 1.2 \times 10^{23} cm^{-3}$. Assume room temperature and $\Phi_0 = 0.566V$. Calculate the depletion region depths (X_n, X_p) for a reverse bias of $1.1V$. Any comments to your results?

Given $(N_A >> N_D)$ we can approximate that

$$x_n \cong \left[\frac{2\,K_s\varepsilon_0\,(\Phi_0 + V_R)}{qN_D}\right]^{1/2} x_p \cong \left[\frac{2\,K_s\varepsilon_0\,(\Phi_0 + V_R)\,N_D}{qN_A^2}\right]^{1/2}$$

Here, ε_0 is the permittivity of free space (equal to 8.854×10^{-12} F/m), V_R is the reverse-bias voltage of the diode, and $K_s = 11.8$ is the relative permittivity of silicon. By replacing the variables in the equation above with the given values, we get:

$$X_n \cong \left[\frac{2 \times 11.7 \times 8.854 \times 10^{-12}\,\text{F/m} \times (0.566\,\text{V} + 1.1\,\text{V})}{1.6 \times 10^{-19}\,\text{C} \times 2.5 \times 10^{18}\,\text{cm}^{-3}}\right]^{1/2}$$

$$X_p \cong \left[\frac{2 \times 11.7 \times 8.854 \times 10^{-12}\,\text{F/m} \times (0.566\,\text{V} + 1.1\,\text{V}) \times 2.5 \times 10^{18}\,\text{cm}^{-3}}{1.6 \times 10^{-19}\,\text{C} \times (1.2 \times 10^{23}\,\text{cm}^{-3})^2}\right]^{1/2}$$

This equals to:

$$X_n \approx 0.0294\mu\text{m}$$
$$X_p \approx 6.12 \times 10^{-7}\mu\text{m}$$

Here we can se that X_n is substantialy larger than X_p. This case is called a single-sided diode.

Problem 6

The small-signal model of a forward-biased diode, from chapter 1 in Analog Integrated Circuit Design by Carusone, Johns and Martin (”CJM”), includes two capacitances.

a) Give a brief explanation about each of the two capacitive contributions and how they emerge.

The two capacitive contributions mentioned in the 1st chapter in Analog Integrated Circuit Design by Carusone is depletion capitance, C_j and diffusion capacitance also called diffusion capacitance C_d

The depletion capitance, C_j arises from the depletion region of a pn-junction. This region comes from charge carriers from both side recombine, creating a region around the junction with immobile charges. This creates an electric field. When we apply reverse bias to the pn-junction, the depletion region widens, and the electric field increases. This behavior can be modeled as a parallel-plate capacitor, where the "plates" are the n-type and p-type regions separated by the depletion region. This capacitance is given by:

$$\mathrm{C_j} = \frac{\mathrm{C_{j0}}}{\left(1 + \frac{\mathrm{V_B}}{\Phi_0}\right)^{\mathrm{m_j}}}$$

where

$$\mathrm{C_{j0}} = \left(1 - \mathrm{m_j}\right)\left[2\mathrm{qK_s}\varepsilon_0 \frac{\mathrm{N_A N_D}}{\mathrm{N_A + N_D}}\right]^{1-\mathrm{m_j}} \frac{1}{\Phi_0^{\mathrm{m_j}}}$$

The diffusion capitance arises from the movement of charge carriers across the junction under forward bias conditions. This process can be modelled as a capacitor storing charge. When a forward bias is applied, C_d is given by:

$$\mathrm{C_d} = \tau_\mathrm{T} \frac{\mathrm{I_D}}{\mathrm{V_T}}$$

b) A diode is biased for a current of $1mA$, and has a transit time of $50ps$. Estimate it's small-signal resistance and diffusion capacitance.

By using the equation for C_d above and assuming that we are in room temperature; $V_T \approx 26mV$ at roomtemperature, we get that $C_D = 3.846 \times 10^{-13} F$.

Appendix