TFE 4152 Design of Integrated Circuits

Exercise 5

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Contents

Problem 1

a) Assume that both the gate lengths as well as W_n for the 45 nm technology in Table 1.5 in "CJM", can have dimensions down to 45 nm. Use $V_{dd} = 1.2$ V. Construct an unskewed static CMOS inverter and explain your choices of transistor dimensions.

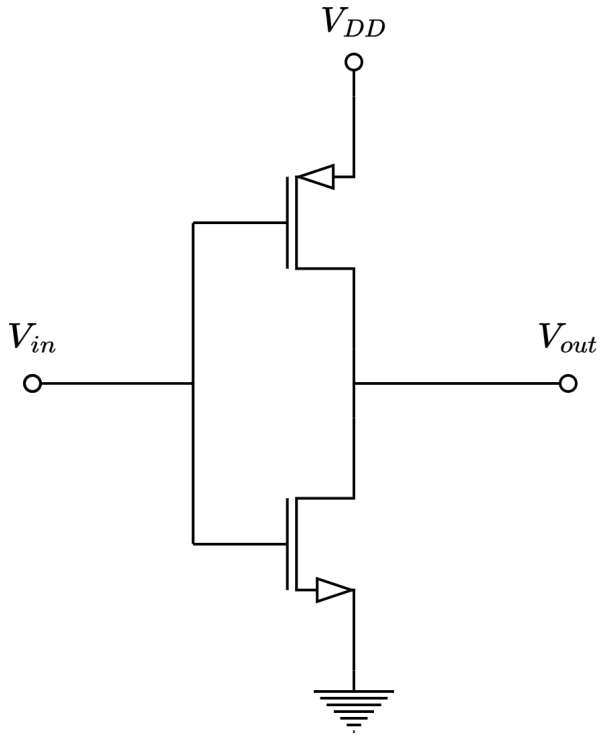

Figure 1: Transistor circuit of a static CMOS inverter

As the goal is to make an unskewed static cmos, we need booth the NMOS and CMOS transistors to have an equal rise and fall time of the output signal. As seen in Table 1.5 in "CJM" the mobility of the NMOS ($280\mu C_{ox}$) is a lot more than the mobility of the CMOS ($70\mu C_{ox}$).

We can use the equation for drive current I_D in saturation to determine what the dimmensions should be

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{tn})^2$$

As we want both current to be the same we get

$$\mu_n C_{ox} \frac{W_p}{L_p} = \mu_p C_{ox} \frac{W_n}{L_n}$$
$$70 \frac{W_p}{L_p} = 280 \frac{W_n}{L_n}$$
$$\frac{W_p}{L_p} = 4 \frac{W_n}{L_n}$$

To ensure the unskewed property, I will keep L the same for both mosfets.

Table 1: Transistor dimmensions

	NMOS	PMOS
W	$45nm$	$180nm$
L	$45nm$	$45nm$

b) For which technologies in Table 1.5 in CJM is it not possible to make a so called symmetric inverter? Explain your answer.

As there is no design rules I'll assume that we can just increase the width of the PMOS to make the transistors symmetric like we did in the previous problem. Therefore the PMOS can always be sized larger to compensate for its lower mobility. We do however see that $0.8\mu m$ and $0.35\mu m$ doesnt have a similar magnitude of V_{t0}, making them more difficult to make symmetric.

c) Why may a symmetric inverter be more desirable than a non-symmetric one? Explain your answer.

We would like a symmetric inverter as

1. They provide consistent signal propagation delays for both high-to-low and low-to-high transitions, which is important for timing analysis and clock distribution.
2. They improve the noise margins, making the circuit more robust to variations in voltage levels.
3. They can help in achieving a more predictable and stable operation of the digital circuit.

d) Use $V_{dd} = 1.2$ V and the 45 nm technology mentioned above. Estimate the parasitic resistances, R_p and R_n, for the PMOS and NMOS transistors in the inverter at the switching point.

$$R_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{DD} - V_t)}$$

$$R_n = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{t0})} = \frac{1}{280 \cdot 10^{-6} \cdot (1.2 - 0.45)} = 23.8k\Omega$$

$$R_n = \frac{1}{\mu_p C_{ox}\frac{W_p}{L_p}(V_{GS} - V_{t0})} = \frac{1}{7010^{-6} \cdot \cdot \frac{180}{45} \cdot (1.2 + 0.45)} = 23.8k\Omega$$

e) Find expressions for the rise- and fall-times for the symmetric inverter from problem 1 a) when 10% and 90% of the full voltage swing are used as limits for the corresponding rise- and fall-times. (The lecture notes from October 23rd contain information that might be useful.)

Fall time

$$t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right) \quad , \tau_n = R_n C_{out}$$

$$\begin{aligned} t_f &= \tau_n \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right) \\ &= \tau_n \ln(10) - \tau_n \ln\left(\frac{10}{9}\right) \\ &= \tau_n \ln(9) \\ &= \tau_n 2.2 \end{aligned}$$

Rise time

$$\begin{aligned} t_r &= \tau_p \ln\left(\frac{1}{9}\right) \\ &= \tau_p 2.2 \end{aligned}$$

f) Assume that the total capacitance seen on the output of the inverter is 5fF**. Estimate the rise- and fall-times when** 10% **and** 90% **are used as limits.**

$$t_n = R_n \cdot C_{out} \cdot 2.2 = 23.8 \cdot 10^3 \cdot 5 \cdot 10^{-9} \cdot 2.2 = 0.2618mS$$
$$t_p = R_p \cdot C_{out} \cdot 2.2 = 23.8 \cdot 10^3 \cdot 5 \cdot 10^{-9} \cdot 2.2 = 0.2618mS$$

g) What is the maximum operating frequency of the inverter from 1f **)?**

$$f_{max} = \frac{1}{t_r + t_f} = \frac{1}{2 * 0.0002618} = 3820$$

h) An inverter has a V_{OH} of 1.92 V, **V_{IH} of** 1.58 V, **V_{IL} of** 0.68 V **and a V_{OL} of 0.17 V. Find it's noise margins, NM_H and NM_L, as defined in your textbook by Weste Harris.**

$$NM_L = V_{IL} - V_{OL} = 0.68V - 0.17V = 0.51V$$
$$NM_H = V_{OH} - V_{IH} = 1.92V - 1.58V = 0.34V$$

i) Consider when two such inverters are coupled in series, and the voltage at the output of the first one drops by 0.5 V **when the first inverter outputs the worst-case logic 1. Which consequences could follow?**

This can result in V_{OH} from the first inverter being lower than V_{HI} on the second inverter, making the second inverter interpet the inputsignal as low.

j) Similarly - what could happen if 0.5 V **of noise were added to a worst-case logic low signal at the output of the first inverter?**

This can result in V_{OL} from the first inverter being higher than V_{IL} on the second inverter, making the second inverter interpet the inputsignal as high.

k) Explain about one or more important differences between latches and flip-flops.

Flip-flops are edge triggered, while latches are input triggered

1) Draw a timing diagram including the data input signal, the clock signal, and the Q and Q' outputs for a negative-edge triggered D-flip-flop.

Table 2: Timing diagram

D	CLK	Q	Q'
x	$\uparrow$	Q	Q'
0	$\downarrow$	0	1
1	$\downarrow$	1	0

Problem 2

The following problems are related to the design of a Finite State Machine. The lecture notes from the 11th of October might be useful for some of the questions. (Those who did exercise 4 may find it useful to reuse parts of their solutions in this problem).

a) Make a state diagram that describes a Finite State Machine ("FSM") that detects sequences of 101 on it's x input. The output, y, should be high if, and only if, the mentioned sequence is detected.

If your FSM should happen to enter any undefined state, let it return to the initial state when the earliest input is detected.

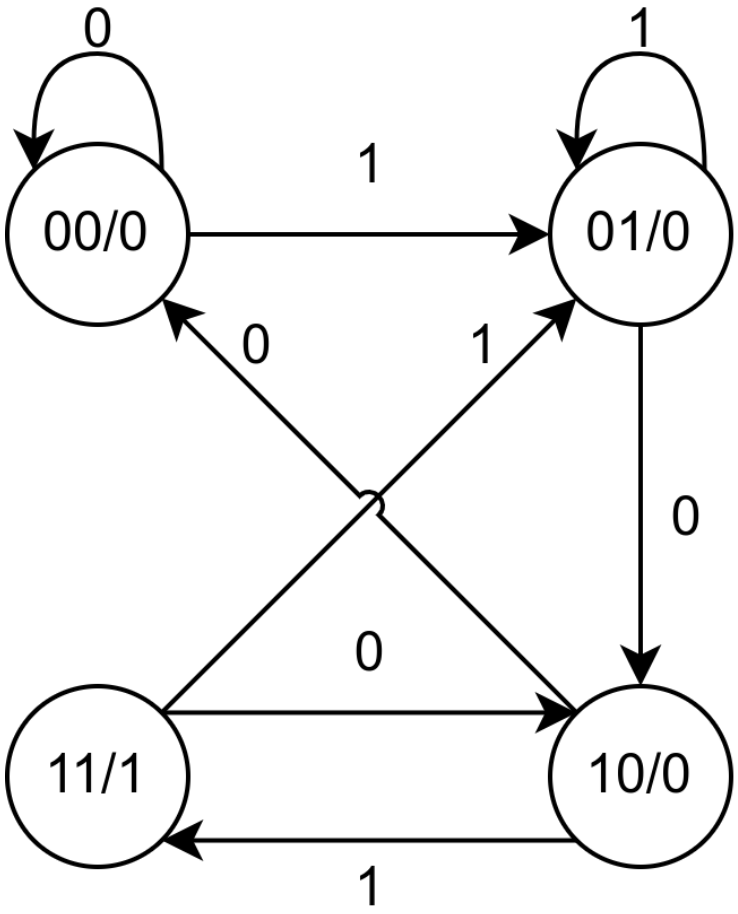

Figure 2: a Finite State Machine ("FSM") that detects sequences of 101 on it's x input.

b) Show the corresponding state table.

Table 3: State table

Current state		Input	Next state		Output
A	B	x	A_{next}	B_{next}	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	0	1	1

c) Use one or more positive edge triggered D-flip-flops and find the flip-flop input equations, as well as a Boolean expression for the y output.

$$y = AB\bar{x} + ABx = AB$$

Table 4: A

A	B	x=0	x=1
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	0

Table 5: B

A	B	x=0	x=1
0	0	0	1
0	1	0	1
1	0	0	1
1	1	0	1

d) Show how the combinatorial logic part could be implemented in Verilog, for a Moore machine implementation (where the output is defined by the state only).

```
module FSM(
    input A;
    input B;
    output y;

);
and g1(y, A, B)
end module
```

e) Estimate the total number of transistors that would be needed to implement your combinatorial logic part of the FSM from the previous problem, assuming that you are restricted to basic Boolean gates (NAND, NOR, INVERT, XOR et cetera).

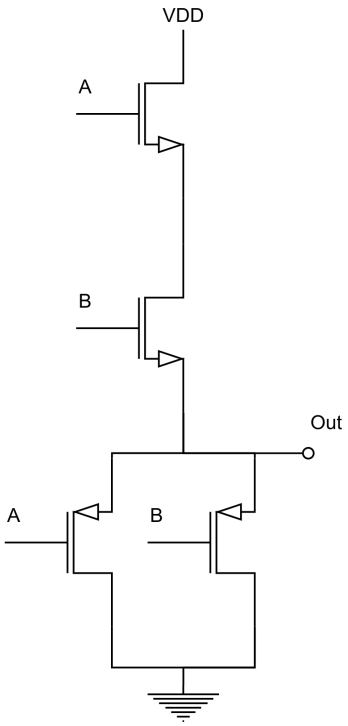

Figure 3: AND gate using transistors

Using the design in figure 3, we need a total of 4 transistors to implement the combinatorial logic part of the FSM

f) Using the same restrictions as for the previous question, try and see if you can find an implementation that uses fewer transistors. What's the total number now?

No, my design is perfect.

g) Are you aware of any logic implementation style other than static CMOS that might have been used for the implementation of the combinatorial logic?

no, not yet. I assume that there is given this question.

h) Choose one alternative logic implementation style and mention one potential positive side of the alternative, and one negative.

you could implement it using a NAND and a NOT gate to implement the same, which would be worse as it would require more transistors (6) (using CMOS)

i) Explain how you would like to simulate the FSM, and verify it's functionality. How should the input signal and the clock signal be related, for example?

I would simulate it in a simple logic gate simulator on web as this isnt the most complex FSM. I would expect the FSM to trigger whenever clock goes from low to high.