TFE 4152 Design of Integrated Circuits

Exercise 4

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2023-10-25

Contents

Problem 1

Sketch transistor-level schematics for each of the following functions using CMOS logic.

a) $Y_1 = A'B + AC'$

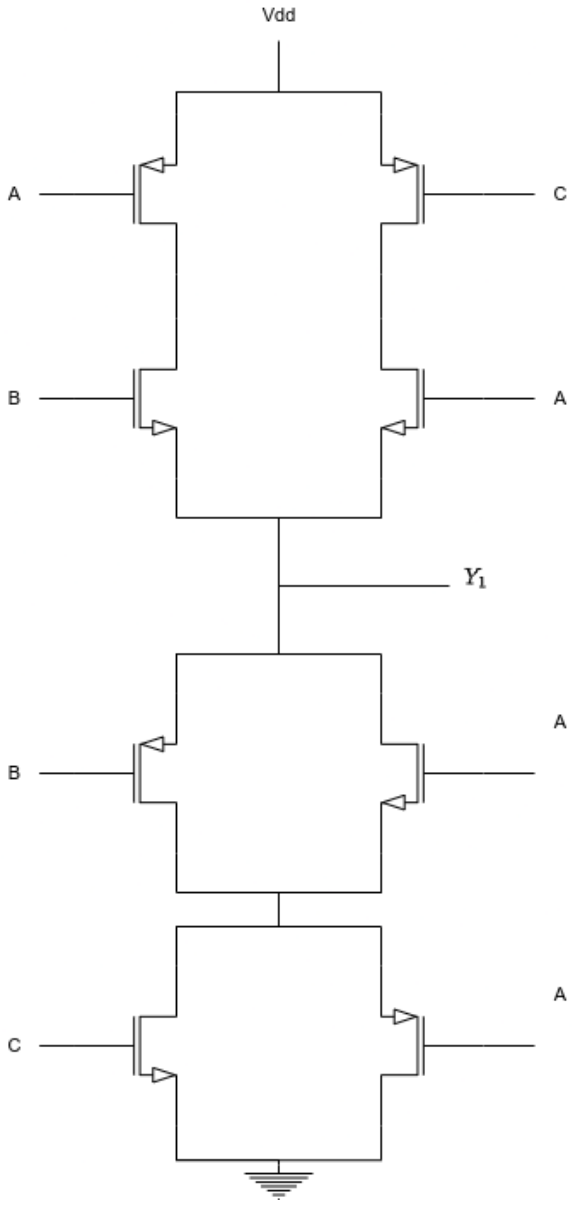

Figure 1: implementation of $Y_1 = A'B + AC'$.

b) $Y_2 = A'BC + AB' + A'B'C$

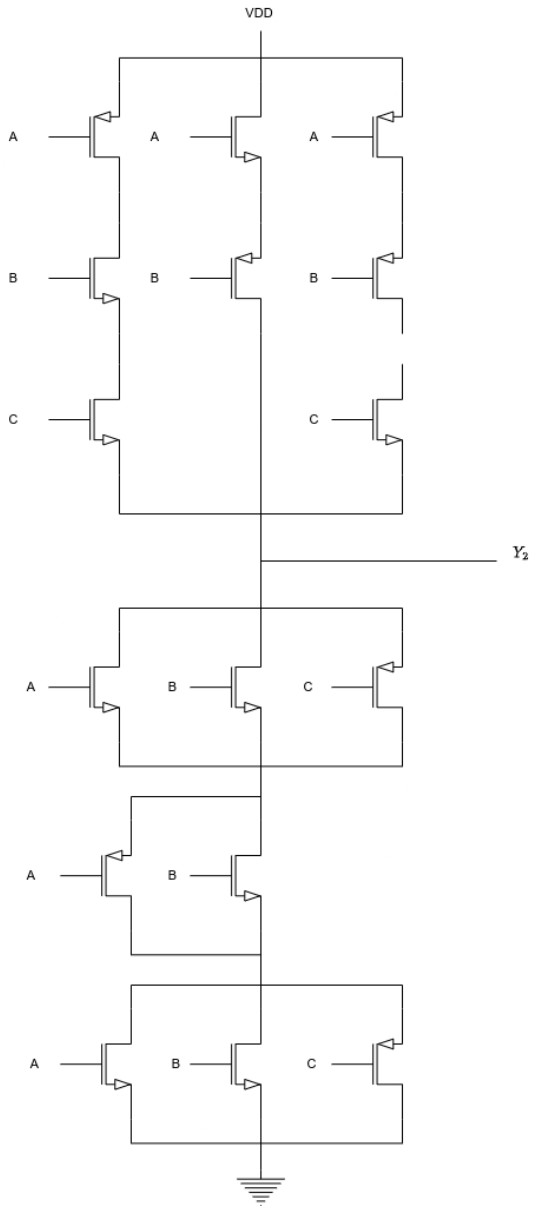

Figure 2: implementation of $Y_2 = A'BC + AB' + A'B'C$

c) The logic implementation style that is most common is static CMOS. Can you explain about any reasons for this?

As CMOS circuits composes of a pull-up network, which is a set of PMOS transistors connected between VDD and the output line and pull-down network, which is a set of NMOS transistors connected between GND and the output line. This way there wil never be a direct path between

VDD and GND. This offers a strong immunity from noise.

d) Show how you could implement the function $Y_3 = xz' + x'y$ using basic Boolean gates (like for example NAND2, INV, OR etc). Aim for the lowest number of transistors for your implementation, having static CMOS in mind. What's your total number of transistors, then?

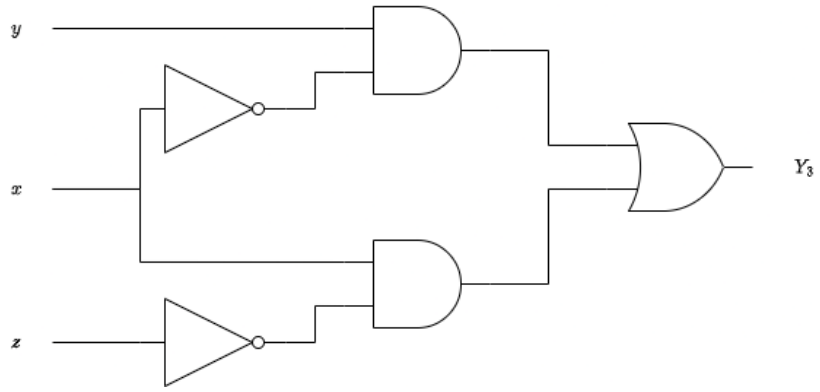

Figure 3: implementation of $Y_3 = xz' + x'y$ using basic boolean gates

Using this implementation I have use 16 transistors.

e) Write your own gate-level Verilog code that implements the Boolean function $D_A = A'B + AC$ '.

```
module D_a ( A ,B ,C ,d_a );
input A ;
wire A ;
input B ;
wire B ;
input C ;
wire C ;
output d_a ;
wire d_a ;
//}} End of automatically maintained section
not G1(An, A);
not G2(Cn, C);
and G3(AnB, An, B);
and G4(CnA, Cn, A);
or G5(d_a, CnA, AnB);
endmodule
```

g) Use File → New → Waveform ... and Stimulators to make a simulation demonstrating that the function D_A = A′B + AC ', based on your code, demonstrating the correct functionality. Include a screendump showing the simulated results, and compare them to a truth table for the function. Comment on your results.

Table 1: Truth table for $D_A = A'B + AC'$

A	B	C	Y_1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

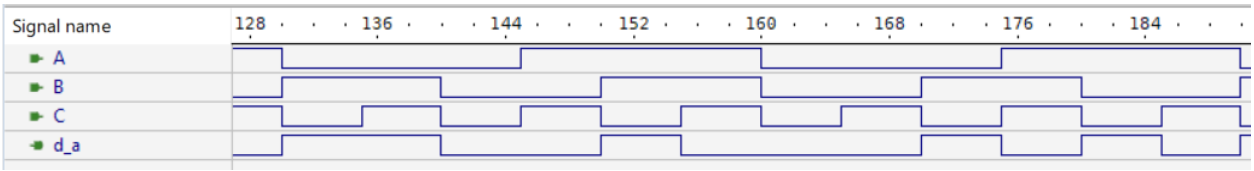

Figure 4: Simulation demostrating the function D_A = A′B + AC.

After carefully inpecting the simulation and the truth table, I can confirm that I somehow didn't fail.

Problem 2

A NMOS switch is connected in series with an inverter as seen in Figure 5. Assume that the total capacitance at node X is C_X = 12fF, that $V_A = V_{DD}$ = 1.8 V and that C_x is initially discharged to 0 V**. M1 and M3 both have** W = 0.5μm **and** L = 0.22μm**. M2 have** W = 1.5μm **and** L = 0.18μm**. Use process parameters for the** 0.18μm **CMOS process in Table 2. You may ignore channel length modulation and the body effect.**

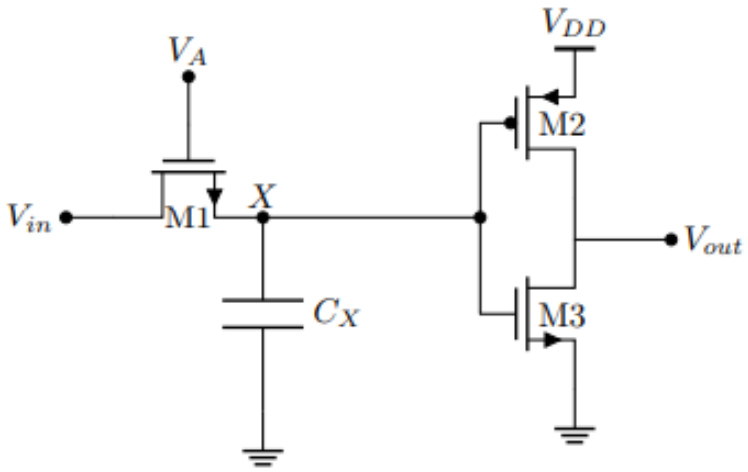

Figure 5: Inverter driven by a single NMOS switch.

Table 2: MOSFET parameters for a 180 nm transistor technology, from CJM.

Parameter	NMOS	PMOS
Technology	180 nm	
μC_{ox} [µA/V^2]	270	70
V_t [V]	0.45	-0.45
λL [µm/V]	0.08	0.08
C_{ox} [fF/µm^2]	8.5	8.5
t_{ox} [nm]	5	5
n	1.6	1.7
σ [1/V]	1.7	1.0
m	1.6	2.4
$C_{ov}/W = L_{ov}C_{ox}$ [fF/µm]	0.35	0.35
$C_{db}/W = C_{sb}/W$ [fF/µm]	0.50	0.55

a) Ignoring subthreshold operation of transistor M1, what is the voltage that would occur on node X if V_{in} changed from 0 V to $0.9V_{DD}$?

By the ignoring subthreshold operation, we can assume that I_D is given by

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2$$

in terms of M2 (PMOS):

$$I_{D2} = \frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2} (V_{DD} - V_X - V_t)^2$$

and for M3 (NMOS):

$$I_{D3} = \frac{\mu_n C_{ox}}{2} \frac{W_3}{L_3} (V_X - V_t)^2$$

At switching we have that

$$\frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2} (V_{DD} - V_X - V_t)^2 = \frac{\mu_n C_{ox}}{2} \frac{W_3}{L_3} (V_X - V_t)^2$$

$$\frac{\frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2}}{\frac{\mu_n C_{ox}}{2} \frac{W_3}{L_3}} (V_{DD} - V_X - V_t)^2 = (V_X - V_t)^2$$

$$\frac{\frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2}}{\frac{\mu_n C_{ox}}{2} \frac{W_3}{L_3}} (V_{DD} - V_t)^2 - 2 (V_{DD} - V_t) V_X + V_X^2 = V_X^2 - 2V_X V_t + V_t^2$$

$$\frac{\frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2}}{\frac{\mu_n C_{ox}}{2} \frac{W_3}{L_3}} (V_{DD} - V_t)^2 - 2 (V_{DD} - V_t) V_X + V_X^2 - V_t^2 = V_X^2 - 2V_X V_t$$

solving in python:

```
from sympy import symbols, solve

# Redefining the variables and the given equation
mu_n, C_ox, W_2, L_2, W_3, L_3, V_DD, V_t, V_X =
symbols('mu_n C_ox W_2 L_2 W_3 L_3 V_DD V_t V_X')

# Given equation
equation = (mu_n*C_ox/2 * (W_2/L_2) / (mu_n*C_ox/2 * (W_3/L_3))) *
 (V_DD - V_X - V_t)**2 - (V_X - V_t)**2
```

```
10
11 # Solving for V_X
12 V_X_solution = solve(equation, V_X)
13 print(V_X_solution)
14 [(L_2*V_t*W_3 - L_3*V_DD*W_2 + L_3*V_t*W_2 + sqrt(L_2*L_3*W_2*W_3)*
15 (-V_DD + 2*V_t))/(L_2*W_3 - L_3*W_2), (L_2*V_t*W_3 - L_3*V_DD*W_2 +
16 L_3*V_t*W_2 + sqrt(L_2*L_3*W_2*W_3)*(V_DD - 2*V_t))/(L_2*W_3 - L_3*W_2)]
```

$$V_X = \frac{L_2 V_t W_3 - L_3 V_{DD} W_2 + L_3 V_t W_2 \pm \sqrt{L_2 L_3 W_2 W_3}\,(-V_{DD} + 2V_t)}{L_2 W_3 - L_3 W_2}$$

this is wrong, the kok says $V_X = V_A - V_t = 1.8V - 0.45V = 1.35V$

> *wtf!??? I give up in life, fuck this*
> — Peter Pham, 20:43 2023-10-25

> *I'll never work with transistors when I finish stuDYING, NOBODY understand this shit*
> — Miki Tecle Hagos, 17:32 2023-10-25 : after looking at this problem for 3 hours

b) How can you decrease the rise-time for the voltage signal at node X by changing the switch transistor M1? Explain.

As the current dependent on $I_D \propto \frac{W}{L}$, we can increase the width to increase the current, that way the capacitor will charge up faster and give us a decreased rise-time.

Problem 3

Draw the schematics for a similar state machine (”Moore type”) that detects sequences”101”, and output a logic 1 if, and only if, such a sequence is detected.

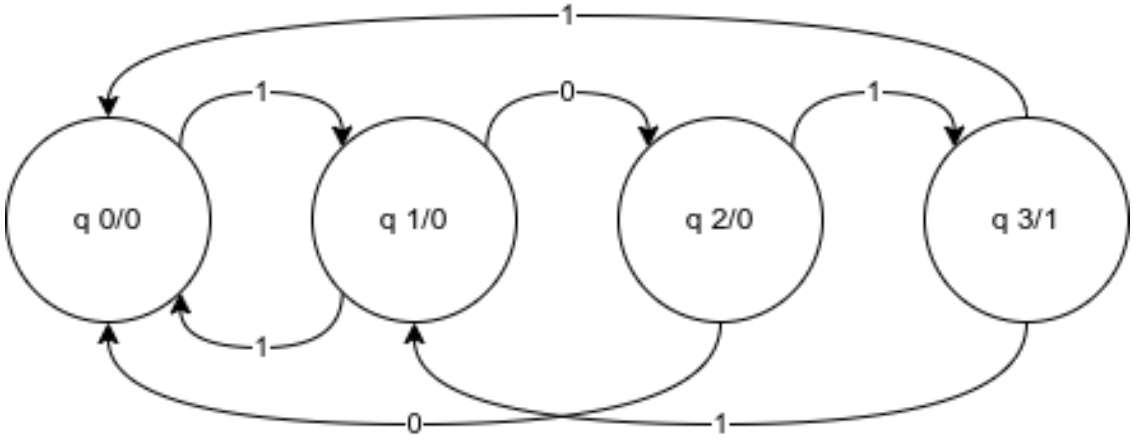

Figure 6: Moore machine

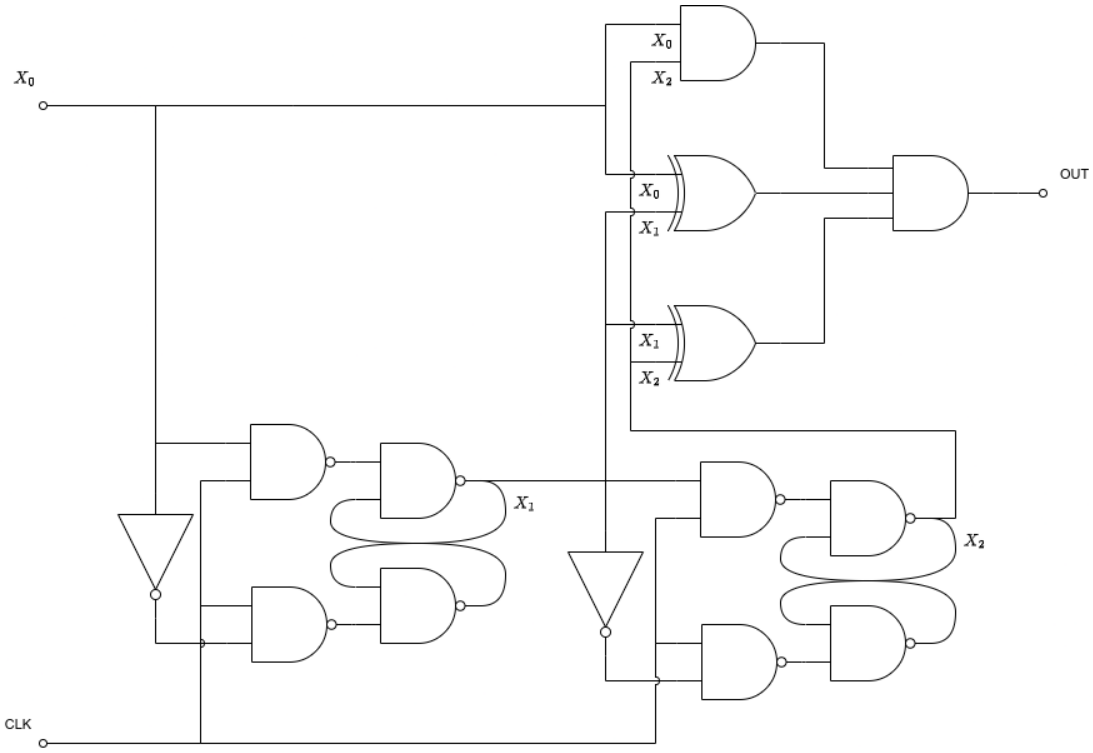

Figure 7: Schematic using Boolean logic gates

It started as:

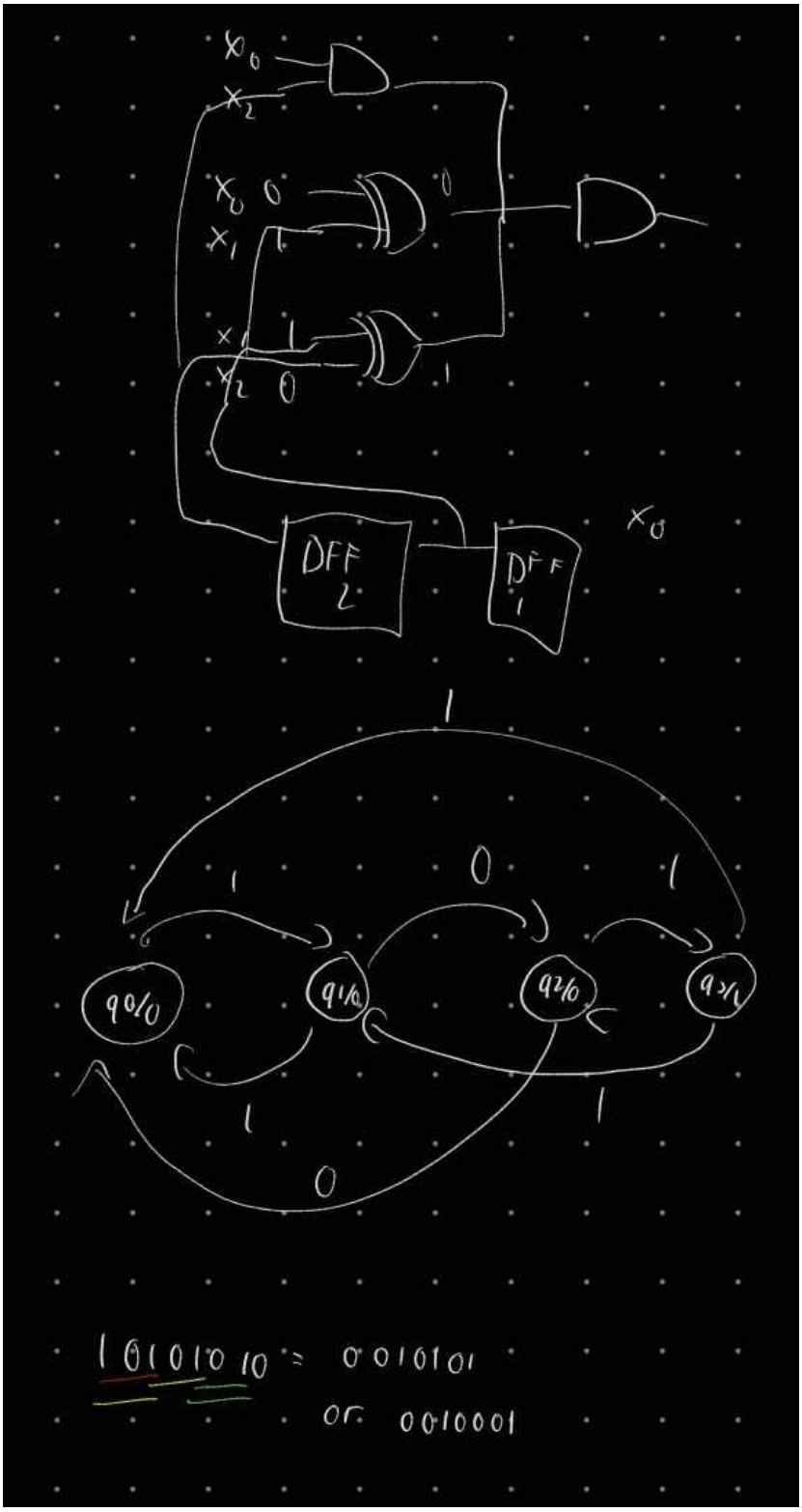

Figure 8: It all began with...

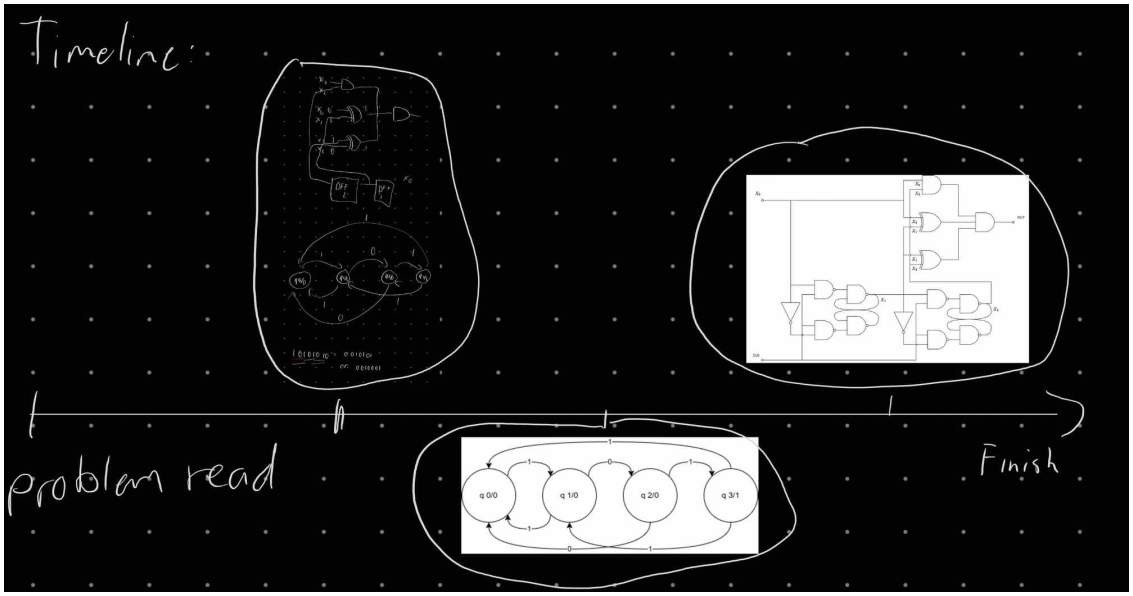

Figure 9: The diffrent steps, from making the state diagram until the schematics including Boolean logic gates

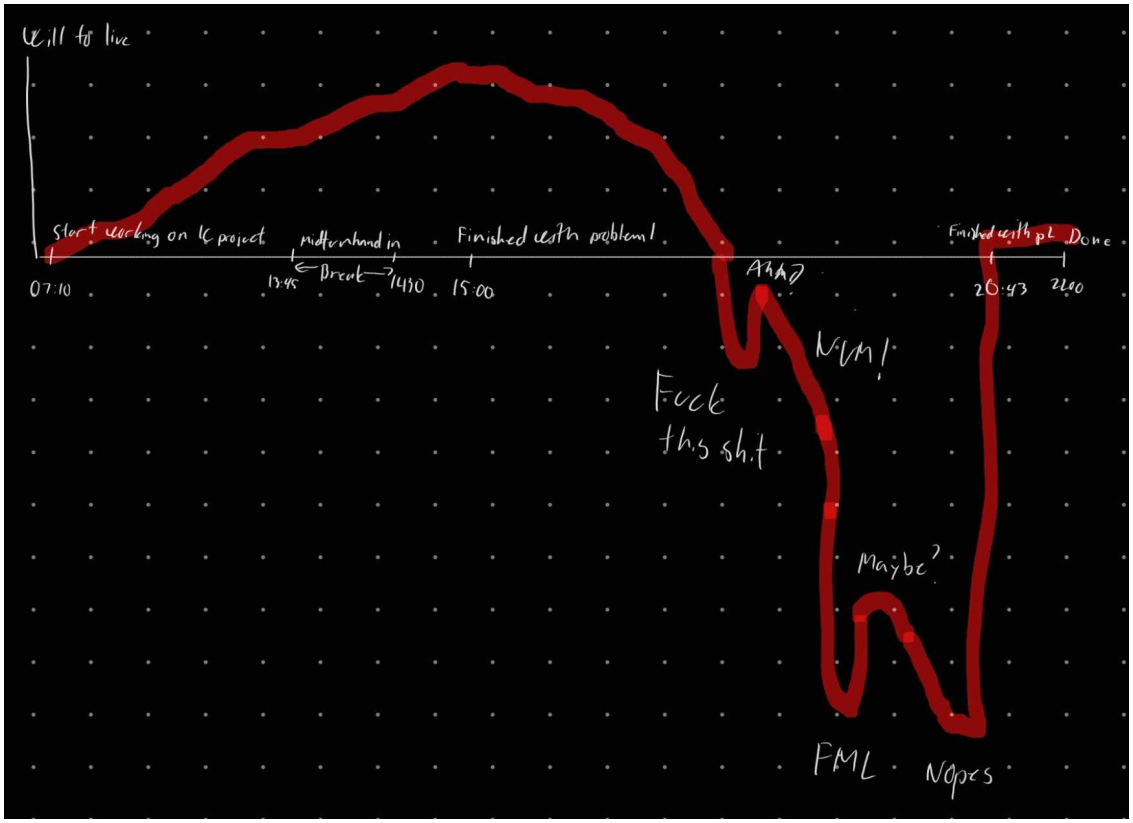

Figure 10: You owe me my braincells back

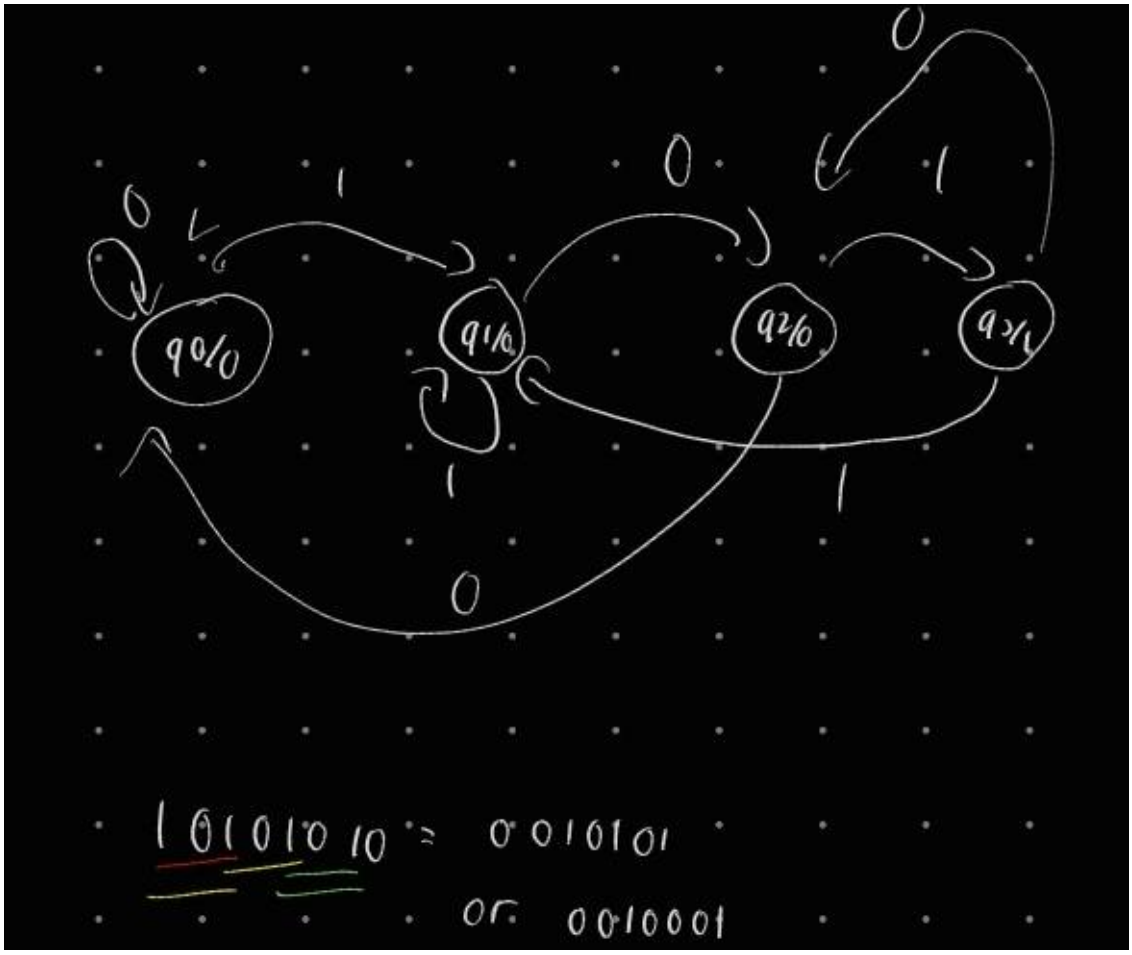

Figure 11: whoop, realised that I was wrong, revised plot

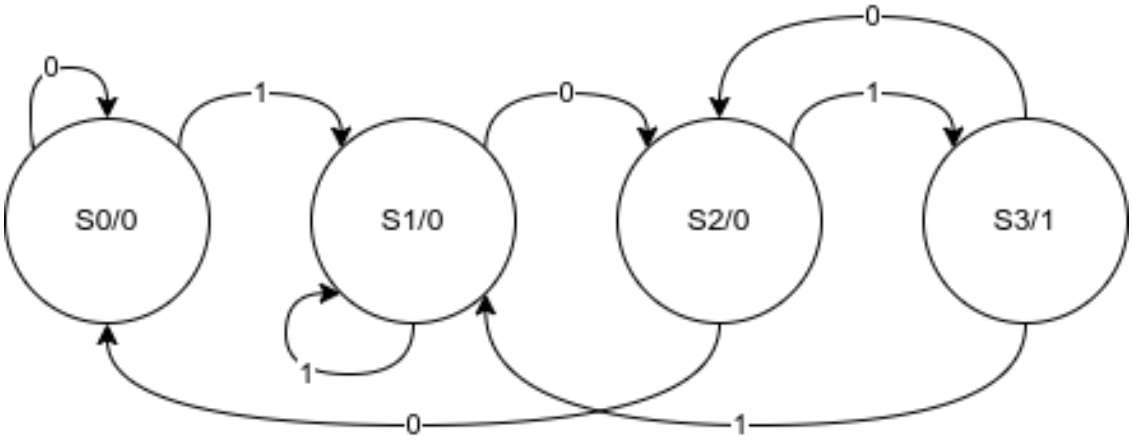

Figure 12: Revised schematic

The schematic using Boolean logic gates was done correctly tho, hopefully. . .

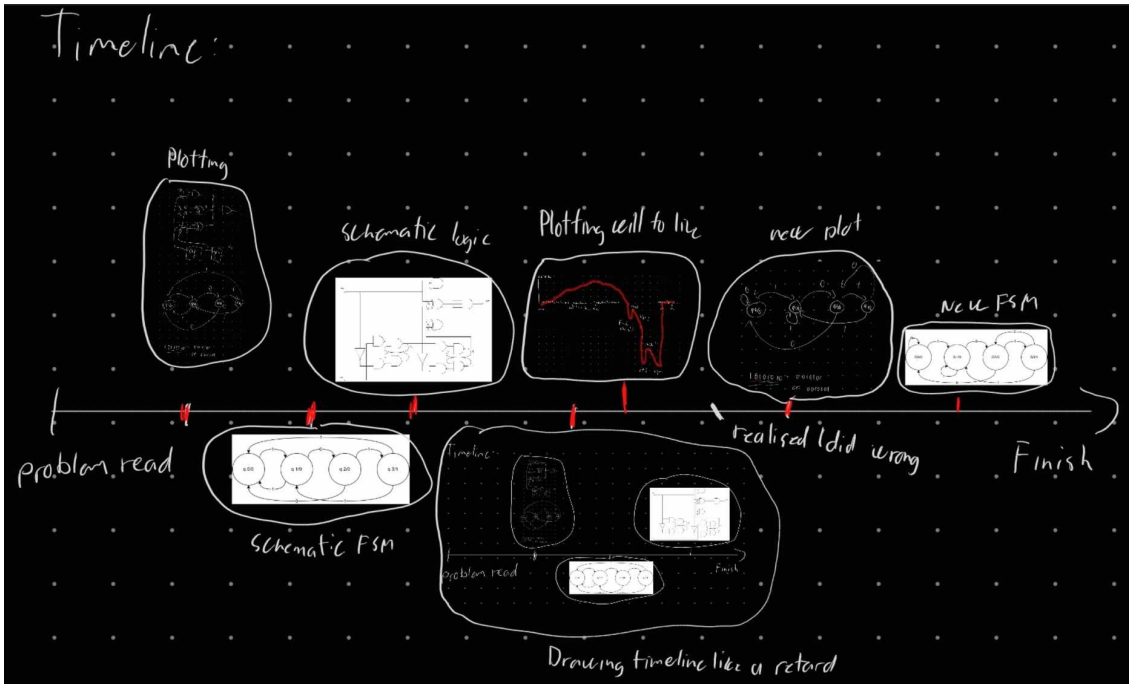

Figure 13: The_diffrent_steps,_from_making_the_state_diagram_until_the_schematics_including _Boolean_logic_gates_V2

My last 3 braincells at 22:34: Here