TFE 4152 Design of Integrated Circuits

Exercise 2

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Contents

Problem 1

From the problem text, we are given this information:

Table 1: NMOS Transistor Parameters in 180 nm Technology

Parameter	Unit/Equation	Value
V_{eff}	V	0.2
V_{Drain}	V	0.2
V_{Source}	V	0
W	μm	0.5
L	μm	0.2
T	K	293
μC_{OX}	$\frac{\mu\text{A}}{\text{V}^2}$	270
V_{t0}	V	0.45
$\lambda \cdot L$	$\frac{\mu\text{m}}{\text{V}}$	0.08
C_{OX}	$\frac{\text{fF}}{\mu\text{m}^2}$	8.5
t_{OX}	nm	5
n	–	1.6
θ	$\frac{1}{\text{V}}$	1.7
m	–	1.6
$\frac{C_{OV}}{W} = L_{OV}C_{OX}$	$\frac{\text{fF}}{\mu\text{m}}$	0.35
$\frac{C_{db}}{W} \approx \frac{C_{sb}}{W}$	$\frac{\text{fF}}{\mu\text{m}}$	0.5

a) What can you say about the region of operation for the transistor, based on the description above?

The region of operation where $\text{V}_{\text{DS}} > \text{V}_{\text{DS-sat}}$, the drain current is in is independend of V_{DS} and is called the active region:

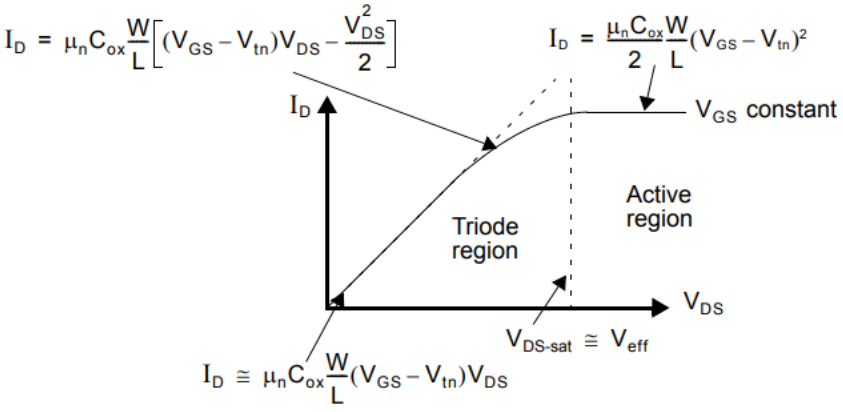


Figure 1: The I_D versus V_{DS} curve for an ideal MOS transistor. For $V_{DS} > V_{DS\text{-sat}}$, I_D is approximately constant.

Based on the paramters in the table and figure above we can say that the region of operation is when $V_{DS} > 0.2V$ as $V_{DS\text{-sat}}$ is given by

$$V_{DS\text{-sat}} = V_{GS} - V_{tn} = V_{eff}$$

b) Consider a similar case as described above. except that V_{DS} is increased by 50mV. Can you estimate the resulting drain current, I_{DS}?

From figure 1, we can se that the current I_D changes marginaly in the active region when V_DS increases, therfore the resulting drain current can be estimated to be

$$I_D = \frac{2.7 \cdot 10^{-4}}{2}\frac{5 \cdot 10^{-5}}{2 \cdot 10^{-5}}(0.2)^2 = 13.5\mu A$$

c) Estimate the maximum value for V_{eff} given that you would avoid mobility degradation for this transistor.

Due to mobility degadation, increases in V_{eff} beyond $\frac{1}{2\theta}$:

- fail to provide significant increases in small-signal transconductance,
- reduce the available signal swing limited by the fixed supply voltages, and
- reduce transistor intrinsic gain A_i dramatically

Therefore the maximum value for V_{eff} given that i would avoid mobility degradation for this transistor is

$$V_{\text{eff}} < \frac{1}{2 \cdot 1.7}$$
$$V_{\text{eff}} < \frac{5}{17} V$$

d) Calculate the small signal output resistance for the transistor when it's operating in the active region, and square-law behaviour holds.

We can use this equation

$$r_o = \frac{1}{\lambda \cdot I_D}$$

to find the small signal output resistance using the current I_D found in b)

$$r_o = \frac{1}{0.4\frac{1}{V} \cdot 13.5\mu A} = 185.2k\Omega$$

e) What would be the small-signal output resistance if the W/L ratio was kept, and the gate length multiplied by 3?

By keeping the W/L ratio, we know that the current I_D will stay the same,

$$\Lambda = \frac{0.08}{0.6} = \frac{2}{15}\frac{1}{V}$$

This gives us

$$r_o = \frac{1}{\frac{2}{15}\frac{1}{V} \cdot 13.5\mu A} = 555.6k\Omega$$

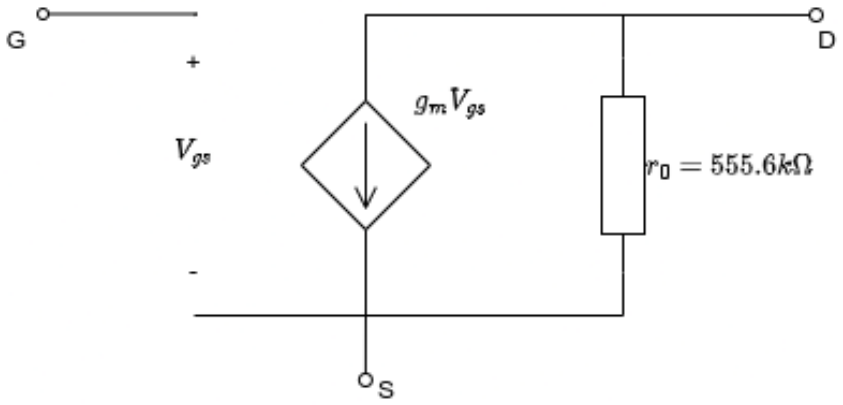
f) Calculate the small-signal transconductance, g_m, for the transistor under the conditions relevant for problem b), above.

The small-signal transconductance, g_m is given by

$$\frac{2I_D}{V_{eff}} = \mu_n C_{ox} \frac{W}{L} V_{eff}$$

$$g_m = \frac{2I_D}{V_{eff}} = \frac{2 \cdot 13.5\mu A}{0.2V} = 1.35 \cdot 10^{-4}$$

g) Indicate roughly the value for g_s and draw the low-frequency small-signal schematics for the transistor in the active region, and include relevant values based on what you have been asked to find, this far. Use r_{out} from 1 d)**.**



h) Problem 1 c) relates to mobility degradation for relatively high values of V_{DS}. Can you point to any other potential problems that could emerge from high V_{DS} voltages, especially for the shortest gate-lengths?

i) Make a sketch of the small-signal diagram from 1 g **), where you include the parasitic capacitances.**

j) Consider the layout in Figure 2.14 in CJM and an implementation in the 0.8μm **process from Table** 1.5in **CJM for your calculations, and Let C_{js} have a value of nfF in your expression. Find an expression for the smallsignal capacitance between the source and bulk nodes.**

k) Estimate the minimum V_{GS} required for this NMOS transistor to be in the active region.

l) Circuits may in some cases operate with a supply voltage below the absolute values of both the pmos and nmos threshold voltages. Could you explain about when this could be beneficial for analog or digital circuits, or both?

Problem 2

Problem 3

Problem 4