TFE 4152 Design of Integrated Circuits

Exercise 3

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Contents

Problem 1

a) Which circuit could the layout in Figure 1 represent? Explain your answer.

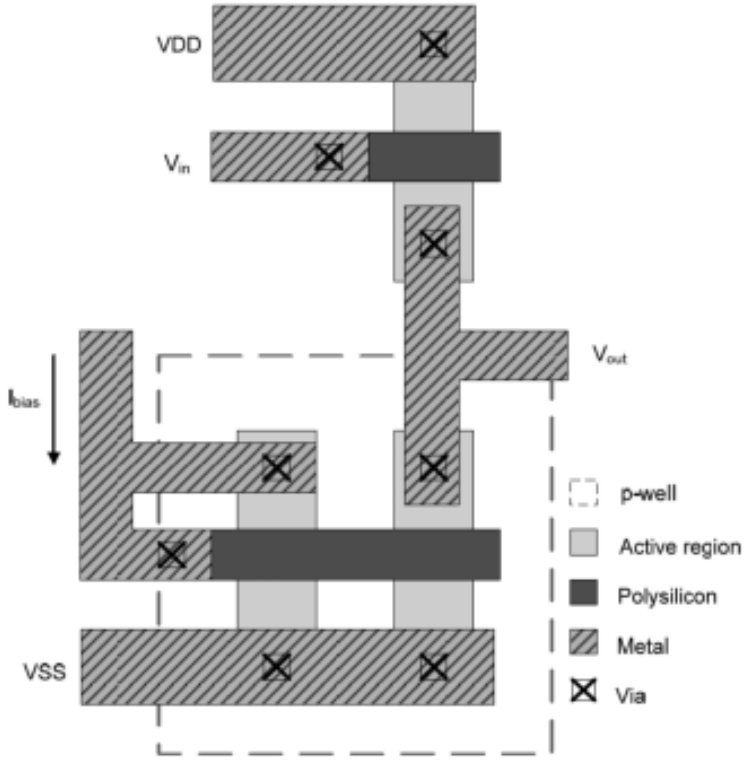

Figure 1: Elements of a layout.

In figure 1 we can se a simple current mirror in the p-well, and a source follower. Here the current mirror supplies the bias current of source-follower. These transistors together are commonly used as *voltage buffers*. Some of the perks of using this circuit as a source foller is that it maintains the signal input signal without affecting the system in itself as it usally have a high input impedanse and low output impedanse, which is important in maintain the amplitude and integrity of the input signal.

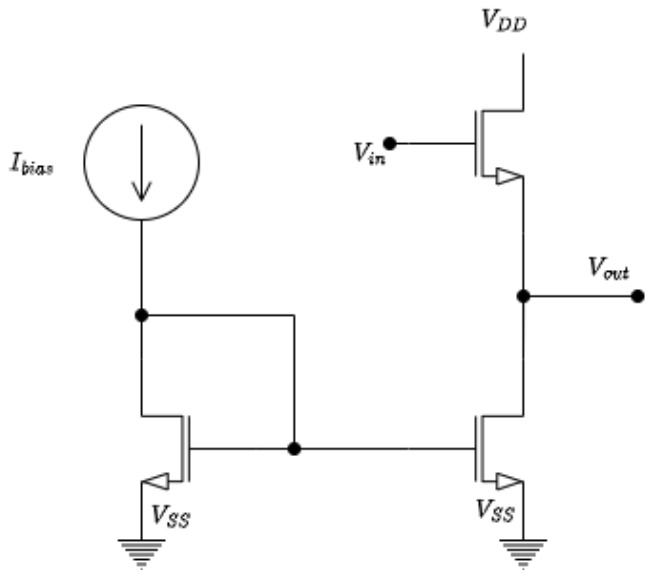

Figure 2: Circuit diagram of a source follower

b) Do you know a name for the circuit depicted in Figure 3?

Here we can se a common-source amplifier with a current-mirror active load.

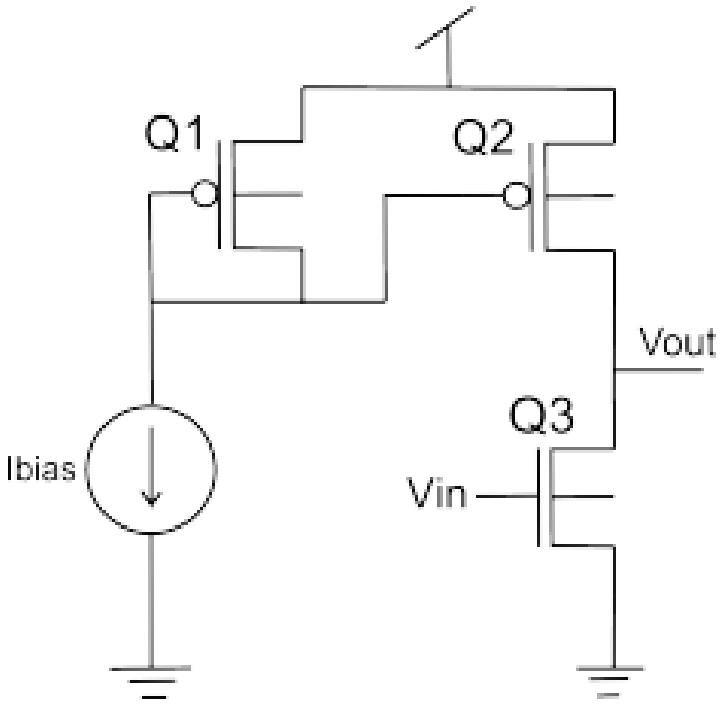

Figure 3: A common-source amplifier with a current-mirror active load.

c) Could you explain about a couple or more useful applications for the circuit in Figure 3?

This single-stage amplifier with an active load topology is often used as it has a high input impedance. It gets its high impedance from using an active load. By using an active load the circuit takes advantage of the nonlinear, large-signal transistror current-voltage relatiopnship to provide large small-signal resistances without large dc voltage drops This way it achieves high impedance without the use of excessively large resistors.

d) Write an expression for the voltage gain of the circuit, $V_{\text{out}}/V_{\text{in}}$, and explain how it could be developed.

By looking at the small-signal equivalent circuit for the common-source amplifier in figure 4 where V_{in} and R_{in} are the Thévenin equivalent of the input source, while assuming that both transistors are in the active region. The output resistance, R_2, is made up of the parallel combintaion of the drain-to-source resistance of Q_2, that is, r_{ds2} and the drain-to-source resistance of Q_3, that is, r_{ds3}. Using small-signal analysis, we have $v_{gs3} = v_{in}$, and therefore,

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = -g_{\text{m3}}R_2 = -g_{m3}\left(r_{ds2} \| r_{ds3}\right)$$

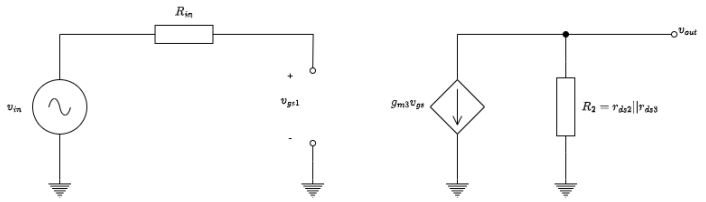

Figure 4: A small-signal equivalent circuit for the common-source amplifier.

Problem 2

Some effects of process variations related to the current mirror in Figure 5 should be investigated. In this problem, we want $I_{D,M1} \approx 10\mu$A. The supply voltage is set to $V_{DD} = 1.8$ V. The transistor technology that will be used is a 180 nm **transistor technology.**

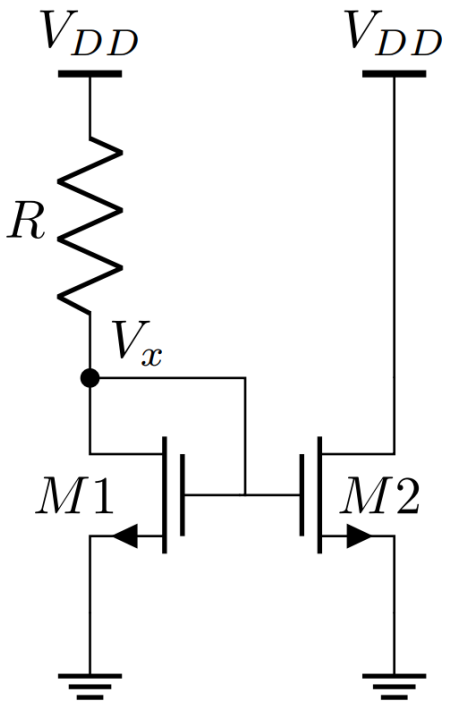

Figure 5: Current mirror using a resistor.

a) Show that the voltage at node V_x is $V_x = V_{tn} + V_{eff}$, where $V_{eff} = V_{GS,M1} - V_{tn}$

In other words, the task is to show that $V_x = V_{GS,M1}$, as you can see in figure 5, V_x is at the same node as $V_{GS,M1}$, as $V_{GS,M1}$ is basically the gate-source voltage then the voltage at node V_x must be equal to $V_x = V_{tn} + V_{eff}$, where $V_{eff} = V_{GS,M1} - V_{tn}$. (Is this a trick question?)

b) Use $\mu_n C_{ox} = 250\mu\text{A/V}^2$ and $V_{tn} = 0.45$ V and find the voltage at node V_x. Use $W/L = 5$ for both transistors and $L = 1\mu$m.

Assumin that we are in the Active region, we can use the equation for I_D

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{tn})^2$$

As we need to find $V_{GS,M1}$

$$V_{GS,M1} = \sqrt{I_{D,M1} \frac{2}{\mu_n C_{ox}} \frac{L}{W}} + V_{tn}$$

this gives us

$$V_{GS,M1} = \sqrt{10\mu A \cdot \frac{2}{250\mu A/V^2} \cdot \frac{1\mu m}{5\mu m}} + 0.45V = 0.576V$$

The voltage at node V_x is $V_x = 0.576V$

c) Then find a suitable value for R to satisfy our current requirement of $I_{D,M1} \approx 10\mu$A. Use AIM-Spice to simulate your circuit to find $I_{D,M1}$.

As $V_{DD} = 1.8V$ and $V_x = 0.576V$, we get $V_R = 1.8V - 0.576V = 1.224V$. Using ohm's law $\frac{V}{I} = R$ we get

$$R = \frac{1.224V}{10^{-5}A} = 122400\Omega$$

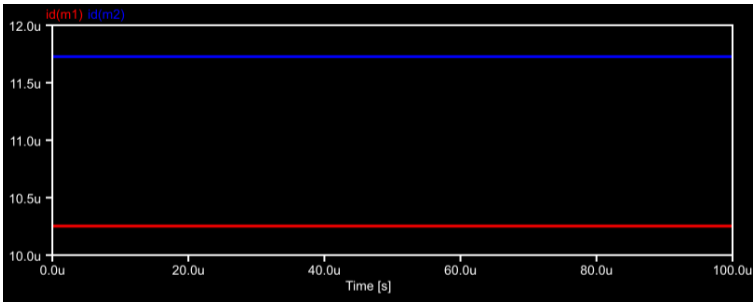

Figure 6: Simulated $I_{D,M1}$ and $I_{D,M2}$

d) Use AIM-Spice to simulate the current $I_{D,M2}$ through M2 over corners. Try for TT, SS and FF. Write the simulated values down in a table.

Table 1: Simulated values of $I_{D,M2}$ in different corners

Corner	$I_{D,M2}$ $[\mu A]$
TT	11.73
SS	10.59
FF	12.90

e) Use AIM-Spice to simulate the output impedance $r_{ds,M2}$ over corners. Try for TT, SS and FF. Write the simulated values down in a table.

Table 2: Simulated values of $r_{ds,M2}$ in different corners

Corner	$r_{ds,M2}$ $[k\Omega]$
FF	282
SS	480
TT	367

f) How will these variations affect the gain of an amplifier?

Process variations, as observed in sections d) and e), can notably impact the performance of an amplifier in several ways, particularly its gain. Let's analyze how the variations in $I_{D,M2}$ and $r_{ds,M2}$ across different corners (TT, SS, FF) could affect the gain.

- **Variations in $I_{D,M2}$:** From Table 1, it is evident that $I_{D,M2}$ exhibits variations across different process corners. The deviation of $I_{D,M2}$ from its intended value (around $10\mu A$) might impact the biasing of the MOSFETs in the current mirror, potentially affecting the quiescent (DC) operating point of any amplifier stage utilizing this current mirror. This could, in turn, influence the linearity and dynamic range of the amplifier.
- **Variations in $r_{ds,M2}$:** As observed in Table 2, the output impedance, $r_{ds,M2}$, also varies with process corners. The gain of a MOSFET amplifier in a configuration where $r_{ds,M2}$ contributes to the load (such as a common source amplifier with diode-connected load) is directly proportional to this output impedance. Therefore, variations in $r_{ds,M2}$ due to process variations will directly impact the gain of such amplifiers.

Problem 3

a) Simulate a simple current mirror built from NMOS transistors having a biasing current of 100 microampere, W/L = 10 and V_{dd} = 1 V using AIMSpice. The minimum gate length allowed in the 90 nm gpdk process is 100 nm. Display output current as a function of the voltage accross the output.

stuck with error message:

Listing 1: Error message

```
Circuit: *current mirror using a resistor
Warning: premature EOF
Error on line 10 : m1 2 2 0 0 gpdk090_nmos1v_x l=0.1u w=1u
unable to find definition of model w - default assumed

error:  no unlabeled parameter permitted on mosfet

Error on line 11 : m2 1 2 0 0 gpdk090_nmos1v_x l=0.1u w=1u
unable to find definition of model w - default assumed

error:  no unlabeled parameter permitted on mosfet
```

Listing 2: NMOS SPICE Netlist

```
*current mirror using a resistor

* Power Supply
vdd 1 0 1.8V

* Current Source
I1 1 2 10U

* MOSFET Definitions
M1 2 2 0 0 gpdk090_nmos1v_x L=0.1u W=1u
M2 3 2 0 0 gpdk090_nmos1v_x L=0.1u W=1u

* Simulation Commands
Vgate 3 0 1V
.dc Vgate 0 1 0.1

* Parameters and Includes
```

```
18  .param proc_delta = 1
19  .param vt_shift = 0
20  .include /home/peter/Shcool/TFE4152_Design_of_Integrated_Circuits/Exe
```

b) Find g_m for the transistor connected directly to the current source and r_{ds} for the transistor connected to the output of the simple current mirror.

c) Simulate a cascode current mirror built from 4 NMOS transistors, having a biasing current of 100 microampere, $W/L = 10$ and $V_{dd} = 1$ V, using AIMSpice. Display the output current as a function of the voltage accross the output. Find g_m for the transistor connected directly to the current source and r_{ds} for the transistor connected to the output. Compare the cascode current mirror with the simple current mirror, and explain about the main differences.

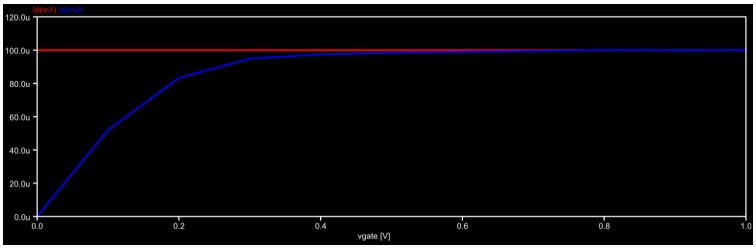

Figure 7: Display of the output current as a function of the voltage accross the output.

The transconductance of a MOSFET in the saturation region is given by the formula:

$$g_m = \sqrt{2 \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D}$$

where: - μ_n is the electron mobility, - C_{ox} is the oxide capacitance per unit area, - W/L is the aspect ratio of the MOSFET, - I_D is the drain current.

this gives us

$$g_m = \sqrt{2 \cdot 100\mu A/V^2 \cdot 10 \cdot 100\mu A}$$

$g_m = 0.447\frac{mA}{V}$

To find r_{ds} we can use

$$r_{ds} = \frac{1}{\lambda \cdot I_D}$$

where $\lambda = 0.14/L$ and $L = 1\mu M$. This gives use

$$r_{ds} = \frac{1}{14000 \cdot 100 \cdot 10^{-6}} = 0.714\Omega$$

d) In the Exercises folder on BlackBoard you find the file 20230930∗**.cir as well as well as the** $INV*$**.cir file. Use these files to simulate the 3-stage ring oscillator for the different corners TT, FS, SF, FF and SS. What are the important differences that you can observe from the behaviours in different corners? Can you explain these differences? (A "Final time" for your transient analysis may be for example 1 ns.)**

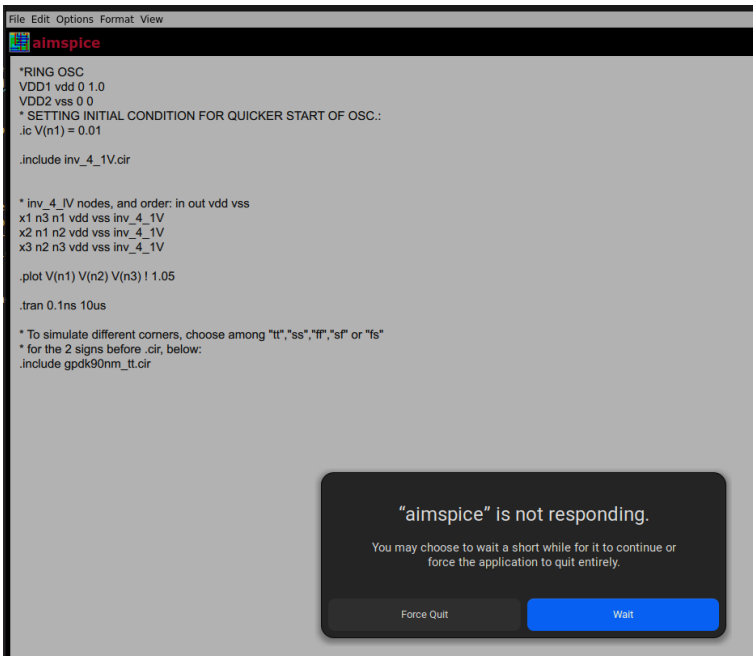

Figure 8: dude, thats it. nå er jeg i breakdown. plis godkjenn

e) Use the NMOS transistor from the simple current mirror mentioned above to design a common source amplifier using a current mirror for it's active load. Show simulated results and report figures that you find most relevant for the amplifier.