TFE4152 Design of Integrated Circuits

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Contents

Introductions

Artificial Intelligence (AI) is changing many parts of our lives, and the computational requirements for AI algorithms have surged immensely. At the heart of these computations lies the Multiply Accumulate (MAC) operation, a fundamental process at the chip level for AI [3]. These MAC circuits are also used in other areas, like signal processing [2].

A lot of researchers are trying to make these MAC circuits work better. One idea is called in-memory computing. This means doing the MAC operations right where the data is stored, so we don't waste time moving it around, this can be implemented using multi-bit storage capability, long cycling endurance, simple erase/write operation, etc [3]. Different kinds of memory can be used for this, but each has its challenges. A significant issue with these circuits is their power consumption. In particular, complementary metal-oxide-semiconductor (CMOS) circuits, which are widely used, have two main types of power consumption: static and dynamic. The static power, also known as leakage power, happens because of small currents that are always there, even when the circuit isn't actively doing something. This power consumption is mainly because of the type of transistors used and the way they're made [1].

With this in mind, our research project aims to explore the design and optimization of a MAC unit with a focus on minimizing static power consumption.

Theory

Modern computers typically consist of multiple levels, as illustrated in Figure 1. Based on the figure, AI would likely be categorized under Level 5. While the figure indicates that Level 0, the **Digital Logic Level**, is the lowest level, there exists another level beneath it, known as the **Device Level**. At this level, designers engage with individual transistors. To comprehend the inner workings of these transistors, one must delve into solid-state physics and understand integrated circuits.
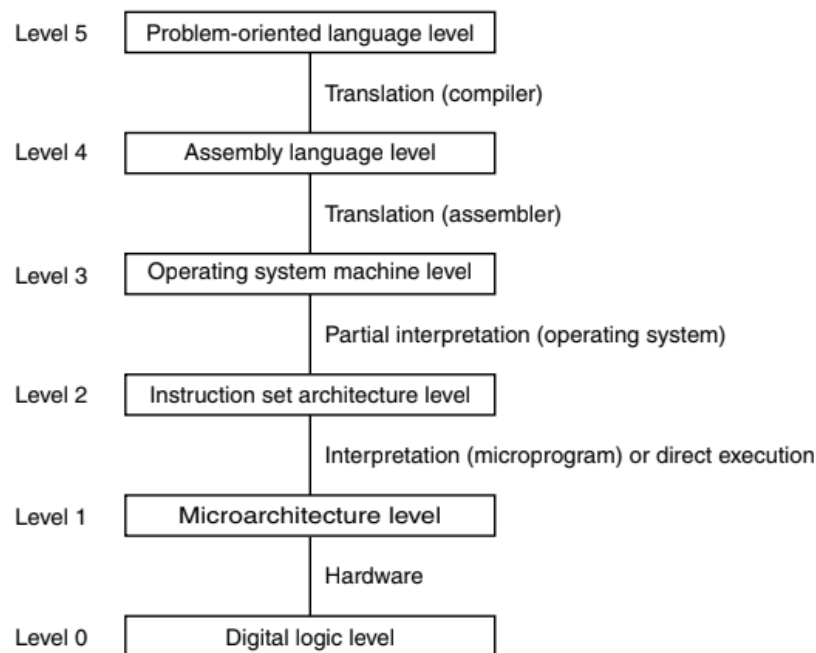
Level 5   Problem-oriented language level

          Translation (compiler)

Level 4   Assembly language level

          Translation (assembler)

Level 3   Operating system machine level

          Partial interpretation (operating system)

Level 2   Instruction set architecture level

          Interpretation (microprogram) or direct execution

Level 1   Microarchitecture level

          Hardware

Level 0   Digital logic level

Figure 1: A six-level Computer

CMOS

advanced

Method

Problem 4: Fast Fourier Transform (FFT) [2 points]

References

[1]   Anton Beloglazov et al. *Advances in computers. / Volume 82*. Elsevier/Academic Press, 2011.

[2]   Department of Electronic Systems NTNU. *Project in TFE4152 Design of Integrated Circuits*. Oct. 2023. (Visited on 10/24/2023).

[3]   Yin Wang et al. An in-memory computing architecture based on two-dimensional semiconductors for multiply-accumulate operations. In: *Nature Communications* 12 (June 2021). DOI: 10.1038/s41467-021-23719-3. URL: https://www.nature.com/articles/s41467-021-23719-3 (visited on 10/24/2023).