STM32L4 - DFSDM

Digital filter for Sigma-Delta modulators interface

Revision 3.2

Hello, and welcome to this presentation of the STM32 Digital Filter for Sigma-Delta modulators interface. The features of this interface, which behaves like ADC with external analog part and configurable speed versus resolution ratio, will be described.

DFSDM: introduction and typical usage

Behavior like ADC with scalable speed/resolution and external analog front end
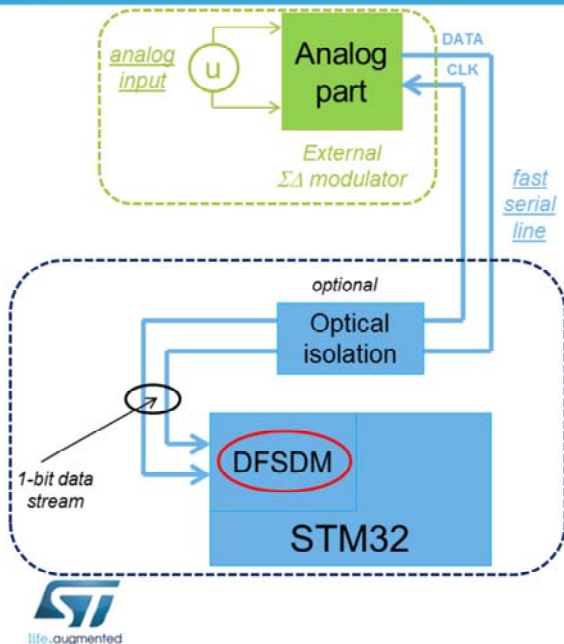
The DFSDM Peripheral is a new digital peripheral inside the STM32 products. Its behavior is finally like standard ADC with the analog part outside the microcontroller.

The main benefit is to move analog part outside microcontroller and to propose an internal digital part with wide range of features. The DFSDM represents the digital part which is connected to analog part by fast serial interface. The external analog part is usually Sigma Delta modulator offered by wide range of vendors.

This feature offers the possibility to choose a specific analog part according the user needs, like galvanic isolation for motor control or metering applications, with low noise and high precision analog part for sensor data acquisition applications or cheap analog part for price sensitive applications. Finally the analog part provides

digitized data for DFSDM.

The digital part (represented by DFSDM peripheral) performs a digital signal processing from external data. Therefore it offers a scalable ratio solution between speed and resolution but also an additional functionality integrated in standard built-in ADC (like analog watchdogs, injected and regular conversions, flexible triggering system, break signal generation, extreme detector). Digital MEMS microphones providing a PDM output data format can be directly connected to DFSDM which can process directly the audio signal.

The DFSDM is able to process the external serial data and also the internal parallel 16-bit data transfer provided by CPU or DMA from memory.
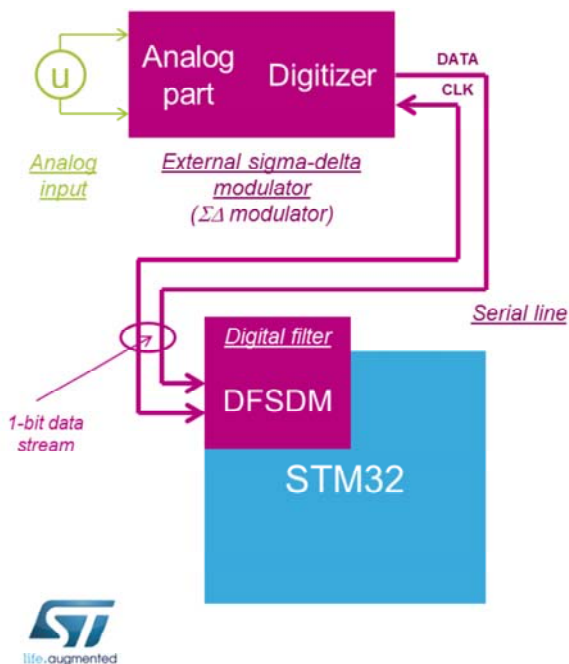
The DFSDM was developed due to need for a sigma-delta ADC with scalable speed vs. resolution.
More than 16-bit accuracy inside a microcontroller is problem because of noise from digital part.
The solution is to move the analog part outside the microcontroller.
The speed vs. resolution ratio setting is a task for the internal digital part, which is the digital filter in the hardware.
Although it behaves like a complete analog-to-digital converter with an external analog front end, the DFSDM is purely digital with its analog part outside the microcontroller.
The DFSDM integrated inside STM32 products provides the digital part of the complete sigma-delta ADC with an external analog part – which is the sigma-delta modulator.

Both parts are connected through the serial interface which provides a 1-bit sigma-delta stream. The average value of this stream represents the analog value on input. Applications can benefit from the easy connection – just 1 or 2 wires are needed. Thanks to the analog located outside the microcontroller, there is less noise caused by the microcontroller. The balance between speed and resolution according application needs can be set by configuring the digital filter.

Key features

Decreased CPU burden and low-latency HW safety features

- Transceivers
  - Fast serial input (20 MHz):
    - SPI or Manchester-coded mode (with clock absence detection)
    - Clock output generation
  - Internal 16-bit parallel data input
    - write by CPU/DMA
    - input from internal ADCs (*)

- Filters
  - Sinc1, Sinc2, Sinc3, Sinc4, Sinc5, FastSinc filters with oversampling ratio up to 1024
  - Integrator with oversampling ratio up to 1024

Application Benefits
- Support from various $\Sigma\Delta$ modulators suppliers (ST, TI, Analog Devices)
- Speed vs. resolution selection by filter configuration
- Internal data postprocessing (SAR ADC results, ...)
- Additional functions: watchdog, short-circuit detector, extremes detector, offset correction

(*) STM32L45x/46x/49x/4Ax devices only

Transceivers provide the serial connection to the external sigma-delta modulator. They support serial connections with configurable protocols (SPI or Manchester) and configurable parameters. Their functions will be explained later in detail. Transceivers also have support for internal 16-bit parallel data inputs which will be written to the DFSDM input data registers by the CPU or DMA and optionally by internal ADCs (for STM32L45x/46x/49x/4Ax devices only).
Filters are the core of DFSDM function – they perform 1-bit stream filtering to provide higher output resolution at lower speeds. There is an additional integrator behind the digital filter which provides additional data averaging. Applications can be designed with various types of Sigma-Delta modulators (from various vendors). The parallel data input feature can perform post-processing of any internal data (for example, internal ADC streams,

audio data filtering, etc.). There is set of additional functions which will be explained later in detail.

Block diagram
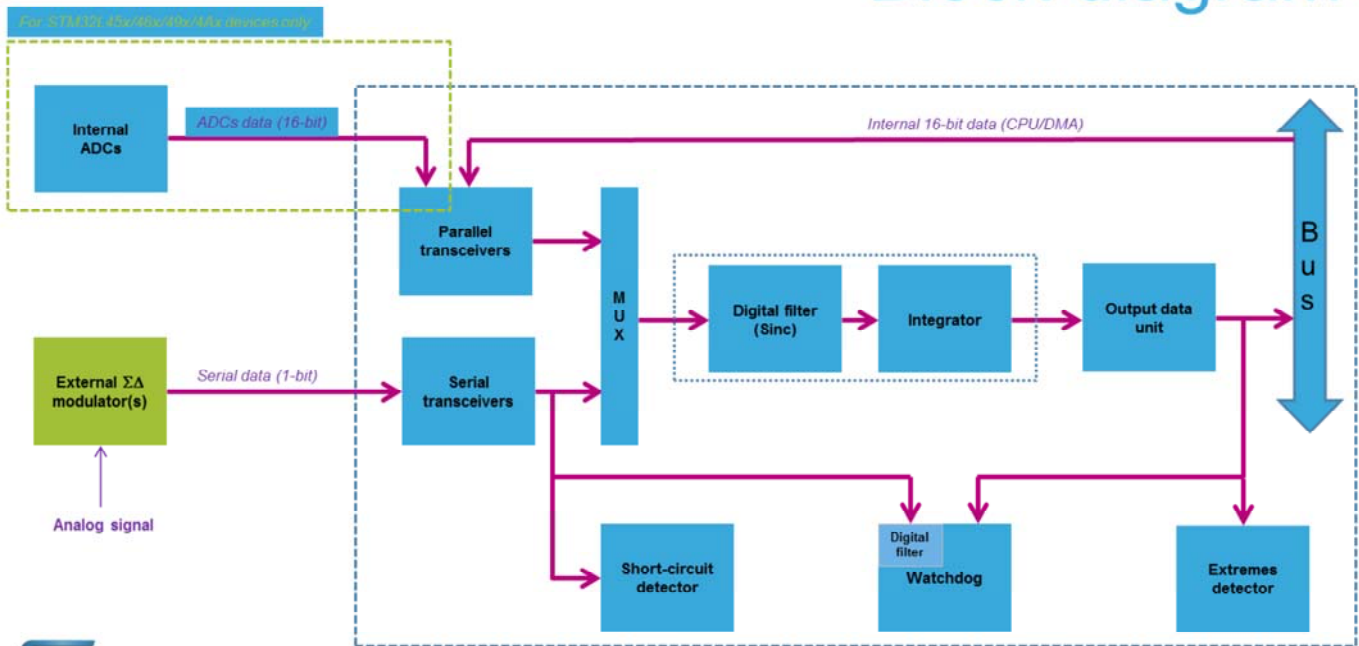
The entire Digital Filter for Sigma Delta Modulators interface consists of:

- 8 Serial transceivers
- 4 Sinc filter parts and integrators
- 4 Output data units
- 4 Analog watchdogs
- 8 Short circuit detectors
- 4 Extreme detectors
- 8 Parallel data input registers

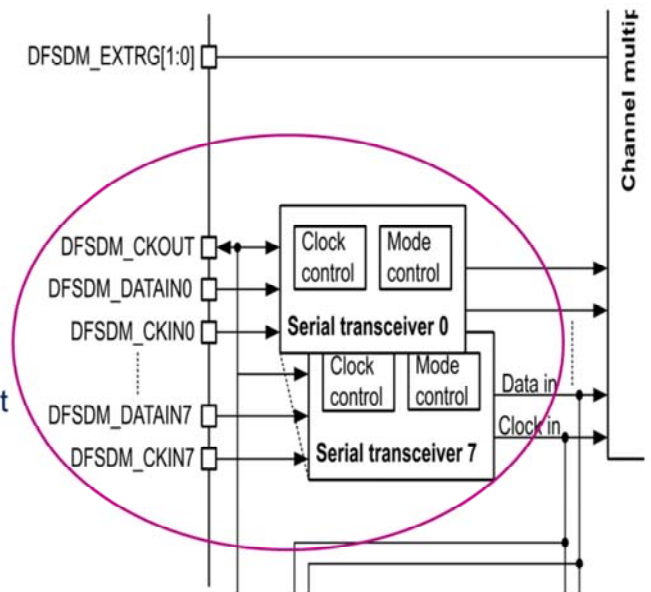For STM32L45x/46x devices, the configuration is only one half - 4 transceivers and 2 filters and integrators. The STM32L45x/46x/49x/4Ax devices feature parallel inputs from internal ADCs.

Serial transceivers

Compatible with any ΣΔ modulator output protocol

- To receive raw 1 bit serial stream from ΣΔ modulator and provide data & clock to the filter stage (up to 8 input serial channels)

- Any ΣΔ modulator output protocol support:
  - SPI mode (clock and data wire): falling/rising sampling edge, data rate measurement, clock presence detection
  - 1-wire Manchester-coded mode: lowest system cost (single isolator per input channel)

- Output clock generation on external pin:
  Divider from system clock or audio PLL clock

DFSDM_EXTRG[1:0]

DFSDM_CKOUT
DFSDM_DATAIN0
DFSDM_CKIN0

Clock control | Mode control
Serial transceiver 0

DFSDM_DATAIN7
DFSDM_CKIN7

Clock control | Mode control
Serial transceiver 7

Data in
Clock in

Channel multip

Serial transceivers provide the connection to the external Sigma-Delta modulator.

SPI mode works up to 20 MHz (or the DFSDM clock divided by 4). There are configurable options including sampling edge selection, data rate measurement, and clock presence monitoring.
1-wire Manchester-coded mode (where clock is recovered from the data) works up to 10 MHz (or DFSDM clock divided by 6). A synchronization detection feature is also available in Manchester mode.
Manchester mode also offers the lowest system cost in case of optical isolation of the Sigma-Delta modulator – then only one single isolator per input channel is necessary.
The DFSDM clock features a clock output signal to drive the Sigma-Delta modulator. It can be used as a source

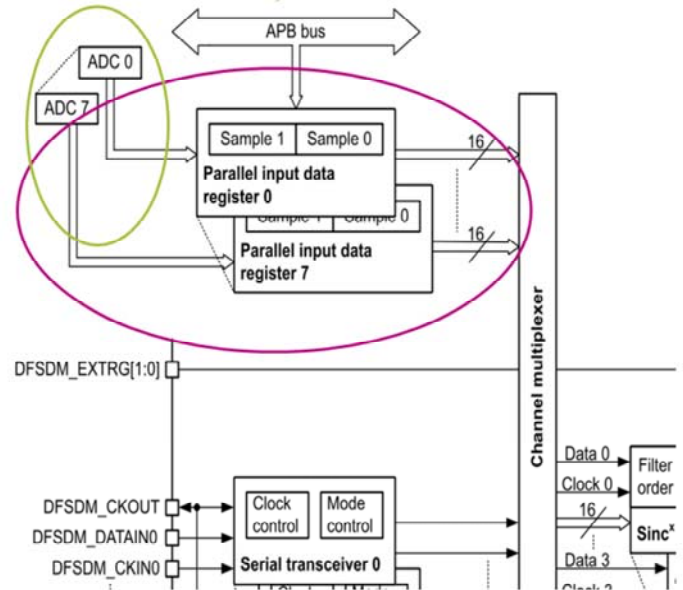for the SPI clock input by internal interconnection in order to save external pins.

The clock output has an adjustable division factor and can be driven either from the System clock or from the fine-tuned Audio PLL clock.

Parallel transceivers

Fast hardware filtering of internal data

For STM32L45x/46x/49x/4Ax devices only

- To receive 16-bit parallel data stream from internal sources to the filter stage (up to 8 parallel channels/registers)

- Data post processing
  - From RAM data buffer (write by CPU or DMA to input registers)
  - From internal ADC output data (direct ADC input to registers)

APB bus

ADC 0

ADC 7

| Sample 1 | Sample 0 |

Parallel input data register 0

16

| Sample 1 | Sample 0 |

Parallel input data register 7

16

DFSDM_EXTRG[1:0]

Channel multiplexer

DFSDM_CKOUT

| Clock control | Mode control |

Data 0

Filter order

DFSDM_DATAIN0

Clock 0

16

DFSDM_CKIN0

Serial transceiver 0

Sinc^x

Data 3

life.augmented

Parallel transceivers provide parallel inputs from internal data sources; for example, from memory buffers.
Parallel inputs are usually used for fast hardware filtering of internal data from the ADC or any data collected from a communication peripheral.
Data can be written to the DFSDM parallel input registers by the CPU or DMA configured in memory-to-memory transfer mode.
In STM32L45x/46x/49x/4Ax devices the internal Analog to Digital converters can provide parallel data directly to the DFSDM parallel input registers.

Sincx/x digital filter

CPU free digital filtering

- Digital filter stage to perform digital filtering of input data stream
  - Mean value of input data stream from $\Sigma\Delta$ modulator is the final ADC value ("averaging")
  - Sinc filter: performs moving average over given number of samples (oversampling ratio)

- Configuration options:
  - Filter type: Sinc1, Sinc2, Sinc3, Sinc4, Sinc5, FastSinc
  - Oversampling ratio:1-1024 (can be bypassed)
  - Speed vs. resolution balance selection
  - Filter data resolution is 31-bit max
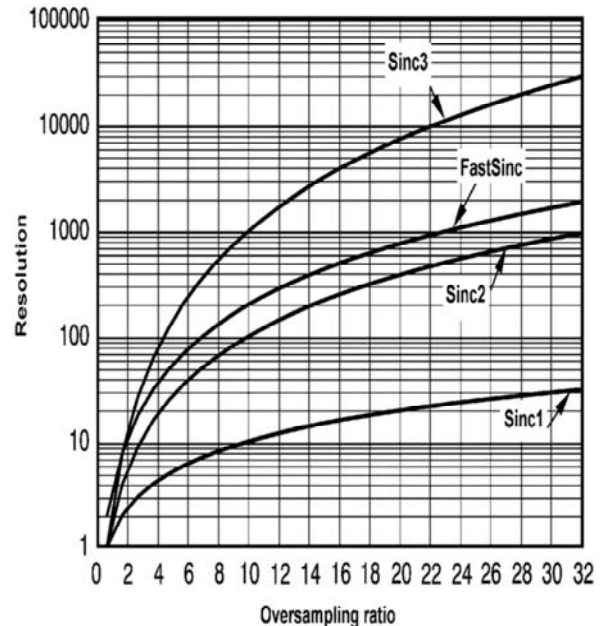
The digital filter averages the 1 bit input data stream from the Sigma-Delta modulator into a higher resolution, but with a slower data output.
The digital filter is Sinc X type with an order from 1 to 5.
A FastSinc type filter is also available for selection.
The oversampling ratio means how many samples will be averaged in a single filter run. The oversampling ratio can be selected in a wide range from 1 to 1024.
Not all combinations of filter order and oversampling ratios are available because in higher filter orders the oversampling ratio must be reduced to not overflow over the 31-bit data width (which is the internal filter resolution).

Additional increase of resolution

- Integrator stage performs additional signal processing – averaging of data from digital filter (summing N samples)

- Configuration:
  - 1 to 256 samples to sum
  - Can be bypassed

- Final result is sent to the output data unit
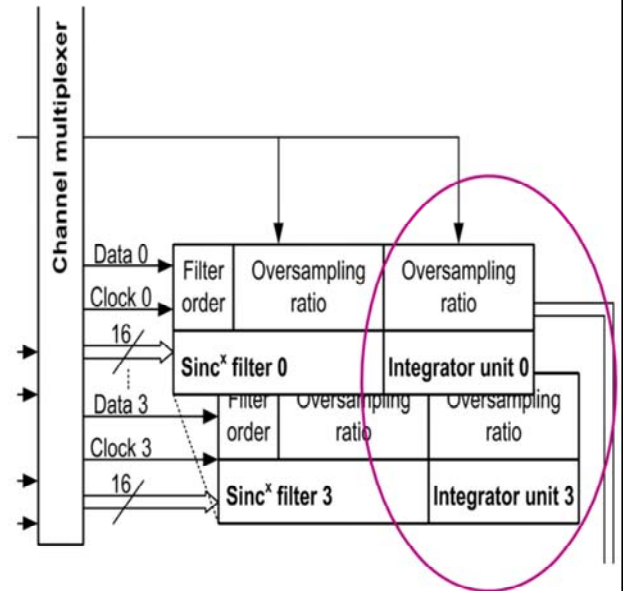
The Integrator unit performs additional simple averaging of data provided by the digital filter. It provides just a simple summing of the data coming from the digital filter. The number of samples to be summed can be set from 1 to 256. The correct configuration must take care that the final data length fits into the 31-bit width, which is the resolution of the internal integrator. The width of the data coming from the digital filter must also be taken into account.

CPU-free external offset removal and data formatting

- Performs final post-processing functions on final data:
  - Offset compensation/subtraction
  - Programmable right-bit-shifting

- Offset correction feature:
  - Offset is stored in register by user (from user calibration procedure) - for each input channel

- 24-bit final data register width:
  - Configurable right bit shift to convert internal 31-bit resolution into final data register resolution

Right bit-shift count

Calibration data correction unit

DFSDM data 0

DFSDM data 3

Data output

APB bus
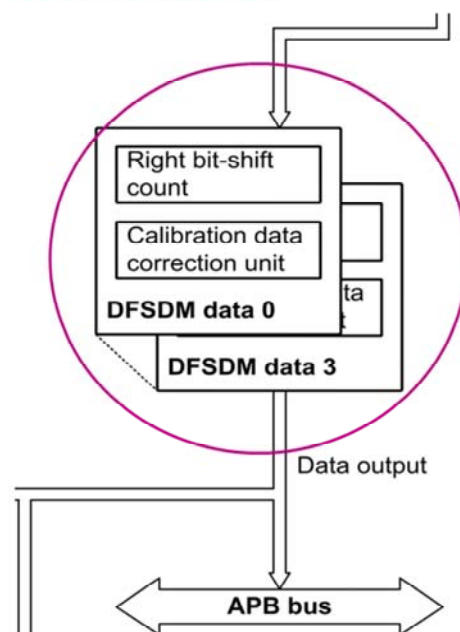
The output data unit adjusts the final data before they are written to the final data register.
An offset value that will be automatically subtracted from the data result for each channel can be defined in the offset register. The correct offset values are determined using the calibration procedure. This calibration procedure should be programmed in user firmware and depends on the type of Sigma-Delta modulator connected and application needs.
The maximum resolution of the final output data register is 24 bits, but the internal resolution can go up to 31 bits. But certain applications have their own constraints; for example, 8-, 12-, 16-, or 24-bit data resolution.
Therefore, there is an option to perform a right-bit-shift of the data to provide the final data result with the required width and not overflow the 24-bit width of the final data register. Right-bit-shift is configurable from 0 to 31 bits.

The final resolution then depends on the digital filter and integrator settings as well as the right-bit-shift option.

Analog watchdog

Safety and emergency functions
such as monitoring of critical motor control values

- Emergency function if analog value is outside selected boundary
  - Final data result monitoring
  - Or independent input channels data monitoring

- Support for safety/emergency functions
  - Break or Interrupt signal generation
  - Separate flags for high and low boundary

- Input channels monitoring has configurable filters:
  - Sinc1, Sinc2, Sinc3 filter with an oversampling range 1 to 32
  - Watchdog data filters are available for user
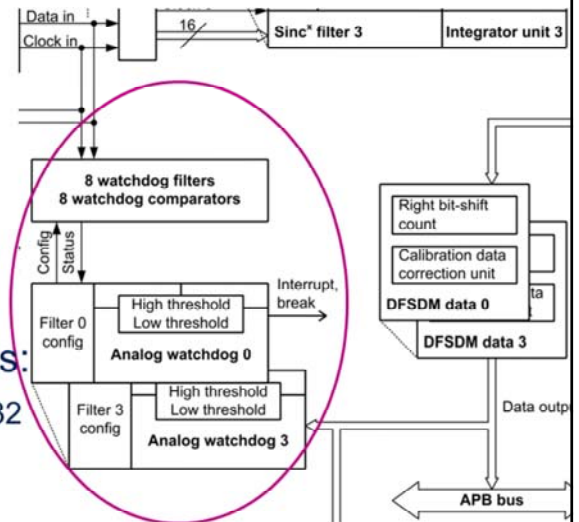
The analog watchdog monitors sampled analog data to see if it remains within the selected high and low threshold values. The input to the analog watchdog function can come from the result of the final converted data or directly from the input serial channels through a configurable filter.

If data exceeds the allowed boundaries, an interrupt can be invoked or a break signal generated. If an interrupt is invoked, the software decides about the next actions. If a break signal is generated, this break signal can perform a safety function directly by hardware; for example, stop a timer which controls the motor.

There are separate high and low threshold levels and separate flags for each threshold to know if a threshold has been reached.

The analog watchdog can monitor 2 types of data. The first type is standard output data as with as standard

ADC. The second type of data can come from serial transceivers through configurable dedicated filters. This second option allows to select faster signal monitoring when the required speed and resolution is set by the filter parameters. Each serial channel watchdog filter is configurable from 1 to 3 and its oversampling ratio in range from 1 to 32. The data from these watchdog filters can also be read by user firmware.

Short circuit detector

Very fast safety and emergency functions such as motor control short-circuit monitoring

- Very fast detection of critical state:
  - Saturation of input signal for longer time means overcurrent (short circuit) or overvoltage

- Detection if signal is saturated for given time
  - Configurable time: 1 to 256 consecutive 1s or 0s in the $\Sigma\Delta$ stream (all 1s or 0s)

- Independent monitoring on all input channels
  - Also if main conversion is stopped
  - Interrupt generation (for software intervention) or break signal (for example: to shutdown PWM generation with no latency)
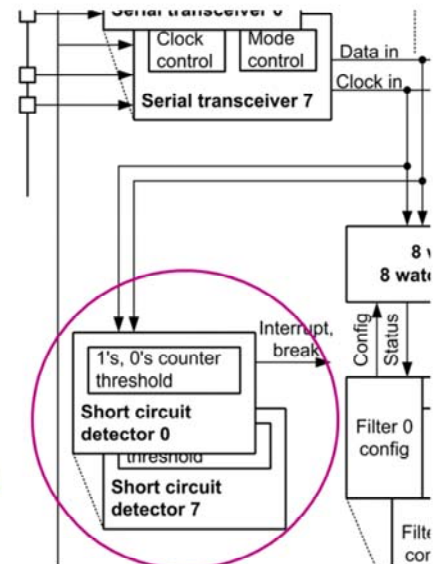
The short-circuit detector monitors input serial channels for a saturation state. When an input signal is saturated, it means that it is outside the allowed measurement range and therefore there is an overflow or underflow of the signal. When measuring current, this event usually detects an overcurrent (or short circuit), or an overvoltage when measuring the voltage.

Detection of input signal saturation is based on monitoring the input serial data stream coming from the sigma-delta converter and watching if there is a consecutive set of ones or zeroes for a relatively long time. This maximum saturated time can be set in the range from 1 to 256 of sampled input data which will have the same value: zero samples or one samples. Monitoring is performed independently from the main conversion. The main conversion can perform

conversion from another channel or can also be stopped. All input channels can be monitored in parallel with their own saturated time setting.

When a saturation event is detected, an interrupt can be invoked or a break signal generated. Then, just as with the analog watchdog, the software decides the following actions or the hardware break signal can perform a safety function without any software latency. For example, it can stop the timer which controls the motor in the event a short-circuit is detected.

Extremes detector

Hardware detection of peak values
Example: audio data normalization

- Watching for minimum and maximum values in data output results

- Store the maximum and minimum values of the output data values into registers for selected channels

- Hardware monitoring of extremes values

- Extremes values are refreshed by software (by reading min/max registers)
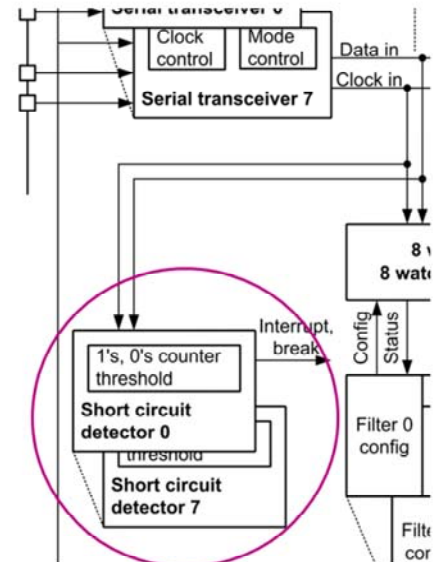
The extremes detector monitors output results and stores the extreme values into minimum and maximum registers as well as the associated channel number. Monitoring of data for extremes is only performed on selected channels to ensure that channels do not mix different input levels.
Stored extreme values are refreshed each time the values are read in the register.

Conversion type selection

- **Regular conversions**
  - Only one channel selection (from 8 input channels)
  - Launched by software only (no HW trigger)
  - Continuous mode feature
  - Can be immediately interrupted by injected conversion (with flag signaling this interruption)

- **Injected conversions**
  - Can be set on more input channels (to add them into injected selection group)
  - Scan mode: by trigger event are converted all selected channels (whole group)
  - Single mode: by trigger event only one channel is converted and next is selected
  - Launched by SW or HW trigger: timers outputs or external pins
  - No continuous mode (can be emulated by timer triggered mode)

Regular conversions have less priority and can be interrupted by an injected conversion. If the regular conversion was interrupted by an injected conversion, it is restarted once the injected conversion is finished and this interruption is indicated as a flag for this delayed regular conversion. Regular conversions can be launched only by software and there is no scan mode available. Regular conversions can run in continuous mode, in which is there is no channel switching, and they can be performed in fast mode without filter refill. Regular conversions are used for measurements for which timing is not critical; for example, when measuring temperatures or slow signals.

Regular conversions are also typical used for continuous conversions from one channel only; for example, audio or energy-measurement applications.

Injected conversions have high priority. They can interrupt regular conversions immediately and start just after being triggered. Any of the input channels can be assigned into an injected channels group. There are two modes of conversion behavior: scan mode and single mode.

In scan injected mode, all channels from the injected channels group are converted (starting from the lowest to the highest channel number in a group) when a trigger occurs.

In single injected mode, only one channel from the injected channel group is converted and the next channel from the injected group is selected for the next conversion. The next trigger will start this next channel conversion and another higher channel from group is selected.

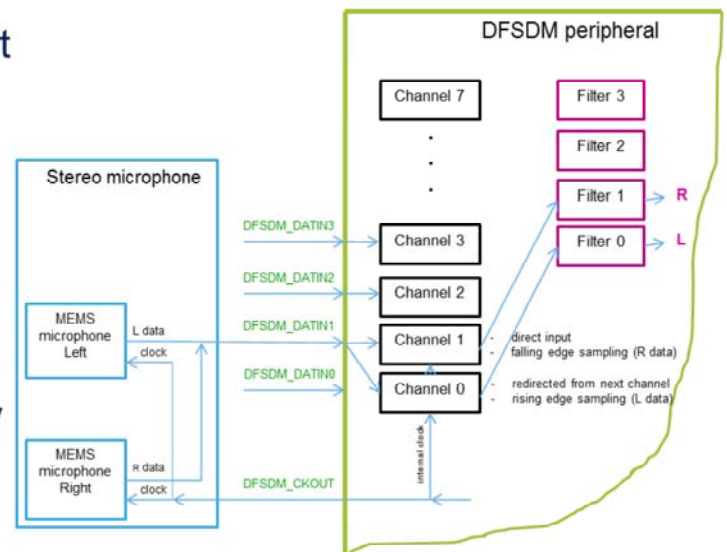Injected conversions can be launched by software or by hardware (from timers or an external pin).

Injected conversions cannot run in continuous mode, but this mode can be emulated using a periodic timer trigger.

Those modes make it possible to choose the correct conversion mode according to application requirements.

The MEMS microphone provides a pulse density modulated (PDM) data signal whose format is theoretically like the Sigma-Delta bit stream from Sigma-Delta modulator.

The MEMS microphone has stereo support if two microphones are connected in parallel with common data and clock signals:

Rising clock edge samples left audio data.

Falling clock edge samples right audio data.

Implementation into DFSDM transceivers requires this configuration:

Channel 0 uses redirection input from channel 1.

Channel 1 uses direct input.

Channel data (left vs. right) are separated inside by selecting either the rising or falling edge in the SPI configuration of channels.

The clock signal is provided by the DFSDM clock output because the MEMS microphones are slaves and need an external clock for data sampling and communication.

Interrupt event	Description
End of conversion (regular/injected)	Set when conversion finishes (separate flags for regular and injected conversion).
Data overrun (regular/injected)	Set if injected converted data were not read from output data register (by CPU or DMA) and were overwritten by a new conversion (separated flags for regular and injected conversion).
Analog watchdog	Set if converted data (output data or data from analog watchdog filter) crosses over/under high/low analog watchdog thresholds register (separated flags for high/low crossing detection).
Short-circuit detector	Set if the number of stable data samples crosses over selected short circuit thresholds.
Channel clock absence	Set if there is clock absence on input serial channel clock pin.

A set of interrupts related to DFSDM events has been implemented to increase CPU performance.
This table lists all the DFSDM interrupt sources:
- End of conversion events, with separate flags for regular and injected conversions.
- Data overrun events, with separate flags for regular and injected conversions.
- Analog watchdog events.
- Short-circuit detector events.
- Channel clock absence event.

DMA request	Description
End of conversion (regular/injected)	DMA request is set when conversion finishes (regular or injected conversion).

- DMA requests can be enabled to decrease the CPU intervention to transfer converted data into memory.

- DMA "memory-to-memory" transfer mode can be used also as parallel data input source – to transfer 16-bit data into parallel input data register
  - Memory to memory DMA transfer must be used with parallel data input register as target address

To decrease the CPU intervention, conversions can be transferred into memory using a DMA transfer. DMA transfers for injected and regular conversions can be enabled separately.
The direct memory access controller (DMA) can be used also as method for fast data transfers into parallel data registers. In this case, the parallel data are transferred from the memory buffer into the parallel data register by using the DMA. The DMA should be therefore configured in memory-to-memory transfer mode where the target address is the address of the parallel input data register.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Low-power run	Active.
Low-power sleep	Active. Peripheral interrupts cause the device to exit Low-power sleep mode.
Stop 0/Stop 1	Frozen. Peripheral registers content is kept.
Stop 2	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.
Shutdown	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

The DFSDM peripheral can be active only in Run and Sleep modes. In all other low-power modes, including Stop, Standby and Shutdown modes, the DFSDM must be disabled.

Very fast signal processing in hardware: consumption reduction.
All existing ΣΔ modulators speeds are supported.

- Clock speeds
  - Maximum DFSDM clock: Same as system clock (max. 80 MHz)
  - Maximum input serial clock into channel (Input data rate)
    - SPI mode: DFSDM clock divided by 4 (max 20 MHz)
    - Manchester mode: DFSDM clock divided by 6 (max 10 MHz)
  - Maximum output frequency on clock output: DFSDM clock divided by 4 (max. 20 Mhz)

- Output data rate
  - Depends from filter and integrator oversampling ratio (FOSR, IOSR):
    - Output data rate = Input data rate / (FOSR * IOSR) , where: FOSR = 1-1024, IOSR = 1-256

DFSDM performance depends on the maximum allowed input data rate because each input data sample causes the next digital filter operation. DFSDM allows operation at a maximum input data rate of 20 MHz in SPI mode or 10 MHz in Manchester mode.
Parallel data inputs have the same performance, so parallel data can be put into DFSDM at full 20 MHz speed using either the CPU or DMA.
Applications benefit from DFSDM high-speed processing which now supports all existing sigma-delta modulator speeds.

Application examples 1

- **Stereo MEMS microphone playback**
  - Only 2 wires are used to connect 2 microphones (stereo) – common clock and data wire with different sampling edges for left and right channel (and using DFSDM feature: redirection of data from given input channel pin to another channel data input).
  - Regular conversions are used for two DFSDM interfaces in continuous mode.
  - Low CPU load: one DMA transfers output audio data to RAM and second DMA transfers those data to I2S interface (which sends them to external audio codec and headphones).

- **Pt100 thermometer**
  - An external STPMS2 device (dual-channel, second-order sigma-delta modulator) is used to sense 2 input channels
  - One channel senses voltage on Pt100 sensor, second channel senses current over Pt100 sensor (on shunt). Ratio of channels data results is the Pt100 sensor resistance.
 - Injected scan conversion is used for those 2 channels with 1-sec periodic timer trigger.

The STM32L4 evaluation board can be used to run two simple application examples to help you explore the digital filter for Sigma-Delta modulators interface.
The first example is a demonstration of the MEMS microphone directly connected to the DFSDM peripheral. Data from the microphone are processed by DFSDM with correct filter settings and then collected into a memory buffer using regular continuous conversions and the DMA. Recorded data from the microphone are then immediately sent by the DMA from this buffer to the I2S peripheral and played by headphones.
The second example is a Pt100 thermometer which uses an external STPMS2 sigma delta modulator which monitors two channels. One channel senses the voltage and second one senses the current on the Pt100 sensor. Both channels are sampled using timer-triggered injected conversions in scan mode. Software then computes the

Pt100 resistance from collected data and finally the temperature.
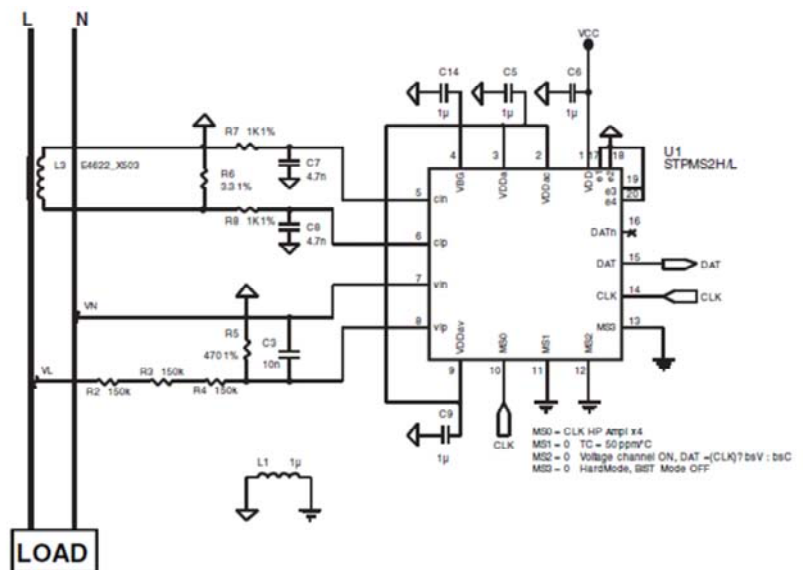
Application examples 1

PT100 measurement using SigmaDelta STPMS2
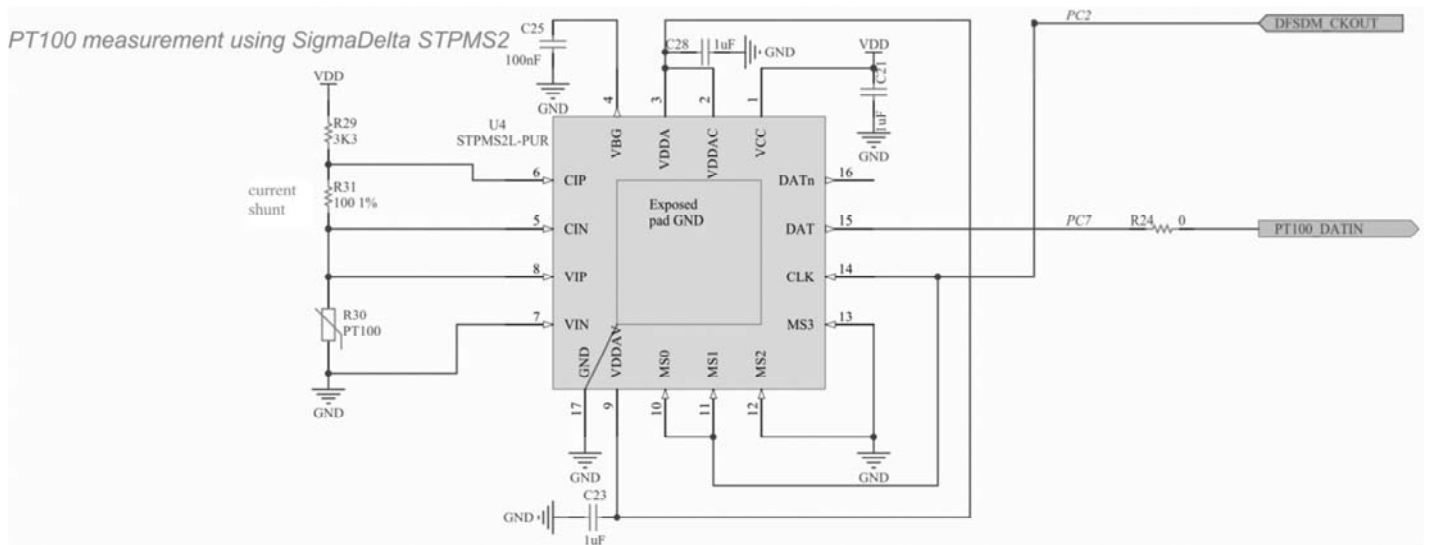
This schematic shows an example of the Pt100 thermometer. Here you can see how the STPMS2 device senses the voltage and current over the Pt100 sensor. Sensed data are sent from the STPMS2 device to the DFSDM peripheral through the serial interface.

Application examples 2

- **Electricity meter with STPMS2**
  - External STPMS2 device (dual ΣΔ modulator) is used to sense 2 input channels: voltage and current.
  - Current is sensed by current transformer (or by shunt). Voltage is sensed by voltage divider.
  - Voltage and current samples are sent to DFSDM by serial interface (clock and data wire only).
  - The DFSDM then process the voltage and current samples into wide resolution. Finally STM32 firmware calculates electric power and energy using FFT analysis.

This example shows a typical one-phase electricity meter design using an STPMS2 device and STM32 microcontroller.

The STPMS2 is a dual-channel, Sigma-Delta modulator designed for electricity meter applications. It has voltage and current channel inputs. The current channel features a programmable gain amplifier to cover a wide range of measured currents. Sampled 1 bit data are sent by the serial interface to the host device (which is here the DFSDM interface). Both voltage and current 1 bit data samples are sent on the same data wire, but the voltage is sampled on the rising clock edge while the current is sampled on the falling clock edge. The clock is provided by the DFSDM and can run up to 4 MHz.

The DFSDM then processes the voltage and current channel 1 bit data streams into output data with a higher resolution and slower data rate. Finally, the firmware

uses FFT analysis to calculate the electric power and energy from the current and voltage samples.

Application examples 3

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- 3-phase electricity meter
  (using shunts, no transformers)
  - Voltages are sensed by resistor dividers.
    One DFSDM filter with 3 multiplexed
    inputs is used to scan 3-phase voltages.
  - Currents are sensed by shunt resistors
    with galvanic isolated ΣΔ modulators.
    One or two isolation lines per phase are
    necessary only for current data transfers
    to DFSDM channels (Manchester-coded
    mode requires only 1 line).
  - STM32 firmware calculates electric
   power and energy.
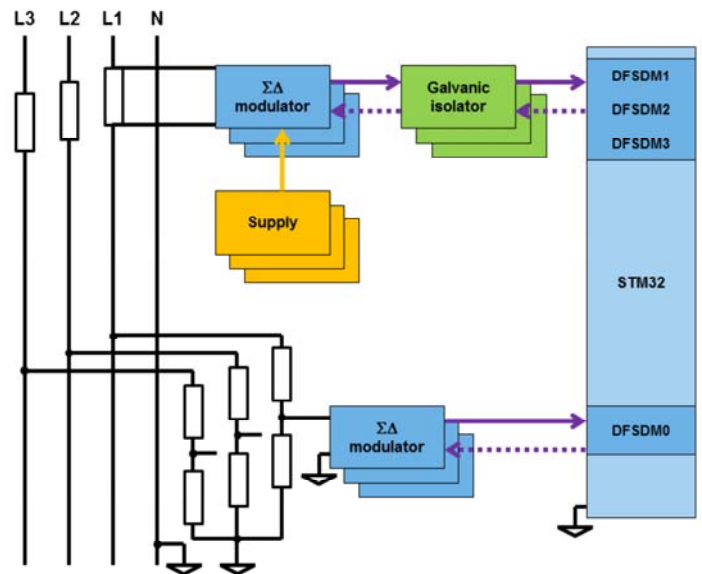
This example shows a 3-phase electricity meter design using shunt resistors for sensing current. There is no need to use expensive current transformers.
Voltages are sensed by three resistor dividers and external Sigma-Delta modulators.
Currents are sensed by three shunt resistors. Each shunt resistor voltage is sensed by one Sigma-Delta modulator. Because each Sigma-Delta modulator operates at a high-phase voltage, galvanic isolation is used for data transfers into the DFSDM. If the Sigma-Delta modulator uses the Manchester-coded serial protocol format (and has an internal clock source), only one isolator per phase is necessary. If the Sigma-Delta modulator uses the SPI serial format, two isolators per phase are necessary.
Each Sigma-Delta modulator is powered from a separate DC supply voltage.

Application examples 4 ◼ 24

- 3-phase motor control
  - Used galvanic isolation for ΣΔ modulators: data and clock wires (for Manchester coding: data only)
  - DFSDM performs 3 measures from the same bit stream, in parallel:
    - High-accuracy low speed measure, synchronized to the PWM period (uses main Sinc filter)
    - Continuous overload monitoring by watchdog (medium speed)
    - Continuous short-circuit detection with ultra-fast response (to disable the PWM generator)
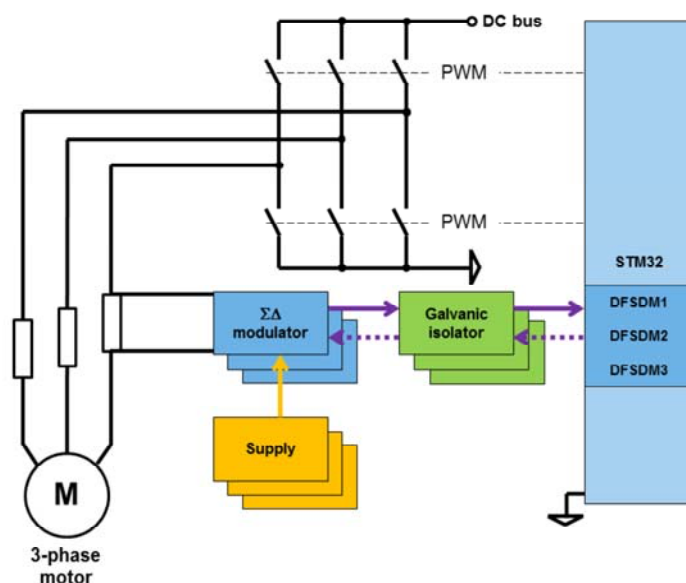
This example is related to a 3-phase industrial (high-voltage, high-current) motor drive, where floating shunts and galvanic isolation are standard. A single reading channel is represented here, while in the application, 2 or 3 channels are used for the current in addition to 2 or 3 channels for the voltage. The currents are usually measured simultaneously by 3 DFSDM channels while the voltage can be measured sequentially with the same DFSDM channel.

The same bit stream is processed 3 times:

1st: For high-accuracy measurements, the main filter is used over a relatively long time. This measurement is done synchronously with a PWM period to avoid switching noise and have regular samples.

2nd: The watchdog channel uses the same bit stream with its own (lower order) filter, continuously monitors the signals and invokes an interrupt in case of overload, with

medium reaction time.

3rd: The short-circuit detector is used to detect very rapidly a modulator saturation (continuous series of zeroes or ones with a programmable length), and automatically disables the PWM generator (through a dedicated DFSDM to the timer interconnection by a break signal).

Related peripherals

- Refer to these peripheral trainings linked to this peripheral:
    - RCC (DFSDM clock control, DFSDM enable/reset)
    - Interrupts (DFSDM interrupt mapping)
    - DMA (DFSDM output data transfer, parallel data input)
    - GPIO (DFSDM input/output pins, triggers)
    - Timers (DFSDM trigger, break signal)
    - Peripherals interconnect matrix (DFSDM interconnection)

The peripherals listed here influence DFSDM behavior. Please refer to the corresponding peripheral training for complete information.

Differences with STM32L47x/48x devices

- There is no DFSDM in STM32L41x/42x/43x/44x devices
- The number of channels is :
  - 8 on STM32L47x/48x/49x/4Ax devices
  - 4 on STM32L45x/46x devices
- The ADC output is connected to DFSDM parallel input channels in STM32L45x/46x/49x/4Ax devices

This slide presents the key differences between product devices.