CS1021 Tutorial #3
Condition Code Flags

(a) Determine whether the Overflow flag would be set after performing each of the following 4-bit arithmetic operations. (Assume a 4-bit microprocessor and a 4-bit 2's Complement system are being used.) Explain your answers.

(i) $0100_2 + 0010_2$

(ii) $0101_2 + 0100_2$

(iii) $1110_2 + 0101_2$

(iv) $1101_2 + 1001_2$

(b) Consider the sets of ARM Assembly Language instructions below. In each case, calculate the value stored in the destination register and state whether each of the N (Negative), Z (Zero), C (Carry) and V (Overflow) flags would be set or clear (1 or 0) after the execution of the highlighted instruction. Provide a detailed explanation for your answer in each case.

(i)

```
1    LDR     R0, =0xC0001000
2    LDR     R1, =0x51004000
3    ADDS    R2, R0, R1
```

(ii)

```
1    LDR     R3, =0x92004000
2    SUBS    R4, R3, R3
```

(iii)

```
1    LDR     R5, =0x74000100
2    LDR     R6, =0x40004000
3    ADDS    R7, R5, R6
```

(iv)

```
1    LDR     R1, =0x6E0074F2
2    LDR     R2, =0x211D6000
3    ADDS    R0, R1, R2
```

(v)

```
1    LDR     R1, =0xBE2FDD2E
2    LDR     R2, =0x41D022D2
3    ADDS    R0, R1, R2
```

(c) Find pairs of 32-bit values which, when added together using the ADDS instruction, cause the following combinations of the conditions code flags to be set or cleared (1 or 0).

(i) N = 0; Z = 0; C = 0; V = 0

(ii) N = 1; Z = 0; C = 0; V = 0

(iii) N = 0; Z = 0; C = 1; V = 0

(iv) N = 1; Z = 0; C = 1; V = 0

(v) N = 0; Z = 1; C = 1; V = 0

(vi) N = 0; Z = 1; C = 0; V = 0

(vii) N = 1; Z = 0; C = 0; V = 1

(viii) N = 0; Z = 0; C = 1; V = 1

(ix) N = 0; Z = 1; C = 1; V = 1