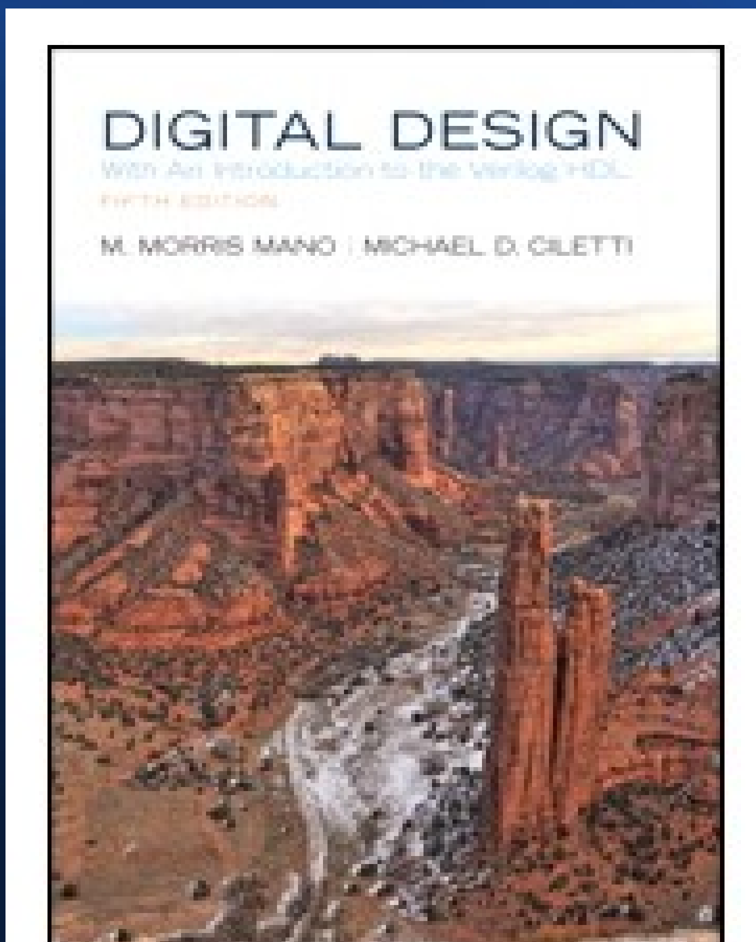
CS1026 Digital Logic Design II

https://www.scss.tcd.ie/John.Waldron/cs1026/cs1026.html

http://www.mypearsonstore.com/bookstore/product.asp?isbn=0132774208



Digital Design, 5th Edition

By M. Morris Mano,
Michael D. Ciletti

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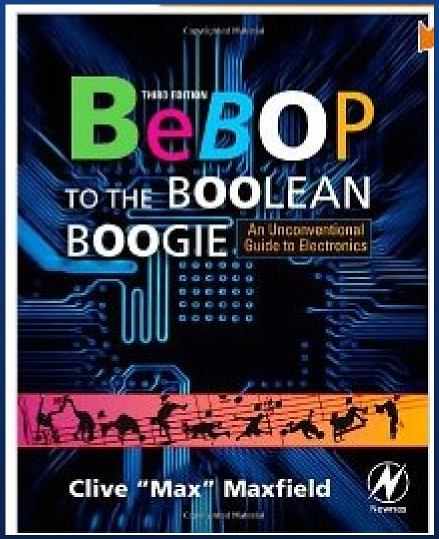
Also recommended, written in a more informal style

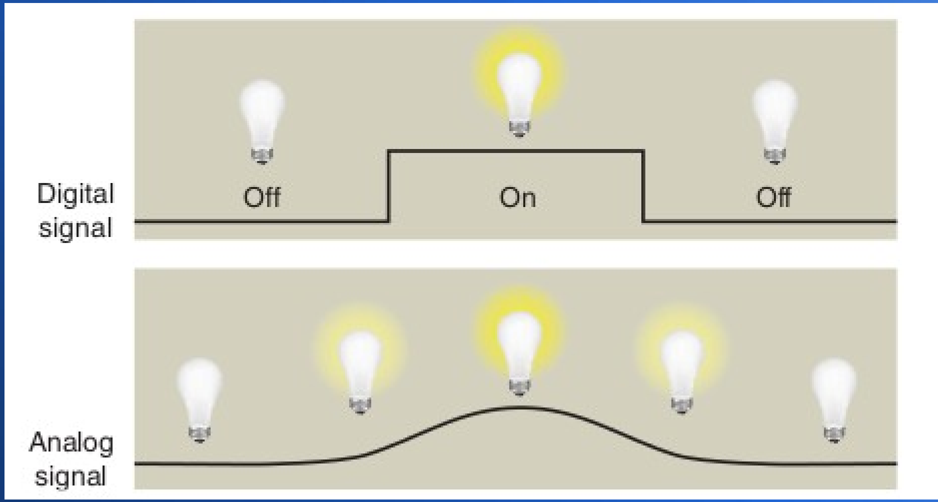


Bebop to the Boolean Boogie,
Third Edition: An Unconventional Guide to Electronics

Clive Maxfield

The only electronics book in the world to include a Seafood Gumbo recipe

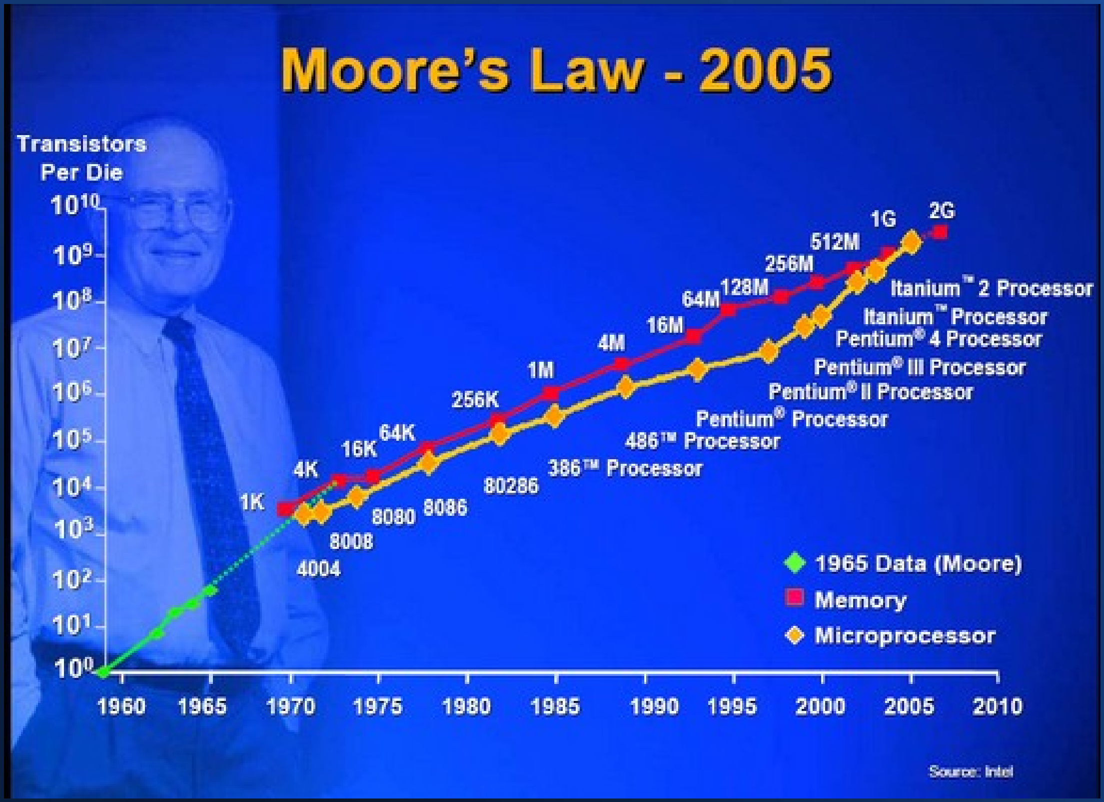
Publication Date: December 23, 2008 | ISBN-10: 1856175073 |
ISBN-13: 978-1856175074 | Edition: 3



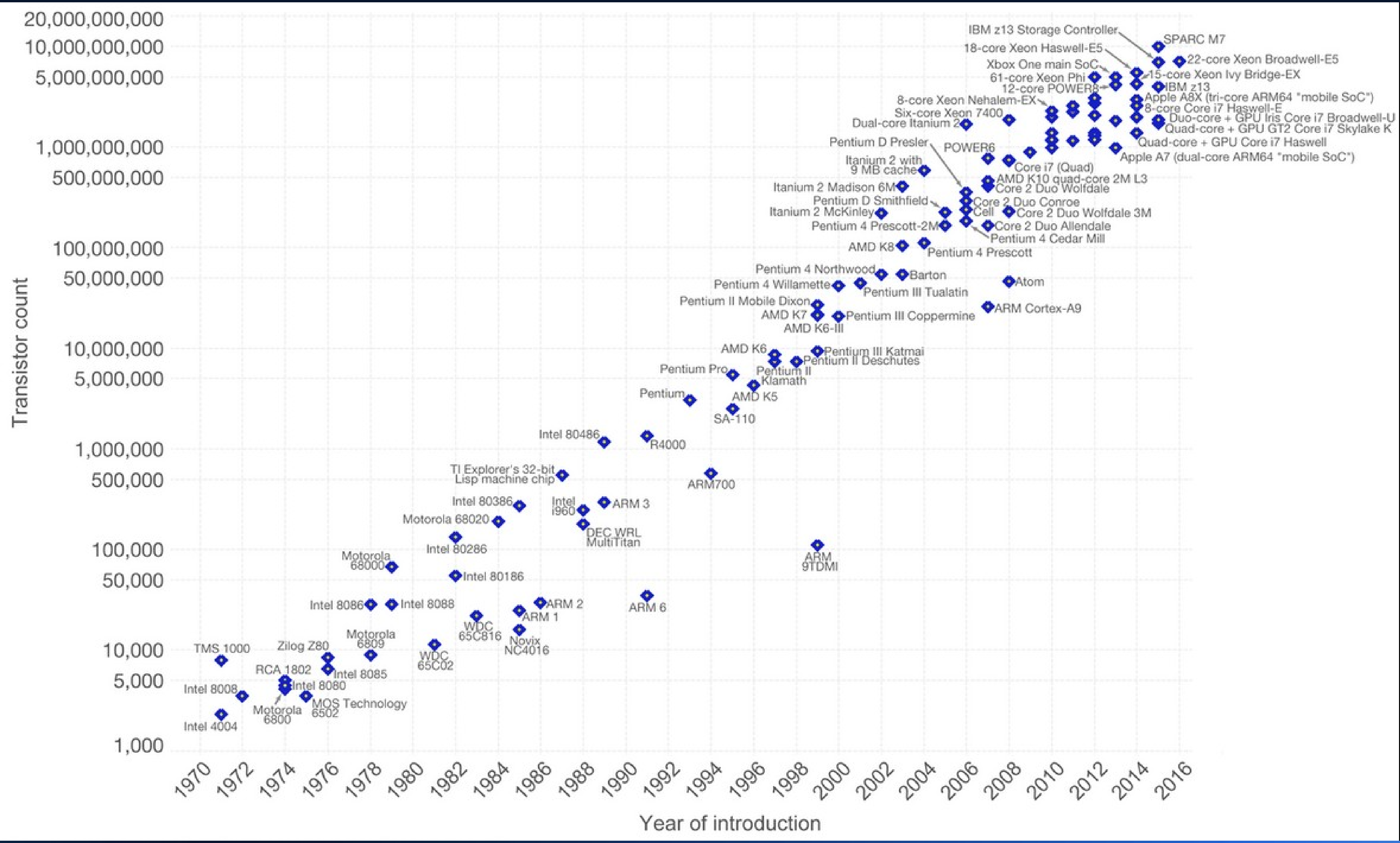
Digital electronics represent signals by discrete bands of analog levels, rather than by a continuous range. All levels within a band represent the same signal state. Relatively small changes to the analog signal levels due to manufacturing tolerance, signal attenuation or parasitic noise do not leave the discrete envelope, and as a result are ignored by signal state sensing circuitry.

The transistor count of a device is the number of transistors in the device. Transistor count is the most common measure of integrated circuit complexity. According to Moore's Law, the transistor count of the integrated circuits doubles every two years.

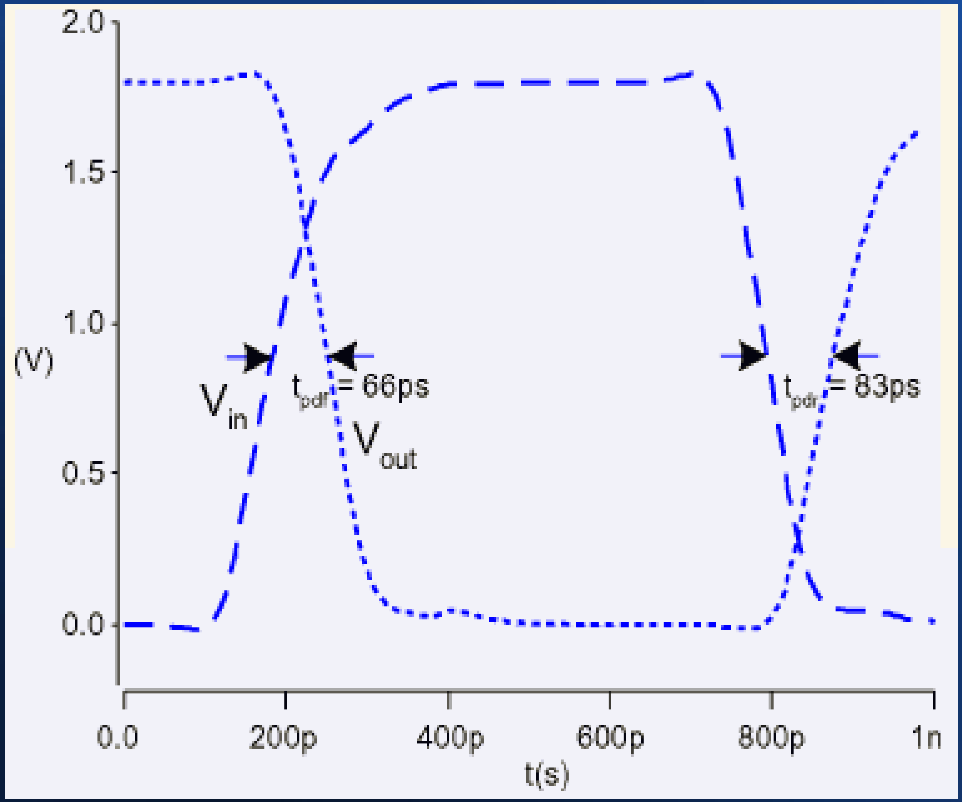
On most modern microprocessors, the majority of transistors are contained in caches.



ICs can be made very compact, having up to several billion transistors and other electronic components in an area the size of a fingernail.


Transistor count
20,000,000,000
10,000,000,000
5,000,000,000
1,000,000,000
500,000,000
100,000,000
50,000,000
10,000,000
5,000,000
1,000,000
500,000
100,000
50,000
10,000
5,000
1,000
1970
1972
1974
1976
1978
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000
2002
2004
2006
2008
2010
2012
2014
2016
Year of introduction
IBM z13 Storage Controller
SPARC M7
18-core Xeon Haswell-E5
22-core Xeon Broadwell-E5
Xbox One main SoC
15-core Xeon Ivy Bridge-EX
61-core Xeon Phi
IBM z13
12-core POWER8
Apple A8X (tri-core ARM64 "mobile SoC")
8-core Xeon Nehalem-EX
8-core Core i7 Haswell-E
Six-core Xeon 7400
Duo-core + GPU Iris Core i7 Broadwell-U
Dual-core Itanium 2
Quad-core + GPU GT2 Core i7 Skylake K
Pentium D Presler
POWER6
Quad-core + GPU Core i7 Haswell
Apple A7 (dual-core ARM64 "mobile SoC")
Itanium 2 with 9 MB cache
Core i7 (Quad)
AMD K10 quad-core 2M L3
Itanium 2 Madison 6M
Core 2 Duo Wolfdale
Pentium D Smithfield
Core 2 Duo Conroe
Itanium 2 McKinley
Cell
Core 2 Duo Wolfdale 3M
Pentium 4 Prescott-2M
Core 2 Duo Allendale
Pentium 4 Cedar Mill
AMD K8
Pentium 4 Prescott
Pentium 4 Northwood
Barton
Pentium 4 Willamette
Atom
Pentium III Tualatin
Pentium II Mobile Dixon
ARM Cortex-A9
AMD K7
Pentium III Coppermine
AMD K6-III
AMD K6
Pentium III Katmai
Pentium II Deschutes
Pentium Pro
Pentium II Klamath
Pentium
AMD K5
SA-110
Intel 80486
R4000
TI Explorer's 32-bit Lisp machine chip
ARM700
Intel 80386
Intel i960
ARM 3
Motorola 68020
DEC WRL MultiTitan
Intel 80286
ARM 9TDMI
Motorola 68000
Intel 80186
Intel 8086
Intel 8088
ARM 2
ARM 6
WDC 65C816
ARM 1
Motorola 6809
Novix NC4016
TMS 1000
Zilog Z80
WDC 65C02
RCA 1802
Intel 8085
Intel 8008
Intel 8080
MOS Technology 6502
Motorola 6800
Intel 4004

Inverter Delay



t_{pdr}: rising propagation delay

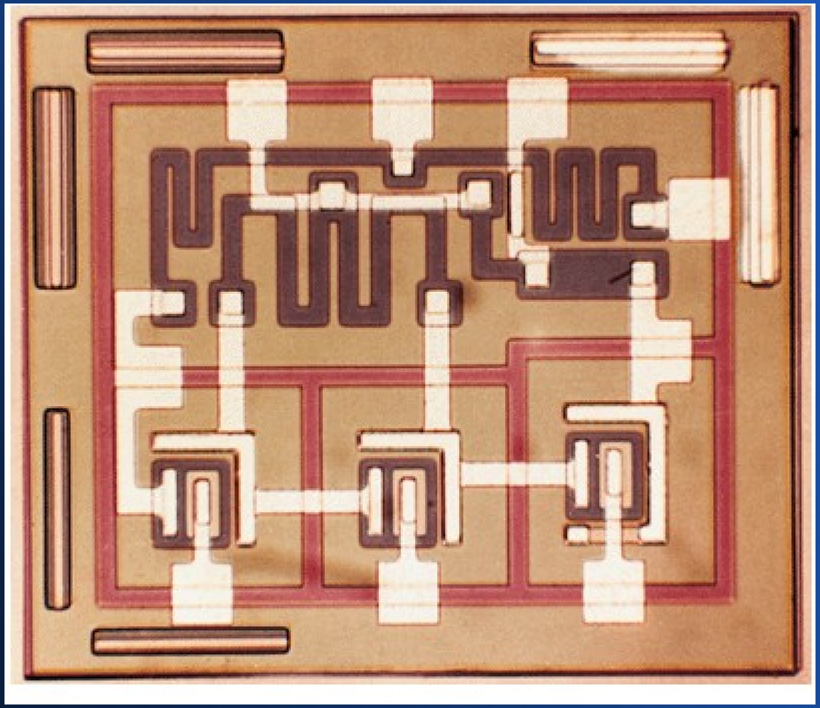
- From input to rising output crossing $V_{DD}/2$

t_{pdf}: falling propagation delay

- From input to falling output crossing $V_{DD}/2$

Pico is a unit prefix in the metric system denoting one trillionth, a factor of 10^−12 (0.000000000001). this was one of the original 12 prefixes defined in 1960 when the International System of Units was established.

This amplifier circuit from Siemens was mass produced in 1965. Containing three transistors and five resistors on a 1.5 mm square chip



15-Core Xeon Ivy Bridge-EX, Transistor count = 4,310,000,000
22 nm process, 23 mm x 23mm = 541 square mm

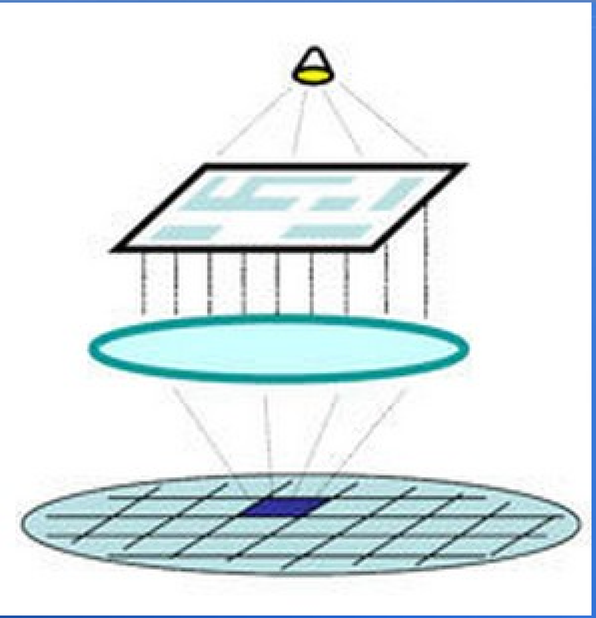
Lithography

Lithography originally used an image drawn with oil, fat, or wax onto the surface of a smooth, level lithographic limestone plate.

The stone was treated with a mixture of acid and gum arabic, etching the portions of the stone which were not protected by the grease-based image.

When the stone was subsequently moistened, these etched areas retained water; an oil-based ink could then be applied and would be repelled by the water, sticking only to the original drawing.

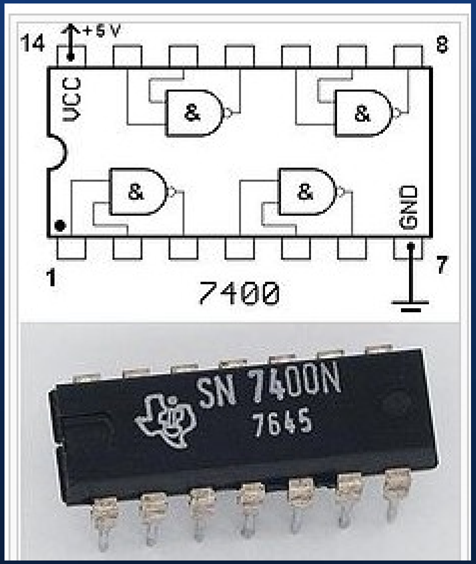
The word lithography comes from the Greek lithos, meaning stones, and graphia, meaning to write. It means quite literally writing on stones.

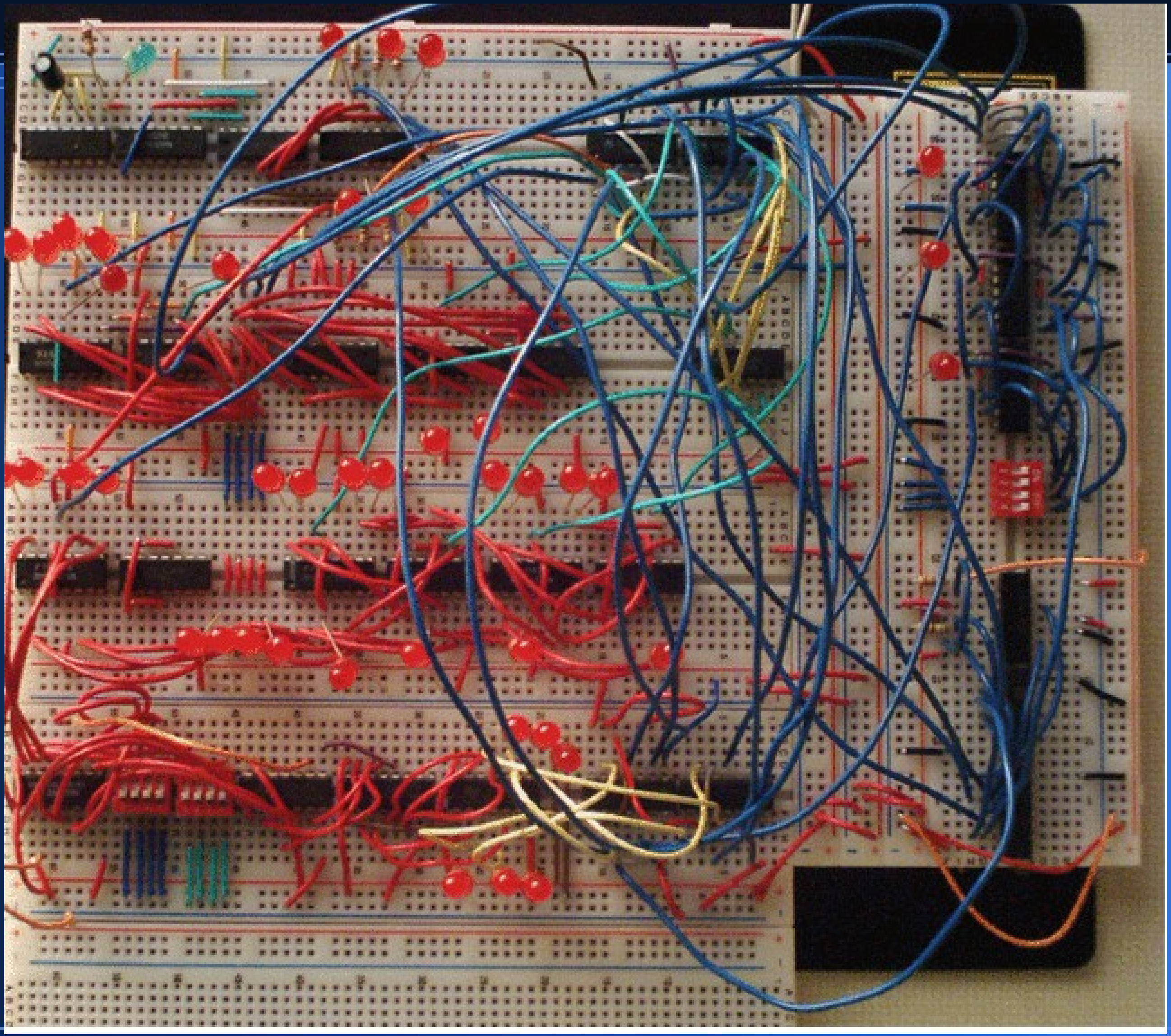


In the case of semiconductor photolithography, our stones are silicon wafers and our patterns are written with a light-sensitive polymer called photoresist.

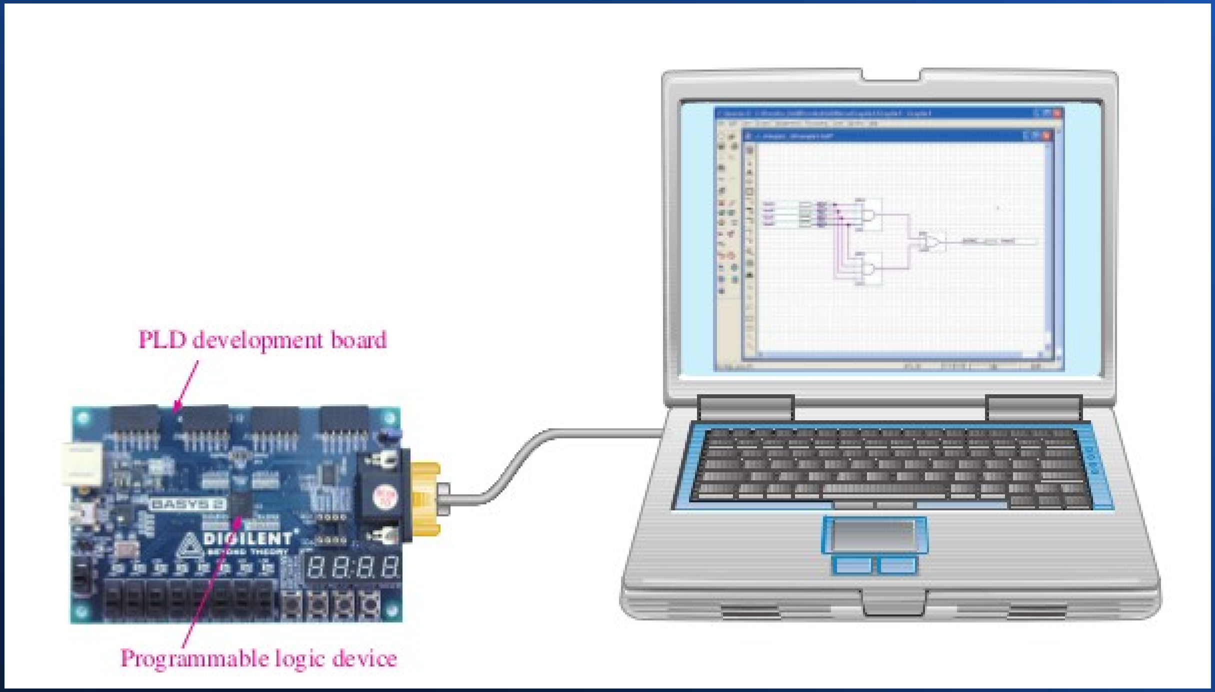
To build the complex structures that make up a transistor and the many wires that connect the millions of transistors of a circuit, lithography and pattern transfer steps are repeated at least 10 times, but more typically are done 20 to 30 times to make one circuit.

Each pattern being printed on the wafer is aligned to the previously formed patterns and slowly the conductors, insulators, and selectively doped regions are built up to form the final device.


14
+5 V
8
VCC
&
GND
1
7
7400
SN 7400N
7645



Verilog HDL is a hardware description language used to design and document electronic systems. Verilog HDL allows designers to design at various levels of abstraction. It is the most widely used HDL with a user community of more than 50,000 active designers.



Logic Synthesis

Verilog is used in two ways

Model for discrete-event simulation

Specification for a logic synthesis system

Logic synthesis converts a subset of the Verilog language into an efficient netlist

One of the major breakthroughs in designing logic chips in the last 20 years

Most chips are designed using at least some logic synthesis

Logic Synthesis Tools

Mostly commercial tools
• Very difficult, complicated programs to write well
• Limited market
• Commercial products in $10k – $100k price range
Major vendors
• Synopsys Design Compiler, FPGA Express
• Cadence BuildGates
• Synplicity (FPGAs)
• Exemplar (FPGAs)
Academic tools
•SIS (UC Berkeley)

Testing

- Testing is one of the most expensive parts of chips
  - Logic verification accounts for > 50% of design effort for many chips
  - Debug time after fabrication has enormous cost
  - Shipping defective parts can sink a company

- Example: Intel FDIV bug
  - Logic error not caught until > 1M units shipped
  - Recall cost $450M (!!!)

Logic Verification

- Does the chip simulate correctly?
  - Usually done at HDL level
  - Verification engineers write test bench for HDL
    - Can't test all cases
    - Look for corner cases
    - Try to break logic design
- Ex: 32-bit adder
  - Test all combinations of corner cases as inputs:
    - 0, 1, 2, 2^{31}-1, -1, -2^{31}, a few random numbers
- Good tests require ingenuity

Synthesis and HDLs

- **Hardware description language (HDL) is a convenient, device-independent representation of digital logic**

Verilog

```
input a,b;
output sum;
assign sum <= {1b'0, a} + {1b'0, b};
```

Compilation and Synthesis

Netlist

```
g1 "and" n1 n2 n5
g2 "and" n3 n4 n6
g3 "or" n5 n6 n7
```

Mapping

FPGA **PAL** **ASIC (Custom ICs)**

- **HDL description is compiled into a netlist**
- **Synthesis optimizes the logic**
- **Mapping targets a specific hardware platform**

Sequential logic

In digital circuit theory, sequential logic is a type of logic circuit whose output depends not only on the present value of its input signals but on the sequence of past inputs, the input history.

This is in contrast to combinational logic, whose output is a function of only the present input.

That is, sequential logic has state (memory) while combinational logic does not.

Synchronous sequential circuits

Digital sequential logic circuits are divided into synchronous and asynchronous types.

In synchronous sequential circuits, the state of the device changes only at discrete times in response to a clock signal.

In asynchronous circuits the state of the device can change at any time in response to changing inputs.

Nearly all sequential logic today is clocked or synchronous logic.

In a synchronous circuit, an electronic oscillator called a clock (or clock generator) generates a sequence of repetitive pulses called the clock signal which is distributed to all the memory elements in the circuit.

The basic memory element in sequential logic is the flip-flop.

The output of each flip-flop only changes when triggered by the clock pulse, so changes to the logic signals throughout the circuit all begin at the same time, at regular intervals, synchronized by the clock.

Asynchronous sequential logic

Asynchronous sequential logic is not synchronized by a clock signal; the outputs of the circuit change directly in response to changes in inputs.

Asynchronous logic is more difficult to design and is subject to problems not encountered in synchronous designs.

The main problem is that digital memory elements are sensitive to the order that their input signals arrive; if two signals arrive at a flip-flop or latch at almost the same time, which state the circuit goes into can depend on which signal gets to the gate first.

Therefore, the circuit can go into the wrong state, depending on small differences in the propagation delays of the logic gates.

This is called a race condition