CS1026 Digital Logic

Assessment Guidelines

This course is assessed by a written exam in May (80%) and continuous assessment throughout the year (20%). The exam paper structure will be the same as last year's paper. To pass the module, students must achieve an overall mark of 40%. If you fail in the annual exams you will have the chance to resit a supplemental paper in late August or early September. In this case 100% of the marks are for the written paper. Students must submit satisfactory course work in each year. Students who fail to do so, or whose attendance is unsatisfactory, may be refused permission to take all or part of the annual examinations for the year. The rest of this document covers the first half of the course before Christmas only, which provides half the exam and half the continuous assessment.

The continuous assessment is based on reports of laboratory sessions constructing basic combinational digital logic circuits using 7400 series chips and breadboards. These labs are aimed to give you experience of the physical reality underlying the theory of digital logic. You will also learn the problem solving, testing and debugging skills needed to work with digital hardware.

You must buy and maintain a hardcover lab book and write a report covering each laboratory assignment. Assignments are only accepted in a lab book, it is not feasible to accept material on individual pieces of paper or electronic devices. Throughout this course marks are awarded for punctuality, neatness, organisation, spelling, ability to communicate technical information and results. The lab book must be kept up to date and will be examined by the Lecturer or Demonstrator during the term. You must hand in your lab book no later than 4pm Monday, 18th December 2017, to the School of Computer Science and Statistics Reception, Ground Floor, The O'Reilly Institute. The office does not accept submissions after 4pm. Do not forget to write your name, student number and course clearly on the cover.

If you miss a small part of the continuous assessment contact the Demonstrator, it will be assumed you have a valid medical or personal reason and you will be scheduled at an alternative time. If you miss a large percentage of the continuous assessment then you need to get medical certificates or other supporting documentation and attach to the inside cover of your lab book when you submit it.

A report should be between one and two A4 pages in length and contain

- Title
- Date
- Aim (To design logic to yield F=1 when ...)
- Analysis (start with a truth table, then Kmaps, ...)
- Logic Diagram
- Results (table of test inputs, test outputs)
- Conclusion

At the first lab you will be given a kit with the following components which you keep until the last lab, when you return it to the demonstrator. You must return you wiring kit at your last lab.

- 1 x 7404 Hex Inverter
- 1 x 7425 Dual 4-Input NOR Gate
- 1 X 7400 Quad 2-input NAND
- 2 x 7411 Triple 3-Input AND Gate
- 1 x 74138 3 to 8-line decoder/demultiplexer
- 1 x 74151 8-line to 1-line data selector/multiplexer
- 1 x LED
- 1 x 8-WAY SWITCH
- 1 x RES PACK 2.2K
- 2 x RES 2.2Kohm
- 1 x RES 470ohm
- 1 x Wiring kit

There are also extra wires in a cabinet in LG36 which will have longer wires and spares. Try to keep the original kits as intact as possible as we can use them again. There are 10 IC extractor tools in the cabinet for the class to share, please use them when packing up at the end of a lab session, they might lengthen the life of the IC's.

Some precautions:

- Do not drop it – the AC transformer is heavy and can break loose.
- Do not connect +5V and GND together!
- Do not connect a gate output to +5V – mostly it will survive, but there is no protection so eventually the output will fail.
- Do not connect switch outputs to +5V or GND.
- Turn off AC power when pulling out wires, otherwise accidental connections like the above might occur.