## CS1026 II Assignment 6

Write a Verilog dataflow description

module BCD\_Adder (Sum, Carry\_out, Addend, Augend, Carry\_in);

of a four-bit binary coded decimal adder.

Begin by writing a four bit binary adder module. Instantiate this twice in your binary coded decimal module and use structural verilog to provide the outputs.

CS1026 II 1