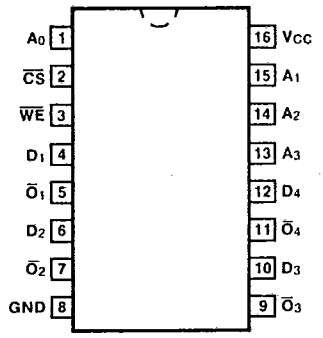
T-46-23-08

54S/74S189
54LS/74LS189

64-BIT RANDOM ACCESS MEMORY
(With 3-State Outputs)

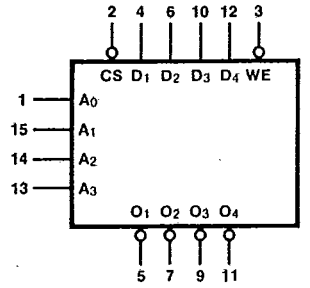
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '189 is a high speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

- **3-STATE OUTPUTS FOR DATA BUS APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S189PC, 74LS189PC		9B
Ceramic DIP (D)	A	74S189DC, 74LS189DC	54S189DM, 54LS189DM	6B
Flatpak (F)	A	74S189FC, 74LS189FC	54S189FM, 54LS189FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.63/0.16	0.5/0.013
$\overline{CS}$	Chip Select Input (Active LOW)	0.63/0.16	0.5/0.013
$\overline{WE}$	Write Enable Input (Active LOW)	0.63/0.16	0.5/0.013
$D_1 - D_4$	Data Inputs	0.63/0.16	0.5/0.013
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	162/10 (50)	10/10 (5.0)

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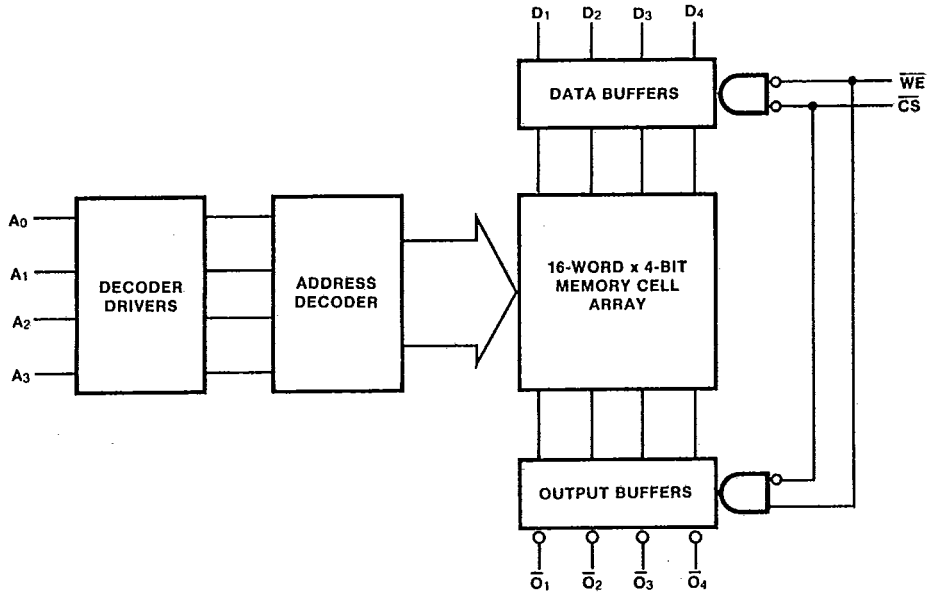
FUNCTION TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage	XM		0.5		0.4	V	V_{CC} = Min I_{OL} = 16 mA ('S189) I_{OL} = 8.0 mA (54LS189) I_{OL} = 16 mA (74LS189)
		XC		0.45		0.5		
V_{OH}	Output HIGH Voltage	XM	2.4		2.8		V	V_{CC} = Min I_{OH} = 2.0 mA (54S189) I_{OH} = 6.5 mA (74S189) I_{OH} = 0.4 mA ('LS189)
		XC	2.4		2.8			
I_{OS}	Output Short Circuit Current		-30	-100	-80*		mA	V_{CC} = Max
I_{CC}	Power Supply Current			110		40	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$, Gnd

*Typical Value

AC CHARACTERISTICS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S C_L = 30 pF, R_L = 300 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Access Time, HIGH or LOW, A_n to $\overline{O}_n$	XM XC		50 35		37* 37*	ns	Figs. 3-1, 3-20
t_{PZH} t_{PZL}	Access Time, HIGH or LOW, $\overline{CS}$ to $\overline{O}_n$	XM XC		32 22		10* 10*	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189)
t_{PHZ}	Disable Time $\overline{CS}$ to $\overline{O}_n$	XM XC		25 25			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189) C_L = 5 pF
t_{PLZ}	Disable Time $\overline{CS}$ to $\overline{O}_n$	XM XC		25 17				
t_{PZH} t_{PZL}	Access Time, HIGH or LOW, $\overline{WE}$ to $\overline{O}_n$	XM XC		40 30			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189)
t_{PHZ}	Disable Time $\overline{WE}$ to $\overline{O}_n$	XM XC		30 20			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189) C_L = 5 pF
t_{PLZ}	Disable Time $\overline{WE}$ to $\overline{O}_n$	XM XC		32 20				

AC OPERATING REQUIREMENTS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{WE}$	0 0		10* 10*		ns	Fig. 3-21
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to $\overline{WE}$	0 0		0* 0*		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{WE}$	20 20		25* 25*		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{WE}$	0 0		0* 0*		ns	
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-14
t_h (L)	Hold Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-13
t_w (L)	$\overline{WE}$ Pulse Width LOW	20		25*		ns	Fig. 3-14

*Typical Value

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