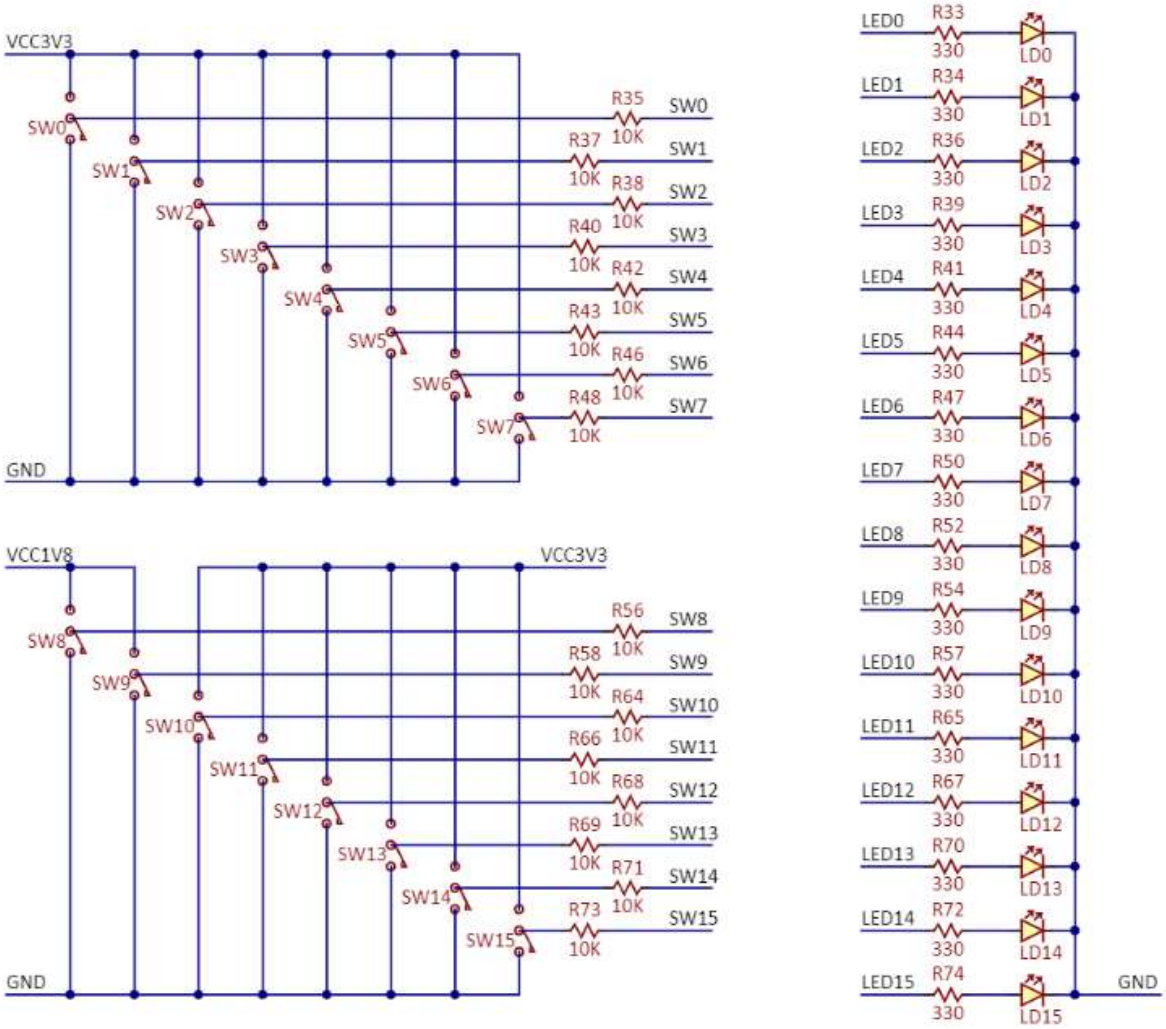
Laboratory 3 - Vivado

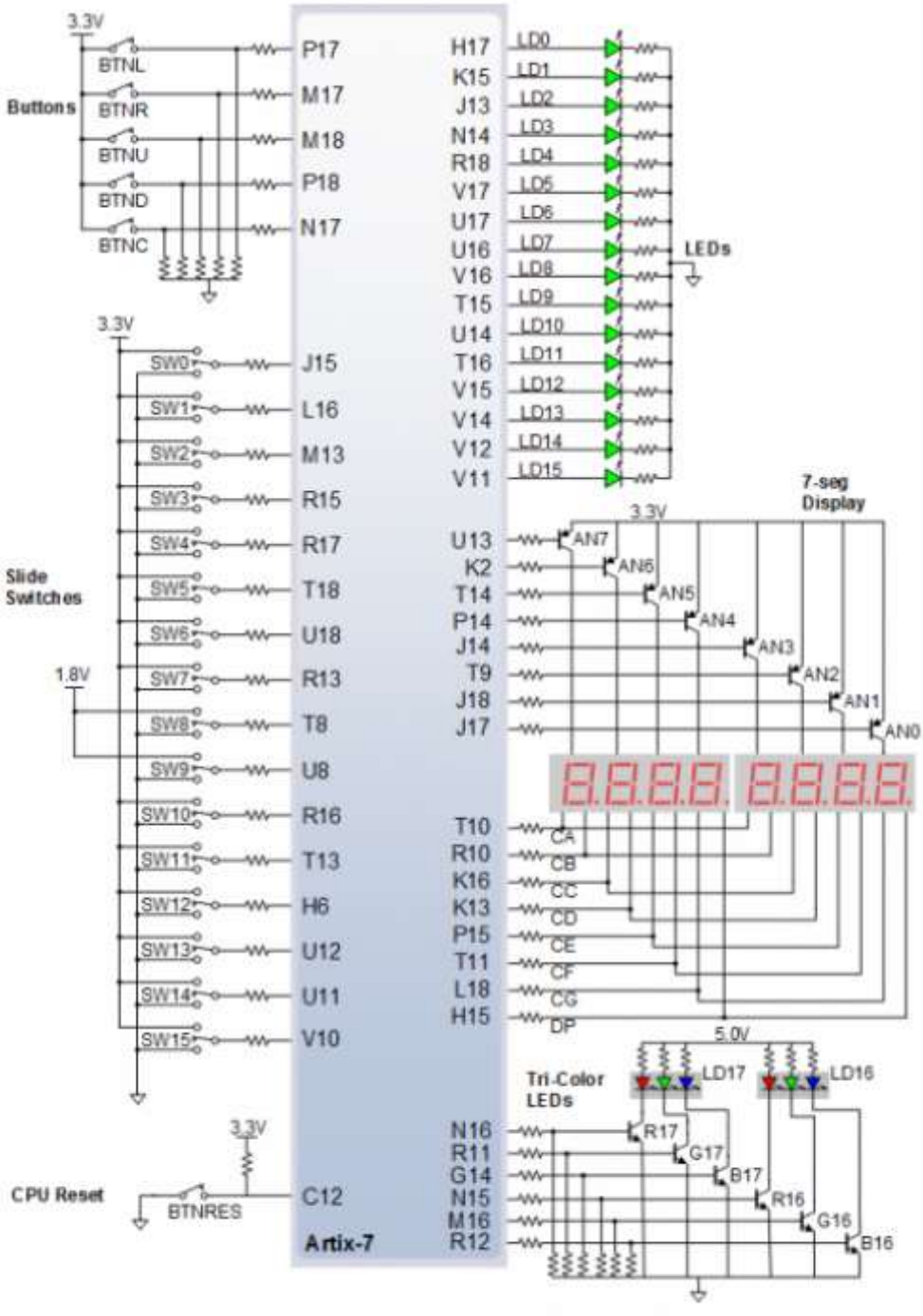
Nexys FPGA

More information on GitHub Tomáš Frýza

My GitHub

Preparation of Laboratory


VCC3V3
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
GND
R35 10K
R37 10K
R38 10K
R40 10K
R42 10K
R43 10K
R46 10K
R48 10K
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
VCC1V8
VCC3V3
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
GND
R56 10K
R58 10K
R64 10K
R66 10K
R68 10K
R69 10K
R71 10K
R73 10K
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
LED0 R33 330 LD0
LED1 R34 330 LD1
LED2 R36 330 LD2
LED3 R39 330 LD3
LED4 R41 330 LD4
LED5 R44 330 LD5
LED6 R47 330 LD6
LED7 R50 330 LD7
LED8 R52 330 LD8
LED9 R54 330 LD9
LED10 R57 330 LD10
LED11 R65 330 LD11
LED12 R67 330 LD12
LED13 R70 330 LD13
LED14 R72 330 LD14
LED15 R74 330 LD15
GND



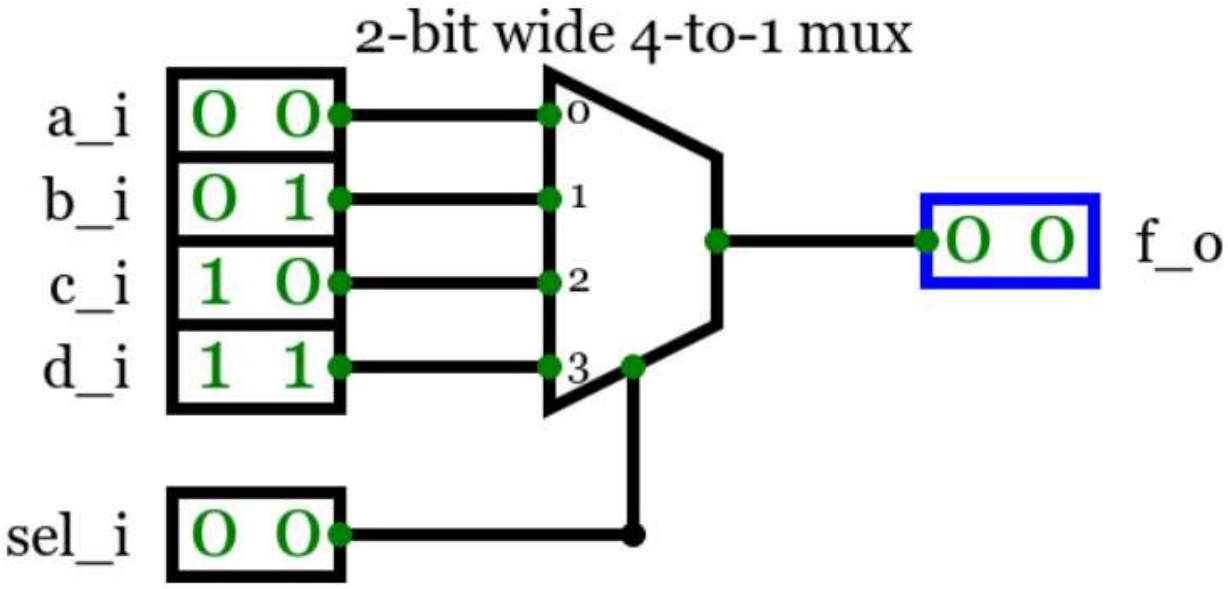
Install Vivado

Creating project

Laboratory - Multiplexer

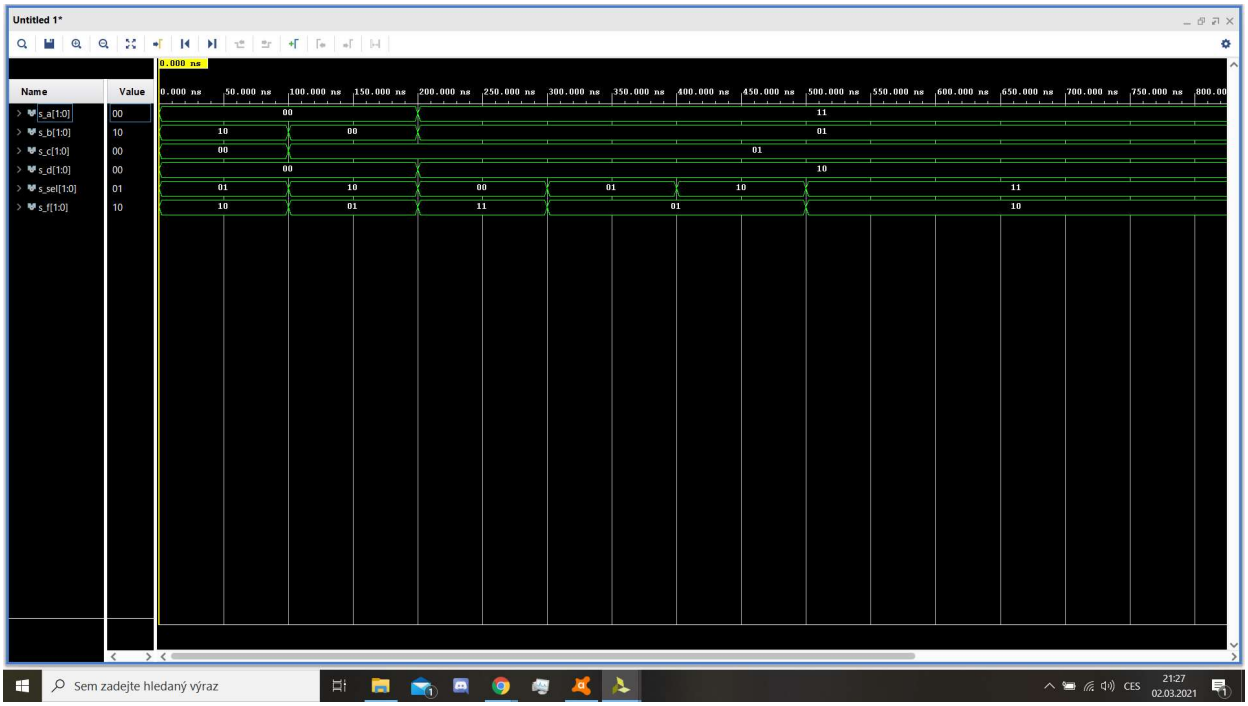
Comparator_4

Select sel_i[1:0]	Output f_o[1:0]
0 0	a_i[1:0]
0 1	b_i[1:0]
1 0	c_i[1:0]
1 1	d_i[1:0]



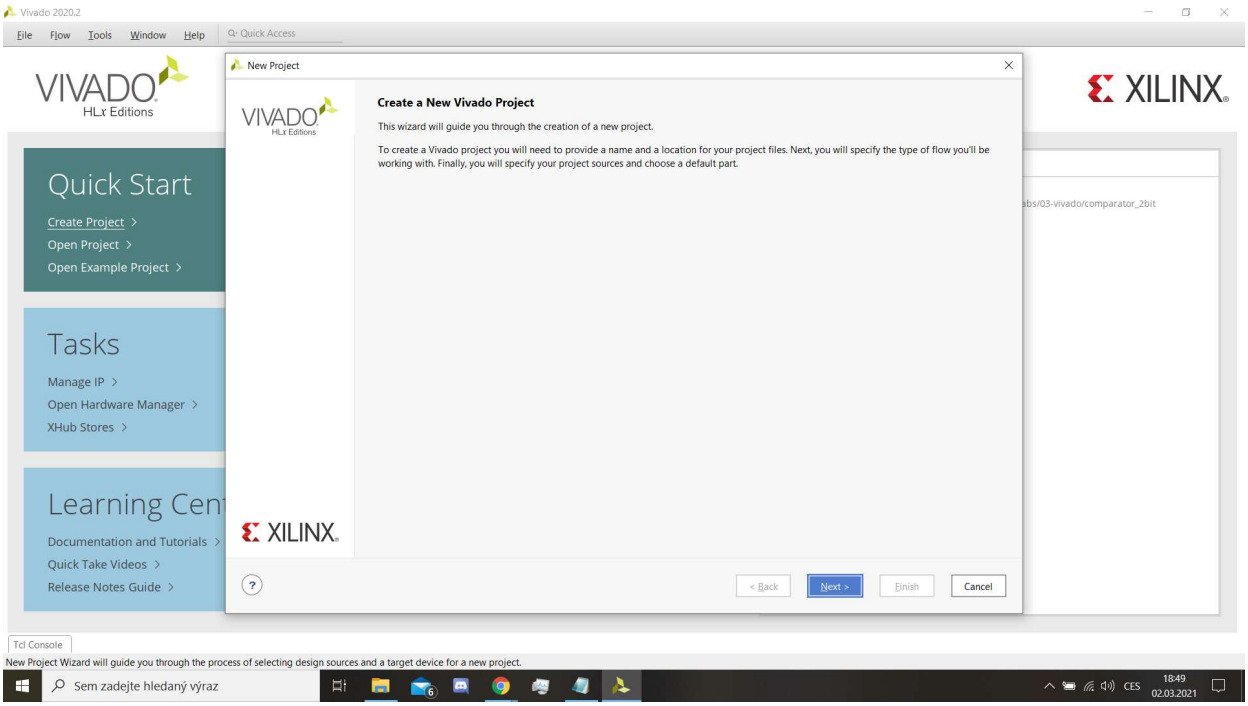

```
-------------------------------------------------------------------------
architecture Behavioral of mux_2bit_4to1 is
begin
f_o <= a_i when (sel_i = "00") else
       b_i when (sel_i = "01") else
       c_i when (sel_i = "10") else
       d_i;

end architecture Behavioral;



-------------------------------------------------------------------------
    p_stimulus : process
    begin
        -- Report a note at the begining of stimulus process
        report "Stimulus process started" severity note;

        s_a <= "00"; s_b <= "10"; s_c <= "00"; s_d <= "00";
        s_sel <= "01"; wait for 100 ns;

        s_a <= "00"; s_b <= "00"; s_c <= "01"; s_d <= "00";
        s_sel <= "10"; wait for 100 ns;

        s_a <= "11"; s_b <= "01"; s_c <= "01"; s_d <= "10";
        s_sel <= "00"; wait for 100 ns;
```

```
        s_sel <= "01"; wait for 100 ns;

        s_sel <= "10"; wait for 100 ns;

        s_sel <= "11"; wait for 100 ns;

        -- Report a note at the end of stimulus process
        report "Stimulus process finished" severity note;

        wait;
    end process p_stimulus;
```

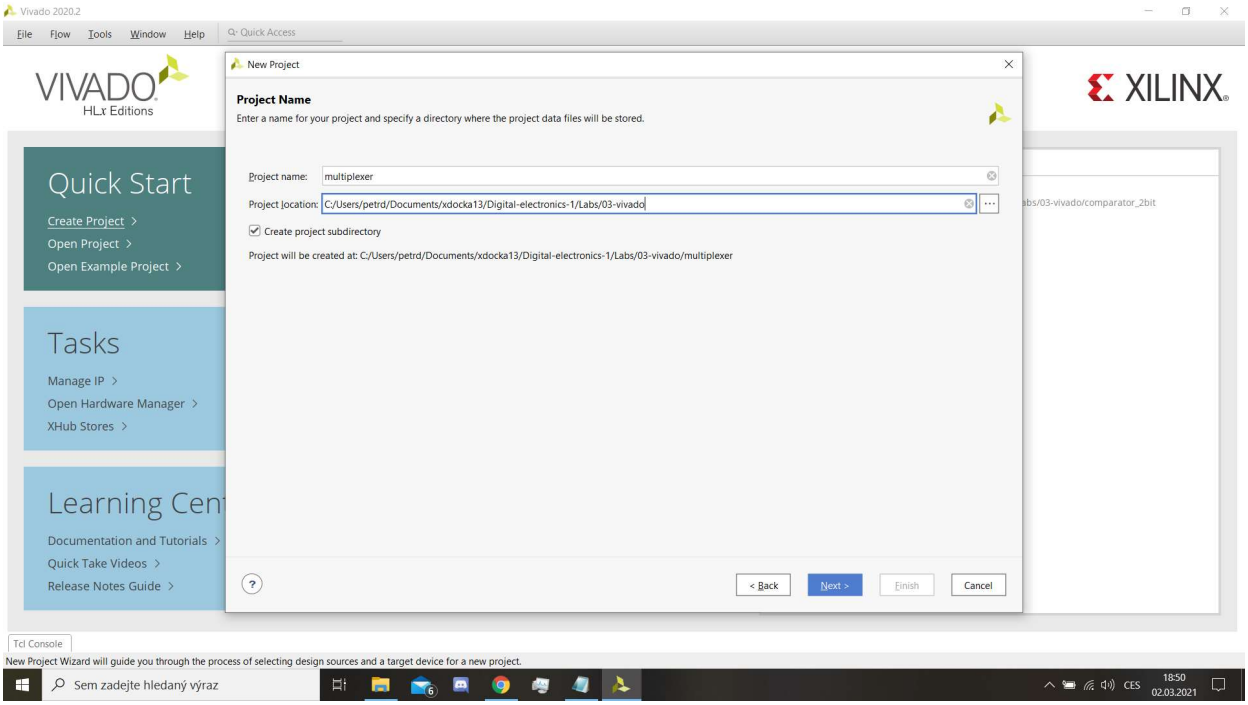


Tutorial

Step 1


Vivado 2020.2
File Flow Tools Window Help
Quick Access
VIVADO HLx Editions
XILINX
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores
Learning Cent
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
New Project
Create a New Vivado Project
This wizard will guide you through the creation of a new project.
To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
< Back
Next >
Finish
Cancel
Tcl Console
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.
Sem zadejte hledaný výraz
CES
18:49
02.03.2021

Step 2


Vivado 2020.2
File Flow Tools Window Help
Quick Access
VIVADO HLx Editions
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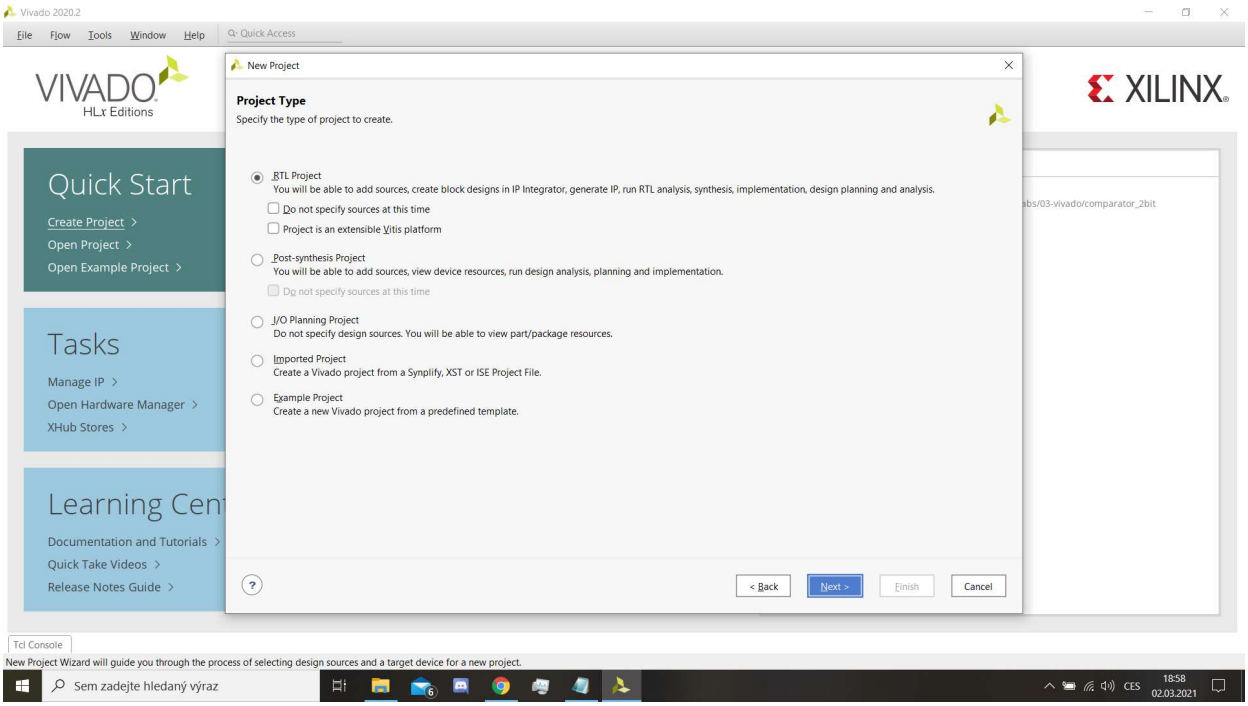
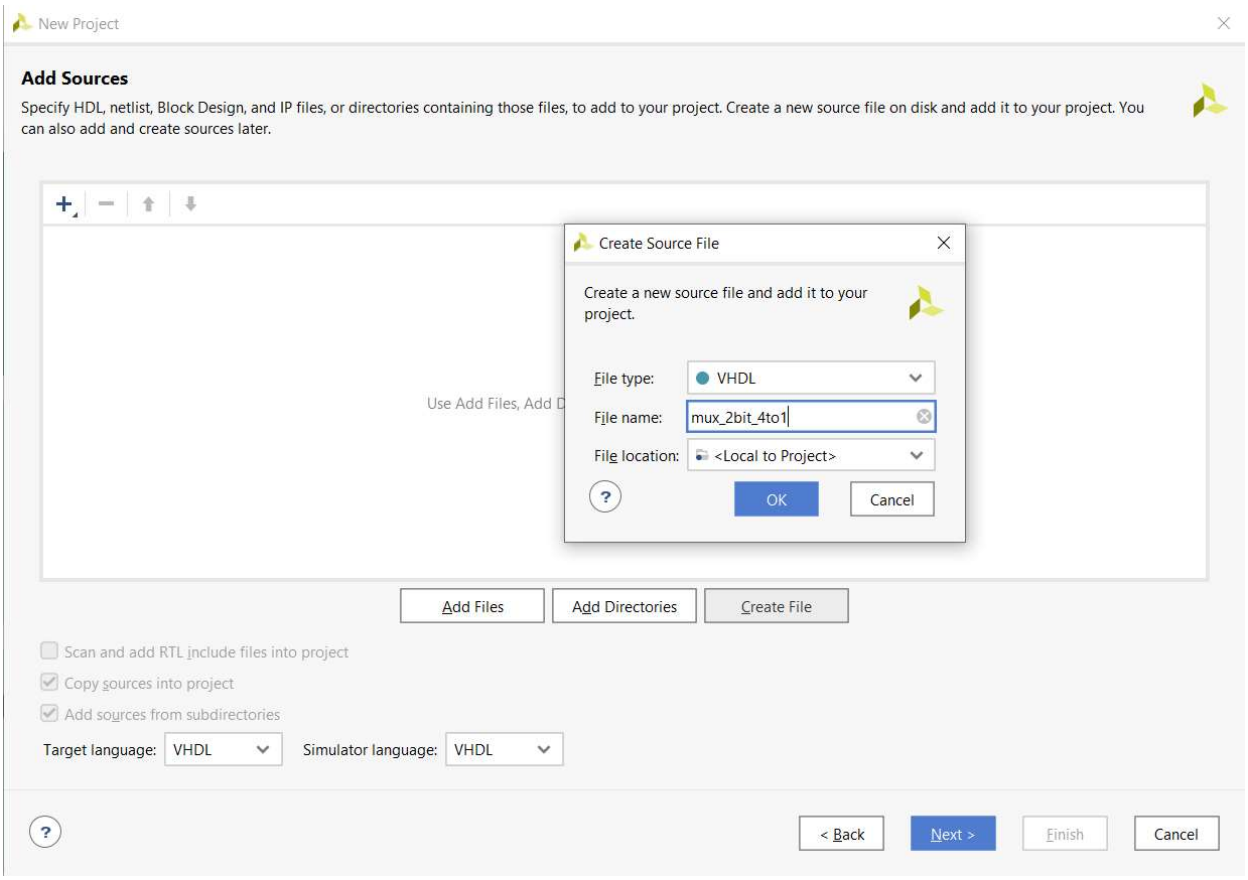
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores
Learning Cent
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name: multiplexer
Project location: C:/Users/petrd/Documents/xdocka13/Digital-electronics-1/Labs/03-vivado
Create project subdirectory
Project will be created at: C:/Users/petrd/Documents/xdocka13/Digital-electronics-1/Labs/03-vivado/multiplexer
< Back
Next >
Finish
Cancel
Tcl Console
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.
Sem zadejte hledaný výraz
CES
18:50
02.03.2021

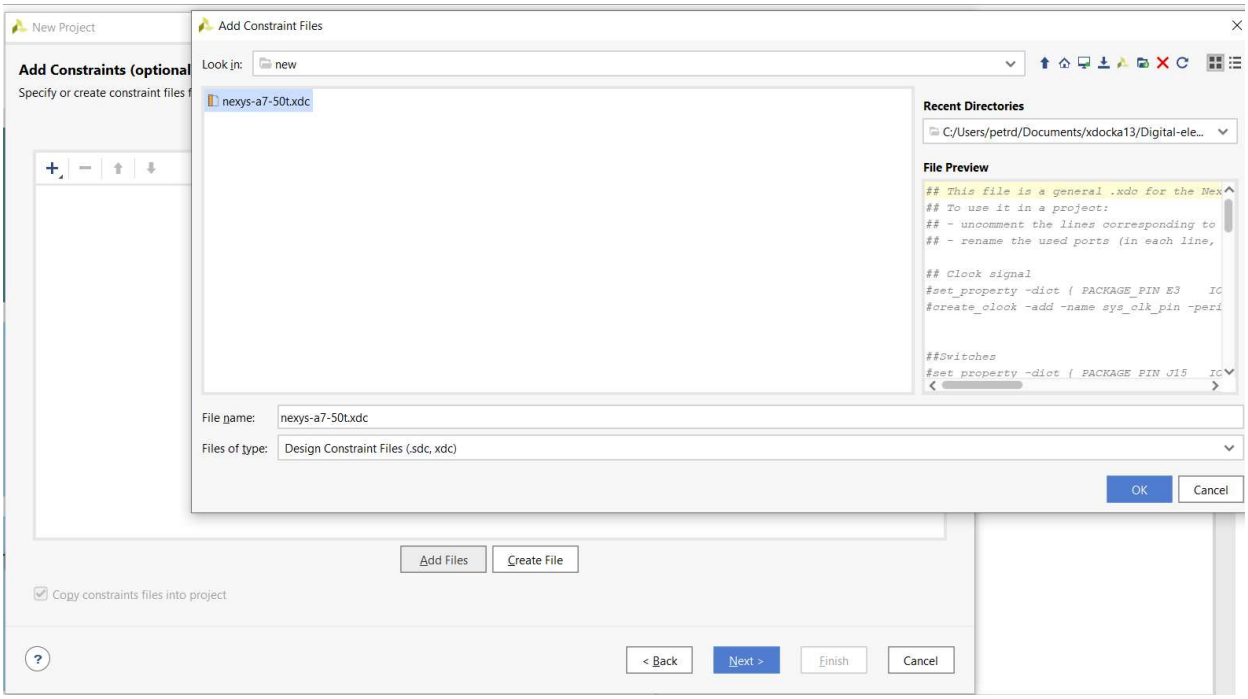
Step 3


Vivado 2020.2
File Flow Tools Window Help
Quick Access
VIVADO HLx Editions
XILINX
New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores
Learning Cent
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
< Back
Next >
Finish
Cancel
Tcl Console
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.
Sem zadejte hledaný výraz
CES
18:58
02.03.2021

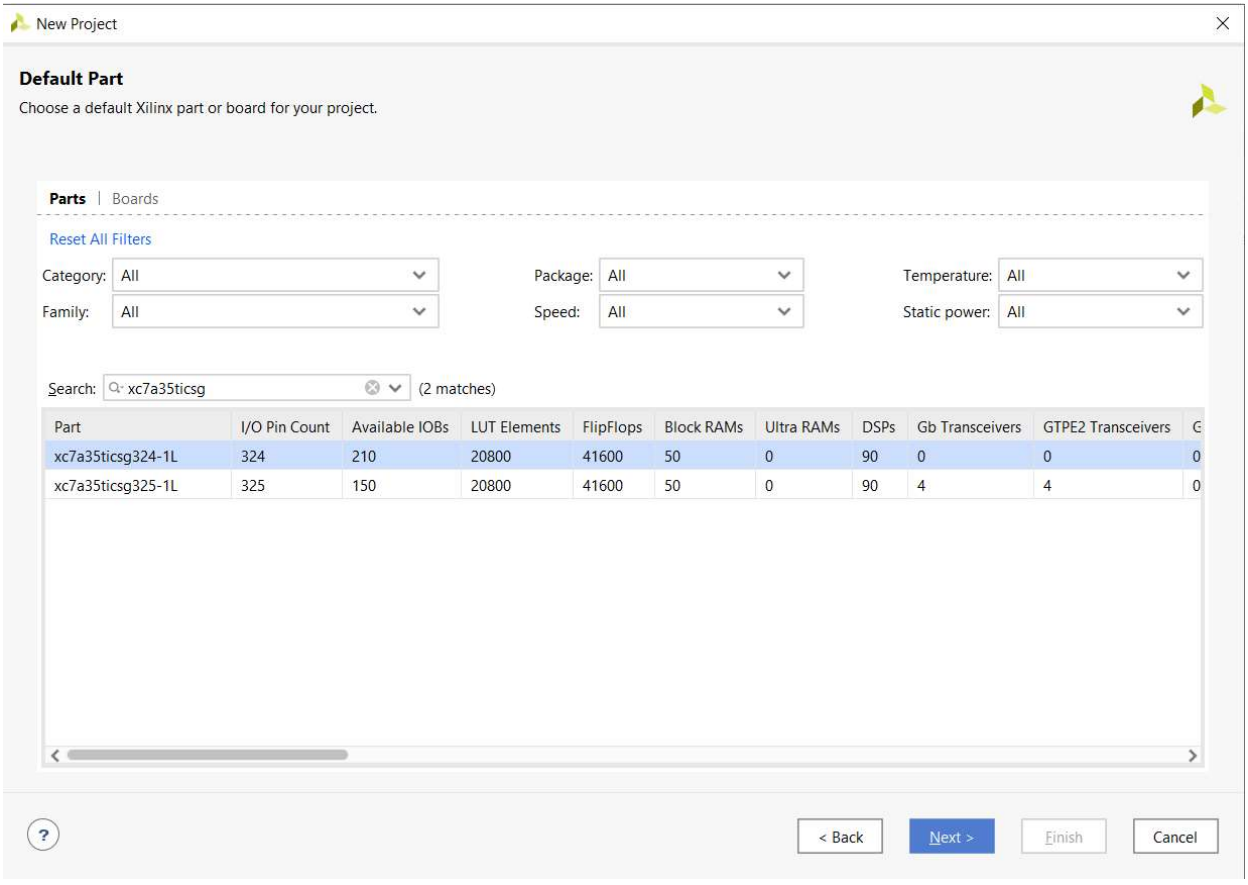
Step 4


New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Create Source File
Create a new source file and add it to your project.
File type: VHDL
File name: mux_2bit_4to1
File location: <Local to Project>
OK
Cancel
Use Add Files, Add D
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel

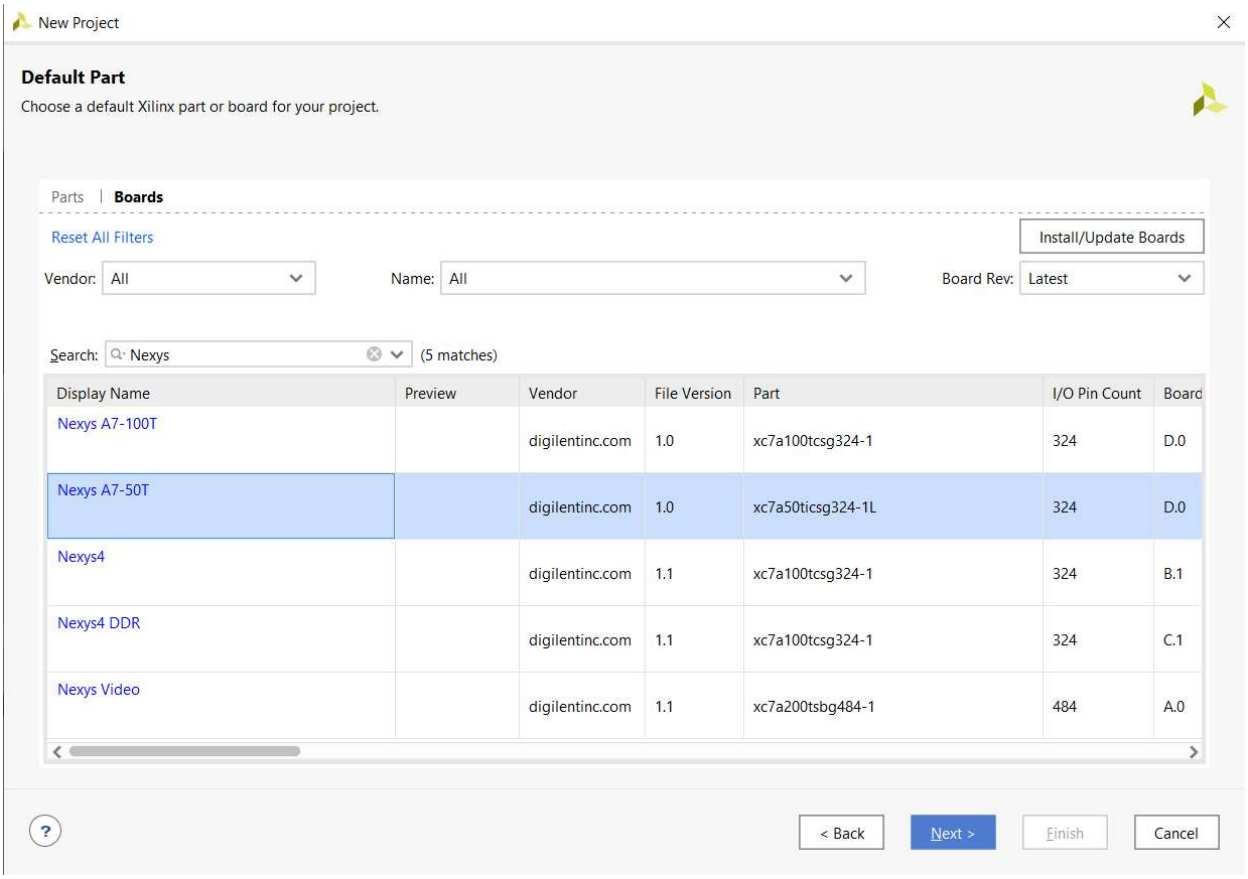
Step 5


New Project
Add Constraints (optional
Specify or create constraint files
Add Constraint Files
Look in:
new
nexys-a7-50t.xdc
Recent Directories
C:/Users/petrd/Documents/xdocka13/Digital-ele...
File Preview
This file is a general .xdc for the Nex
To use it in a project:
- uncomment the lines corresponding to
- rename the used ports (in each line,
Clock signal
#set_property -dict { PACKAGE_PIN E3
#create_clock -add -name sys_clk_pin -peri
##Switches
#set_property -dict { PACKAGE_PIN J15
File name:
nexys-a7-50t.xdc
Files of type:
Design Constraint Files (.sdc, xdc)
OK
Cancel
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

Step 6

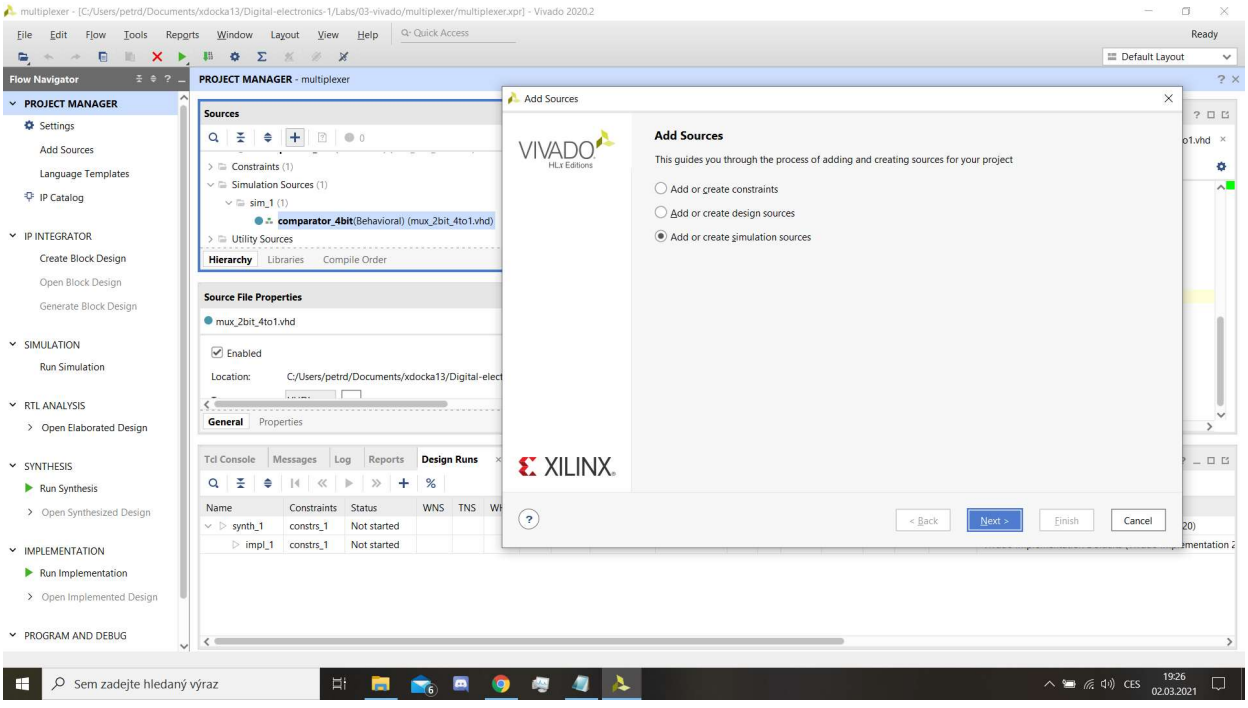

New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Category: All
Package: All
Temperature: All
Family: All
Speed: All
Static power: All
Search: xc7a35ticsg
(2 matches)
Part
I/O Pin Count
Available IOBs
LUT Elements
FlipFlops
Block RAMs
Ultra RAMs
DSPs
Gb Transceivers
GTPE2 Transceivers
xc7a35ticsg324-1L
324
210
20800
41600
50
0
90
0
0
xc7a35ticsg325-1L
325
150
20800
41600
50
0
90
4
4
< Back
Next >
Finish
Cancel

Step 7

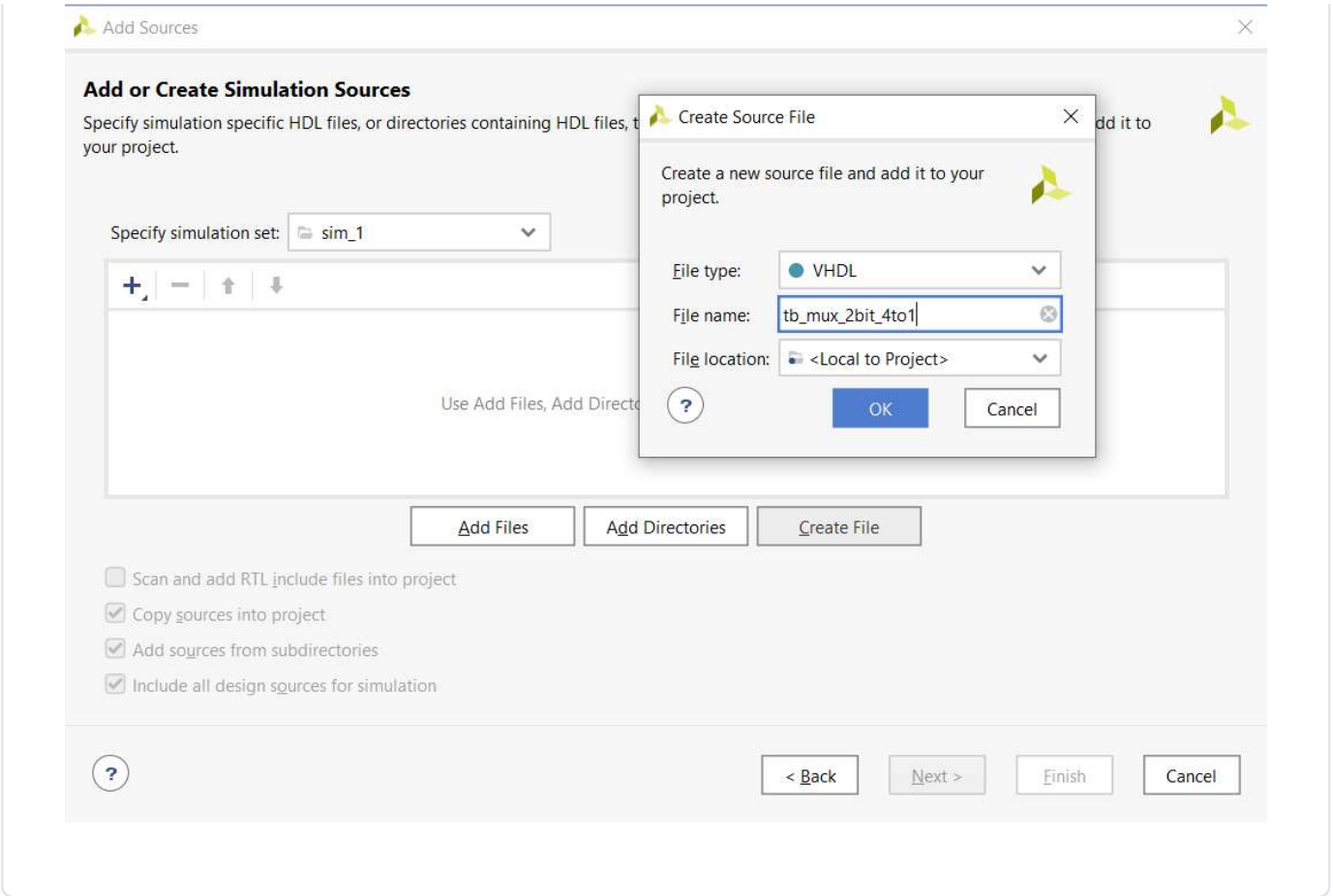


Other tables must give "Ok" or "Yes".

Step 8



Step 9


Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, t
your project.
dd it to
Specify simulation set:
sim_1
Use Add Files, Add Directo
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel
Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
tb_mux_2bit_4to1
File location:
<Local to Project>
OK
Cancel