

# ICARUS connectivity test — December 2018

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## Abstract

We present here the updated procedure and results of the connectivity tests done on the TPCs wire planes of the ICARUS detector on December 2018. The test verified the connection of the TPC wires up to the connectors to the readout boards just outside the cryostats. All wires were tested on all three planes, with the exception of the shorter wires in the second induction and in collection planes, that are read out from one of the eight chimneys at the end of the detector.

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## 1 Introduction

ICARUS detector comprises two twin modules, counting more than 50,000 wires[1], each one independently read out. The goal of a “connectivity test” is to verify the electric continuity from each wire to the readout boards. In fact, the aim is to diagnose major problems early enough that they can be immediately fixed, reduced or mitigated. In particular, we aim to detect and correct any complete failure on a cable, which carries 32 contiguous channels, to attempt the correction of failures involving a few contiguous channels, and to record isolated single channel failures.

A first test was performed starting on August 2018[3], where connectivity was verified between the wires and the cables bringing the signal to the chimneys. This report describes in detail the test performed on December 2018<sup>1</sup>, which extends the test to the decoupling and biasing boards (DBB) and the interface connector on the flanges. This is part of the wider connectivity test effort, which is described in [3]. The relevant detector configuration is described in section 2 and the test methodology is described in section 3. A summary of some of the findings are reported in section 4.

Details of the operations are described in appendix A and appendix B.

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<sup>1</sup> Part of the data has been eventually collected in February 2019.

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## 2 Detector description

To check:

- bias voltage levels on the wire planes
- grounding
- the general description of the connections

The ICARUS detector includes two modules (T300), each with two TPC's sharing the cathode, which will be kept at a potential of  $-75\text{ kV}$ . Each TPC anode is made of three wire planes (fig. 1), which are kept at a potential close to the ground. The first one, commonly called first induction plane, has horizontal wires, each about 10 meters long and spanning half of the detector, and kept at  $-300\text{ V}$ . Each half plane includes 1056 channels, all ending on the sides of the anode plane frame. Three millimeters away, the second plane ("second induction plane") is made of wires at an angle of  $\pi/6$  from the vertical ( $\pi/3$  from the horizontal wires) at ground (0 V). Its wires can be grouped in three sets: the longest ones, terminated on the top and on the bottom of the anode plane frame<sup>2</sup>, the shorter ones that terminate on the bottom and on the side of the anode frame, and the shorter ones that terminate on the top and on the side of the frame. Located other 3 mm away, the third plane ("collection plane") is similar to the second induction plane, but with angle  $\pi/6$  of the other side of the vertical, and at 300 V. Its wires follow the same categories.

At the top termination, or at the side termination if no top one is present, the wires are pinned in groups of 32 on a board (*Comb-to-Cable Interface*, CCI) and their signal conveyed to a 68 pin connector. Each board is about 11 cm long ( $32 \times 3\text{ mm} / \cos \pi/6$ ) on the top frame. The connector hosts a twisted pair cable, with 34 pairs of wires, one in each pair connected to the wire and carrying the signal, and the other twisted around the former to shield it from interference. The highest two pairs (number 33 and 34) of the cable are not used for transmission of signal. In the final configuration of the detector, shield wires are grounded via the readout boards, but in the detector configuration at time of the test readout boards are not present yet and the shield wire electric potential is expected to be floating. It became evident in the previous connectivity test that, regardless the design intentions, some of the shield wires are actually grounded to the detector, while others are not grounded. This feature has been confirmed by previous observations from the time when the detector was being refurbished at CERN. All the cables are cut to be of the same length, resulting into the ones to the closest wires having a lot of spare length, and into the ones to the farthest wires having little to none.

Cables from the top of the anode frame are tied in bundles of 18, half from the second induction and half from the collection plane, to pass through a "chim-

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<sup>2</sup>The wires are spaced at  $d = 3\text{ mm}$ , and their terminations are spaced at  $2/\sqrt{3}d = 3.46\text{ mm}$ .

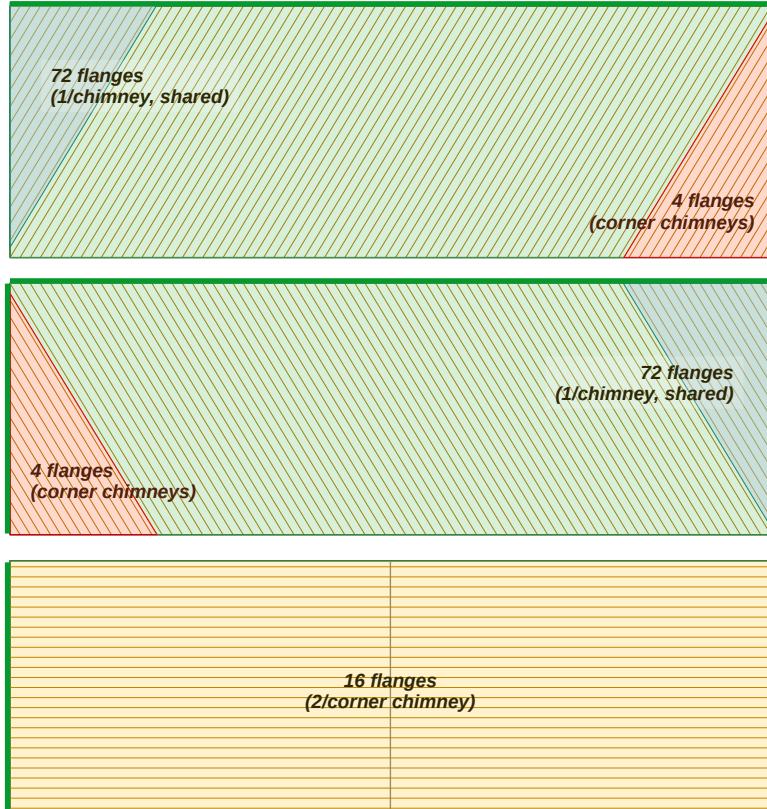
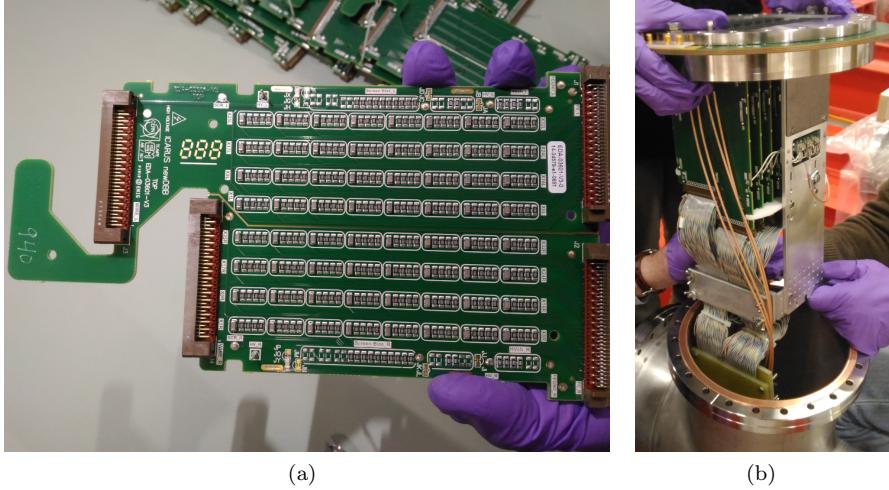


Figure 1: The wires in a single TPC (not in scale!) coded by category. The top plane (*collection*) and middle plane (*second induction*) feature three different categories of wires: side-to-bottom (*in red*), top-to-bottom (*in green*) and top-to-side (*in blue*), while the last plane (*first induction*) has middle-to-side wires (*in yellow*). The thick green borders represent the sides where the TPC wires are connected to the 68-wire cables.



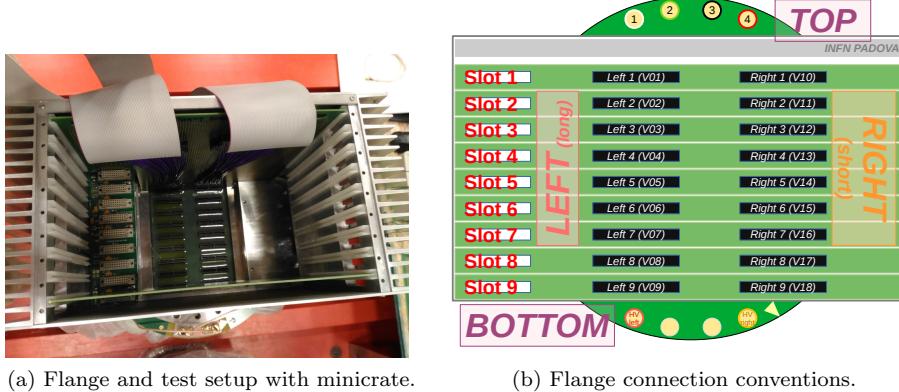
(a)

(b)

Figure 2: (a) a decoupling and biasing board; (b) a flange with nine DBB’s being positioned back into its chimney. The four golden cables connect to the test capacitance at the bottom of the anode frame. On the right side, the distribution of bias voltage can be seen, from a single cable into three and then nine channels to the long side of each DBB via white wires.

ney” with a single flange (“top chimney”). Likewise, cables from the sides are also bundled, two bundles collecting all the 33 first induction plane cables (bundles of 18 and 15 cables) and another bundle collecting the 18 from the other plane, and lead to one of the tall chimneys at the ends of the modules (“corner chimneys”) featuring three flanges each.

At the flange, the 18 cables are connected to decoupling and biasing boards[4] (DBB, fig. 2a). In the top flanges that host cables from two different planes, each one of the nine boards on a single flange serves a cable from the second induction plane and one from the collection plane. Its purpose is twofold: to deliver the bias voltage of the wire plane, and to convey the induced current as a potential for the front end to read (removing the bias voltage via a  $10\text{ nF}$  capacitor). The board is split into two insulated halves: each can serve a different plane with a different bias voltage. For its physical characteristics, the two halves are sometimes referred to as long (or tall) and short; in the blueprints, they are called *left* (L) and *right* (R), respectively. The two sides are identical, both functionally and component-wise, but they are insulated from each other because of the different bias voltage they have to distribute. In addition to some circuitry common to all channels within a half board, each channel also has its own dedicated circuitry, independent and insulated from the other channels. The DBB offers four connectors: two are 68-pin connectors with clips, which host the cables from the wires, one side for each plane. The others, also one per board side, plug directly into the flange. In addition, the board has two



(a) Flange and test setup with minicrate.

(b) Flange connection conventions.

Figure 3: (a) Test set up with a readout minicrate mounted on a flange of a top chimney, plus test board, and (b) illustration of the external connections of a flange with the nomenclature conventionally used during the connectivity test. The triangular marking (at the bottom right of the flange) sets the orientation. The test pulse cables used to be referred to with color tags, and we'll keep that tradition for consistency (see section 3.3).

wires, also one per side, to be connected to the bias voltage distribution on the flange frame. A flange is the interface between the cold environment inside the cryostat and the outside, warm environment, where the front end readout is. It exposes nine pairs of connectors (each backed by a single DBB), and four SMA connectors (wire female, shield male) on each of two sides. Of the two sets of four, the bottom one (defined as in fig. 3b) hosts the distribution channel of bias voltage for the left side of the DBB's on the leftmost connector, and for the right side on the rightmost connector, while the central ones are unused. The set on the top of the flange hosts the four cables distributing the test pulses to the wires connected to the bottom of the anode frame, which we'll describe next.

The termination boards on the bottom of the anode frame feature a test capacitor of sorts (fig. 4), where the dielectric material is the board itself, and the electrodes are the terminating wire on one side, and a band of deposited conductor on the other, which spans all 32 wires. This band can be connected to a cable for injecting test pulses. When doing so, a signal, differentiation of the test pulse, is induced on all the wires, from which it can be read via readout or via a specific testing setup. There are four test pulse cables departing from each flange to serve the 18 cables (576 wires) the flange connects to (fig. 5). Two cables are connected to the second induction plane, while the other two are connected to the collection plane. The general rule is that one of the two cables is connected to a daisy chain of eight termination boards, while the remaining one serves a single board (fig. 6). This rule has been observed to have quite

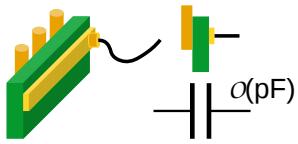


Figure 4: Illustration of the path for the test pulses from the flange to the wires.

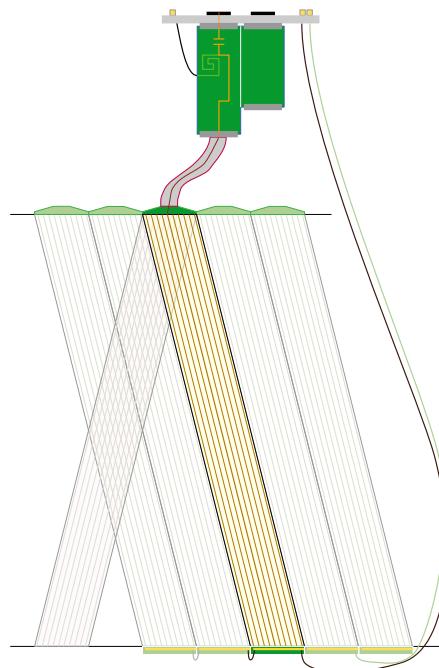


Figure 5: Illustration of the path of test pulses from the flange to the wires and back to the front-end (see section 3 for more details).



Figure 6: Distribution of the test pulse to the boards with the test capacitance.

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some exceptions (see fig. 15). The cables themselves have been color-tagged, but that tag is not visible from the outer side of the flange: instead, a convention is followed as illustrated in fig. 3b. While swapping bias voltage cables would have catastrophic effects, swapping test pulse cables has little to no effect beside adding some confusion, since the colors are purely conventional. These flanges are spread across the length of the detector, one per chimney, in four columns each one roughly above one of the anodes, with the exception of the end chimneys which will be described shortly. On top of the flange, a minicrate with VME bus will be mounted (as in fig. 3a), hosting nine readout boards into as many slots, with each one matching a single DBB.

The description above reflects the installation of wires terminated at the top of the anode frame. That includes all the full length wires from second induction and from collection planes, plus the half among the shorter ones which are terminated at top (green and blue categories in fig. 1), and it leaves out the other half of the shorter wires on those planes (red in that figure), plus all the wires from the first induction plane (yellow in that figure), all of which are terminated on the sides of the frame. To read out these wires, their cables (with different length) are brought up to the chimneys at the end of the detector (rows 1 and 20). These chimneys are special in that they stack three flanges instead of hosting just one: the top two serve the first induction plane (fig. 7), and the bottom one serves the shorter wires<sup>3</sup> and they have no connection to test pulse cables. They still have two bias voltage lines, which may be connected to any of the four SMA connectors. None of these wires is provided with a test capacitor, therefore the test pulse connectors are disconnected. The number of wires on first induction plane, 1054, requires 33 connectors with 32 channels each. Since all the flanges are standard, they have 18 connectors each. As a consequence, of the two flanges dedicated to that plane, one has three connectors not connected to any wire. Due to readout bus requirements, a “master” board always needs to be plugged into the first “slot”, and for this reason it was chosen to always have a fully connected DBB in the first slot of each flange.

Most of the components are physically keyed to prevent mounting them in any but the right way. That includes the minicrates (with different step on the top and bottom screw holes), the slots (with a shorter and a longer side), the 68 pin connectors, and also the connectors on the flange to the readout board (each split into a shorter and a longer side). The SMA connectors, instead, are not keyed nor marked in any way, and conventions need to be followed to identify each of them.

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<sup>3</sup>These wires all belong to the same plane, either second induction or collection. The shorter wires from the other plane terminate on the top and they are served by a different chimney.

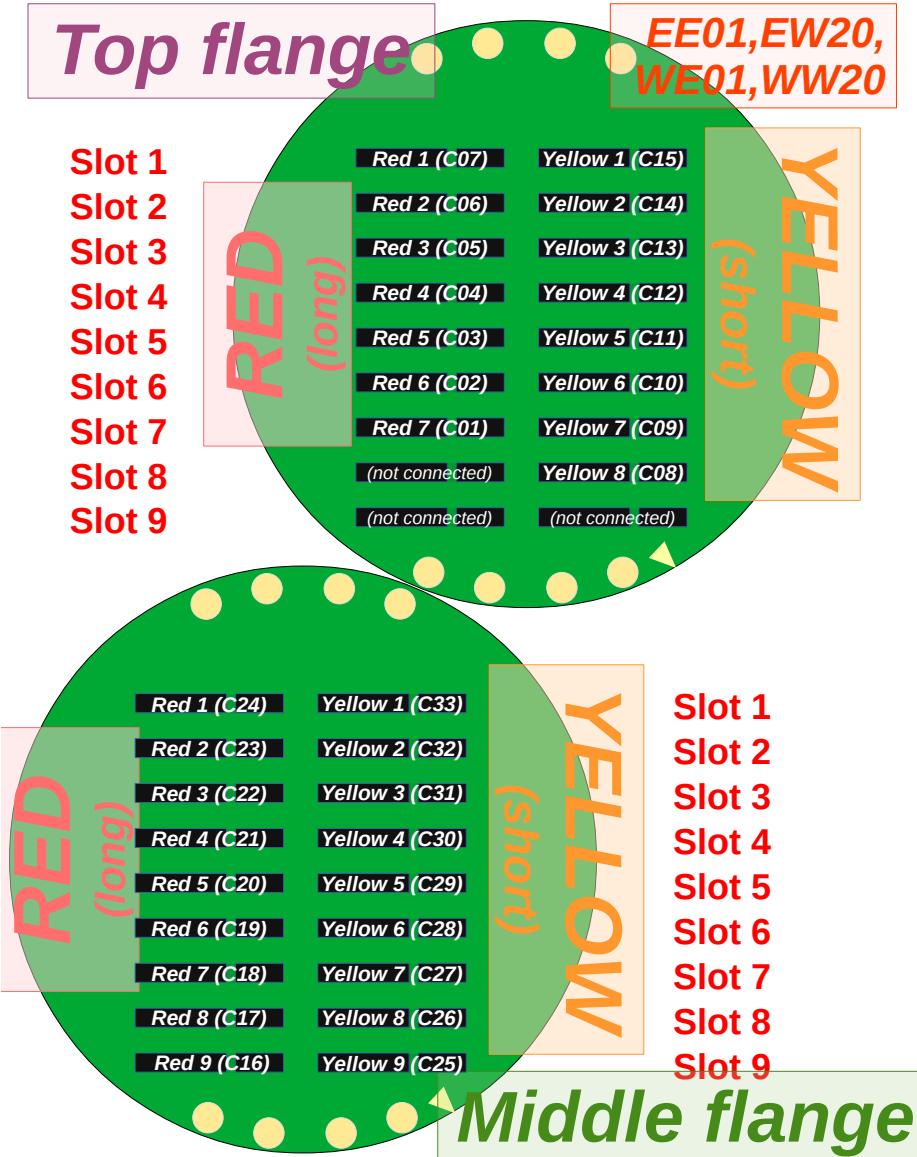


Figure 7: Illustration of the external connections of the flanges serving horizontal wires. The triangular marking sets the orientation. Due to the relative orientation, the “left” and “right” labeling becomes confusing, and we resort to an arbitrary color coding instead.

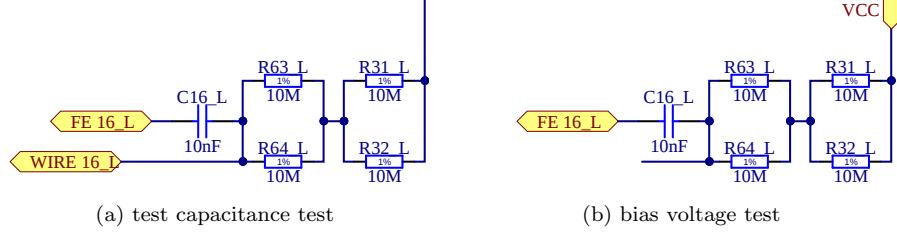


Figure 8: DBB circuitry[4] involved in (a) test capacitance pulsing and (b) bias voltage pulsing tests. The test pulse is entering through (a) “WIRE” and (b) “VCC” port, and it is in both cases read out of the front-end port “FE”.

### 3 Test methodology

This test follows broadly the same principles as the one performed in September 2018. To test the electrical continuity, a test pulse is sent, and a response is read, this time from the connectors to the readout on the flange.

We perform two tests, by probing two different paths. The first path is equivalent to the one used in September 2018 (fig. 5): a test pulse is sent through the test pulse cables at the bottom of the anode frame, where it is distributed typically to 32 or 256 wires (for the single termination card and for the eight daisy chained ones, respectively). The pulse propagates through the wires, the termination card at the top of the anode frame, the 68 pin cables, the DBB and finally though the interface connector on the flange, where it is picked up by our test apparatus. The signal path within the DBB (fig. 8a) can be appreciated from [4], where it enters through a “WIRE” port (e.g. WIRE 16\_L) and through the 10nF capacitor induces onto the front end (e.g. FE 16\_L).

The second path (fig. 9) starts by pulsing a bias voltage inlet. From there, the pulse is propagated to one side of the nine DBB (labeled “Cable AWG20” in [4]) through the common and the channel-specific circuitry (fig. 8b) before reaching the front-end readout. It should be noted that the bias voltage circuitry is designed for a constant, large voltage (300 V), while the test pulse is small (a few volt) and rapidly changing. Therefore, features observed in this test may be not significant for the regular operation of the detector.

These two paths test different paths of the circuitry (fig. 8). The first path (fig. 8a), pulsing the wire through the test capacitance, tests the full signal path, and barely grazes the DBB circuitry. The second one (fig. 8b) instead skips the wire but goes through most of the DBB components. The flanges had gone through a specific test for bias voltage distribution, that test is not sensitive enough to pin down a failure on a single channel. Also, as will be described in the result section (section 4), having a test including the wire and one excluding it allowed to pin down very precisely a faulty installation where a 68 pin cable was not correctly connected.

Both the paths we use for testing are necessarily *discontinuous*: both include a

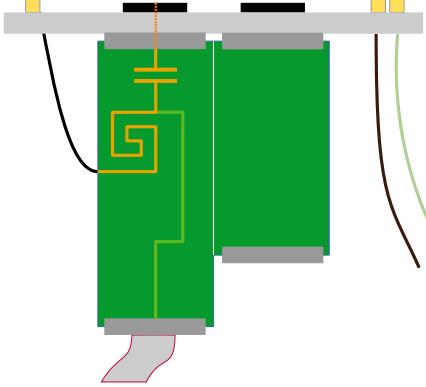


Figure 9: Illustration of the path of the test signal in the bias voltage connectivity test. The test pulse is injected through the bias voltage connector (left side), and follows a short path to the flange connector (represented in orange), bypassing the TPC wire (gray ribbon cable).

10 nF capacitor on the DBB just in front of the front end outlet, and in addition the wire path also includes an uncalibrated, picofarad-level capacitance on the bottom termination card. As a consequence, the test can't directly verify the continuity of the paths, and we rather have to interpret its response.

The bias voltage path bypasses the wire altogether, and it is therefore the same for all flanges on all chimneys, including the ones serving the first induction plane. In addition, for a few flanges the test on the bias voltage path was performed also before the flange being mounted on the detector. That configuration is effectively almost identical to the one on the detector, with the exception that the wire is not connected at all and, for example, does not contribute to pick up noise.

To test the first induction plane wires, a modified test was devised: because those wires lack a test capacitance, signal is induced on them from the wires *on one of the other planes*. This results in the path shown in fig. 10. The pulse is injected into a chimney on the same column, chosen to maximize the overlap of the pulsed wires with the ones to be tested. To have the large signal possible, the pulse cables are chosen which are connected to eight daisy-chained test capacitance cards. This path is effectively equivalent to adding a capacitance in series to the test capacitance, this one made of air dielectric and wired arms. As a rough idea of the configuration, each first induction plane wire can be considered an arm 3 mm wide, and as long as  $\approx 90$  cm (that is, the space covered by the 256 pulsed wires:  $8 \times 11$  mm of each card), far 3 mm from the other arm. The chimney chosen to be pulsed was always 5 chimneys away from the end, that is chimneys 06 and 15, close to the middle of the first induction plane. No difference was observed in the signal induced by pulsing one plane or

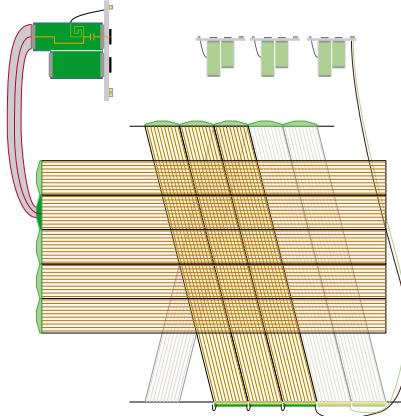


Figure 10: Illustration of the path of the test signal for the first induction plane wires.

the other of that chimney, despite one of them being twice as far as the other. It should be noted that in this configuration all the 1056 wires of the half plane are pulsed at the same time. This increases the amount of cross talk between the 68-wire cables.

No connectivity test was performed on the  $\approx 4000$  short wires shown in fig. 1 as red category.

### 3.1 Test setup

The test pulse is generated with a “test box” designed by Mark Convery (fig. 11), which includes a pulse generator and also provides amplification of the response to the pulse. After amplification, the responses are digitized by a four-channel oscilloscope ([Tektronix TDS 3054C](#)) and sent to a program running on a laptop, which can record them as waveforms (fig. 12). The path followed by the test pulse is illustrated in the following paragraphs.

The test boxes are the same used in the testing of September 2018, including the dead channels (channel 2 in one of the boxes, channel 18 in the other), with some upgrade. The boxes are powered by three 1.5 V AA batteries, and they now include a voltage regulator that stabilizes the output at about 3.3 V. The test pulses are emitted at a rate of 100 Hz, each one a positive square wave of 3.3 V with a duration of about 100  $\mu$ s. Each test box includes two outlets for the same pulse. One is sent directly to the oscilloscope to work as a trigger. The other is sent to the detector via a lemo to SMA cable: it will be plugged either to the test pulse cable or to the bias voltage distribution, to implement one of the two test paths described in section 3. The response to these pulses is read from the front end connectors on the flange. The standard setup includes the installation of an empty readout minicrate, its only purpose to provide me-



Figure 11: The older one of the two test boxes used for generating the test pulse and selecting and amplifying the response to it.

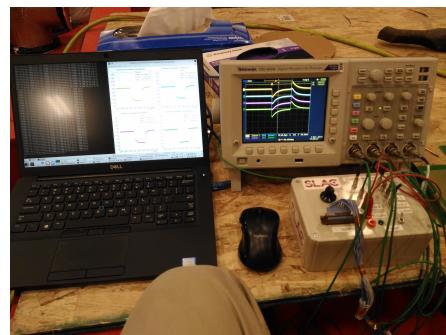


Figure 12: Connectivity test readout setup.

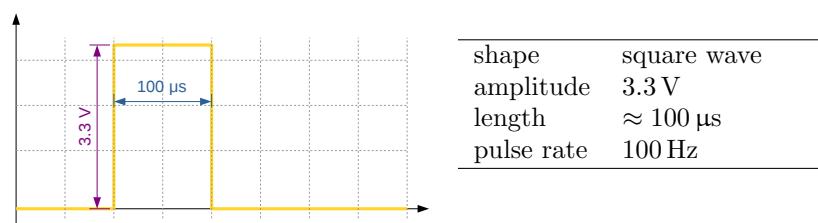


Figure 13: Illustration and specifications of the pulse used in connectivity tests.

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chanical support, and in it a board shaped as a readout board, which is in effect just a passive adapter from the front end connector to a 68 pin cable: each of these “fake” readout boards includes two such adapters, converting at once both the left and the right side connectors, and allowing for two different 68 pin cables. At a time, the correct one of the two cables (for example, the left one when the test is currently pulsing the left bias voltage distribution path) is plugged back into the test box, conveying signals from the 32 channels from the DBB side it is connected to. The test box contains a eight position switch that selects four contiguous channels among the 32 from the cable. Signals from the four channels are amplified and offered each on an independent outlet. These four channels are sent to the oscilloscope for digitization and visual inspection. The oscilloscope can be driven by commands sent via Ethernet from a laptop, where a simple data acquisition program drives the readout and recording of the digitized waveforms. One of the test boxes also offers “direct”, non-amplified versions of the signal.

Noise and grounding have been an issue in the previous session of tests. Depending on the grounding of the shield wires, they do actually act as shield, or they rather act as antennas picking up noise. The upgraded test boxes allow the option of connecting all the shield wires to the ground (which is effectively the oscilloscope ground). This option was regularly used in the December 2018 testing session. It results into reduced noise and also in reduced signal response, allegedly because of reduction of cross talk from other cables. In addition, we grounded the oscilloscope chassis to the detector.

### 3.2 Data acquisition

The Tektronix TDS 3054C oscilloscope can digitize and send out the input signals, providing  $10^4$  samples per channel, each sample with 8-bit precision<sup>4</sup>. The custom data acquisition code reads a sequence of waveforms from each oscilloscope channel. Each waveform is stored in its own comma-separated value file (CSV), with a resolution of  $0.1\ \mu\text{s}$  for the time and  $10\ \text{mV}$  for the signal amplitude. Therefore the waveform samples span 1 millisecond, and they are at baseline in roughly 60 – 80% of the time.

The testing procedure included cycling across all 8 switch positions of the test box for each connection, and recording 10 waveforms for each of the 4 channels monitored in the selected position. For each switch position, therefore, 40 waveforms are recorded. The total data size as stored in the final form is about 500 MiB per chimney.

### 3.3 Labelling

We use the following labeling conventions:

**chimneys** are laid out in four “columns” and twenty “rows”:

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<sup>4</sup> The oscilloscope alternatively allows for 9 bit ADC conversion, at the cost of doubling the data size

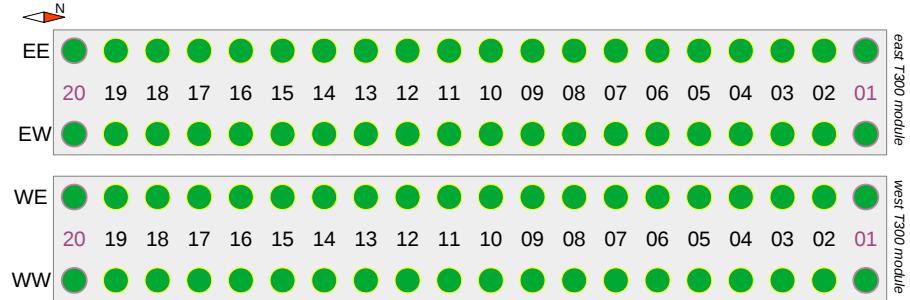


Figure 14: Disposition and labeling of the chimneys. End chimneys (01 and 20) are circled in magenta.

- columns are labeled geographically, with the position of the module first (East or West) and then the side within the module (also East or West)
- rows are numbered 01 (the most northern one) to 20 (the most southern one, the side neutrino beams come from)

Chimneys 01 and 20 are taller and host three flanges, and they have been called “end”, “corner”, or “tall” chimneys;

**flanges** are rarely referred to directly; we’ll use the letter F followed by the flange number, that effectively went from 1 to 100 (there are 96 flanges mounted on the detector, but spares were produced as well)

**cables** (68-wire cables) are numbered from 01 to 18, except for the ones serving the first induction plane, where the range extends to 33; the cables have a letter tag too, which can be V (east side of each module), S (west side of each module), or A/B/... in the end chimneys; since this cable tag does not add any information, occasional inconsistencies are nonconsequential

**channels** and wires are usually identified by a number between 1 and 32 within each cable, with channel 1 being the one marked by the red wire on the cable itself. In connectivity test context, a 4-channel oscilloscope is used for digitization, and a channel  $c$  might be designed by test box switch position ( $p$ ) and oscilloscope channel ( $CH$ ) instead: the numerical rule is  $c = 1 + 4(p - 1) + (CH - 1)$

**position** of the switch in the test box spans the range 1–8, where position 1 covers channels 1 to 4, position 2 covers channels 5 to 8, up to position 8 covering channels 29 to 32

**oscilloscope channel** is one of the four channels of the oscilloscope; we use to color-code them as yellow (CH1), cyan (CH2), green (CH3) and magenta (CH4), after the color the oscilloscope associates them to. In general it is

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recommended that the channel as defined above is used instead, which is not bound to this specific test.

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## 4 Test results

This section summarizes the results of the connectivity tests performed in December 2018, February 2019 and March 2019 (see appendix A for details on the different sessions).

### 4.1 Test pulse responses

### 4.2 Observed issues (and mitigations)

### 4.3 Status of the channels

The mitigation or resolution of issues was attempted immediately as they were discovered, and the status was changing very often. Reports have been posted daily into ICARUS electronic logbook[5] (see appendix A); here we do not attempt to relate the evolution of the status, but rather describe the final status as we knew it following the analysis and discussion of the information we collected. The following information is also available in [2].

In total, we have identified 29 issues involving overall **54** channels. Issues can be grouped in some categories:

- non-responsive channels (26 channels)
- front-end signal connection failure (4 channels)
- broken wires (9 channels)
- larger response (5 channels)
- extremely larger response (10 channels)

It should be clear that the category names are just a possible interpretation of the issue deduced from the observations. In other words, for example there is no conclusive evidence that the wire of any channel in the category “broken wires” is actually broken.

#### 4.3.1 Non-responsive channels

The channels in this category show no response to the test capacitance pulse, and a somehow reduced response to bias voltage pulse.

Three 68-wire cables are known to have been physically damaged. As the final action was taken on March 2019, there was no more access to the full extent of the cables. Since the damage on the cables could not be directly observed, the decision was made to actively shear in a controlled way the cable wires corresponding to the channels already damaged. The new cut was performed close to the connector of the cable to the DBB, in a volume expected to be in gaseous argon when the detector is operational. It is understood that these wires won’t be biased, which will affect the electric field uniformity. The wires on EW20 B01 and WE20 D33 are believed to be at the border of the TPC, though,

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hence outside the fiducial volume.

The 26 affected channels are:

- EW20 B01 channels 1–15, now sheared
- WE20 D33 channels 22–28, now sheared
- WW20 B15 channel 1, now sheared
- EW01 A15 channel 4
- EW20 B33 channel 14
- WE01 C02 channel 1

#### 4.3.2 Front-end signal connection failure

Response to neither test capacitance nor bias voltage pulses are observed. These observations can be explained by a failure in the connection between DBB and front-end. In such cases, it is not excluded that the circuitry upstream of the connector is operational, in which case the wire would still be biased and responding, although we will still not see its response. It was confirmed for some of the channels that the pin on the external front-end connector on the flange was damaged.

The 4 affected channels are:

- EE15 V08 channel 20
- WW08 S11 channel 29
- EW01 A27 channel 13
- WW01 A33 channel 30

#### 4.3.3 Broken wires

These channels present a regular response to bias voltage pulses, but a very reduced response to test capacitance pulses, possibly caused by only cross talk on the cables.

The 9 affected channels are:

- EE15 V08 channel 20
- WW08 S11 channel 29
- EW01 A27 channel 13
- WW01 A33 channel 30
- EW03 S13 channel 29
- EW08 S11 channel 16

- 
- EW11 S10 channel 6
  - WE11 V16 channel 6
  - WE16 V12 channel 6
  - WE17 V01 channel 18
  - WE19 V04 channel 7
  - EW01 A17 channels 19 and 20
  - EW01 A21 channel 19

#### 4.3.4 Larger response

Some channels present a response to test capacitance pulses that is noticeably larger than the average of the adjacent channels, up to twice as large. The response to bias voltage pulsing is also moderately larger.

The 5 affected channels are:

- EE05 V01 channel 18
- EE04 V18 channel 14
- EE06 V17 channel 7
- EE09 V02 channel 27
- WW01 A18 channel 24

#### 4.3.5 Extremely larger response

Some channels show a response to bias voltage pulses that saturates the test box amplifiers (1.6 V), and the response to test capacitance pulses is also many times larger than average.

The 9 affected channels are:

- EE02 V01 channel 8 and 9
- EW19 S18 channel 24 and 25
- WE02 V01 channel 8 and 25
- WW19 S18 channel 8 and 25
- WW02 S09 channel 20

The first four pairs present a clear symmetry, and it has been conjectured that it is an effect of the reinforcement plates replacing the short wires at some of the corners of the anode frame.

The anomalous response observed on EE02 V01 channel 12 might also be an effect caused or amplified by the test box because of the presence of the other anomalous channel 9.

---

#### 4.4 Map of pulse cable connections

The connection of test pulse cables to the test capacitance cards follows a pattern dictated by the geometry of the detector. Nevertheless, numerous cases have been observed where the connections did not follow the expected pattern. In February 2019 the “definitive” mapping of pulse cable to 68-wire cable was compiled. Despite it being definitive, there is more than a bit of arbitrary decision involved, especially in the cases where pulsing different pulse cables seem to yield similar responses. Also note that 9 cables of the chimneys on rows 02 and 19, and 8 of the chimneys 03 and 18 are actually *not* connected to a test capacitance, being in the “blue” category (see fig. 1), and the reported cable is the one that was pulsed for the test, with the understanding that it is *one of the cables* which yield the largest response.

The map is reported as table in fig. 15.

#### 4.5 Collected data

Data was collected systematically, in December 2018 for all chimneys except for the four chimneys that were not yet installed: WE02, WE03, WE04 and WW02. Further acquisition happened on February 2019.

After data acquisition, some flanges were replaced together with their DBB’s. That is the case for EE08, WE02 and WW02, the data of which does not reflect the installed flanges any more. In addition, WE03 and WE05 had one DBB replaced after data acquisition (DBB #5 serving V05 and V14, and DBB #1 serving V01 and V10, respectively).

The data is currently stored in ICARUS data area at  
`/icarus/data/commissioning/connectivityTest/201812/chimney`  
and archived in ICARUS dCache area at  
`/pnfs/icarus/persistent/commissioning/connectivityTest/201812/archive`.  
The data obsoleted by the changes reported above is still kept in the old sub-directory.

| chimney | chimney column EE |  |  |       |  |  | chimney column EW |  |  |       |  |  | chimney column WW |  |  |       |  |  |
|---------|-------------------|--|--|-------|--|--|-------------------|--|--|-------|--|--|-------------------|--|--|-------|--|--|
|         | left              |  |  | right |  |  | left              |  |  | right |  |  | left              |  |  | right |  |  |
| 1       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 2       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 3       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 4       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 5       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 6       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 7       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 8       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 9       |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 10      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 11      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 12      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 13      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 14      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 15      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 16      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 17      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 18      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 19      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |
| 20      |                   |  |  |       |  |  | 1                 |  |  | 1     |  |  | 1                 |  |  | 1     |  |  |

Figure 15: Pulse cable color (and number: see fig. 3b) used to test each cable. Each flange has six entries in the table, three for the left side and three for the right one. The first entry shows the pulse cable used to pulse the first 68-wire cable (V1 or S1), the second entry for the second to the eighth (V2–V8 or S2–S8), the third for last one (V9 or S9). The next three entries pertain cables V10 or S10, then V11–V17 or S11–S17, and finally V18 or S18.

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## A Operative details

The tests subject of this report happened in three distinct sessions:

**December 2018** the first extensive test including the DBB and flanges took place. All mounted chimneys were eventually covered in three weeks, and the data from the test was recorded. This excludes WE02, WE03, WE04 and WW02, which at that time were not physically available yet.

**February 2019** another session was scheduled and took place in February 2019, with the goal of performing the test in the final chimney configuration; it was split in two subsessions because for half of the chimneys optical flanges were going to be installed, and that installation could accidentally impact the connections of the other components in the chimney. All the chimneys were again tested, but the only recorded data was for the few chimneys that were missing it from December 2018.

**March 2019** saw the last session take place, after an extensive intervention on all flanges to deposit glue on the clamps holding the 68-wire cables.

### A.1 December 2018 test

### A.2 February 2019 test

### A.3 March 2019 test

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## B Test software

### B.1 Data sets

The original acquisition software grants the operator some options that affect the name of the waveform files. An acquisition-driving code was developed that reduces those options and enforces a file name pattern:

`waveform_CH<channel>_CHIMNEY_<chimney>_CONN_<cable>_POS_<position>_<index>.csv`

where the elements, defined in section 3.3, are:

`<channel>` is the *oscilloscope channel* the waveform is read from, which ranges from 1 to 4

`<chimney>` is in the form `<module><side><row>`, WE07

`<cable>` is the label of the cable plugged in the test box, e.g. V05

`<position>` is the setting of the test box switch

`<index>` is a waveform counter; following Sergi's convention, this is a sequential number unique within waveforms on the same connector and oscilloscope channel. Assuming that 10 waveforms are taken per channel, position `POS_1` will have indices from 1 to 10, `POS_2` from 11 to 20, and so on, up to `POS_8` with indices 71 to 80.

320 waveform files are expected per cable (10 waveforms for each of 32 channels, split in 4 oscilloscope channels and 8 test box switch positions), and 5760 per chimney. These files are stored in separate directories, one per chimney. The name of the directory follows the same convention as above, that is `CHIMNEY_<chimney>` (e.g. `CHIMNEY_WE07`).

The whole data set taken in the test session of August 2018 is currently stored in Fermilab dCache at the path:

`/pnfs/icarus/persistent/commissioning/connectivity/201808`

### B.2 Data format

Each waveform is stored in its own comma-separated value file (CSV). The file name follows the pattern described above. Each line in the file corresponding to a sample, totaling 10000 lines for each waveform. Each sample is described by values in floating point text representation, with scientific notation: time in seconds, and signal level in volt. For example:

```
0.0,2.08  
1e-07,2.08  
2e-07,2.12  
[...]
```

No metadata is saved in the file. This data format can be easily read directly by ROOT `TGraph`.

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### B.3 Streamlined interactive data acquisition

The original code by Sergi Castells required the operator to change parameters on the command line on each acquisition, plus an additional step at the end of the test each connector, that is to reset a counter stored in a text file.

After a few interactions with this approach, we wrote additional software (*test driver*) automating most of the steps required from the operator. This enforced a specific procedure both for testing and for software setup.

The procedure comprises testing one chimney at a time, and proceeding from connection 18 (V18 or S18) down to 1 (V01 or S01), and on each connector test the channel switching the test box to the position from 1 to 8 in strict sequence. The whole sequence must be strictly followed.

More details about the software used for data acquisition and its setup can be found in ??.

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## C Glossary and abbreviations

**DBB** *Decoupling and Biasing Board*,

**T300** each of the two modules of the ICARUS detector, including its own cryostat, two drift volumes (TPC), for a reference argon mass of 300 tonnes

**TPC** (*Time Projection Chamber*) is defined as a unit including a single uniform drift volume, a cathode and a (composite) anode. In ICARUS, each cathode is shared by two TPCs. This is also the definition of TPC used in the official simulation and reconstruction software (LArSoft)

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## References

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- [2] M. Convery, G. Petrillo, and Y.-T. Tsai. Icarus connectivity test: list of identified issues. *SBN DocDB 11703*, March 2019. URL <https://sbn-docdbcert.fnal.gov/cgi-bin/cert>ShowDocument?docid=11703>.
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- [4] DBB. Icarus decoupling and biasing board (dbb 2018) schematics. *SBN DocDB 10693*. URL <https://sbn-docdbcert.fnal.gov/cgi-bin/cert>ShowDocument?docid=10693>.
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