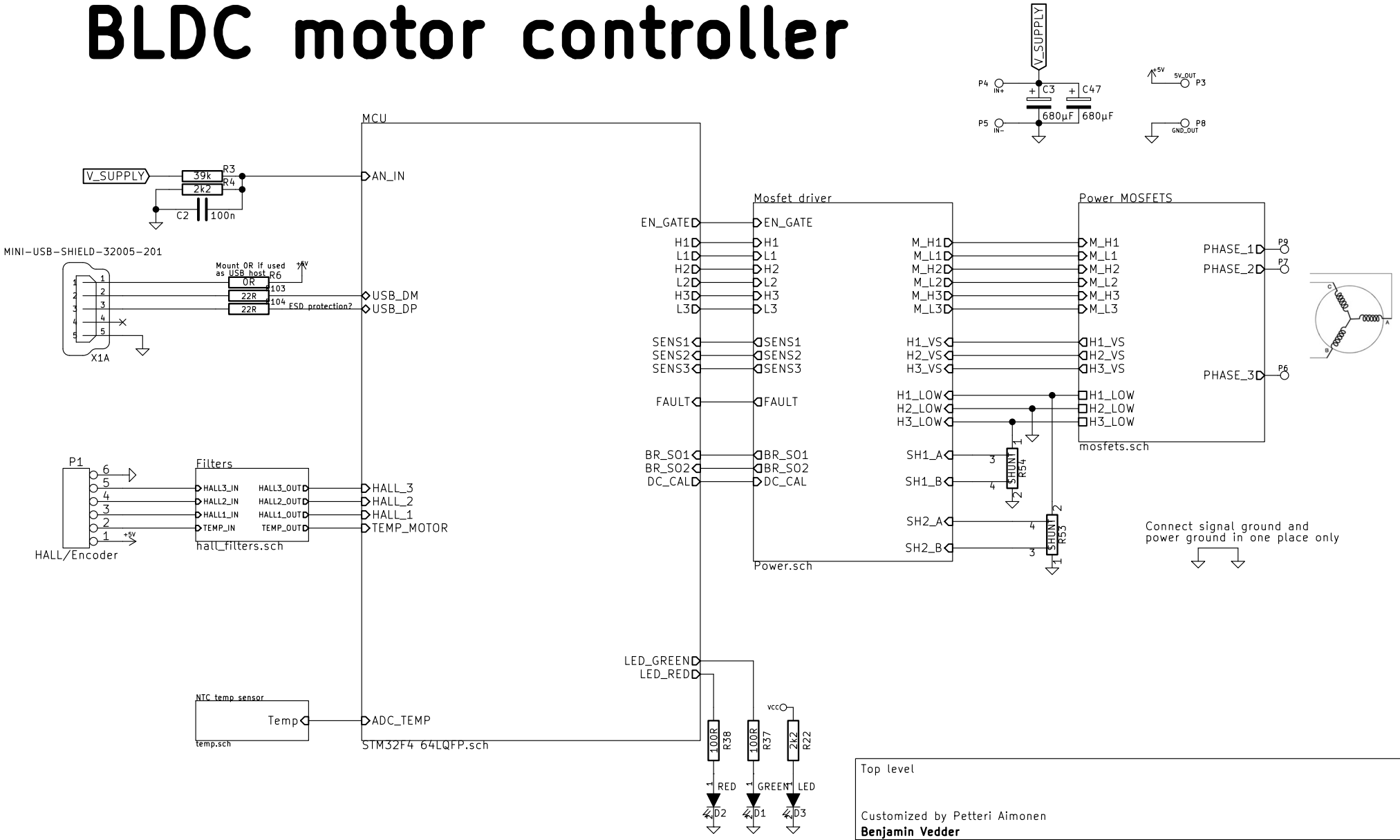
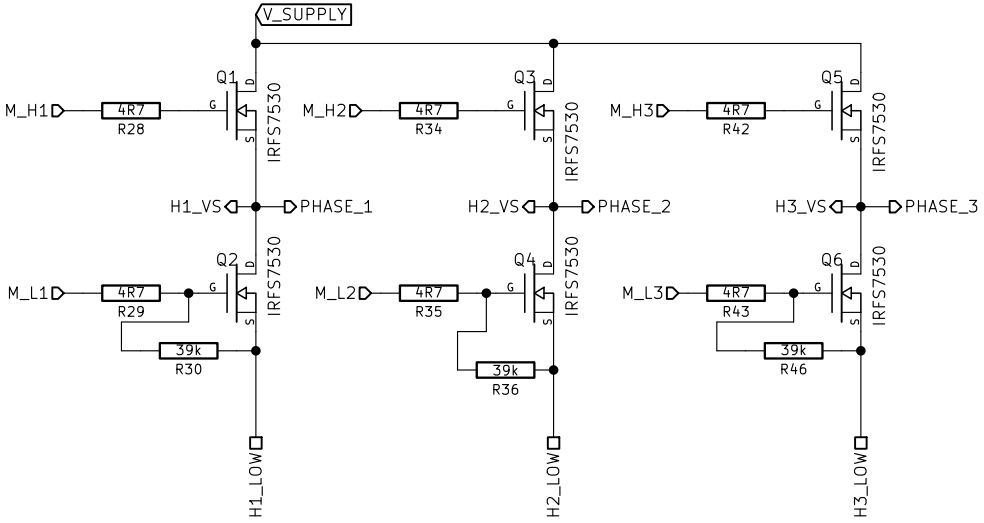
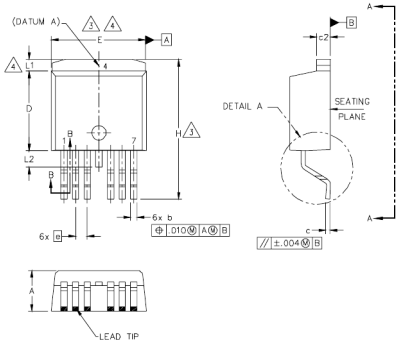
BLDC motor controller



Top level		
Customized by Petteri Aimonen **Benjamin Vedder**		
Sheet: / File: BLDC_4.sch		
Title: BLDC Driver 4.10		
Size: A4	Date: 2015-10-25	**Rev: 4.10-jpa**
KiCad E.D.A. kicad 4.0.1-3.201512221401+619838ubuntu15.10.1-stable	Id: 1/6	





Customized by Petteri Aimonen

Benjamin Vedder

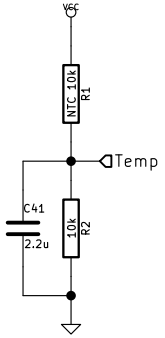
Sheet: /Power MOSFETS/

File: mosfets.sch

Title: BLDC Driver 4.10

Size: A4	Date: 2015-10-25	**Rev: 4.10-jpa**

KiCad E.D.A. kicad 4.0.1-3.201512221401+619838ubuntu15.10.1-stableId: 2/6



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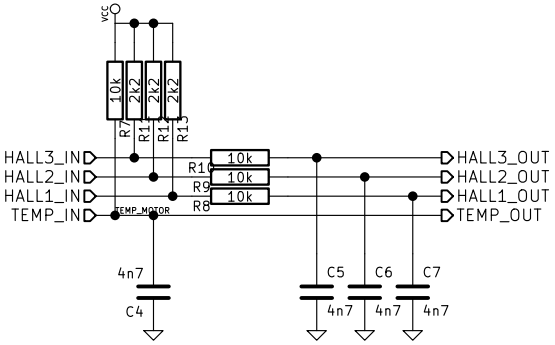
Benjamin Vedder

Sheet: /NTC temp sensor/
File: temp.sch

Title: BLDC Driver 4.10

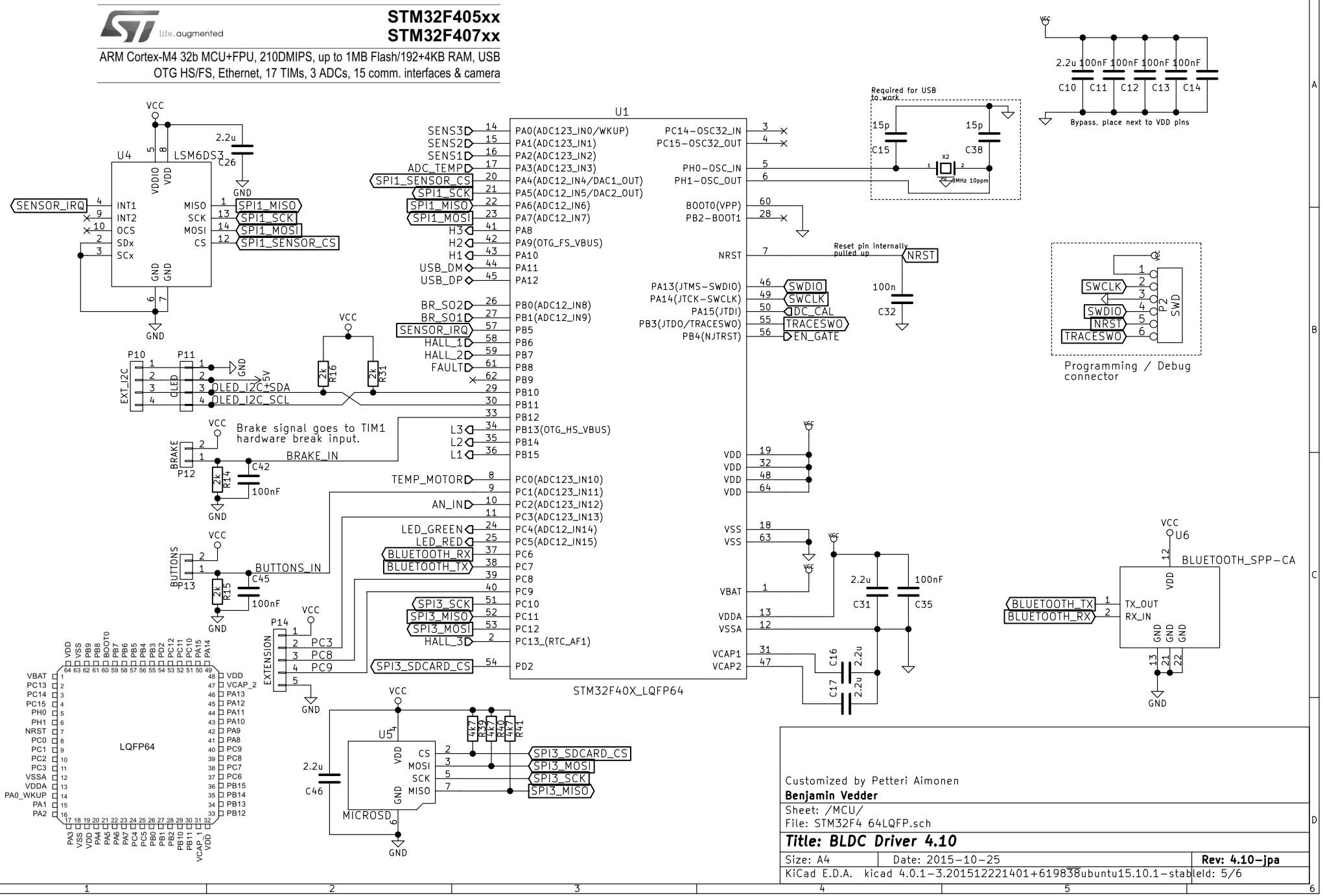
Size: A4	Date: 2015-10-25	**Rev: 4.10-jpa**
KiCad E.D.A. kicad 4.0.1-3.201512221401+619838ubuntu15.10.1-stable	Id: 3/6	



Customized by Petteri Aimonen
Benjamin Vedder
Sheet: /Filters/
File: hall_filters.sch

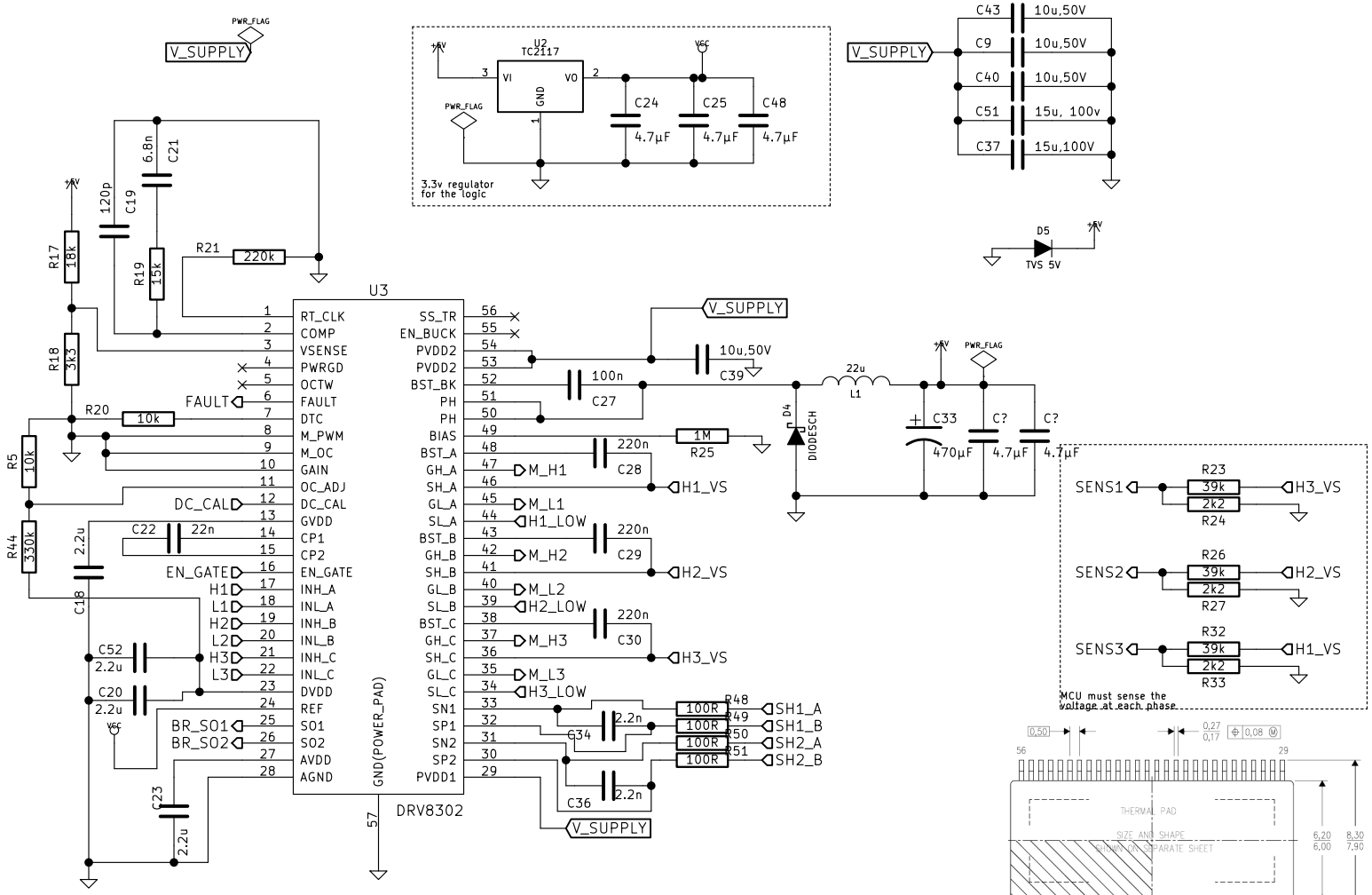
Title: BLDC Driver 4.10

Size: A4	Date: 2015-10-25	**Rev: 4.10-jpa**
KiCad E.D.A. kicad 4.0.1-3.201512221401+619838ubuntu15.10.1-stable	Id: 4/6	


STM32F405xx
STM32F407xx
ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera
U1
STM32F40X_LQFP64
U4
LSM6DS3
U5
MICROSD
U6
BLUETOOTH_SPP-CA
P2
SWD
Programming / Debug connector
Required for USB to work
Reset pin internally pulled up
Brake signal goes to TIM1 hardware break input.
Bypass, place next to VDD pins
LQFP64
Customized by Petteri Aimonen
Benjamin Vedder
Sheet: /MCU/
File: STM32F4 64LQFP.sch
Title: BLDC Driver 4.10
Size: A4
Date: 2015-10-25
Rev: 4.10-jpa
KiCad E.D.A. kicad 4.0.1-3.201512221401+619838ubuntu15.10.1-stableId: 5/6

FEATURES

- Operating Supply Voltage 8V–60V
- 2.3A Sink and 1.7A Source Gate Drive Current Capability
- Integrated Dual Shunt Current Amplifiers With Adjustable Gain and Offset
- Integrated Buck Converter to Support up to 1.5A External Load
- Independent Control of 3 or 6 PWM Inputs
- Bootstrap Gate Driver With 100% Duty Cycle Support
- Programmable Dead Time to Protect External FETs from Shoot Through
- Programmable Overcurrent Protection of External MOSFETs
- Thermally Enhanced 56-Pin TSSOP Pad Down DCA Package



RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNITS
PVDD1	DC supply voltage PVDD1 for normal operation	Relative to PGND	8		60	V
PVDD2	DC supply voltage PVDD2 for buck converter		3.5		60	V
C_{AVDD}	External capacitance on AVDD pin (ceramic cap) 20% tolerance			1		µF
C_{DVDD}	External capacitance on DVDD pin (ceramic cap) 20% tolerance			1		µF
C_{GVDD}	External capacitance on GVDD pin (ceramic cap) 20% tolerance			2.2		µF
C_{CP}	Flying cap on charge pump pins (between CP1 and CP2) (ceramic cap) 20% tolerance			22		nF
C_{BST}	Bootstrap cap (ceramic cap)			100		nF
I_{DIN_EN}	Input current of digital pins when EN_GATE is high				100	µA
I_{DIN_DIS}	Input current of digital pins when EN_GATE is low				1	µA
C_{DIN}	Maximum capacitance on digital input pin				10	pF
C_{O_OPA}	Maximum output capacitance on outputs of shunt amplifier				20	pF
R_{DTC}	Dead time control resistor range. Time range is 50ns (-GND) to 500ns (150kΩ) with a linear approximation.		0		150	kΩ
I_{FAULT}	$\overline{FAULT}$ pin sink current. Open-drain	V = 0.4 V			2	mA
I_{OCTW}	$\overline{OCTW}$ pin sink current. Open-drain	V = 0.4 V			2	mA
V_{REF}	External voltage reference voltage for current shunt amplifiers		2		6	V
f_{gate}	Operating switching frequency of gate driver	Qg(TOT) = 25 nC or total 30 mA gate drive average current			200	kHz
T_A	Ambient temperature		–40		125	°C

Customized by Petteri Aimonen
Benjamin Vedder
Sheet: /Mosfet driver/
File: Power.sch

Title: BLDC Driver 4.10

Size: A4 | Date: 2015-10-25 | **Rev: 4.10-jpa**
KiCad E.D.A. kicad 4.0.1-3.201512221401+619838ubuntu15.10.1-stableId: 6/6