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Packaging CPUs or ASICs for Shipment

Document Number and Revision: 912-1696 Rev 08

Overview

This document describes the packaging instructions for CPUs or application specific integrated units (ASICs) shipped by suppliers to suppliers or to Oracle, by Oracle to suppliers, and between Oracle sites.

Audience

This document is for all Oracle suppliers and Oracle sites responsible for packaging CPUs or ASICs for shipment.

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1. Packaging CPUs or ASICs

1.1 Materials Required

- Appropriate CPU or ASIC trays
- ESD corrugated boards
- Plastic strapping or ESD Velcro straps
- ESD bags with moisture barrier properties
- ESD labels
- ESD bubble wrap
- CPU or ASIC box (original, preferred with anti-static foam inserts)
- Humidity indicator card (HIC) for ball grid array (BGA) components
- Desiccant for BGA components
- Moisture-sensitive identification label (MSID) for BGA components
- Moisture-sensitive caution (MSC) label for BGA components
- Molded anti-static foam

1.2 Equipment Required

- Pencil vacuum
- Strapping machine
- Vacuum sealer for BGA components

1.3 CPU or ASIC Packaging by CPU or ASIC Type

Refer to *Table 1-1, CPU or ASIC Packaging Counts by CPU or ASIC Name*, on page 3, for a list of correct trays to be used and the maximum number of CPUs or ASICs allowed for each tray by CPU or ASIC name.

NOTE 1: To prevent damage to CPUs, do not use land grid array (LGA) or BGA trays for pin grid array (PGA) devices, or PGA trays for LGA/BGA devices.

Table 1-1 CPU or ASIC Packaging Counts by CPU or ASIC Name

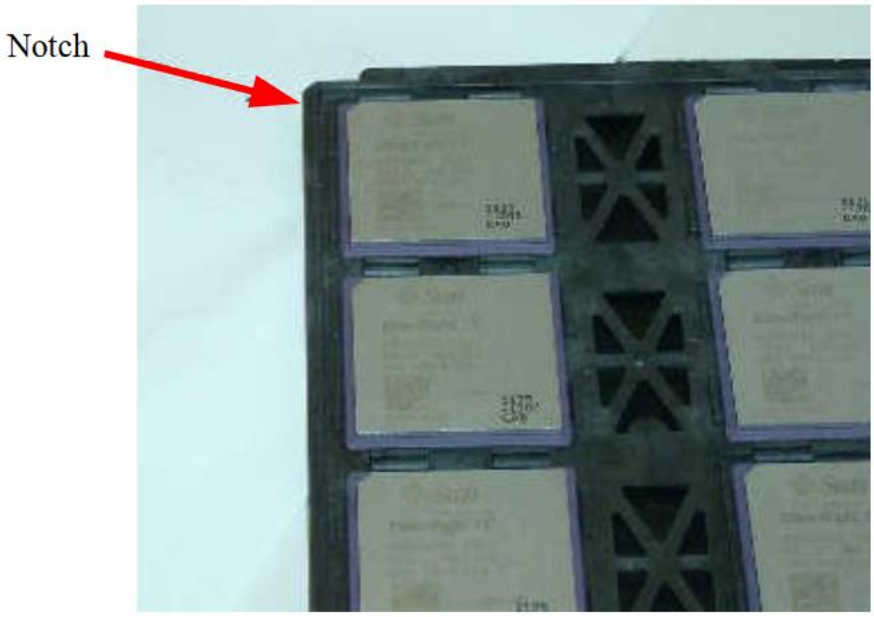
CPU or ASIC Name	CPU or ASIC Type	Tray Matrix Orientation	Maximum CPUs or ASICs for a Tray	Maximum Trays for a CPU or ASIC Box	Maximum CPUs or ASICs for a CPU or ASIC Box	Supplier Tray Part Number	Active?
Yosemite Falls	BGA	2 x 5	10	5 Full + 1 Cover	50	JT1515101-06 Rev A	Yes
T5	BGA	2 x 5	10	5 Full + 1 Cover	50	JT1515101-06 Rev A	Yes
M6	BGA	2 x 5	10	5 Full + 1 Cover	50	JT1515101-06 Rev A	Yes
M7	BGA	2 x 4	8	5 Full + 1 Cover	40	JT1616101-06 Rev A	Yes
Sonoma	BGA	2 x 6	12	5 Full + 1 Cover	60	JT1554501-06 Rev A	Yes
Yuba	BGA	2 x 10	20	5 Full + 1 Cover	100	JT1402501-06 Rev B	Yes
Phantom	PGA	2 x 5	10	5 Full + 1 Cover	50	RHM-768B	No
Cheetah++	LGA	2 x 6	12	5 Full + 1 Cover	60	eN BG4545 1.9 0206 6	No
Jaguar	LGA	2 x 6	12	5 Full + 1 Cover	60	eN BG4545 1.9 0206 6	No
Panther	LGA	2 x 6	12	5 Full + 1 Cover	60	eK BG4545 2.0 0206 6	No
Jalapeno	PGA	2 x 6	12	5 Full + 1 Cover	60	eK BG4545 2.0 0206 6	No
Niagara	LGA	2 x 5	10	5 Full + 1 Cover	50	eK LGA5151 2.2 0205 6R.1	No
Niagara2	BGA	2 x 6	12	5 Full + 1 Cover	60	eK BG4545 2.0 0206 6	No
Victoria Falls	BGA	2 x 6	12	5 Full + 1 Cover	60	eK BG4545 2.0 0206 6	No
Rainbow Falls	BGA	2 x 5	10	5 Full + 1 Cover	50	eK PGA5151 2.5 0205 6	No
Zambezi	BGA	3 x 9	27	5 Full + 1 Cover	135	eNH BG3131 2.2 0309 6	No

1.4 Procedure

NOTE 2: All personnel handling these parts must comply with Oracle ESD standards and practices. Refer to ANSI/ESD S20.20-2014, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).

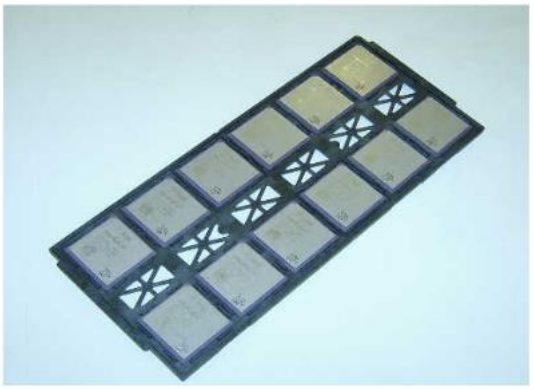
1. Using a pencil vacuum, place each CPU or ASIC into the appropriate CPU or ASIC tray. Ensure that each CPU or ASIC is correctly oriented with the top left corner (notch) of the CPU or ASIC pointing towards the notched-edge of the tray. Refer to *Figure 1-1, CPU or ASIC Orientation*, on page 4.Figure 1-1 CPU or ASIC Orientation

Figure 1-1 CPU or ASIC Orientation



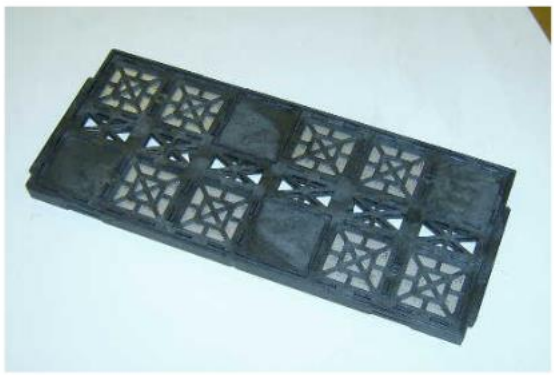
2. Place one CPU or ASIC for each slot. No stacking of CPUs or ASICs is allowed. When the tray is filled, place another tray on top while maintaining orientation with the bottom tray. Refer to ***Error! Reference source not found.***, ***Error! Reference source not found.***, **Error! Reference source not found.**. For the maximum number of CPUs or ASICs allowed by CPU or ASIC name for each tray, refer to *Table 1-1, CPU or ASIC Packaging Counts by CPU or ASIC Name*, on page 3.

Figure 1-2 CPU or ASIC Tray Orientation



3. The maximum for each box is five full trays plus an empty tray. Always place an empty tray on top of the last tray containing parts. Refer to *Figure 1-3,* Empty Tray Placement*, below*.

Figure 1-3 Empty Tray Placement



4. Place ESD corrugated boards on the top and bottom of the stack of trays. Refer to
5.
6.

7. Figure 1-4, ESD Corrugated Board Placement*, below*.

Figure 1-4 ESD Corrugated Board Placement

8. Place two straps around the boards, approximately two inches from each end. Refer to *Figure 1-5, Strap Placement*, below.

NOTE 3: When using ESD Velcro straps, place the straps in the same location as the band straps. Ensure that the ESD Velcro straps fit snugly. Secure the trays firmly.

Figure 1-5 Strap Placement

9. *For PGA and LGA components, insert each tray into an ESD bag and tape the bag closed with ESD labels. Refer to*
10.
11.

12. Figure 1-6, Tray Sealed with ESD Labels, *below.*

Figure 1-6 Tray Sealed with ESD Labels

NOTE 4: For all BGA components, refer to the IPC/JEDEC specification, *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*, J-STD-033B.1.

13. For BGA components with attached solder balls, the components, trays, corrugated boards, and straps must be dry baked according to the *IPC/JEDEC specification, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*, J-STD-033B.1 (http://www.jedec.org).

14. For BGA components that are dry baked, include a HIC and a desiccant in the ESD bag. These ESD bags must be vacuum sealed and labeled with a MSID label and a MSC label. Refer to *Figure 1-7, Tray Sealed with MSID and MSC Labels*, below.

Figure 1-7 Tray Sealed with MSID and MSC Labels

15. Place the tray in a 5" x 6.5" x 14" box. Ensure that the molded anti-static foam for the bottom and four side walls insert is in place. Refer to
16. *Figure* 1-8, *Tray Placement in a Box with Bottom and Four Side Walls Insert*, on page 8.

Figure 1-8 Tray Placement in a Box with Bottom and Four Side Walls Insert

17. If the stacked trays are not full to the top, place an appropriate amount of ESD bubble wrap into the box to ensure that the trays are secure and snug before placing the molded anti-static foam on top. Refer to *Figure 1-9*, *Bubble Wrap Placement in a Box*, below and
18.
19.

20. Figure 1-10, *Placing the Molded Anti-Static Foam on Top*, on page 9.

Figure 1-9 Bubble Wrap Placement in a Box

Figure 1-10 Placing the Molded Anti-Static Foam on Top

21. Place two straps around the box, approximately two inches from each end. Refer to *Figure 1-11*, *Strap Placement*, below.

NOTE 5: Clear packing tape can also be used to close the box.

Figure 1-11 Strap Placement

22. Place the required labels on one end of the box, see
23.
24.
25. Figure 1-12, *Label Placemen*, below. Refer to the appropriate process specification for label content requirements.

Figure 1-12 Label Placement

2. Packaging Requirements

The following requirements apply to packaging CPUs or ASICs:

- Use the correct tray type specified for each CPU or ASIC. Refer to *Table 1-1, CPU or ASIC Packaging Counts by CPU or ASIC Name*, on page 3.
- Orient the CPUs or ASIC properly in the tray.
- Do not place any types of tapes on the trays.
- Do not adhere any labels to the components.
- Each CPU or ASIC slot must contain only one unit. Do not stack CPUs or ASICs.
- Do not mix different part numbers in the same box.
- All shipments must be in overpack boxes.

Reference Information

Reference Documents and Records

Document Title	Number	ESO Controlled [1]	
		Yes	No
Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)	ANSI/ESD S20.20-2014		X
IPC/JEDEC, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices, *J-STD-033B.1:* http://www.jedec.org	N/A		X

[1] All references to documents controlled by Engineering Services were current when this document was released. All hard copies of this document are to be used for reference only.

Document History and Approvals

Dash	*Rev*	*Date*	*Description of Change*	*Originator*
01	A	23 Mar 2004	Initial release.	N/A
02	A	29 Jun 2004	Updated Table 1-1. Made edits throughout the document.	N/A
03	A	1 Nov 2005	Updated to current StarOffice template; Updated Table 1-1; Updated Section 1.4: Step 3 and Step 8.	N/A
04	A	10 Sep 2007	Added ASIC references. Added new Steps 6, 8, and new Figure 1-7.	N/A
05	A	18 Jun 2008	Updated Table 1-1; updated Section 1.1; updated Section 1.4: Step 6, 8, 9, and 10; replaced new image for Figure 1-8 and Figure 1-9; added Figure 1-10; and updated Section 2.	N/A
06	A	19 Oct 2011	Updated *Table 1-1* for new CPU and ASIC tray part numbers and removed canceled CPU and ASIC references.	N/A
Agile History				
Rev		***Date***	***Description of Change***	***Originator***
07		30 Oct 2015	Updated Table 1-1 - added new column (named “Active?”) for part status and added new parts to table.	N/A
08		12 Jan 2023	Reformat to Redwood Template. Update attachment category to Misc. No content changes.	N/A

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