Document Number and Revision: 910-1021 Rev13

Printed Circuit Board Assembly Workmanship Standards

Overview

Provide a brief explanation as to what the document is about. The purpose of the document is:

- To specify critical PCBA handling, material and process requirements that shall be followed by Oracle's EM partner, to ensure Oracle's product quality and reliability standards.
- To establish Oracle's PCA acceptance/nonacceptance quality requirements that are different or more stringent than Industry standards (IPC-A-610, Class 2).

NOTE: IPC-A-610, Class 2 standard applies for all Oracle products. An exemption, for Tekelec's Eagle Platform products, IPC-A-610 Class 3, latest revision requirements will apply in its entirety for all boards

Order of precedence:

1. Oracle Assembly Drawings
2. Printed Circuit Board Assembly Workmanship Standards, 910-1021-xx
3. Acceptability of Electronic Assemblies, IPC-A-610, Class 2
4. Requirements for Soldered Electrical and Electronic Assemblies, J-STD-001

NOTE: In order to approve conditions that do not meet Oracle or IPC standards, approval by the responsible Oracle PE or SE must be documented using the appropriate Oracle Deviation, Waiver or ECO process.

Audience

This document is for all Oracle engineers and EMs responsible for designing and assembling Oracle PCBAs to ensure acceptable workmanship and quality standards.

TABLE OF CONTENTS

ACRONYMS

ACRONYM	DEFINITION
AOI	Automatic Optical Inspection
APTT	Advanced Process Technology Team
BGA	Ball Grid Array
BOM	Bill of Materials
CPU	Central Processing Unit
ECO	Engineering Change Order
EM	Electronics Manufacturers
ICT	In Circuit Testing
PCA	Printed Circuit Assembly
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PE	Product Engineer
ppm	Parts Per Million
PTH	Pin Through Hole
PWB	Printed Wiring Board
QFN	Quad Flat No lead package
ROL0	RO - Rosin flux composition; L - Low activity level; 0 - Less than 0.05% Halide by weight
SE	Supplier Engineer
SIR	Surface Insulation Resistance
SMD	Surface Mount Devices
SMT	Surface Mount Technology
SPI	Solder Paste Inspection
SCO	Supply Chain Operations

INTRODUCTION AND BACKGROUND

Many questions arise inside the Oracle manufacturing community regarding PCBA standards. Some of these issues, related to acceptability of solder joints lie outside IPC-A-610 (acceptance standard) and specific to Oracle board assemblies. This document answers those questions. In addition to acceptance standards, this document also specifies important material, handling and process requirements needed to meet Oracle's quality and reliability targets.

1. IDENTIFICATION AND MARKING REQUIREMENTS

1.1

Stamping inks must be permanent. Labels must be able to withstand the high temperatures of assembly and cleaning processes without any degradation in scanning performance or legibility.

1.2

Refer to Oracle Specification 950-4477-xx on label requirements.

2. COMPONENT HANDLING REQUIREMENTS

2.1 Moisture sensitivity:

Industry standard J-STD-033 shall be followed on handling, packing and use of moisture sensitive devices to avoid moisture induced failures such as 'pop-corning'.

2.2 Electrostatic Discharge (ESD) control:

Compliance with ANSI/ ESD S20.20 is required for handling ESD sensitive devices. The following additional requirements shall also apply:

- Resistance range for ESD safe work surfaces must be between 1x10^5 Ohms and 1x10^9 Ohms point to point and point to groundable point.
- Personnel handling bare CPU's or BGA's must do so only while wearing an ESD wrist strap that is connected to ground at an ESD workstation equipped with a constant monitoring device that emits visual and audible alerts in the event there is a failure in the wrist strap grounding.
  - This requirement does not apply If CPUs or BGAs remain in their tray, reel, or tape as would typically be the cased during the load operation at SMT pick and place machines. Only the standard ANSI/ESD S20.20 requirements apply under those conditions

2.3 Process limits:

IPC/JEDEC J-STD-020 guidelines shall be followed for allowable maximum component temperatures during assembly process.

2.4 Age of components:

Component supplier documentation should be followed to determine acceptable component shelf life prior to soldering. If not specified, a default two-year date code requirement is applied to all Oracle components that require soldering. However, it is acceptable to use material with date codes older than two years, subject to passing solderability testing as per IPC J-STD-002 and on receipt of a formal concession from Oracle. Records of all such solderability tests must be retained.

After passing solderability testing, components have a shelf life that is considered acceptable for 6 months. PCBs that are coated with Organic Solderability Preservative (OSP), have a one-year shelf life, but can be re-coated at the PCB supplier to restart a one-year shelf life. This OSP re-coating can only be completed once on a PCB.

3. SOLDERING MATERIAL REQUIREMENTS

Oracle generally does not mandate EMs to use a particular type/vendor for solder paste, wave flux, rework flux and flux core wire solder. However, the solder paste and other fluxes selected by Oracle's EM partners shall satisfy the following general requirements to ensure reliability of Oracle products. The EMs must provide qualification data to Oracle APTT. The data will be reviewed by APTT before approving it for use on Oracle products. Any changes after initial approval must follow Oracle's Product and Process Change Notification (PPCN) process 923-2465-xx.

3.1 Solder paste requirements for Lead-Free assembly and rework:

3.1.1. Lead-Free Alloy: SAC305 (96.5%Sn/3.0%Ag/0.5%Cu)

3.1.2. Particle size: Type 3 or Type 4 (IPC J-STD-005).

3.2 Flux chemistry requirements (Includes solder paste flux, wave flux and rework flux):

3.2.1. No-clean flux chemistry.

3.2.2. Activity level: ROL0 as per IPC J-STD-004 requirements.

3.2.3. Pass Surface Insulation Resistance (SIR) test IPC-TM-650 section 2.6.3.7, as defined in IPC-J-STD- 004 Pass-Fail Criteria.

3.2.4. Pass Telcordia GR-78, Section 13.1 SIR and Electromigration test.

3.2.5. All fluxes used in PCBA process; SMT solder paste, wave flux, rework flux and fluxed core wire solder must be compatible with each other. The combination should Pass IPC-TM-650 section 2.6.3.7 for SIR chemical compatibility.

3.3 Wave alloy requirements:

3.3.1. Lead-Free Alloy: SAC305 (96.5%Sn/3.0%Ag/0.5%Cu)/SN100C (Sn99.3%/Cu 0.7% +Ni+Ge)

3.4 PTH Rework Alloy requirements:

3.4.1. Lead-Free Alloy: SAC305/ SN100C (Sn 99.3%/Cu 0.7% +Ni+Ge)

3.5 Cored wire requirements:

3.5.1. Lead-Free Alloy: SAC305 (96.5%Sn/3.0%Ag/0.5%Cu)

4. SMT PROCESS REQUIREMENTS

4.1 Solder paste inspection:

After printing process (top and bottom side), every board shall be inspected using an automatic 3D Inline SPI machine. The SPI machine shall be set to measure critical printing parameters: solder paste volume, height, print off-set and smearing. The SPC upper and lower limits should be properly determined and set to eliminate false calls and escapes by correlating AOI data.

4.2 Reflow profile:

For every Oracle PCBA, a reflow profile shall be established, verified and recorded to ensure reflow and time falls within the acceptable range of solder paste, PCB and components. Refer to IPC/JEDEC J-STD-020 for guidelines for establishing reflow profile.

4.3 Inert Reflow:

The use of Nitrogen is mandated during reflow soldering of Oracle products.

4.4 AOI:

Every Oracle PCBA (top and bottom side) must be inspected using an Inline AOI machine, after the SMT reflow process.

5. WAVE SOLDER PROCESS REQUIREMENTS

5.1 Wave profile:

For every Oracle product, a wave profile must be established, verified and recorded.

5.2 Inert Atmosphere:

The use of Nitrogen is mandated for wave soldering process for better solderability and reducing dross.

5.3 Solder contamination analysis:

The solder pot must be monitored periodically for Pb and Cu contamination. The EM must maintain the solder pot with acceptable contaminant levels defined in IPC-J-STD-001.

6. ACCEPTANCE STANDARDS

6.1 X-Ray Inspection Standards

Oracle PCBAs with hidden joints (top and bottom side) must be inspected using an automatic x-ray machine to inspect for solder joint bridging, opens/insufficient, voids and barrel-fill percentage. In Table 6-1, Oracle X-Ray guidelines and acceptance standards are defined.

NOTE: For Tekelec's Eagle Platform products, IPC-A-610 Class 3 applies instead of Class 2, in Table 6-1.

Table 6-1 Accept or Reject Condition

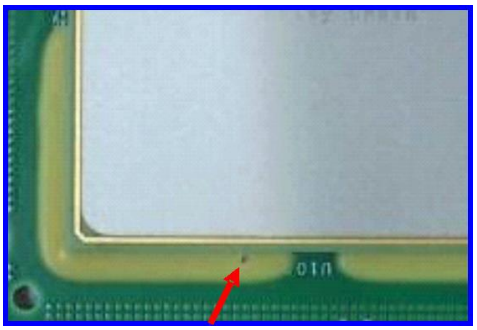
CONDITIONS	DEFINITION	ACCEPT	REJECT
SMT Bridging	Two or more pads joined with solder.	Same as IPC-A-610 Class 2	Same as IPC-A-610 Class 2
SMT Opens	Gross open condition: Solder ball appears as a dark image. Solder ball which appears as a light image is caused by missing solder.	Same as IPC-A-610 Class 2	Same as IPC-A-610 Class 2
BGA voids	Light areas in a darkened solder joint.	Total voiding < 25% x-ray image area. (and) The diameter of single largest void must be less than or equal to 25% of the solder ball diameter.	Total voiding > 25% x-ray image area. (or) The diameter of single largest void > 25% of the solder ball diameter.
Thermal Plane Voids (QFN Type parts)	Voids in thermal plane connections under QFN type components.	The total void area must be less than 50% of the thermal plane area unless	Void area greater than component specification requirement or greater than 50% of thermal plane area if

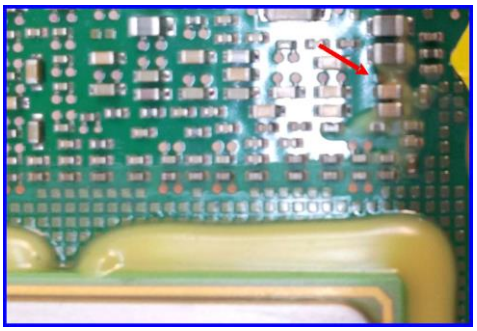
		component specification requires less.	not specified in component specification.
Mis-shaped joints with solder in via hole	Loss of masking material at the pad/trace/via interface area causing solder to wick down the trace and into via.	Oval joint with solder on trace but not on via pad.	Reject pads with oval shaped solder joints with solder extending down the trace into the via. These are considered reliability hazards due to insufficient solder.
PTH Holefill	Amount of solder filling a Plated Through Hole connection.	Same as IPC-A-610 Class 2	Same as IPC-A-610 Class 2

6.2 Edge Bonding Acceptance Standards:

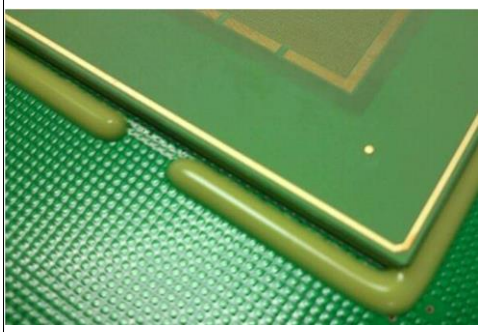
When edge bonding is required per the Oracle BOM or Assembly drawing, the following criteria apply:

Target		90% pattern coverage Fully adhesive cured Properly bonded with CPU edge No smear No bubble/hole

Acceptable		Material smear
		Small Void (bubble)

Acceptable		Non-smooth surface [Note: Exposure of the package bottom edge and fillet disruption are not allowed.]
Acceptable		Excess Material [Note: This appears after ICT test.]
		Hole [Note: Exposure of the package bottom edge is not allowed.]

Reject		Less than 90% pattern coverage

Reject		Non-bond with CPU edge

7. REPAIRS/REWORK

The Class 2 product requirements of IPC-7711/21 Rework, Modification and Repair of Electronic Assemblies apply to all repairs, unless otherwise specified.

Baking temperatures for assemblies prior to hot air rework must be maintained within the range of 105 +/- 5 degrees C to avoid component damage. Bake temperatures are subject to any product-specific requirements listed in FAB or 504 assembly drawing. Bake time shall be 24 hours minimum.

Rework processes must be qualified and approved by Oracle SCO Personnel prior to use on production product.

7.1 Maximum number of allowable reworks

The removal and replacement of a component during a rework process is considered to involve two heat cycles, one to remove the bad component and immediately redress the site, and one to solder the new component in place.

7.1.1 The maximum number of reworks on a site that requires hot air rework is two times, or four heat cycles.

7.1.2 The maximum number of reworks on a soldered-in through hole component site is two reworks, or four heat cycles.

7.1.3 The maximum number of reworks per SMD passive component and leaded SMD component is unlimited, except as otherwise specified in this document, and as long as the IPC 610 standard on solder joint quality is met.

7.1.4 The removal of pressfit device does not require heat cycles but requires mechanical force to remove and reinstall the device. The maximum number of reworks for a pressfit device is 2 times.

7.1.5 If pending rework on a PCA violates the above guidelines, the Supplier must contact the responsible Oracle Product Engineer and provide a proposal with analysis for the disposition of the board.

7.2 PTH Rework

7.2.1 The minimum remaining copper thickness after repair and/or rework on SMD pads/lands, and within component plated through holes, especially at the knee of the hole where the surface pad connects with the plated hole wall, is 0.00050 inches.

7.2.2 PWAs with damaged hole barrels and/or exposed glass fibers in the plated-through hole (PTH) area must be scrapped after:

7.2.2.1 Root cause failure analysis

7.2.2.2 Corrective action is documented

7.3 Rework Wires

7.3.1 Rework wires must be located a minimum of 0.200 inches from the edges of the PWB.

7.3.2 The wires used for rework and repair must be 30 AWG UL-listed insulated wire, unless otherwise specified.

Note: Permission to add jumper wires for non-ECO related work requires prior approval by a Oracle Product Engineer or Supplier Engineer through a formal Oracle Deviation (DA). No jumper wire repairs are permitted on clock traces.

7.4 Trace Repairs

7.4.1 The number of repairs to cut or damaged traces is permitted on external layers only and must not exceed three repairs per board.

7.4.2 Scrap all boards that require repairs to more than three traces, or where glass fibers or inner layers have become exposed.

Related Information

REFERENCE DOCUMENTS AND RECORDS					
Document Title	**Number**	**ESO Controlled**		**Quality Record**	
		Yes	**No**	**Yes**	**No**
Oracle America Quality Policy Manual	923-1607-xx	x			x
Fabrication Specification-Printed Wiring Board	950-1009-xx		x		x
Identification, Labeling, and Bar-coding Standards for Assemblies	950-4477-xx		x		x
Supplier Chain Product and Process Change Notification (PPCN) Request Procedure	923-2465-xx	x			x
Rework of Electronic Assemblies	IPC-7711		x		x
Repair and Modification of Printed Boards and Electronic Assemblies	IPC-7721		x		x
Acceptability of Printed Boards	IPC-A-600		x		x
Acceptability of Electronic Assemblies	IPC-A-610		x		x
Component Mounting Guidelines for Printed Boards	IPC-CM-770		x		x
Qualification and Performance of Permanent Solder Mask	IPC-SM-840		x		x
Test Methods Manual - Bow & Twist	IPC-TM-650		x		x
Requirements for Soldered Electrical and Electronic Assemblies	J-STD-001		x		x
Standard for Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices	J-STD-033		x		x
Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)	ANSI/ESD S20.20		x		x
Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices	IPC/JEDEC J-STD-020D		x		x
Requirements for Soldering Pastes	J-STD-005		x		x
Solderability Tests for Component Leads	J-STD-002		x		x
Requirements for Soldering Fluxes	J-STD-004		x		x
Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment	Telcordia GR-78		x		x

Document History and Approvals

Dash	Rev	Date	Description of Change	Originator
01	A		Initial release.	N/A
	B	10 May 1989	Minor Revisions	N/A
	C	13 Jun 1990	Chapter 7 revised. Entire doc edited	N/A
	D	24 Jul 1991	Chapter 6 removed; major revisions; illustrations added	N/A
	E	27 Nov 1991	Change Quality Manual part number	N/A
	F	8 Sept 1993	Add TAB assys and misc changes	N/A
03	G	17 May 1994	Add marking of country origin	N/A
03	G	18 Feb 1997	Removed from ECO control and -03 inactivated.	N/A
04	A	11 Mar 1997	Control assumed by "Owner" per ECO WO_10221. Format updated (figs & tables auto-numbered). Added list of figures, list of tables, cover sheet., E-mail appvl page, logo. Added info on BGAs; ext SBus conn. tilt tol.; pad & trace rework limitations. Added note and "Owner" above	N/A
04	B	26 Nov 1997	Pulled into Tech Comm template. Editorial changes only, no content modification.	N/A
05	A	30 Jun 1998	Added sec 5.7, fig 5-6. Changes to tables 8-1 and 10-1. Changes to Sec 8.6.1, 10.3.	N/A
06	A	04 Oct 2000	Major revision of document to simplify it.	N/A
07	A	03 Nov 2004	Minor revision of document. New SO template.	N/A
08	A	18 Dec 2006	Added Section 6.	N/A
Agile History				
Rev		***Date***	***Description of Change***	***Originator***
09		16 May 2014	Major Revision to simplify and reorganize the document. Removed outdated and IPC-A-610 redundant information. Added new sections 2, 3, 4, 5 and section 6.2 to the document. Section 7.1.1 changed to "The maximum number of reworks on a site that requires hot air rework is two times, or four heat cycles." Removed reference to IPC 7095.	N/A
10		11 Dec 2015	Revised Section 2 to include ESD requirements additional to ANSI/ESD 20.20. 1) Minimum ESD Workstation resistance, 2) ESD wrist straps grounded via constant monitoring device required for personnel handling of CPU's and BGA's. 3) Revised Section 7 to clarify bake parameters for assemblies prior to hot air rework. 4) Removed inapplicable reference to IPC-A-610 in Table 6-1 for BGA Void criteria. IPC-A-610 criteria is significantly looser for acceptance of BGA Voids.	N/A
Fusion History				

11	23 Jan 2019	Updated to clarify Age of Components, section2.4, and add alternate SN100C Wave Alloy to section 3.3, previously approved for rework.	N/A
12	1 April 2019	PDF file not showing pictures	N/A
13	4 Feb 2022	Updated to Redwood Template 7301497	N/A

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