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External Manufacturer (EM) Printed Circuit Board Assembly (PCBA) Design for (DF*) Requirements

Document Number and Revision: 923-3664 Rev 06

Overview

This document describes the requirements for an External Manufacturer (EM) when performing Design For (DF*) (DF* Manufacture [DFM], DF* Test [DFT]) reviews of Printed Circuit Board Assemblies (PCBAs). These requirements apply to Oracle designs managed through the Job Tracking System (JTS)..

Audience

This document is for Oracle individuals and EM's that conduct PCBA DF* reviews on PCBAs managed through the JTS.

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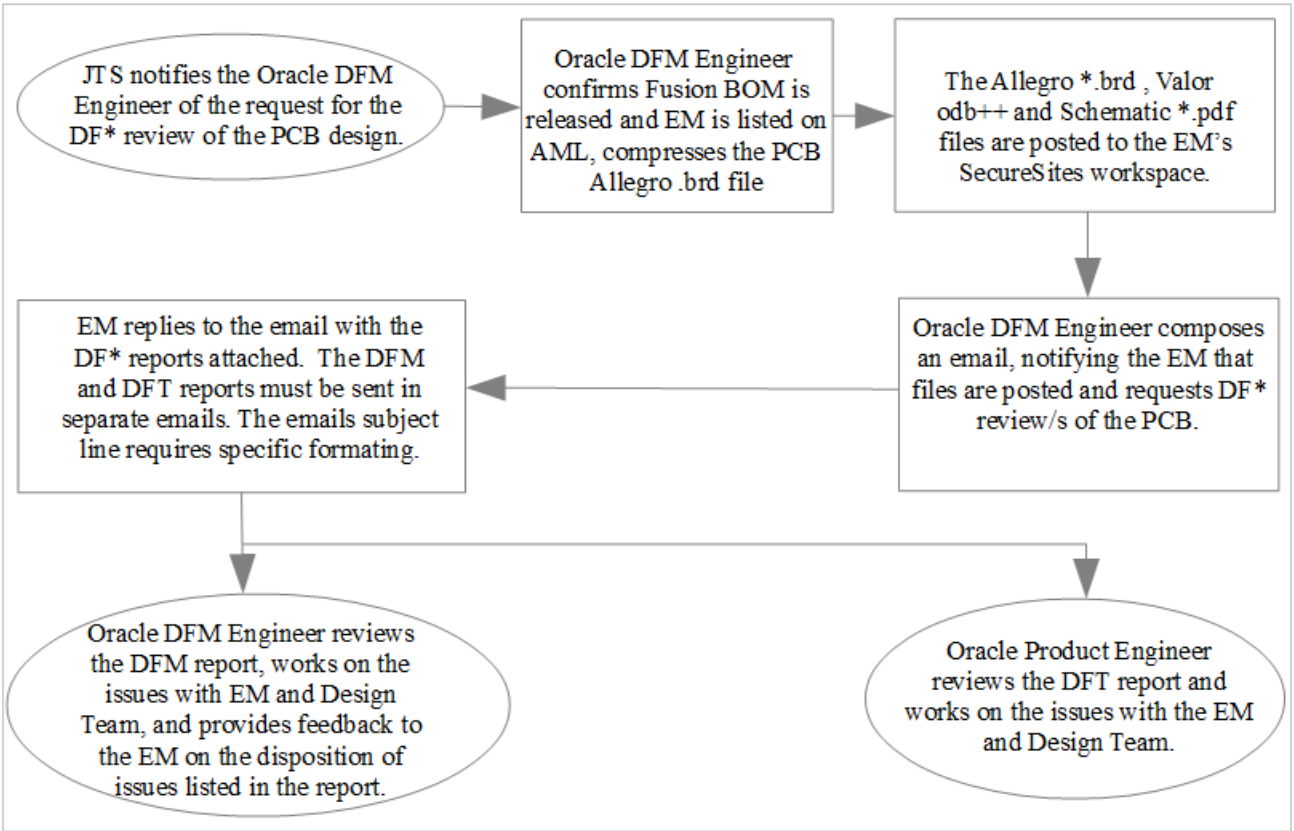
Introduction

PCBs designed internally at Oracle are managed in the Oracle JTS. Joint design models (JDMs) and outside design models (ODMs) are not managed in the JTS.

This document contains the requirements and expectations regarding the DF* process that are conducted by the EMs.

Triggered by the JTS, Oracle requests DFM and DFT reviews of a PCBA design from the EMs who are identified as the intended assembly vendors for that design. The job detail sheet in the JTS lists the intended assembly vendor (EM).

1 DF* Process Flow



1. DFM Engineer is notified via JTS that a DFM review has been requested.
2. DFM engineer posts board and schematic files in the Public Document's folder within responsible EM's SecureSites workspace.
3. DFM engineers notify EM via email that the board files are available for review. All Oracle individuals involved in the review stages are copied on this initial email.
4. DFM report submitted by EM is reviewed, all issues are evaluated against DFM guidelines and fixed where possible. All parties are notified of the final disposition of DFM issues. DFT report is reviewed by the Product Engineer, the issues are worked out with the EM and the design team.

5. DFM approval is signed off in the JTS by the DFM Engineer and DFT approval is signed off by the PE.

2 SecureSites

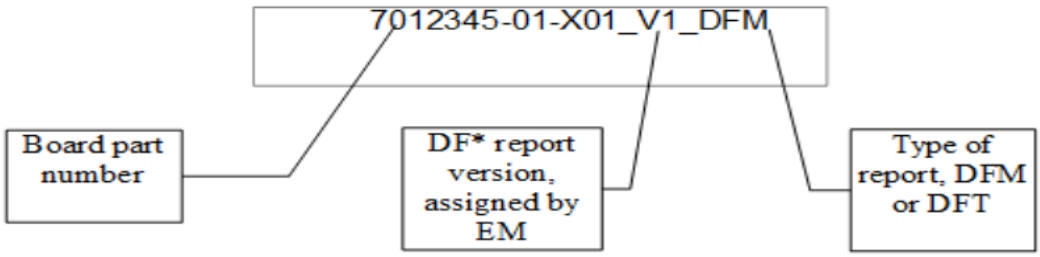
SecureSites is a secure, browser-based application, used to transfer data files between Oracle and its partners. Oracle sets up a SecureSites account for each EM. The EM identifies their individuals that must have access to their respective site. Contact Oracle DFM Engineering for access to appropriate SecureSites folders.

3 Email Format Requirements

The EM sends the DFM or DFT report(s) to Oracle in email as an attachment with a specific email subject line, upon the completion of the DF* reviews. Refer to *Figure 3-1, Email Subject Line Format Requirements*.

- All parties in the original DFM or DFT email request must be copied. The EM can add additional persons to the cc list as needed.
- The attached report(s) must follow the same naming conventions as the email subject line except for the file extensions. The reports must be created in either Oracle Open Office or Microsoft Excel.
- DFM Engineering is responsible for report archival of the DFM and DFT reports.

Figure 3-1 Email Subject Line Format Requirements



4 DF* Requirements

DF* reviews must add value to the PCB design process by providing timely and easy to read reports with an accurate and valid list of DF* issues.

4.1 DF* Report Time Guidelines

- The turnaround time is measured from the start time to the stop time:
    - **Start time:** The clock starts when Oracle makes a request through an email to the EM.
    - **Stop Time:** The clock stops when the EM delivers the report to Oracle through an email.
- 72 hrs. - The very first Initial DFM (or Final DFM, if no Initial) on a new project design, for example moving from an X5 project to X7, whether a make-from or totally new layout.
- 48 hrs. - All reviews after the first one, including initial, final, and/or board revisions (new part number, same project). Depending on extents of changes made, Oracle may consider extending the 48-hour turn to 72 hours. This decision is made by the Oracle DFM Engineer and the requesting Oracle Design Engineer.
- Note: DFM/DFT report delivery is based EM time zones, e.g. 72 hrs. must include three full 8 hour work-shifts in the EM's time zone. Delivery of the DFM/DFT report from EM may be carried into next day with adjustment for time-zone difference.

4.2 DF* Review Requirements

Automated software such as Valor or Fabmaster must be employed. In addition to automated DFM/T reviews the EM is to provide the following, when applicable:

- Identify all Intrusive Reflow components and provide keep-out areas for solder paste overprinting and/or solder preforms.
- Identify and provide keep-out areas around all BGA's that require edge bonding.
- For components that potentially have coplanarity issues, identify and provide keep-out areas for solder paste overprinting.
- On boards requiring selective wave soldering, identify direction of wave and components that require thieving bars.
- On boards requiring solder paste printing, identify the print direction.

4.3 DF* Report Format

Provide the following:

- A tracking matrix which lists the fab part number and the date of the review
- A summary of open and closed items, listed by severity. All issues must be weighted according to severity, for example: hot (red), warm (yellow), and cold (blue), where:
    - **Hot (red):** the issue has direct effect on manufacturing, the cost of the product, or the quality of the product
    - **Warm (yellow):** the issue has impact on manufacturing, quality, or cycle time, it can be mitigated by work-arounds
    - **Cool (blue):** the issue has low impact on manufacturing, quality, or cycle time
- Visual examples of the issues
- A number assigned for tracking purposes, with the dates the issue was opened and closed

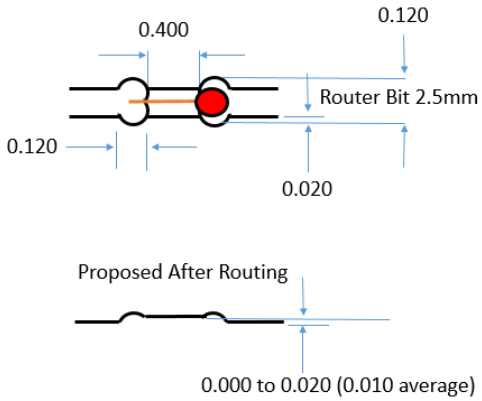
5 EM Fab Responsibilities

There are some aspects of the fab design that fall under the responsibility and control of the EM, such as the panelization of the fab, and Paste mask artwork.

5.1 Fab Panelization

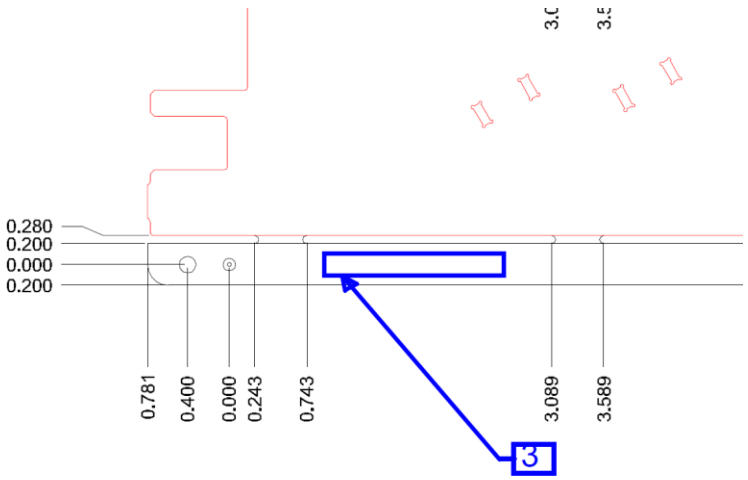
- The fab panelization breakaway requirements of the assembly EM facility are developed and managed by the assembly EM providing the finished boards, and after depanelization, are in full compliance with Oracle Specification: Printed Circuit Board Assembly Workmanship Standards, 910-1021-xx.
- Oracle recommended fab panelization breakaway detail and dimensions.

Figure 5-1, Oracle recommended route tab



- Oracle does not panelize board designs in multiple board arrays for PCBA manufacturing purposes. When required it is the responsibility of the EM to develop the detailed multiple-up panel drawing and share it, in both *.pdf and *.dxf file formats, with Oracle and the fab supplier.
- When an individual PCB is required to be fabricated as a multi-up panel with handling rails or single-up panel with handing rails, on the panelization drawing, the EM shall flag an area on one of the handling rails where space is available and indicate via flagnote that the PCB fabricator shall add silkscreen marking for "FAB MADE IN _ _ _ _ _ " text. Silkscreen marking minimum text height shall be 50 mils. Reference Figure 5-1, FAB MADE IN _ _ _ _ _.

Figure 5-2, FAB MADE IN _ _ _ _ _



3 PCB fabricator shall add silkscreen text for "FAB MADE IN _____" in area indicated. Text shall be same color as PCB silkscreen. Minimum text height to be 50 mils.

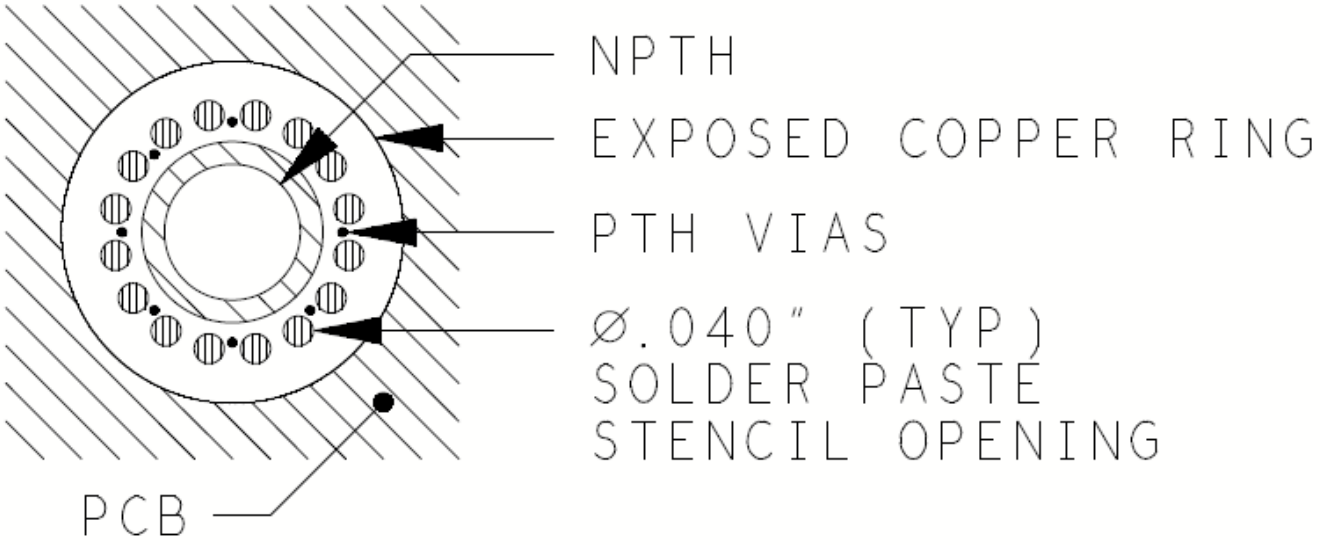
- In a situation where an odd shaped PCB design is assembled as a single board, Oracle adds breakaway, handling rails, and tabs to straighten the edges of the board, to accommodate the assembly process. In addition to providing a panel drawing the EM is to provide a dxf file containing the board outline including required handling rails, breakaway/routed tab dimensions and locations, and any tooling holes and/or fiducials located in the handling rails. This data then becomes part of the Oracle Allegro board database.
- EM shall provide necessary panel drawing/dxf file(s) with each first pass DFM report (first pass defined as the first time a DFM request is made with a newly assigned Oracle part number) and any subsequent passes in which the board outline or panel requirements change. This data shall follow the same naming conventions as the DFM report except the _DFM is replaced by _PNL, for the panel drawing, and _DXF, for the panel dxf file along with appropriate file extensions.
- EM shall also provide Oracle with their final panel drawing, based on Oracle's released fabrication data, at the same time it is provided to the board fabricator. The panel drawing should reflect board part and dash number along with EM revision and shall be provided in both *.pdf and *.dxf file formats.

5.2 Paste mask

Oracle fab design package includes Paste mask with clearances for all surface mount device contact surfaces for the application of solder paste during assembly. Assembly EM-directed specific changes to the Paste mask artwork contained in Oracle fab design package data can be made by the EM, at the EM's discretion, without prior approval by Oracle, with the following exception;

No changes are allowed to the .040" diameter Paste mask openings provided on any solder mask exposed copper ring surrounding a PCB Non-Plated Through-Hole (NPTH), and containing a circular array of Plated Through-Hole Vias. Reference Figure 5-2, Exposed Copper Ring.

Figure 5-3, Exposed Copper Ring



Document History and Approvals

	Rev	Date	Description of Change	Originator
01	A	12 Nov 2007	Initial release.	N/A
Fusion History				
Rev		***Date***	***Description of Change***	***Originator***
02		20 Jun 2011	Update to conform with Oracle requirements	N/A
03		26 May 2017	1. Sections 1 and 2 updated to reflect changes to file transfer process from SunExchange to Beehive Online Workspaces. 2. Section 3 updated to reflect new report archival process. 3. Section 4 added additional requirements for EM reviews. 4. Section 5.1 updated to reflect new PCB panelization requirements. 5. Section 5.2 removed via plugmask requirements and renamed 5.3 Pastemask to 5.2 Paste mask.	N/A
04		16 Oct 2017	1. Section 5.1 updated to reflect new PCB panelization requirements.	N/A
05		29 May 2020	Updates to Revision 04:	N/A

		Section 3 – Removed reference to archival location and “page 5” for email format requirements. Section 4 – Report time guidelines modified to better define review period. Section 5 – Added paragraph and details for handling rails marking requirements.	
06	10 Mar 2022	Section 1 – Replaced “BEEHIVE ONLINE” with “SecureSites” Edited flow chart to include DFM Engineer to confirm Fusion release of BOM and AML. Section 2 – Replaced “BEEHIVE ONLINE” with “SecureSites” Section 4 – Edited reporting guidelines to clearly outline delivery expectations. Added requirement for EM to provide solder paste print direction in feedback. Removed Identify all test-point vias that are required to be filled and capped. Section 5 – Replaced “APT Process Technology (APT)” with “Oracle Specification”, added text stating “Oracle recommended fab panelization breakaway detail and dimensions.” Added Figure 5-1, changed existing 5-1 to 5-2, 5-2 to 5-3.	N/A

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