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In-Circuit Test (ICT) Design for Testability

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Overview

This document describes the general in-circuit test (ICT) design for testability criteria for the printed circuit board (PCB) electrical designer. The implementation of Design For Testability (DFT) requirements produces testable boards that can be repaired in the most cost effective manner.

Audience

This document is for PCB Electrical Design Engineers and Product Engineers with ICT responsibilities.

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Introduction

In-Circuit Test Strategies

In-Circuit Test engineers understand the capabilities and limitations of ICT systems and test fixturing. They can therefore provide board design guidelines that are intended to maximize the test coverage that ICT can provide for any given board design. Adherence to the guidelines provides an opportunity to develop and implement ICT strategies that result in optimum ICT coverage.

Cost Benefits

Adherence to recommended ICT Design for Testability (DFT) guidelines results in improved board test yields during subsequent stages of the overall board test process. The diagnosis provided by ICT is very specific and allows for rapid, low cost identification and repair of manufacturing faults.

Poor compliance with DFT guidelines increases costs because the resulting test escapes allow a higher percentage of faults to remain undetected until post ICT test steps. Diagnosing faults detected after ICT is much more difficult and expensive. The Design Engineer who develops boards that are DFT compliant reduces manufacturing costs throughout the life of the product.

1 ICT Electrical Design Rules

1.1 Pull Up and Pull Down Resistors

For digital device inputs that are intended to be fixed in the high or low state, use pull up and pull-down resistors rather than connecting them directly to power or ground rails. The ICT system can then drive these inputs to the logic state required to verify that the device is operating correctly. Also, if the inputs are Output Enable, Direction, Write Enable, etc. then the ability to control them will assist with digital test isolation.

When multiple inputs on the same device require pull up or pull-down resistors, the preference is for each pin to have its own pull up or pull-down resistor. When multiple device inputs are connected, it can result in an ineffective or compromised test at ICT.

Pull up and pull-down resistor requirements:

- Terminate all floating inputs on ICs with a resistor tied to either a power or ground. This is not necessary when device inputs have internal pull up or pull-down resistors.
- The pull up or pull-down resistor value must not be less than 50 ohms due to tester driver limitations. The ICT output driver circuits cannot reliably drive low value pull up or pull-down resistors.

1.2 Free Running Clocks

Provide a means of inhibiting all frequency sources on the board. Free running clocks interfere with the testing of other digital devices on the board and contribute to ambient fixture electrical noise. The use of tri-state oscillators or external gates that can be disabled is required.

1.3 Batteries and Voltage Sources

When voltage sources are on the board during ICT, there is potential for damage to the ICT system during un-powered tests. Batteries on the board must be attached to the board using sockets so that the battery can be installed after ICT. The potential for tester damage also applies when large value capacitors are on the board, because once charged, they become voltage sources. Capacitor control techniques are addressed in other best practices documents.

1.4 I2C Devices

These devices are required on board programming during ICT. Please provide device all Pins Accessible (Tps assigned to device pins) for ICT.

2 Boundary Scan Design Guidelines

2.1 Interconnect Boundary-Scan

ICT Boundary-Scan and Standalone Boundary Scan Design Requirements:

- The boundary-scan implementation and the development of devices must comply with IEEE 1149.1 and 1149.6 specifications (refer to IEEE Standard Test Access Port and Boundary Scan Architecture, 1149 and IEEE Standard for Boundary Scan Testing of Advanced Digital Networks, 1149.6).
- All Boundary Scan (Bscan) devices should be configured into a single scan chain or made to look to Bscan test software as though the devices are in a single chain meaning that every scan device receives the same TCK, TMS and TRST signal activity. JTAG ports of different scan devices can have different voltage requirements, voltage translation devices such as the TI 74AVC*T245 family of devices can be used to ensure that all Bscan devices receive their required voltages. The TDO pin of each device in the scan chain must be connected to the TDI pin of the next device in the chain with voltage level translation as required.

- For any Bscan device, JTAG pins (TDI, TDO, TMS, TRST and TCLK) must not be connected to other pins of the same device.
- If a large number (>20) of Bscan devices are on the board, the TMS and TCK signals must be buffered to keep the trace lengths to less than 40 inches. Traces longer than this cause the Bscan tests to be unstable and execute at a much slower clock rate, thereby increasing test times.
- Avoid chains of more than 14,000 scan cells on each scan ring. Longer chains may be used with the approval of EM ICT Engineer because upgraded ICT Equipment Pin Cards are required to support longer chains.
- Do not include non-IEEE 1149.1 compliant Boundary Scan devices in the scan ring.

Refer to *Figure 2-1 Example of a Single and Multiple Device Boundary-Scan Chain* for single and multiple device boundary-scan tests.

2.2 Device level Boundary Scan

Device level Boundary-Scan is the testing of Bscan devices as individual components. There is no Bscan test interaction between devices.

All Jtag port pins, TDI, TCK, TMS, TDO and TRST do not need to be connected to other Bscan devices, only pull up and pull-down resistors.

2.3 1149.6 AC Boundary Scan

AC Boundary Scan is used for High Speed Nets (>1GHz) that are capacitively coupled.

- All of the requirements of Section 2.0 also apply to 1149.6 test requirements
- Even though 1149.6 nets are high speed nets, during ICT and Standalone Boundary-Scan, the test signals are in the1Mhz range. For that reason, the signal paths from transmit to receive devices must be capable of operating at 1Mhz. Avoid the use of EMI suppression and filtering techniques that will prevent 1MHz operation on the signal path. The effects of inductors, chokes and transformers in the signal path should be reviewed.

2.4 Additional Boundary-Scan Chain Design Information

All BScan devices have a JTAG port that consists of four mandatory signals, inputs Test Data In (TDI), Test Mode Select (TMS), Test Clock (TCK) and output Test Data Out (TDO). There can also be an optional input signal Test Reset (TRST). Interconnect BScan testing requires that the BScan devices be configured into a chain that share

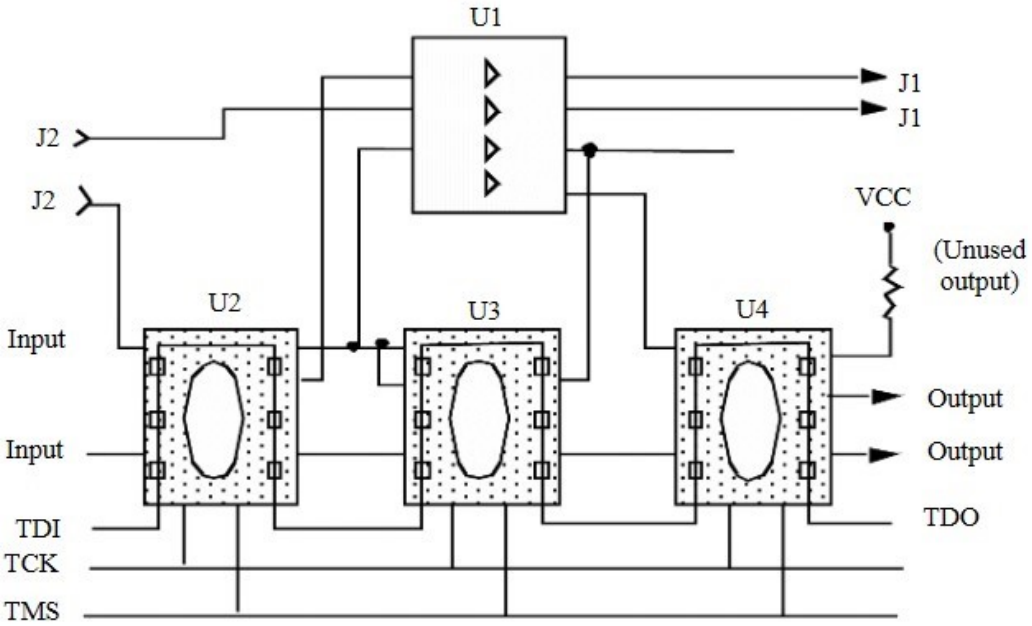
TMS, TCK and TRST. The TDO signal of each device in the chain must be connected to the TDI input of the next device in the chain. Do not include any FPGAs or Service Processors that contribute to power supply control in the chain. When detailed board schematics are available, OPs Eng will review them and provide feedback.

If there are incompatibilities in JTAG device port pin electrical requirements, mainly voltage levels, solutions must be implemented by adding buffers, voltage level converters, etc. to ensure that JTAG device chain requirements are met. The objective is for all JTAG port device input pins except TDI to experience the same signal activity with minimal timing skews.

Provide a means of removing devices from the onboard chain. This is necessary in case having one or more specific Bscan devices in the chain negatively impacts the BScan test. If so then there must be a way to remove it. This can be done by providing zero ohm resistors between TDI and TDO pins of each device in the chain and isolating TMS and TRST, if present, with series 0 ohm resistors and pulldown resistors on the device side of the series resistor. Ops could then choose to have isolation resistors Nostuffed as needed.

Many of the above Bscan requirements can be achieved by the use of a Scan Path Multiplexer such as the TI SCANSTA112, 10mm BGA package or similar device.

Figure 2-1 Example of a Single and Multiple Device Boundary-Scan Chain



3 Physical Layout Design Rules

Refer to Document 990-1028 for board layout design guidelines

4 Board Size

The maximum board size to accommodate standard ICT fixturing is 19 inches x 24 inches. Larger boards require custom fixturing which increases the time and cost required to build fixtures.

5 Level 2 DFT Report

Historically, Oracle PCBA External Manufacturers (EMs) provide Oracle with DFT Reports. The reports are created using information from the Allegro PCB CAD file and include the following information about the PCBA. The EMs are required to provide the standard DFT report within 72 hours of receiving a DFT report request.

- Net Count
- Quantity & Percentage of Nets with test points
- Probe mix by size 100, 75, 50, 39 mils
- Identifies Problem Nets with the types of DFT Violations
- Shows Single Device Pin No Connect Nets
- Lists all Device & Pin Connections for nets that have DFT Violations

The Reports do not assign any level of priority to the nets with DFT violations. To obtain the highest PCBA test coverage during ICT, the ideal situation is for all nets on the board to have test points assigned to them. Rarely is this ideal situation achieved. There are various reasons for this, the most common being electrical signal integrity concerns, and lack of space on the PCB to provide test points. The Level 2 DFT Report is a means of prioritizing the nets without test points so that the problem nets that have the greatest impact on test coverage get the attention they need before the Product Engineer assigned to the board give DFT approval.

Five levels of priorities have been defined. They are:

1 Must have a probe point: Large Test Coverage Loss
2 Needed: Test Coverage Loss of Component Pins on the Net
3 Not Needed: Negligible Coverage Loss
4 Can't Probe: High Speed Net with Signal Integrity Concerns
5 Not needed: No Connect Pin

The following additional checks must be made as part of the Level 2 DFT Analysis:

- Verify that JTAG Port and Compliance pins have probe points
- Verify that nets required for ICT Device Programming have probe points
- Verify that nets required for LED characterization have probe points.

Any of these nets without probe points are assigned to Category 1

Level 2 DFT Analysis is presented to the Engineering Board Owner with a request that probe points be assigned to Category 1 and 2 Nets.

The EMs have estimated that the Level 2 ICT DFT report takes 4-6 days to produce.

5.1 Recommendations for Requesting Level 2 DFT Reports

Level 2 DFT Reports should be requested for the following situations:

- There are Boundary Scan devices on the board
- There is Memory Device Programming required during ICT other than FRUID
- The board is considered to be a medium or high complexity board

5.2 Files Needed to Product Level 2 DFT Reports

File	How Used	Source
Standard EM DFT Report	Identify Nets with DFT Violations	External Manufacturer
Board Electrical Schematic	Determine Circuit Functionality of Nets without Test Points	Product Design Engineering
Device Data Sheets	Determine Device Functionality of Nets without Test Points	Device Manufacturer or Oracle
Boundary Scan Description Language (BSDL)	Determine Bscan Device Port and Compliance Pins	Device Manufacturer or Oracle if Internal Design
Allegro Testprep file	Determine Category 4 High Speed and other NO_TEST Property Nets	Oracle CAD Group: Included in DFT Report Request File Package

6 ICT Fixture, Boundary Scan Fixture or Both? Decision Process

Line	Question	If Yes	If No
1	Are there any Bscan Devices?	Go to Line 2	No Bscan Testing required. ICT only for structural testing. Go to Line 6
2	Are all Bscan Devices sufficiently tested by ICT?	ICT only, no standalone Bscan. Go to Line 6	Go to Line 3
3	Can ICT provide an electrical environment that allows successful Bscan Testing?	Bscan Testing can be done at ICT. ICT Fixture only, BScan Fixture not required. Go to Line 6	Bscan Fixture should be considered. Go to Line 4
4	Can Untested Nets be tested later in the production test process rather than during structural tests?	Go to Line 5	Go to Line 5
5	Is Bscan required to maximize test coverage in the overall structural test strategy?	Bscan Test Fixture required. Go to Line 6	Bscan Test Fixture not required. Go to Line 6
6	Finalize ICT / Boundary Scan Decision		

7 Test Message Reporting Format

Test message need to be reported Oracle from each test run as either a Pass or Fail.

Format:

Example	Description
&v2S Family: E4-2c	Product Family
&v2S Serial #:465136J+2402AR00B6	Board Serial Number Scanned
&v2S ##########################	Pass/Fail Banner
&v2S #### BOARD ICT PASS #####	
&v2S##########################	
&v1S Testplan-Released 06-22-2023	ICT Testplan Release
&v2S ST:240124072659	Test Start Time
&v2S ET:240124073055	Test End Time
&v2S SN:465136J+2402AR00B6	Board Serial Number - FRU
&v2S Mac:A8698C37FB82	Mac address (IF APPLICABLE)
&v3S P/N:8207341 Rev:19	Board Part Number and Revision
&v3S OPERATOR ID:102059	Test Operator ID
&v2S PF:Agilent3070 Rev:8.30	Tester MFG and PN
&v3S Fixture_ID: XxXX_FIXTURE 1	Test Fixture ID (IF APPLICABLE)
&v2S TESTER:TESTER-2	Tester ID
&v2S **********	

In the case of a failure, the failure message needs to be included before the product information:

Failed Open #1

(209167) SVCIO_IO2_UART_RTS_EN_L_2

r7207_2_c.2

Example	Description
&v2S Family: E4-2c	Product Family
&v2S Serial #:465136J+2402AR00B6	Board Serial Number Scanned
&v2S ##########################	Pass/Fail Banner
&v2S #### BOARD ICT FAIL #####	
&v2S##########################	
&v1S Testplan-Released 06-22-2023	ICT Testplan Release
&v2S ST:240124072659	Test Start Time
&v2S ET:240124073055	Test End Time
&v2S SN:465136J+2402AR00B6	Board Serial Number - FRU
&v2S Mac:A8698C37FB82	Mac address (IF APPLICABLE)
&v3S P/N:8207341 Rev:19	Board Part Number and Revision
&v3S OPERATOR ID:102059	Test Operator ID
&v2S PF:Agilent3070 Rev:8.30	Tester MFG and PN

&v3S Fixture_ID: XxXX_FIXTURE 1	Test Fixture ID (IF APPLICABLE)
&v2S TESTER:TESTER-2	Tester ID
&v2S **********	

8 Best Practices

There are the recommended working standards for testing product in In-Circuit Test

Electro-Static Discharge (ESD) Precautions

All personnel are required to take the necessary precautions to ensure that the product will not be damaged from ESD.

- All test operators are required to perform an ESD check on their heel straps or wrist straps each day before handling any product.
- While performing the test operation or handling product, test operators are required to wear a wrist strap or heel straps (if standing)

8.1.2 Calibration Verification

The Operators must confirm that the test equipment has a valid calibration sticker.

8.1.3 Emergency Shutdown

The Operator must locate the test equipment emergency shutdown switch. In the event of an issue. This switch is to be used to shut down the test equipment.

8.1.4 Test Fixture Handling

All test fixtures must be loaded and removed from the test equipment as required.

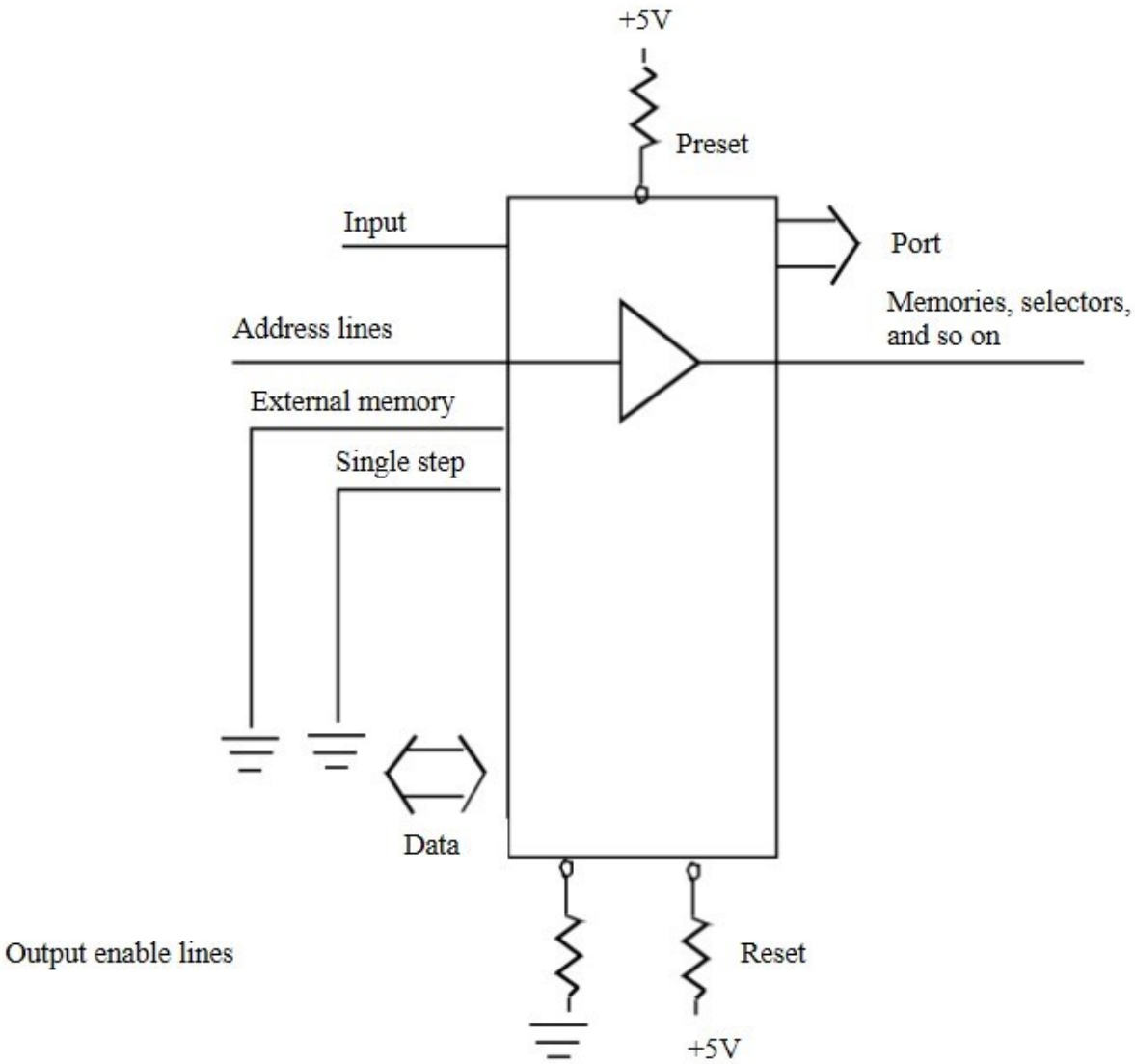
- Ensure the test head receiver is in good operating condition and free of foreign objects.
- A fixture lifter is to be used as necessary.

8.1.5 Test Plan

A golden copy of the test program must be loaded from the test server at the before testing any boards.

Appendix A Design for Testability Problems and Solutions

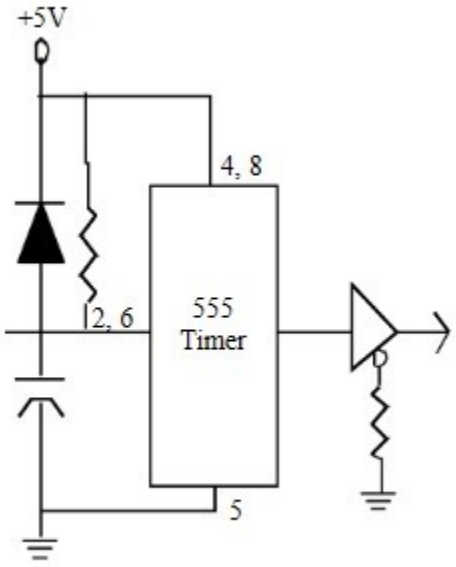
*Figure A-1 Common Digital Device **With** Design for Testability*



High Power Devices

*Figure A-2 High Power Devices **With** Design for Testability*, below, shows higher power devices without and with design for testability.

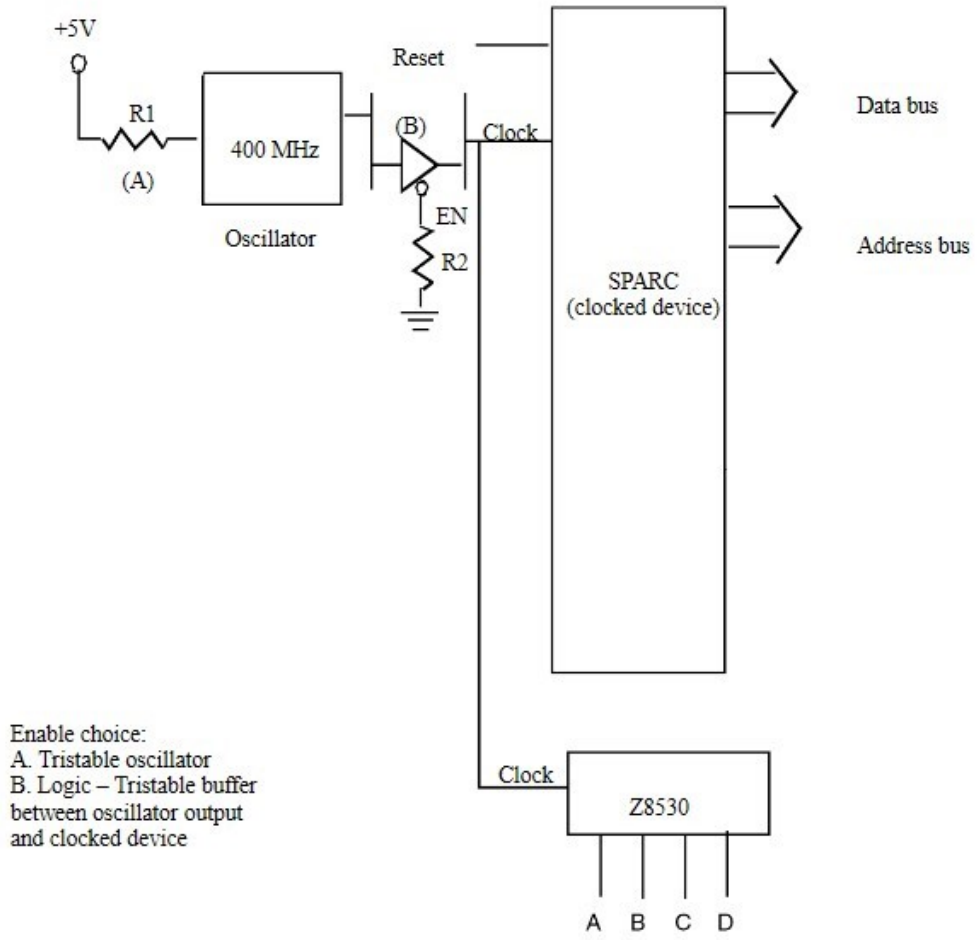
*Figure A-2 High Power Device **With** Design for Testability*



Free-Running Clock Lines

*Figure A-3, Free Running Clock Lines **With** Design for Testability*, below, shows free-running clock lines without and with design for testability.

*Figure A-3 Free Running Clock Lines **With** Design for Testability*



Appendix B ICT Methods

Successful and Unsuccessful ICT DFT

B.1 Successful ICT DFT

In-circuit testers electrically isolate and test components to verify their electrical characteristics. By using electronic guarding techniques that isolate devices from their surrounding circuitry, ICT systems can perform stimulus and response tests on the devices.

• Digital device isolation allows device outputs to be driven to known output states (preferably high) or high impedance states to minimize interference with other digital device tests. If digital device isolation is achieved, the device under test (DUT) can have it's logic functions characterized without interference from outputs of surrounding devices. Many of the electrical DFT guidelines are intended to facilitate digital device isolation.
• For a given analog DUT, device isolation consists of electrically establishing virtual grounds on specific nets surrounding the DUT. If analog isolation is achieved, the DUT can be accurately measured. The majority of analog device related DFT guidelines involve the board layout, rather than circuit design.

B.2 Unsuccessful ICT DFT

Some components are difficult to isolate. They exhibit intermittent behavior during test. For example, if a digital device isn't properly isolated, it's test results are not consistent and fails with various results. Good components fail due to a poor ICT DFT implementation. These unstable tests result in the following:

- Boards are retested to determine if the failing test will pass upon retest.
  • There is an increased number of boards in the diagnosis and repair loop.
  • Operator confidence in the test results causes them to doubt and ignore failing tests.

Related Information

Reference Documents and Records

REFERENCE DOCUMENTS AND RECORDS	
WWOPS Advanced Process Technology: PCBA (DFM/DFT) Guidelines	990-1028
IEEE Standard Test Access Port and Boundary-Scan Architecture	1149.1-1990

Document History

Rev	***Date***	***Description of Change of 911-1235***	***Originator***
06	23 May 2001	Changes to tooling holes and information on component pins; omissions to double-sided reflow requirements.	N/A
07 (A)	04 Jun 2002	Updated to new template and added changes to the boundary scan and the SMD requirements.	N/A
07 (B)	02 Jun 2004	Converted the document to the latest Star Office template	N/A
08	16 May 2005	Removed Section 1.10.2 through 1.10.4, and tolerances in Section 2.	N/A
Agile History			
Rev	**Date**	***Description of Change of 7336429***	**Originator**
01	09 Jun 2016	Initial Release in Agile and assigned new number to 911-1235. (Removed obsolete sections and information; updated to reflect new test and fixturing methods; added Boundary Scan Sections; and removed Board Layout Information that is included in Document 990-1028.)	N/A
02	17 Jun 2017	Added Sections describing the Celestica and Foxconn Level 2 ICT DFT Reports. Added Information describing how to determine if a dedicated Boundary Scan Fixture is needed or Boundary Scan can be implemented on the ICT Fixture	N/A
03	06 Nov 2017	Added Sections Describing the Level 2 ICT DFT Report. Added Section Describing the ICT vs Boundary Scan Fixture Decision Process	N/A
04	01 Aug 2022	Added 1.4 I2C Devices. Update title. Update to Oracle Redwood format.	N/A
05	11 March 2024	Updated IEEE links. Removed broken links. Added Message format Best Practice section.	N/A

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