ORACLE

Fabrication Specification – Printed Wiring Boards

Document Number and Revision: 950-1009-19 Rev 60

Overview

The purpose of this specification is to establish and define requirements for construction of rigid, flex, and rigid-flex printed wiring boards for Oracle. Failure to meet these requirements shall be basis for rejection or disqualification.

Audience

This document applies to printed wiring boards (PWB/PCB Fab) manufactured for Oracle Corporation, directly or indirectly through assembly external manufacturers (EMs).

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1. Scope and Purpose

1.1 This document applies to printed wiring boards (PWB/PCB Fab) manufactured for Oracle Corporation, directly or indirectly through assembly external manufacturers (EMs). The purpose of this specification is to establish and define requirements for construction of rigid, flex, and rigid-flex printed wiring boards for Oracle. Failure to meet these requirements shall be basis for rejection or disqualification.

2. Order of Precedence

2.1 When conflict exists between this specification, the board fabrication drawing, applicable specifications, Oracle's electronic design data, or the purchase order, the following order of precedence shall apply when not otherwise specified herein:

2.1.1 Purchase order or contract that includes waiver or deviation request items approved by Oracle Engineering (reference Appendix A), and may include non-functional receiving facility-specific requirements).
Note: Assembly EM facility-specific requirements such as paste-mask, plug-mask, and panelization requirements that are included or referenced shall be prioritized as 'applicable specifications' in section 2.1.5.

2.1.2 The Oracle electronic design data, and the requirements of Sections 3.0, 4.0, 6.0 and 8.0 of this specification. All outline and cut-out routing features that are not dimensioned on the fabrication drawing shall be determined by the electronic design data. Any and all discrepancies between the electronic design data and the fabrication drawing, or missing needed dimensions and/or tolerances, require notification and resolution by Oracle Engineering (reference Appendix A).

2.1.3 Fabrication Drawings
Any and all discrepancies between the fabrication drawing, any construction stack-up approved prior to receiving the fab drawing, and this specification require notification and resolution by Oracle Engineering (reference Appendix A).

2.1.4 This specification 950-1009-XX

2.1.5 Applicable specifications. Compliance with more stringent assembly EM (external manufacturer or sub-contractor) requirements that increase cost and/or reduce availability shall require prior approval by Oracle's applicable Supplier Sourcing Program Manager.

3. Product Change Notice

3.1 Major printed wiring board (PWB) manufacturing process, material, or equipment changes and/or changes that affect end product specifications (reference section 27) are not permitted when a board design data package is released for volume production.

3.2 All major printed wiring board manufacturing process, material, or equipment changes that potentially affect end product specifications (reference section 27) require prior documented approval by Oracle's applicable Supplier Sourcing Program Manager before they can be incorporated into an Oracle product. The manufacturer shall also notify Oracle's Supplier Sourcing Program Managers in compliance with Oracle's 'Product & Process Change Notice' (PPCN) procedure prior to any affected boards being shipped (reference section 5.2.4).

4. Waivers and Changes

4.1 Waivers and deviations related to the acceptance of a printed wiring board shall be documented. Oracle's cognizant Supplier Sourcing Program Manager will not honor verbal waivers.

4.2 Changes and deviations or waivers to a board design data package (electronic design data and fabrication drawing) may be requested by the printed wiring board manufacturer and/or board assembly subcontractor (assembly EM) for Oracle. These requests shall include a written description of each proposed design or drawing modification (examples: dielectric thickness, impedance requirement), and shall be submitted to Oracle's PC Design Engineering department by e-mail using the format provided in Appendix A (illustrations may be included as attachments). No product incorporating a deviation or waiver is to be shipped without prior documented authorization from Oracle's PC Design Engineering department.

4.3 Assembly EM-specific changes to the paste-mask artwork contained in the Oracle electronic design data may be made as directed by the cognizant assembly EM without the prior approval of Oracle. These changes do not affect the manufacture of the board prior to assembly.

4.4 If any proposed change, deviation or waiver would result in modifying the Oracle net data for a design, then the manufacturing facility shall include in the Appendix A formatted request that they submit for each applicable item; 'This modification will affect Oracle's design net data file.' If this item is subsequently approved by Oracle, the manufacturer shall not proceed until Oracle has provided a new net data file corresponding to this approved request.

5. Applicable Documents

5.1 The following specifications and standards become effective on date of the invitation for bid or as specified on the purchase order for a board design data package.

5.2 Oracle Documents List:

- The Oracle electronic design data packages shall be accessed by supplier facilities with an Oracle account from:
  - SecureSites (for pre-production data): https://securesites-prodapp.cec.ocp.oraclecloud.com/site/authsite/ENG_<Vendor name>_PCDES (for pre-production data)

- Fusion (for production data): https://eeho.fa.us2.oraclecloud.com/fscmUI/faces/FuseWelcome?_adf.no-new-window-redirect=true&_adf.ctrl-state=vsip0dmfc_110&_afrLoop=18412041969782856&_afrWindowMode=0&_afrWindowId=null&_afrFS=16&_afrMT=screen&_afrMFW=1412&_afrMFH=886&_afrMFDW=1920&_afrMFDH=1080&_afrMFC=8&_afrMFCI=0&_afrMFM=0&_afrMFR=96&_afrMFG=0&_afrMFS=0&_afrMFO=0 for the specified unique Oracle printed wiring board (PCB Fab) part number Oracle's fabrication drawing for unique printed wiring board.

- Oracle's Fabrication Specification - Printed Wiring Boards (950- 1009-XX).
- Oracle PPCN Procedure, 923-2465-XX, latest revision

5.3. Applicable 'IPC International, Inc.' documents, including latest Amendments.

5.3.1 IPC-S-100 Standards and Specification Manual

5.3.2 IPC-TM-650 Test Methods Manual

5.3.3 IPC-A-600 Acceptability of Printed Boards

5.3.4 IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards, Class B

5.3.5 IPC-4412 Specification for Finished Fabric Woven from 'E' Glass

5.3.6 IPC-4552 Specification for Electroless Nickel Immersion Gold (ENIG) Plating for Printed Circuit Boards

5.3.7 IPC-4553 Specification for Immersion Silver Plating for Printed Circuit Boards

5.3.8 IPC-4555 Specification for Organic Solderability (OSP) Finish for Printed Circuit Boards

5.3.9 IPC-4562 Metal Foil for Printed Board Applications

5.3.10 IPC-5703 Cleanliness Guidelines for Printed Board Fabricators

5.3.11 IPC-6011 Generic Performance Specification for Rigid Printed Boards

5.3.12 IPC-6013 Qualification and Performance Specification for Flexible Printed Wiring Boards

5.3.13 IPC-2221 Design Standard for Printed Wiring Boards

5.3.14 J-STD-003 Solderability Tests for Printed Boards

5.3.15 IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

5.3.16 IPC-BP-421 General Specification for Rigid Printed Board Backplanes with Press-Fit Contacts

5.3.17 IPC-4103 Specification for Plastic Substrates, Clad or Unclad, for High Speed / High Frequency Interconnection

5.3.18 J-STD-004 Requirements for Soldering Fluxes

5.3.19 J-STD-005 Requirements for Soldering Pastes

5.3.20 J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

5.3.21 IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

5.3.22 IPC-2141 Controlled Impedance Circuit Boards and High Speed Logic Design

5.3.23 IPC-5704 Cleanliness Requirements for Unpopulated Printed Boards

5.3.24 IPC-1601 Printed Board Handling and Storage Guidelines

5.3.25 IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

5.4 Underwriters Laboratory Documents

5.4.1 UL-Recognized Components Index

5.4.2 UL-94 Tests for Flammability of Plastic Materials

5.4.3 UL-746 Polymeric Materials

5.4.4 UL-796 Printed Wiring Boards

5.5 Society of Automotive Engineers & American Metallurgical Society Documents

5.5.1 SAE-AMS-QQ-N-290 Nickel Plating Electrodeposited

5.5.2 SAE-AMS-P-81728 Plating, Tin-Lead, Electrodeposited

5.5.3 SAE-AMS-2418 Copper Plating

5.6 Military Specifications and Standards Documents

- **Note: The use of these documents as multilayer information should in no manner imply that the printed wiring will be used in a military environment.**

5.6.1 MIL-G-45204 Gold Plating, Electrodeposited

5.7 American National Standard Institute Documents

5.7.1 ANSI/ASME Y14.5M Dimension and Tolerance

5.7.2 ANSI Y32.16 Reference Designations

5.8. National Electrical Manufacturers Association Documents

5.8.1 L11-1998 Industrial Laminated Thermosetting Products

5.8.2 L1-4 Test Method for Hot Peel Strength at Equilibrium Temperatures

5.8.3 NEMA 29.3 The manufacturer shall maintain for one year cross-section specimens representative of the processes employed to manufacture printed wiring boards.

5.9 American Society for Testing and Materials Documents

5.9.1 ASTM D 257 DC Resistance or Conductance of Insulating Materials

5.9.2 ASTM B 193 Method of Testing for Resistivity of Electrical Conductor Materials

5.9.3 ASTM D 150-70 Loss Characteristics and Dielectric Constant (Permittivity) of Solid Electrical Insulating Materials

5.9.4 ASTM D 696 Methods of Test for Coefficient of Linear Thermal Expansion of Plastics

5.9.5 ASTM-E-53 Methods for Chemical Analysis of Copper

6. Oracle Supplied Documentation

6.1 Printed wiring board part documentation is generated as it appears looking through the board from layer one, the primary component side. Note: All pre-production printed wiring board design data packages must be received directly from Oracle's designated **'SecureSites'** for that manufacturer.

6.2 Oracle's design data package files are typically in ODB++ format, including embedded aperture format, as the primary source for the aperture lists. Should layer files not have an embedded aperture format, the manufacturer shall use the contents file to generate an aperture wheel for these layer files. The printed wiring board manufacturer shall notify Oracle's PC Design Engineering department when the contents file is used for apertures.

6.3 The board documentation package may contain ODB++ format electronic data file with aperture list, fabrication drawing (Acroread/.pdf, HPGL or RS-274x or RS-274D format) and:

- README.html
- Drill data
- IPC netlist
- Hi-Pot test table
- Special (if required); IST coupons, approved deviation report, CAF and/or other special coupons.

7. First Build and Production Lot Quality Report Cross-section Evaluation and Certification

7.1 All applicable section 7 items for each production lot shall be shipped in the same container (reference section 23), and/or included in an electronic quality report sent to Oracle's applicable Supplier Sourcing Program Manager. This documentation shall be provided at the time of the first shipment from each manufacturing facility, and for the first shipment made to any new Oracle-designated facility. First build documentation shall include:

a) Board stack-up and detailed construction used to meet impedance and Df (loss tangent) requirements.

b) 6X Thermal Stress testing (reference section 25.2) and cross-section evaluation results.

c) Section 24 requirements and a complete dimension check including board flatness measurements (reference section 24.1).

d) Verification of all part number specific requirements as listed on the fabrication drawing.

- **Note: Solderability test results and associated sample board shall be required as specified by Oracle's assembly subcontractor (assembly EM). Unless otherwise specified, if construction stack-up is in full compliance with the fabrication drawing then no other Oracle approval is required (reference section 8.2).**

7.2 For all multilayer boards, cross-sections shall be required to be held by the manufacturer for each new week year date code (reference sections 17 and 7.5) and part number shipped. All cross-section reports shall be identified by the vendor facility code, board part number, and week year date code. A 'first build' cross-section evaluation is required only in conjunction with the first lot of boards manufactured by the vendor for that part number. First build samples for microsectioning shall be taken from boards or coupons processed with production boards in the first lot manufactured of that part number. These first build microsection coupons shall be prepared and finely polished according to IPC-TM-650, Section 2.1.1, and made using low viscosity potting compound that does not shrink during cure (vacuum may also be used to ensure void-free encapsulation). First build documentation shall include the finished cross-section evaluation report which documents the dielectric thickness between each layer with cross-section photos showing all layers and the dielectric thicknesses between them. These are required for each new week-year date code, and shall be taken from a representative board manufactured in the first lot that is made with that week-year date code. Micro-etched cross-sections are required to accurately and clearly show the plated-through hole wall quality and the degree of etch-back at each interconnect (an interconnect is the area where an inner layer copper pad connects to the plated-through hole wall). The board from which samples for microsectioning are taken may also be used as a solder sample board. For all solder mask over bare copper (SMOBC) boards cross-section(s) showing the plated-through hole quality after the final surface metallization process shall not have been subject to additional thermal stress testing before microsectioning (reference section 24.1.1). For each date code a completed cross-section shall show inner layer connections on at least two component holes and at least one for each type of via hole. And a cross-section shall show at least one fine pitch surface mount device (SMD) land that accurately indicates the outer layer copper thickness.

7.3 Crosssection evaluation shall require 500x magnification cross-section photos to check for any separation, particularly for individual press-fit compliant pin connector holes both before and after simulated rework. Also appropriate magnification cross-section photo(s) of other plated-through hole types shall show:

- Inner Layer Annular Ring
- Trace Width
- Copper Wicking
- Inner Layer Copper Thickness
- Backdrill Stub Length
- Press-Fit Compliant Pin connector finished hole size
- LGA Pad Exposed Copper maximum distance in from edges
- Minimum Soldermask Thicknesses

7.4 A characteristic impedance report is required as part of the First Build and Production Lot documentation whenever the fabrication drawing includes controlled impedance requirements. Each impedance report shall show controlled impedance test results (reference section 20.3) and certify that the controlled impedance requirements have been met. Also, special controlled impedance testing shall be required when and as specified on the fabrication drawing or purchase order (example: for correlation of impedance test results). Impedance results shall be traceable to the manufacturer date code, and impedance reports shall be prepared and made available as required for each part number shipped.

7.5 Solder sample board, or approximate 50 x 50 mm (2 x 2 inch) solderability sample taken from the solder sample board used in section 7.1, shall be required with each new date code for each part number and/or new printed wiring board manufacturing facility, unless otherwise specified by the customer. The manufacturing facility shall test the sample board and evaluate according to IPC J-

STD-003 Section 4.2, including inspecting all pads and lands for sufficiently wetted copper. When the 50 x 50 mm (2 x 2 inches) solderability sample is used, the solder sample board from which it was taken shall also be shipped with the solderability sample. The shipment of the solderability sample and/or sample board for that date code shall constitute certification by the manufacturing facility that the J-STD-003 requirements have been met for that date code and part number.

7.6 All cross-sections, solderability and other part inspection test results shall reference the printed wiring board manufacturer's facility, part number and date code. The printed wiring board manufacturer shall keep for reference one cross-section for each part number and date code shipped for at least six months from the date of delivery. If cross-sections are kept for less than one year, then a complete set of photos of each of these cross-sections shall be kept for reference by the manufacturer for at least one year from the date of delivery.

7.7 The documented electrical parameters used for testing all bare boards in a lot, and the board quantity Hi-Pot tested, shall be included in each lot quality report. If any of the impedance and/or microsection coupons included with every working panel (not every board within an array) are defective or fail, then unless shown to be isolated to the coupon and an alternate coupon on the working panel exists (reference section 20.3.2) the manufacturer shall scrap the entire working panel and conduct 100 percent coupon inspection and evaluation of the remainder of the lot.

7.8 The printed wiring board manufacturing facility shall provide an EU-RoHS 'certification of conformance' (CoC), in .pdf file format, along with each first build lot quality report. Each EU-RoHS CoC shall include their company letterhead/brand/logo, authorized signature and date, the Oracle part number, the applicable EU-RoHS directive (example: EU Directive 2011/65) when stating that there are no exemptions to declare.

8. Front End Design and Film Requirements

8.1 The printed wiring board manufacturer shall inspect the board design data package and determine its acceptability for their manufacturing processing and this specification.

8.1.1 Acute angles shall be mitigated by the manufacturer adding up to 0.05 mm (0.002 inches) of copper fill-in and up to 0.10 mm (0.004 inches) in length, except on external layer area array pads or escape vias.

Instances of copper slivers between adjacent clearances be removed without prior approval by Oracle Engineering (reference Appendix A for notification and change request procedure) if width is less than 0.06 mm (0.0024 inches) for ½ oz copper layers, less than 0.075 mm (0.0030 inches) for 1 oz copper layers, less than 0.11 mm (0.0044 inches) for 2 oz copper layers.

8.1.2 In order to meet minimum annular ring requirements for plated-through holes, the manufacturing facility may add copper only where needed by reducing the associated split plane clearance locally, or by reducing clearance to adjacent copper where needed down to 0.25 mm (0.010 inches) minimum local copper clearance.

8.1.3 The manufacturing facility shall request tear-dropping or equivalent on internal layers if recommended using the procedure described in Appendix A. However, only Oracle shall generate all electronic design data for internal layers with tear-dropping.

8.1.4 Oracle design data that has retained non-functional unconnected pad on some layers are not to be removed.

8.2 All design-related issues, including any discrepancy between the electronic design data, the fabrication drawing, any pre-approved construction stack-up and this specification, shall require the manufacturer to notify Oracle's PC Design Engineering department. This notification shall be made using the procedure and format shown in Appendix A. If an issue could or will affect order delivery dates, the manufacturer shall also notify the board buyer/purchasing agent immediately.

8.3 The electronic design data shall be the determining standard with respect to the pattern information contained and location of same with respect to true grid positions.

8.4 The manufacturer shall create laser plotting files and in-house CAD/CAM data for use in their manufacturing processes as necessary to meet this specification. However, holes, pads and traces may not be moved from their original location as shown on the board design data package without prior authorization through Oracle's PC Design Engineering department (reference Appendix A).

8.5 Whether or not Oracle design data includes any tear-dropping or pad-slabbing, the manufacturer shall not add or remove any of these local inner layer and/or external trace width modifications at pad to trace connections unless otherwise specified on the fabrication drawing.

8.6 Changes to the external layer copper thieving not otherwise permitted within this specification may be requested using the procedure described in Appendix A.

8.7 Breakaways, panelization, cut-outs and other off-board areas may be used for a variety of PCB Fab and PCBA manufacturing purposes such as adding coupons, copper features to mitigate low pressure areas and improve resin flow during press lamination, and other features, only as permitted by the Oracle “OCE PCB CER Spec” (7300291-01, Section 1). Prior approval by Oracle Engineering is required (reference Appendix A) for the addition of any on-board features or adjustments of soldermask coverage, unless otherwise specified herein.

8.8 The addition of or changes to the use of copper filling on internal layers (similar to copper thieving on external layers) can be requested using the procedure described in Appendix A. However Oracle, not the printed wiring board supplier, shall generate all electronic design data for internal layers with copper filling.

8.9 Copper islands smaller than 0.13 x 0.13 mm (0.005 x 0.005 inches) on plane layers (completely cut off by adjacent hole clearances from the surrounding plane area) shall be removed. Sharp points or copper peninsulas caused by barely overlapping adjacent plane clearances shall be trimmed to have minimum 0.13 mm (0.005 inches) radius or width.

8.10 For sequential lamination boards, adding lands on subcomposite external layers is permitted.

8.11 For boards that require copper edge plating around the perimeter, where ground plane areas are less than 0.50 mm (0.020 inches) from the board edge, these areas may be extended to beyond the board edge to ensure connection to the edge plating.

8.12 When degrees of board rotation are specified on an Oracle printed wiring board drawing, the entire design image shall be rotated accordingly, including all associated impedance and other coupons required by Oracle. As viewed from Top/Layer One, the board shall be rotated from alignment with the specified laminate machine/grain direction in the clockwise direction, unless otherwise specified on the Oracle drawing.

8.13 The supplier shall conduct a thorough DFM (Design For Manufacturability) review and respond to Oracle using the Oracle PCB Design Technical Questions (TQ) process.

8.13.1 Oracle will upload the data package on the PCDES secure site or onto the Fusion, and inform the fabs by email._1st T.Q. response should be received within two business days from the date the data package was sent from Oracle. Oracle should respond within two business days for the 1st T.Q.

- If there is no 1st T.Q. item, fabs are still required to notify Oracle within two business days. Then, it will be considered the same as 1st T.Q. response. Otherwise, it will be considered as no 1st T.Q. submission.
- 2nd and 3rd T.Q. should be received within two business days from the date fabs received the 1st Oracle response. Oracle should also respond within two business days for the 2nd and 3rd T.Q. There will be no rating for 2nd and 3rd T.Q.
- T.Q. rating (Average) result shall be shared with fabs monthly. When the average is below satisfactory as requested by Oracle, corrective actions would be required from fabs.
  < 1st T.Q. Rating based on the T.Q. received date >
  T.Q. or notice ≤ Two days: 10 points/10 points
  T.Q. = Three days: 7 points/10 points
  T.Q. = Four days: 6 points/10 points
  T.Q. = Five days: 5 points/10 points
  No T.Q. submission or T.Q. ≥ Six days: 0 point/10 points

Outstanding (8 ≤ Average point ≤ 10)
Satisfactory (7 ≤ Average point < 8)
Poor(Average point < 7)

8.13.2 The quality of T.Q. will be rated separately. Rating will be implemented for both 1st and 2nd T.Q.

Rating	Given or No TQ item	Good catch > Unnecessary catch	Good catch < Unnecessary catch	General confirmation	Range
Point	+ 7	+ 3	- 3	+ 0	4 ~ 10

9. Material Requirements

9.1 Material Requirements for Multilayer Boards

9.1.1 Rigid printed wiring boards shall meet the flammability requirement class V-0 of the UL-94 Standard and shall have 130 C minimum 'relative thermal index' (RTI) rating for minimum 1.4 mm (0.055 inches) thickness as determined by UL-746B Standard. Rigid-flex and flexible circuits shall be flame class V-1 or VTM-1 minimum unless otherwise specified on the fabrication drawing.

9.1.2 All multilayer laminates and B-stage (prepreg) material shall conform to the applicable specification listed in section 5. When not prohibited by section 10.7 requirements, single-ply construction is permitted on engineering builds and for volume production after qualification. No change in single-ply construction is permitted during or after production release without prior qualification by Oracle.

9.1.3 The following limits apply unless otherwise specified on the printed wiring board drawing.

	GLASS FABRIC WEIGHT (IPC-4412)		RESIN CONTENT (WEIGHT PERCENT)	
	Min. Nominal	Max. Nominal	<0.1 mm Thick	<1.0 mm Thick
Single-ply Core	N/A	165 gm/m^2 (4.9 oz./yard2)	Min. 50%	Min. 47%
Single-ply Prepreq	47 gm/m^2 (1.4 oz./yard^2)	165 gm/m^2 (49 oz./yard^2)	Min. 50% before press lamination	Min. 50% before press lamination

9.1.4 Core & Prepreg Dielectric Construction Requirements: For stack-ups with single-ply, only 1078, 1080, 1035, and 1067 are allowed for the adjacent to the external layers.

- To prevent a Glass stop and to make sure enough resin is available to fill the etch copper and roughness, a minimum of 0.4 mil resin thickness (Butter coat 0.2 mil + Safety factor 0.2 mil) is required on top of the target minimum glass thickness after lamination (Refer to IPC-4412B Specification for Finished Fabric).

Glass style	Min Resin thickness adjacent to Layer N (mil)		Min Glass thickness(mil)	Min Resin thickness adjacent to Layer N (mil)		Total dielectric thickness (mil)
	Butter coat	Safety factor		Butter coat	Safety factor	
1035	0.20	0.20	1.10	0.20	0.20	1.90
1067	0.20	0.20	1.40	0.20	0.20	2.20
1078	0.20	0.20	1.70	0.20	0.20	2.50
1080	0.20	0.20	2.10	0.20	0.20	2.90

9.1.5 The dielectric material may be comprised of laminate, prepreg and laminate, or single or multiple plies of prepreg.

9.2 All printed wiring boards shall be constructed using UL recognized base materials, color concentrates, flame retardants, coatings, and other additives evaluated by UL and found suitable for use in the combined printed wiring board construction. Base materials shall meet the minimum direct support of current carrying parts criteria detailed in UL-746E Standard. Carbonized or partially cured laminates are not permitted. All FR-4 and FR-5 and non-ANSI laminate materials used require prior testing proving PLC = 3 or UL-CTI rating of 175 up to 250 volts for minimum 1.4 mm (0.055 inches) thickness.

9.3 The copper foil used shall meet the requirements of IPC-4562. Ductility shall be measured according to IPC-TM-650, Section 2.4.2.1, Flexural Fatigue and Ductility, Foil. IPC-4562 Type E minimum 15 percent elongation copper foil clad laminate on inner layers shall be required for boards exceeding 2.26 mm (0.089 inches) overall thickness glass-to-glass.

9.4 All flux used in the fabrication of the printed wiring board shall conform to the applicable specification listed in section 5, including complete removal of flux along with oil from boards after reflow. Flux used shall not contain any chlorides or Methane Sulphonic Acid (MSA).

9.5 IPC-6011 Class 2 shall apply or other applicable IPC specifications, unless otherwise specified herein. Laminate and bonding materials used in the manufacturing process shall meet the requirements of IPC-6011 Class 3 in IPC-6012 Section 3.2.

9.6 Starting copper foil for external layers and other external plated layers (example: sequential lamination) shall be Standard HTE Type E (IPC-4562), and nominal starting thickness shall not exceed 1/2 ounce (153 gm/m^2) on plated layers when not otherwise specified on the fabrication drawing.

9.7 Glass Transition Temperature (Tg) shall be measured using DSC or TMA (reference IPC-TM-650, Section 2.4) on a regular basis to ensure sufficient degree of cure after lamination.

9.8 Each homogeneous material used in manufacturing printed circuit boards for Oracle that remains with the board when shipped to the assembly EM and/or customer, excepting the primary board surface finish, shall not contain lead (Pb) at a concentration exceeding 0.1 percent by weight, nor cadmium(Cd) at a concentration exceeding 0.01 percent by weight, nor mercury(Hg) or hexavalent chromium(Cr+6) at a concentration exceeding 0.1 percent by weight of the homogeneous material, nor any FR720 (a.k.a. 'PE 68' or 'HP 800', the bis(2,3-dibromopropyl) ether of tetrabromobisphenol A). Reference: Directive 2002/95/EC

9.9 The use of 7628 style glass requires qualification and inspection as needed to ensure less than 10 hollow fibers per 10x10 cm^2 sample.

9.10 The laminate and prepreg material used shall not be manufactured with, and shall not contain the following substances:

- Polybrominated biphenyls (PBB) – CAS# 13654-09-6
- Pentabromodiphenyls (penta-BDE) – CAS# 32534-81-9
- Octabromodyphenyl (octa-BDE) – CAS# 32536-52-0
- Decabromodiphenyl (deca-BDE) – CAS# 1163-19-5
- Chlorinated paraffins

10. Inner Layer Requirements

10.1 Internal copper layers that are chemically treated to improve inner layer bond adhesion (reference IPC-6012, Section 3.3.2.5) shall use a low etch alternative oxide or similar treatment providing at least 0.25 um etch depth. All internal copper layers shall be reverse-treat copper foil, unless otherwise specified or approved by Oracle.

10.2 All through-hole clearance diameters (anti-pads) on finished external layers and on internal plane layers up to 2-oz thickness shall be within +0.050/-0.025 mm (+0.002/- 0.001 inches) of the Oracle design data. All internal plane layers as well as all signal layers require compensation for etch loss.

10.3 Inner layers shall be clean, dry, and kept free from all contamination before press lamination. Ionic cleanliness testing according to section 14.12 shall be done to ensure that cores prior to press

lamination (after treatment promoting adhesion) are in compliance with maximum 1.0 micrograms NaCl (0.6 ug chloride) equivalent per square centimeter of wetted surface or 6.45 micrograms NaCl (3.9 ug chloride) equivalent per square inch of wetted surface.

10.4 Conductor pattern requirements listed in section 12 apply to both inner layers and outer layers.

10.5 Inner layer copper foil peel strength at 125 degrees C shall be minimum 0.51 N/mm (2.9 lbs./inch) and peel strength test method is AABUS.

10.6 Cores made with up to 2-oz. copper plane layers shall have maximum 1.0 micrometers (39 micro-inches) copper surface roughness (Ra) on foil surfaces that contact prepreg and face an adjacent signal layer. Surface roughness shall be measured according to IPC-TM-650, Section 2.2.22, "Non-contact Metallic Foil Surface Topography/Texture."

10.7 Minimum 2-ply construction is required for all prepreg dielectric adjacent to inner layers with greater than 1-oz copper thickness. Single-ply construction is permitted for all core dielectric regardless of copper foil weight, except for dielectric adjacent to plane areas designated as AC voltage (power) on the fabrication drawing. AC voltage plane areas require minimum 2-ply construction for both adjacent core and prepreg dielectric, regardless of copper foil weight or thickness.

11. Drilled Hole Requirements

11.1 Hole dimensional requirements specified on the fabrication drawing apply to finished printed wiring boards, and shall not be deviated from without prior authorization by Oracle. For plated-through hole vias, the nominal finished hole size requirements shall apply to copper plating only. Finished gold over nickel plated-through via holes shall not be plated shut. Microvia requirements are specified in sections 11.10 and 13.3.

11.2 Drilled hole pattern accuracy on both sides of the board, including backdrilling, shall be within a true position diameter of 0.22 mm (0.0085 inches diametral), equivalent to +/- 0.076 mm (+/- 0.003 inches radial) positional tolerance. Except press-fit connector site plated-through holes shall have a true position diameter of 0.10 mm (0.004 inches diametral) when measured from the connector insertion side.

11.3 All plated-through holes shall be drilled without producing excessive resin smear or residue anywhere on the hole walls, then chemically and/or otherwise processed (example: plasma desmear) to minimize hole wall nodules and roughness, and to remove all residue and resin smear prior to plating the holes. Unless otherwise specified herein, all via holes shall meet the acceptance requirements of IPC- 6011 Class 2 in IPC-A-600 and all component holes shall meet the acceptance requirements of IPC-6011 Class 3 in IPC-A-600.

11.4 Maximum nail-heading for HTE copper foil layers shall be 300 percent for plated-through via holes, and 150 percent for component holes. Maximum nail-heading for non-HTE copper foil layers shall be 200 percent for plated-through via holes, and 150 percent for component holes.

11.5 All plated-through component hole sizes are after copper plating unless otherwise specified on the fabrication drawing. No drilling rework of undersized holes is permitted.

11.6 All finished plated-through hole diameters shall be measured perpendicular to the surface of the board using plug (PIN) gauges.

11.7 All drilled holes in multilayer boards shall be cut clean with no visible chipping, gouging, cracking, or extended fibers in the wall of the hole. For production boards all occurrences of broken drill bits within a board shall require the affected circuit board to be scrapped (rework is not allowed).

11.8 When optical precision drilled (OPD) holes are specified on the board fabrication drawing, then precision drilling of these holes is required using optical registration techniques in reference to their local fiducials. The local fiducials are aligned along either the X or Y axis with the precision hole locations noted in the drill data. However optical registration to the local fiducials, and not the drill data, shall be used for drilling these precision holes after all selective board finish plating is completed. The adjacent local fiducials for drilling the OPD holes are located 4.00 mm away from these precision non-plated-through holes (NPTH). The adjacent local fiducials shall be processed with the same gold over nickel finish as local LGA/CGA area or site and may subsequently have primary finish applied over the nickel for better optical registration. On finished boards, each precision hole shall be centered within 0.030 mm (0.0012 inches) of (X=4.00 mm, Y=0.00) or (X=0.00, Y=4.00 mm) as measured from the center of each corresponding local fiducial.

11.9 All microvias shall be laser-ablated rather than mechanically drilled and shall not be pierced (reference IPC-T-50). All microvias shall have a chemically etched copper clearance diameter at the entry surface at least 0.050 mm (0.002 inches) greater than the depth of the microvia target pad prior to laser-ablation, with clean sidewalls and minimal roughness. Default microvia finished hole size tolerance is +0.050 mm (+0.002 inches) / -[finished microvia hole size]. It is acceptable to use controlled UV or YAG (infrared) in addition to CO2 lasers for the ablation of microvias such as blind/skip vias.

11.10 The finished hole sizes that will be backdrilled are defined in the Hole Schedule on the Oracle part number fabrication drawing. There may be several tool numbers requiring the same drill size, but each requires a different backdrill depth. All backdrilled holes with finished hole size smaller than 0.012 inches diameter require primary hole wall surface roughness of no more than 0.0010 inches maximum peak-to-valley (maximum Rt). All backdrilled holes with 0.0060 inches or less backdrill-to-metal spacing require COPPER STRIPE testing (capacitance or backdrill AIO or X-ray method) before vacuum filling of these backdrilled holes with epoxy. Backdrill holes that are shallow (less than 0.014 inches in depth) shall have a minimum backdrill depth of 0.1 mm (0.004 inches) to completely remove just the external copper pad (landless), or only have reduced pad diameter of drill + 0.1 mm (0.004 inches) maximum. In either case Table 2 on the fab drawing shall not apply to these holes and no resin filling after backdrill is required.

12. Conductor Pattern Definitions, Registration Requirements and Defects

12.1 All printed wiring board features are defined by the 1:1 design data in the board design data package, except as otherwise specified herein. The manufacturer shall create their own working artworks and other tools based on their process etch factors and the other processing characteristics to ensure the compliance of the finished product to the board design data package and this specification (the determining standards).

12.2 All conductive pad and land patterns on external layers shall be manufactured with 0.15 mm (0.006 inches) true position tolerance or better. The conductive pads around component holes on external layers shall have minimum external annular ring of 0.040 mm (0.0016 inches) on the primary component side and 0.050 mm (0.002 inches) on the secondary component (bottom) side. All vias shall have an external annular ring of 0.025 mm (0.001 inches) minimum, which is equivalent to worst case tangency (not allowing breakout from external layer pads). Whether for component

holes or via holes, the definition of external annular ring includes the thickness of copper plating in the plated-through hole.

12.3 Internal conductive hole pads shall be sized and registered to the tolerance necessary to maintain an internal annular ring of 0.025 mm (0.001 inches) minimum, (foil only - exclusive of plated copper in the hole) for all component holes and via holes. However, all Oracle board design packages that have plated-through hole pads tear-dropped or otherwise elongated are permitted at those locations to have a minimum internal annular ring down to 0.0025 mm (0.0001 inches) except at the pad to trace junction

12.4 If the finished trace width, pad size, or land size is not otherwise specified on the fabrication drawing, the following limits shall apply.

- All impedance controlled traces on finished boards shall have nominal average width within +0.013/-0.025 mm (+0.0005/-0.0010 inches) of the design trace width as defined by Oracle's design data, requiring adjusting trace widths to compensate for etch loss. Trace width adjustments to better meet specified impedance requirements shall be consistently applied to all nets having the same primary aperture size within that layer. The manufacturer shall promptly notify Oracle's PC Design Engineering department when specified impedance requirements do not allow the above trace width requirements to be met (reference Appendix A for notification and change request procedure). For trace width neck-down segments, such as differential pair trace segments within pin fields, nominal trace widths of reduced width segments on finished boards shall be within +/- 0.013 mm (+/- 0.0005 inches) of the design trace width as defined by Oracle's design data. All non-impedance controlled trace widths on finished board internal layers shall be within +/- 0.013 mm (+/- 0.0005 inches) of the design trace width as defined by Oracle's design data.
- Reductions or nicks in the plated-through hole pad area are acceptable provided the reductions are less than 40 percent when compared with the design data, and that the reductions do not include pad damage or violation of minimum annular ring requirements.
- Protrusions from copper pads, traces, and lands shall not exceed 0.030 mm (0.0012 inches) as measured at the base of the conductor.
- Finished plated-through hole pad diameters, when compared with Oracle's design data, shall not be increased by more than 0.10 mm (0.004 inches) without prior approval by Oracle Engineering (reference Appendix A). External layer pads that will be backdrilled may have external layer entry pad diameter reduced to facilitate copper removal during backdrilling, and may have soldermask clearance diameter increased up to 0.10 mm larger than the backdrill drill bit diameter to permit inspection.
- Finished surface mount device (SMD) land width tolerance for all devices with 0.63 mm (0.025 inches) pitch or less shall be +0.050/-0.025 mm (+0.002/-0.001 inches) as defined by the 1:1 design data, unless otherwise specified on the fabrication drawing. The +0.050/-0.025 mm (+0.002/-0.001 inches) requirement also applies to all BGA (or LGA or CGA) device lands and pads. SMD lands with greater than 0.63 mm (0.025 inches) pitch shall have finished width tolerance of +/- 0.050 mm (+/-0.002 inches).

12.5 Conductor characteristics shall meet the requirements of IPC-6011 Class 2 in IPC- 6012, unless otherwise specified herein.

12.6 On all power and ground planes, up to 0.050 mm (0.002 inches) breakout from thermal pads is allowed on all thermal pads making connection to that plane.

12.7 Hole break-out from pads is not allowed. Except maximum of 90 degrees break-out from annular ring is allowed on:

- External layers for vias embedded in 0.50 mm (0.020 inches) wide gold contact fingers.
- Via pads that are tear-dropped at the pad-to-trace junction (ref. IPC Class-2).

13. Plating Requirements

13.1 Compliance with plated-through hole and buried or interstitial via copper plating thickness specifications shall be based upon at least three representative measurements from each hole wall on at least three plated-through holes cross-sectioned in the machine direction (in line with glass fiber reinforcement) on representative board(s), and samples for microsectioning should not be taken from the more isolated circuit areas on a board.

13.2 Surface and hole copper plating of unfilled plated-through via holes, blind vias and microvias shall meet the requirements of IPC-6011 Class 2 in IPC-6012, latest revision. Surface and hole copper plating of all component holes, buried via cores, and filled and capped plated-through via holes and blind vias shall meet the requirements of IPC-6011 Class 3 in IPC-6012.

13.3 Copper plating shall meet the requirements of SAE-AMS-2418. The finished external layer copper thickness after plating (including copper foil thickness) shall meet the requirements of IPC-6011 Class 2 in IPC-6012, Section 3. Except on all finished external layers the trace center-line thickness shall be at least 0.035 mm (0.0014 inches) and shall not exceed 0.075 mm (0.003 inches) copper thickness (pads, lands, and perimeter grounding tracks are not included in this exception).

13.4 Connector site (example: VHDM press fit compliant pin) plated-through hole wall copper thickness shall be 0.025 mm (0.001 inches) minimum. Unless otherwise specified, copper thickness shall not exceed 0.060 mm (0.0024 inches) at any point along the plated-through hole wall.

13.5 Soldermask over bare copper on both sides of the board is required on all boards, and is a requirement regardless of the board finish used.

13.6 Prior to the application of primary board finish, boards shall be completely dry and exposed bare copper clean and free of ionic contaminants before coverage by one of the following:

- Organic Solderability Preservative (OSP) or Pre-Flux/Conversion Coating.
- Electrolytic nickel plating (usually followed by plating gold over the nickel) shall be electroplated nickel according to SAE-AMS-QQ-N-290, low stress type. Nickel or tin-nickel alloy plating shall ensure 1.3 micrometers (51 micro-inches) minimum average thickness in the center of plated-through holes, with no single reading below 1.0 micrometers (39 micro-inches) on plated-through hole walls.
- Selective electrolytic gold plating over nickel, whether using the conventional 'over-hang' process prior to copper etching or the 'body' plating process after copper etching which encapsulates the exposed copper features, shall be minimum 0.50 micrometers (20 micro-inches) thickness electroplated hard gold (MIL-G-45204, TYPE II) over nickel and no voids are permitted (reference IPC-TM-650, Section 2.3.24.2). Minimum nickel thickness on surface pads

and lands with no overhang is 2.5 micrometers (98 micro-inches). The selective surface finish demarcation lines shown on the fabrication drawing may or may not show the exact location, so the PCB Fab manufacturer shall relocate the demarcation line to selectively plate on both top and bottom sides in the same through-hole areas without any via pads having a mixed finish (should be entire OSP or entire Ni/Au). The manufacturer shall notify Oracle's PC Design Engineering department of any needed selective plating demarcation line changes according to section 8.2.

Contact pads that do have nickel overhang shall not exceed 0.01 mm (0.0004 inches) overhang and these specific lands require minimum nickel thickness of 3.8 micrometers (150 micro-inches).

- Organic Solderability Preservative (OSP) shall be used as the primary board finish when specified on the fabrication drawing, and unless otherwise specified shall meet all the requirements of IPC-4555. For qualification, the OSP finish used shall pass IPC-6011 Class 3 wetting balance testing and have category 3 coating durability to ensure a shelf life of 12 months (reference J-STD-003). Surface copper roughness shall be controlled and limited to ensure complete OSP coverage.

- Immersion Silver (ImAg) shall be used as the primary board finish when specified on the fabrication drawing, and unless otherwise specified shall meet all the requirements of IPC-4553. Finished thickness of immersion silver shall meet 4-sigma lower spec limit of 0.050 micrometers (2.0 micro-inches) minimum on BGA pads. Absolute maximum thickness of immersion silver finish shall not exceed 0.51 micrometers (20 micro-inches) on BGA pads. Boards with immersion silver primary surface finish require all via pads to be covered with soldermask if not via-in-pad, due to risk of corrosion in the field. For these board designs if any exposed copper or primary surface finish is not covered by paste-mask, then the PCB Fab supplier shall contact buyer and assembly EM for resolution. Rework by complete removal of silver and replacement with a new deposit over the base copper is not permitted. Rework for exposed copper due to electrical test pin damage or subsequent handling damage is not permitted.

- Immersion Tin (ImSn) shall be used as the primary board finish when specified on the fabrication drawing, and unless otherwise specified herein shall meet all the requirements of IPC-4554. Only immersion tin finishes that have an organic solderability preservative co-deposited with the tin, less than 1000 ppm copper, and conform to a finished thickness requirement of 1.25 +0.25/-0.45 micrometers (50 +10/-18 micro-inches) as determined by SERA are acceptable. Immersion tin coatings shall only be applied after 100 percent electrical testing, and there shall be no subsequent contact with any solderable surface through shipping.

- Electroplated hard gold over nickel shall be used as the primary board finish when specified on the fabrication drawing. This primary board finish shall be 0.18 +/- 0.10 micrometers (7.0 +/- 4.0 micro-inches) thickness electroplated hard gold (MIL-G-45204, TYPE II) over nickel (reference section 13.6.2) and no voids are permitted (reference IPC-TM-650, Section 2.3.24.2).

- Board surface finishes used shall not contain lead (Pb) at a concentration exceeding 0.1 percent by weight, nor cadmium (Cd) at a concentration exceeding 0.01 percent by weight, nor mercury or hexavalent chromium at a concentration exceeding 0.1 percent by weight in the homogeneous surface finish.

- Electroless Nickel Immersion Gold (ENIG) plating, when specified on the fabrication drawing, shall be used as the primary board finish after LPI SMOBC application. All requirements of IPC-4552 latest revision apply except;)a) No ENIG surface finish repair or rework of boards that fail IPC-4552 acceptance requirements is allowed and such material shall be scrapped, (b)

Backdrilling of ENIG-finished plated-through holes shall be done only after application of the ENIG surface finish.

13.7 Contact edge fingers shall be electroplated with hard gold over nickel and shall meet the requirements of IPC-6011 Class 2 in IPC-6012, unless otherwise specified on the fabrication drawing.

13.8 Thermal stress testing (reference sections 24.1.1 and 25.2) shall be performed regularly for evaluating the plating and the integrity of the board.

13.9 Exposed plated copper not coated by a solderability preservative or metal surface finish is not acceptable inside plated-through holes. Any exposed internal layer copper is not acceptable inside slots or inside non-plated-through holes. Plated-through holes where backdrilled require minimum 0.025 mm (0.0010 inches) undamaged dielectric adjacent to internal layer copper (both plane and signal layers). Exposed copper not coated by a solderability preservative or metal surface finish on external layers is not acceptable at trace-to-pad/land connections where the area of exposed copper on trace exceeds 0.13 mm (0.005 inches) in length, on SMD lands within the center 80 percent of the SMD land width, on BGA pads except within 0.080 mm (0.003 inches) of the perimeter, nor on gold over nickel plated pads and lands except as specified in section 24.2.

13.10 Copper plating solution elongation testing (reference IPC-TM-650, Section 2.4.18.1) on a regular basis shall ensure minimum 12 percent elongation on all boards.

14. Soldermask (Permanent Solder Resist) Requirements

14.1 Soldermask shall meet all requirements of both Class T and Class H (for high reliability applications) in IPC-SM-840 (Qualification and Performance of Permanent Solder Mask), and IPC-6011 Class 3 in IPC-A-600 Section 2.9, except that minimum average thickness over center of traces shall be 0.009 mm (0.00035 inches).

14.2 Secondary screened-on soldermask (plug-mask) may be required on component side BGA escape via pads for improved assembly reworkability, and/or on other plated-through via holes for other reasons that do not affect board function. Part number specific plug-mask location requirements provided by the assembly EM have precedence over Oracle's design data for plug-mask (reference section 2.1.1).

14.3 Liquid photoimageable (LPI) primary soldermask is required on both sides. The manufacturer's qualification of soldermask shall ensure that soldermask on finished printed wiring boards does not exceed gloss meter reading of 90 at 60 degree setting (glossy finish is not acceptable). Also soldermask undercut shall not exceed 0.020 mm (0.0008 inches) per side.

14.4 Soldermask on finished boards shall be compatible with common commercially used water and solvent based soldering and assembly cleaning systems. Unless otherwise specified, soldermask color shall be green or blue-green.

14.5 All outer layer traces within 0.25 mm (0.010 inches) of adjacent exposed solderable areas shall be fully encapsulated (covered) with soldermask. Soldermask outline may be adjusted by 0.051 mm (0.0020 inches) maximum to ensure full trace circuit encapsulation by soldermask adjacent to SMD lands on finished boards.

14.6 Soldermask on finished boards shall be fully cured. The use of sub-contractors for the application of soldermask requires prior approval by Oracle according to section 3. No soldermask stripping rework is permitted and any defective panels shall be scrapped.

14.7 All via pad soldermask clearance diameters which are smaller than the corresponding via pad diameter defined in the design data shall be processed to ensure finished boards have these via pad edges completely covered by primary soldermask. Probe test point vias and embedded vias shall not be plugged with second screen mask, and plated-through via holes may only be plugged from one side of the board. The manufacturer may adjust the size of plug-mask received as needed to ensure complete coverage of the underlying via pad. The manufacturer shall immediately notify Oracle's PC Design Engineering department of any discrepancies in the top and/or bottom plug-mask design data (reference Appendix A).

14.8 All test via pads (including probe point pads) and grounding strip surfaces shall be completely free of soldermask and legend (silkscreen) material.

14.9 The external layer pads of all component holes shall be completely free of soldermask and legend (silkscreen) material.

14.10 All metal-defined SMT lands shall be completely free of soldermask and legend (silkscreen) material. For SMT lands with some or all edges that are soldermask-defined, the soldermask design data clearance may be adjusted by up to 0.05 mm (0.002 inches) in order to ensure coverage with no soldermask to metal edge tangency along any SMT land edge. The soldermask design data clearance may also be adjusted by up to 0.05 mm (0.002 inches) to maintain 0.085 mm (0.0033 inches) minimum soldermask web, or to meet other section 14 requirements. However, for BGA pads with elongated or oval copper pads and partly or all soldermask-defined edges the round soldermask design data clearances shall be used as-is.

14.11 Supplier facility's printed wiring board manufacturing process shall meet ionic cleanliness requirement of maximum 1.0 micro-grams NaCl (0.6 ug chloride) equivalent per square centimeter or 6.45 micro-grams NaCl (3.9 ug chloride) equivalent per square inch both before and after soldermask application.

14.12 Ionic cleanliness of boards immediately before and after the application of soldermask shall be controlled by the manufacturer as a routine activity in process control as a requirement for obtaining and maintaining a qualified status. Ionic cleanliness shall be determined with an Omega Meter, Ionograph, or equivalent with a minimum extraction time of 15 minutes and using a 50:50 or 75:25 blend of isopropyl alcohol and water at 20 C minimum. The testing shall be on parts representative of the technology and density processed for Oracle's printed wiring board products. Ionic cleanliness testing as stated in section 14.11 shall be done to ensure ionic cleanliness on product immediately before soldermask application, and on finished product after solder or other board finish application and subsequent standard cleaning. Any ionic cleanliness test failure shall result in all affected product being either reworked or scrapped, and immediate correction of the process is required.

14.13 The preparation process for the application of soldermask may utilize particulate abrasive no larger than 0.090 mm (example: pumice), however the process and abrasive used shall have neutral pH and the preparation process shall not include any caustic, bleach, chlorine, strong acids or corrosive acids. After preparation both the exposed laminate buttercoat surface and the copper surfaces shall be completely dry and not excessively rough. The laminate surface shall have no weave exposure and the copper surface shall not have gouges or pockets that prevent a mild immersion finish from continuously depositing on exposed copper areas.

14.14 Blisters, bubbles and/or foreign material between soldermask and laminate shall not bridge or approach closer than 0.13 mm (0.005 inches) to conductive patterns.

14.15 Soldermask formulation shall not contain any brominated flame retardants, and nominal average elemental chloride (Cl-) content of soldermask (or solder resist) shall not exceed 1,000 ppm.

14.16 Soldermask operations are considered to be a critical process by Oracle. Therefore, soldermask material changes require prior approval by Oracle according to section 3.

14.17 Boards with OSP surface finish can use standard LPI soldermask where soldermask flowing into the blind/skip via can leave some exposed copper at the rim of the hole, which is permitted for easier debug probing after board assembly.

15. Legend Marking Requirements

15.1 The country marking is required on all boards and should be located underneath a large component assembly on the primary component side (top side) as indicated on the silkscreen/legend artwork. Each board shall be marked to indicate the country in which the printed wiring board was manufactured (examples: FAB MADE IN USA, FAB MADE IN SOUTH KOREA, FAB MADE IN JAPAN, FAB MADE IN TAIWAN, FAB MADE IN CHINA).

15.2 Mark the board's revision level (shown on the fabrication drawing) immediately after the etched board part number, using either etch or legend (silkscreen).

15.3 All legend markings shall be in accordance with UL recognized components index. The top and bottom of the printed wiring board may have individual nomenclature patterns.

15.4 Legend and marking ink used shall not contain lead(Pb) at a concentration exceeding 0.1 percent by weight of ink, nor cadmium(Cd) at a concentration exceeding 0.01 percent by weight of ink, nor mercury or hexavalent chromium at a concentration exceeding 0.1 percent by weight in the homogeneous legend or marking ink. Legend shall be non-porous, non-conductive, smooth, and contrasting (does not fade). The legend ink color shall be white when not otherwise specified on the fabrication drawing.

15.5 Legend ink shall not cover plated-through via holes or blind vias, and is not allowed on component hole pads or SMD lands. Manufacturer shall notify Oracle's PC Design Engineering department when removal of legend from these areas is required to meet this requirement. Overlapping legend markings or reduced legend legibility after ensuring minimum clearances are acceptable and do not require notification.

15.6 Legend (silkscreen) shall meet the acceptance requirements of IPC-6011 Class 2 in IPC-6012. The manufacturer shall use the board design data package for generating all legend/silkscreen (and soldermask) artwork and tooling. Width of marking line or clearance forming a character may be reduced or increased by up to 50 percent providing the character is legible. Legend silkscreen and marking character(s) shall be removed from outside the board perimeter and where not over soldermask as needed to meet minimum clearance requirements. If this is not sufficient, then prior approval is required using the procedure provided in Appendix A for notification of design data discrepancies or issues.

16. Dimensioning and Tolerance Requirements

16.1. All board edge dimensions given in millimeters, inches, and degrees shall have the following tolerances unless otherwise specified on the fabrication drawing. Geometric dimensions and tolerances on the fabrication drawing shall also have precedence over this specification.

16.1.1. All two place dimensions in inches (.xx) shall have a tolerance of +/- 0.010 inches except as noted in section 11.2.

16.1.2. All three place dimensions in inches (.xxx) shall have a tolerance of +/- 0.005 inches except as noted in section 11.2.

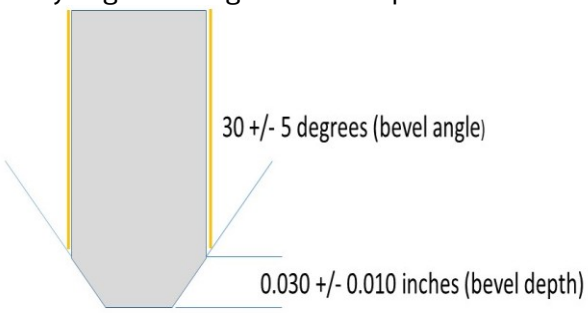
16.1.3. All angles shall have a tolerance of +/- 5 degrees (+/- 0.087 radians).

16.2. Overall board thickness is specified dielectric surface to dielectric surface exclusive of foil, plating, or soldermask. Any lack of compatibility with specified local area metal-to-metal thickness requirements requires notification of Oracle Engineering (reference Appendix A) for resolution. Specified core laminate material thickness tolerance requirements are according to IPC-4101 latest revision, Class C (IPC-6011).

16.3. Finished board thickness shall meet the dimensions specified at every point within given distance of the two edges of the board that fit into card cage guides (as specified on the fabrication drawing). Soldermask and legend (silkscreen) shall be moved in from the two edges and/or milling may be done to meet this requirement provided no circuitry is exposed.

16.4. Edge beveling shall meet the following default dimensional requirements when beveling is indicated on the fabrication drawing and not otherwise specified. Contact hard gold/nickel finished edge fingers which are not recessed can have their full width extended all the way to beveled edges to ensure that no visible tie bar remains. Recessed contact edge fingers cannot be extended, and if any have a remaining external layer tie-bar then removal with selective etch is required. Specified bevel angle and/or bevel depth requirements on the fabrication drawing shall have precedence and priority. Note: Inner layer tie-bars exposed by board perimeter routing are acceptable. Inner layer

tie-bars exposed by edge beveling are not acceptable.



17. Board Identification Requirements

17.1 Printed wiring boards shall have the following information marked in etched (or reverse etched) copper in the location(s) indicated on the fabrication and/or panelization drawing, or on the bottom side near the board edge when a location is not shown.

17.1.1 Manufacturer facility vendor logo, UL recognition logo or vendor ID marking, shall be etched in an area on the secondary component side in a location near the board part number. For small densely designed boards physically shipped multiple up in a working panel these markings may instead be located on each working panel. External layer copper thieving may be removed as needed to make room for these positive copper markings, however any negative imaged markings within an external copper plane area require prior approval by Oracle using the procedure provided in Appendix A.

17.1.2 The board part number shall be marked in etched copper on the bottom side as indicated in the board design data package.

17.1.3 Underwriters Laboratories (UL) printed wiring board 'type' designator.

17.2 All marking shall be permanent and in accordance with UL Recognized Components Directory.

17.3 Where direct current carrying capacity and/or corresponding parts support criteria are specified, as detailed in UL-746E Standard, the required UL symbol along with UL designator (logo) is required (reference UL-796 18A.1, 29.8).

17.4 The manufacturer date code, a week year date code or equivalent marking (example: DDD-y instead of WWYY) traceable to the week and year of manufacture, shall identify the week and year of manufacture that most closely matches the date when the boards were last electroplated with copper. This marking shall be in permanent ink or etched and should be located adjacent to the vendor logo.

18. Repairs during Fabrication and Rework

18.1 All board repairs shall meet the acceptance requirements of IPC-6011 Class 3 in IPC-6012 and IPC-7721, unless otherwise specified herein. Defective material not acceptable for repair shall be scrapped.

18.2 Only on external layers and if more than 2.54 mm (0.100 inches) away from connecting land or pad areas may traces with large nicks or opens be repaired.

18.3 Only on external layers may trace opens, if less than 1.50 mm (0.059 inches) in length, be repaired. Trace opens and large nicks may only be repaired by resistance welding.

18.4 The material used for resistance welding shall be 0.00 to 0.05 mm (0.000 to 0.002 inches) wider than the trace to be repaired.

18.5 Shorts may only be repaired by removing excess material. Conductive epoxy is not an acceptable material for repairs to the printed wiring board.

18.6 Boards with more than 3 repairable opens or large trace nicks on a single layer are unacceptable and shall be scrapped.

18.7 Nicks, cracks, or other localized reduction in trace width of less than 0.025 mm (0.001 inches) below average finished trace width (not design data) is acceptable. Printed wiring boards failing this requirement shall be either repaired or scrapped.

18.8 The printed wiring board manufacturer shall check with ohm-meter each resistance weld repair to ensure a finished resistance across the weld of less than one ohm.

18.9 The manufacturer shall not allow more than two immersion finish (OSP, immersion silver, immersion tin) process steps (maximum of one additional pass per board).

18.10 Printed wiring boards with over-etching of a plane layer are unacceptable and are not to be repaired (reference section 10.2).

18.11 Repairs on external layers and on buried via cores for opens, nicks, cracks, and local width reductions are not allowed.

18.12 Repairs to test traces and/or coupons are allowed for opens and shorts. However, repaired traces shall not be used for measuring impedance or other requirements for customer acceptance. Only representative and un-repaired test traces and/or coupon features shall be used for acceptance or special testing evaluations.

18.13 Cores shall not go through more than one pass through alternative oxide or equivalent low etch treatment prior to press lamination. No core panel rework through this process is permitted and any defective panel shall be scrapped.

18.14 All boards repaired for opens and/or shorts, whether for low or high resistance, require passing 100 percent full electrical test after any rework or repair. Rework or repair of finished boards with inner layer trace opens or shorts is not permitted, such boards shall be scrapped.

18.15 Rework or touch-up with tin-lead solder is not allowed.

18.16 Due to a work stoppage event; prior approval is required by Oracle in order to place in-process board production work on hold before completing press lamination, or after starting drilling and before completing electroless copper plating or a carbon-based direct plating process.

19. Solderability Requirements

19.1 All manufactured printed wiring boards shall meet the acceptance requirements of IPC-6011 Class 3 in IPC- 6012 for Dewetting and Nonwetting, and J-STD-003 Solderability Tests for Printed Boards. When 'J-STD-003 Solderability Test using SnAgCu Alloy' is specified on the fabrication drawing, the composition of the solder paste used shall be Sn96.5Ag3.0Cu0.5 (SAC305) according to J-STD-005, mesh size of -325/+500, and flux used shall be acidic type. Also for this SnAgCu surface evaluation a minimum of 90 percent of each of the surfaces being tested shall exhibit good wetting. The balance of the surface may contain only small pin holes, de-wetted areas, and rough spots provided such defects are not concentrated in one area. There shall be no non-wetting or exposed base metal within the evaluated area. An area of 3.2 mm (0.126 inches) width from the bottom edge of each test specimen shall not be evaluated. Areas contacted by fixtures shall not be evaluated. IPC 'Category III' shelf life is required (up to 12 months in original packaging).

19.2 The solderability requirements of section 19.1 apply to all printed wiring boards received at Oracle or Oracle's assembly subcontractor (assembly EM) for a period of 90 days after receipt.

19.3 Boards with a date code more than one year old shall not be shipped without specific prior documented approval by Oracle's applicable Supplier Sourcing Program Manager. Reference Oracle PCBA Workmanship Standard (910-1021).

19.4 Anti-tarnish material 'Silver Saver' or equivalent shall be used in the overall packaging of immersion silver finished boards.

20. Electrical Requirements

20.1 All boards shall have passed 100 percent finished printed wiring board electrical test (reference IPC-9252) at 100 Vdc test voltage using:

- maximum 10 ohms for continuity
- minimum 10 meg-ohm for isolation

Or at 200 Vdc test voltage using:

- maximum 20 ohms for continuity
- minimum 20 meg-ohm for isolation

All printed wiring boards and board panelizations to be shipped that pass this electrical test shall be stamped with an identifying permanent marking near the board part number identification on the bottom (solder) side of the board or panelization. In addition, boards that have failed electrical test and/or have been repaired shall meet the following requirements.

20.1.1 Test failures caused by wedge voids and/or entrapped plating or plating reagents (example: dielectric withstanding voltage test failure) are unacceptable and not to be repaired.

20.1.2 Finished boards with an open or short on any internal layer are unacceptable and not to be repaired.

20.1.3 Finished boards shall be re-tested (100 percent electrical test) after repair or rework for shorts or opens. Performance of 100 percent visual inspection of failed boards after repair or rework (including soldermask touch-up) is required before re-testing. The visual inspection of repaired or reworked boards shall include inspection for minimum external annular ring, exposed copper on SMD lands, contamination on SMD lands,

applicable section 24 acceptance requirements, and meet the requirements of IPC-6011 Class 2 in IPC-6012.

20.1.4 Locations with interconnect (pad-to-trace) resistance of 0.010 ohms or greater are unacceptable and not to be repaired (interconnect resistance measured at 25 C with a Kelvin type measuring instrument).

20.1.5 Each circuit that fails first-pass 100-percent-coverage electrical testing, and where a defective net is found to have a plated-through hole with front-to-back barrel resistance of 0.010 ohms or greater, is unacceptable and is not to be repaired. Barrel resistance shall be measured at 25 C with a Kelvin-type measuring instrument.

20.1.6 Shorts may only be repaired by removal of excess material. Drilling through dielectric and copper layers to remove excess conductive material (and then fill with resin) is not allowed (such material shall be scrapped).

20.1.7 Printed wiring boards with adjacent layer shorts that are caused by conductive fragments, nodules, lamination voids or processing reagents are unacceptable and not to be repaired.

20.1.8 Printed wiring boards with trace or pattern to barrel shorts due to misregistration are unacceptable and not to be repaired.

20.1.9 Finished copper thickness on all inner layer conductors shall meet the product requirements of IPC-6011 Class 3 in IPC-6012, Section 3.6.2.

20.1.10 Filled and capped plated-through holes and vias shall have finished copper thickness over the hole fill material meet the requirements of section 13.2, with no separation, and to meet this requirement no rework or repair is permitted. Finished surface dimple or depression shall not exceed 0.051 mm (0.002 inches). AOI failures for pinholes or excessive surface dimples requires board to be scrapped (no rework or repair involving cleaning with AL oxide, baking, or microetch).

20.2 Hi-Pot testing (high voltage testing) shall be required as follows on all multilayer boards.

20.2.1 Hi-Pot test requires a maximum 50 Vdc per second rate of rise to at least 500 VDC and held for 5 seconds minimum to verify 50 mega-ohms minimum continuous isolation between adjacent plane layers including split or isolated plane areas on adjacent layers (without causing damage to the electrical characteristics and/or reliability of the finished board). Where the dielectric thickness between adjacent power and ground planes is less than 0.051 mm (0.002 inches), then a minimum voltage bias of 100 VDC per 0.010 mm (0.0004 inches) dielectric thickness shall be used and the volt per second rate of rise shall be reduced accordingly to provide minimum 10 seconds to reach maximum voltage (control current loading).

20.2.2 Adjacent plane layers on finished boards, including small surface plane areas that carry voltage and split plane areas, may be Hi-Pot tested on a minimum 1.0 percent AQL and C=0 basis (minimum 20 parts per date code) only when:

a) All single-ply dielectric between layers is at least 0.08 mm (0.0032 inches) nominal thickness,

b) The finished boards have passed 100 percent electrical testing for shorts at 100 VDC or greater,

c) Where the electronic design data and fabrication drawing show no more than 12 volts differential between adjacent plane layers,

d) Board design does not have any layers carrying AC (alternating current). Otherwise all finished boards shall be 100 percent Hi-Pot tested.

- **Note: For boards manufactured multiple-up on a working panel and which are Hi-Pot tested while still panelized, if not individually tested then any Hi-Pot test failure requires that the entire working panel shall be scrapped, in addition to 100 percent Hi-Pot testing again being required of the entire production lot.**

20.2.3 Where the dielectric thickness between adjacent power and ground planes is less than 0.051 mm (0.002 inches), then a maximum 20 Vdc per second rate of rise shall be used instead of the default rate of rise (reference section 20.2.1).

20.2.4 No repair or rework of either cores or finished boards that fail Hi-Pot testing is allowed (such material shall be scrapped).

20.2.5 All boards that pass Hi-Pot testing shall be marked with an identifying permanent marking in a location on the bottom (solder) side that is free of surface metallization and does not reduce the solderability of plated-through holes or SMD lands.

20.2.6 Hi-Pot Test Table, when included on the fabrication drawing or associated test spreadsheet file, identifies the nets having the same voltage that may be grouped together for Hi-Pot testing. Grouping these nets together requires shorting all nets together, typically by using a dedicated electrical test fixture. The X-Y locations for Hi-Pot testing shown on the fabrication drawing or associated test spreadsheet file allows identification of each unique net to be tested; it is acceptable to use an alternate test point for a net. Combinations between Groups are then tested based upon the Hi-Pot Test Table. Combinations listed as 100 percent must be tested on every board. Combinations listed as AQL may be tested on a sample basis according to section 20.2.2. Using the grouped nets to only test the combinations specified in the Hi-Pot Test Table reduces the number of test combinations needed.

20.3. Impedance (TDR) testing shall meet the following requirements when trace impedance's are specified on the fabrication drawing.

20.3.1. Boards having controlled impedance requirements, except when on-board test traces are specified on the fabrication drawing, require the manufacturer to use off-board impedance test coupons with test traces, guard band traces, and dielectric thicknesses that result in impedances representative of the finished board areas on the working panel (reference IPC-2141). Strip-line impedance testing shall be done with both reference planes connected; either connected within the impedance coupon, or the test probe connects the two reference planes (Note: This type of test probe is required for on-board impedance test traces).

20.3.2. Boards with on-board controlled impedance (TDR) test traces may require impedance testing of each board in every production lot. Otherwise, a minimum of 10 randomly selected working panels per lot shall be tested for boards having controlled impedance requirements. Boards that do not have on-board impedance test traces require the use of off-board impedance coupons (at least two impedance coupons per working panel as described in section 7.7) and shall have test traces, guard band traces, and dielectric

thicknesses that result in impedances representative of finished board areas on the working panel. These impedance coupons when located in the center of a working panel should have TDR test results within +/- 1.0 ohms of impedance coupons located near the edge of a working panel. Production lots that show out of tolerance impedance readings shall have the defective layer(s) tested 100 percent. Traceability of the impedance test results to individual boards or panels is not required unless otherwise specified on the fabrication drawing.

20.3.3. Impedance measurements shall conform to IPC-TM-650, Section 2.5.5.7. The rise time of the TDR pulse as measured at the probe tip (not at the test port) from 10 percent to 90 percent point shall not exceed 200ps. TDR equipment should warm up for 60 minutes before calibration. TDR shall be calibrated at least once per year to reference impedance air lines which themselves are traceable to NIST or equivalent standard. Connection from test port to probe tip shall be made using 50 +/- 0.5 ohms coax cables, with cable connections made using torque wrench set at 5.0 inch/lbs of torque. Impedance requirements are single ended (not differential) unless otherwise specified on the fabrication drawing.

20.3.4. Single-ended impedance traces that are on the same layer as differential pair impedance traces and have nearly the same design trace width shall still require a different aperture size to allow making the different trace width adjustments as needed to better meet their different impedance specification. Any discrepancy requires notification of Oracle Engineering (reference Appendix A) for resolution. Non-impedance traces with the same nominal trace width as impedance traces shall have the same compensation for etch loss on a layer.

20.3.5. Specified impedance-controlled nets that have a designed nominal trace width of less than 0.10 mm (0.004 inches) shall require representative impedance coupon or on-board test trace testing of these characteristic width(s) on every working panel in volume production, unless otherwise specified on the fabrication drawing.

20.3.6. Differential impedance is twice the 'odd mode' impedance; defined as the impedance of a single transmission line when the two lines in a pair are driven differentially with simultaneous signals of the same amplitude and opposite polarity. It is critical to have exact edge alignment, same amplitude, and proper probe placement.

- Test Method 1: One Pulser and Two Samplers

  Ensure amplitude balance by inverting single Pulser output. Four contact pins; two for the (common) reference plane connections and one for each individual input line in the pair. The two lines shall be measured separately and the appropriate formula used to calculate the actual differential impedance. Any skew and/or attenuation must be accounted for on the non-inverted channel.

- Test Method 2: One Pulser and One Sampler

  Track imbalance is determined by measuring the single ended impedance of both tracks and then the parallel impedance of the two tracks is measured. The appropriate formula is used to calculate the actual differential impedance. Use Test Method 3 on a regular basis to verify accuracy of Test Method 2 (i.e., Man, Machine, and Method).

- Test Method 3: Two Pulser and Two Samplers

Test equipment calibration is required daily; adjusting loop gain for damping pulse response, set offset of TDR pulse for cable, phase align the TDR output edges and zero out the sampler offset, and exactly match amplitude from the two Pulsers (of opposite polarity) to within 2.0 percent. There are four contact pins; two for the (common) reference plane connections and one for each individual input line in the pair. The two lines shall be measured separately and the appropriate formula used to calculate the actual differential impedance.

20.4 When specified on the fabrication drawing the supplier shall add Oracle Delta-L 3.0 test coupon(s) to the working panel to be available for testing. Supplier shall add additional layers to the 8-layer basic coupon design between layers 4 and 5 as needed to match the applicable part number construction stack-up and mark each coupon with that part number and supplier facility's week-year date code.

20.4.1 Minimum five Delta-L test coupons with differential impedance pair traces on layers 3 and N-2 shall be tested per IPC-TM-650, 2.5.5, at 12 and/or 16 GHz for each production week-year date code during mass volume production.

20.4.2 The Delta-L test results for each part number shall be included in the supplier facility's monthly CTQ report sent to Oracle, and the coupons tested are to be stored for one month.

20.4.3 When specified, Delta-L testing during mass volume production of that part number is required to ensure all boards shipped are within +/- 5 percent dB/inch of the Oracle-approved value for that board part number.

21. Lamination Requirements

21.1 Acceptance requirements of IPC-6011 Class 2 in IPC-6012 and IPC-A-600 shall apply, unless otherwise specified herein. Laminate material qualification by the printed wiring board manufacturer shall include evaluations of conformance to specifications for degree of cure, moisture content, and 25 Vdc per 0.0010 inch minimum moisture insulation resistance.

21.2 Cracks, chips, dents, delamination or other visible separations of the laminate material caused by mechanical stress that come within 0.51 mm (0.020 inches) of any inner layer conducting media or intrude more than 0.51 mm (0.020 inches) from the board edge are not acceptable.

21.3 Lamination defects that develop before the first assembly reflow thermal excursion (paste and reflow or wave soldering) of the board (may include baking at 120 C (250 F) for 3 hours) are the responsibility of the printed wiring board manufacturer.

21.4 The standard Foil Lamination process shall be used unless otherwise specified on the fabrication drawing. The use of Core Lamination (or CAP construction) process requires prior approval of deviation by Oracle Engineering (reference Appendix A) including identification of alternate dark background areas for board fiducials.

22. Plated Hole Defects

22.1 Any area in a plated-through hole, filled or unfilled plated-through via hole, blind via, or buried via hole, where the thickness of plated copper in the hole is less than the minimum requirements of IPC-6011 Class 2 in IPC-6012, shall be considered a plating void.

22.2 Each plated-through hole, including plated-through via holes, shall not exhibit more than three plating voids. The combined length of voids within a plated-through hole shall not exceed 20 percent of the total plated-through hole wall length.

22.3 The combined area of the voids shall not exceed 10% of the surface area of the total barrel surface.

22.4 Plating voids within 0.013 mm (0.0005 inches) of the barrel to internal conductor interface are unacceptable.

22.5 Plating voids or separations on finished boards that exceed 90 degrees or 25 percent of the circumference of a plated-through hole are unacceptable.

22.6 Circumferential voids of any size are unacceptable. Pinholes or sites with less than 0.00020 inches electroplated copper thickness within component plated-through holes are unacceptable.

22.7 Copper plating thickness variation within plated-through holes between 0.50 mm and 2.00 mm in diameter shall not exceed +/- 0.010 mm (+/- 0.0004 inches). Copper plating folds and/or roughness of the plated-through hole wall which reduce solder thickness sufficient to expose copper or entrap plating reagents are unacceptable.

22.8 Separation of plating from the hole wall (hole wall pull-away, resin recession, or resin voids) on finished boards before thermal stress testing shall not exceed 20 percent of the board thickness, nor 5 percent of all holes, and shall not make contact with the pad-to-hole interconnect.

22.9 There shall be no evidence of cracks in plating or lifted lands, pads, or traces before thermal stress testing.

22.10 Maximum negative etch-back is 0.013 mm (0.0005 inches) when measured at the internal copper foil to barrel interface.

22.11 Maximum average positive resin etch-back from edge of inner layer copper foil within 0.10 mm (0.004 inches) of the barrel interface with the adjacent common dielectric material used for prepreg and most cores in the construction stack-up is 0.013 mm (0.0005 inches).

22.12 Copper wicking or observed radial cracking shall not extend more than 0.051 mm (0.002 inches) out from the drilled hole wall of plated-through holes. The extent of copper wicking or radial cracking may be determined by using either polarized dark field light or white light, provided the metallograph operator/inspector has been trained and measures equivalent results.

22.13 All plated-through hole requirements shall meet the acceptance requirements of IPC-6011 Class 2 in IPC-6012 and IPC-A-600, unless otherwise specified herein.

22.14 Plated-through via holes filled with resin and pre-filled blind vias which then have a copper plated cap shall have fully adherent caps with no separation between the cap plating and the underlying copper. No voids are permitted between the cap plating and the underlying fill material. One void maximum within a filled hole is acceptable when the void is entirely within the resin fill material itself. Maximum depression is 0.051 mm (0.002 inches). Maximum convex bulge of copper pad is 0.025 mm (0.001 inches).

22.15 Maximum average positive resin etch-back from edge of alternate dielectric core material within 0.10 mm (0.004 inches) of the barrel interface with adjacent alternate dielectric material in hybrid laminate constructions is 0.02 mm (0.0008 inches).

23. Packing and Shipping

23.1 Prototype boards shall be either shrink wrapped or similar vacuum-assisted skin-packaging, or packaged for shipment in polyethylene bags with one board per bag and packaged flat in groups of up to 10 boards. All boards shall be packaged for storage and handling according to IPC-1601, sealed and taped to prevent movement, warpage and excessive moisture absorption.

23.2 All finished printed wiring boards for shipment shall be clean, dry, free of moisture, and cooled to room temperature before packing in containers each marked with the following information on one end and off to the side:

- The board part number, and only one part number is permitted within a box or package.
- Sequence shown for each shipping container (example: 1 of 2, 2 of 2).
- The date codes may be different within a shipment. However, boards with different date codes shall be bundled separately by date code if present within the same container.
- Each container containing certificate of conformance, cross-sections, solder samples, coupons, and/or TDR reports (impedance test results) shall be labeled “certification of conformance, cross-section, solder sample, coupon, TDR information enclosed” on the outside of the container before shipment.
- Packing slip shall indicate the purchase order number, the complete part number including revision level, and the number of shipping containers within the shipment. Mark container in the shipment that contains the packing slip.
- The printed wiring board manufacturer's bare board packaging material used shall be resistant to moisture absorption: Water Vapor Transmission (38 +/- 2 C, 95 +/- 5 percent RH) less than 0.010 gm/m^2 per day.

23.3 The use of loose and small packing material such as 'peanuts' or 'popcorn' is not acceptable.

23.4 Printed wiring boards shall not be stored, processed, or transported without intermediate packaging sufficient to protect the boards from damage. Packaging shall be clean, dry, and ensure storage of boards for at least six months without corrosion, visible fingerprints, excessive moisture absorption, mold, or loss of solderability (reference section 19).

23.5 All shipping boxes and containers shall have each corner protected with corrugated cardboard, foam tape, or Styrofoam sufficient to ensure against deterioration and physical damage during shipment handling and storage. The containers used shall meet 1378 kPa (200 psi) Mullen Burst Test rating and meet the requirements of consolidated freight classification rules in effect at the time of shipment. Container boxes shall not exceed 18 kg (40 pounds weight).

23.6 All OSP, immersion silver or immersion tin finished boards for production shall be vacuum-packed and sealed for protection against moisture and air-borne contamination, then packaged securely in an opaque reinforced box as described in section 23.4 without inducing warpage during

shipment. Any desiccant or moisture indicator card used shall not contact any board surface finish or metallization. Desiccant bags, gloves, and pH neutral separation sheets or any other material shipped with the boards shall not contain sulfur (maximum 50 ppm sulfur dioxide). Reference IPC-1601, Printed Board Handling and Storage Guidelines.

24. Acceptance

24.1 All printed wiring boards referencing this specification, and all boards manufactured from Oracle.

board design data, shall meet the acceptance criteria defined in this specification and as listed below:

24.1.1 Plated-through hole 'Structural Integrity' shall meet the requirements of IPC-6011 Class 2 in IPC-6012 Section 3.6 after thermal stress testing according to IPC-TM-650, Section 2.6.8 (Test Condition B) and Section 2.6.27. Except there shall be no evidence in the plated-through hole cross-sections of any cracking or columnar copper grain structure. Lifted lands shall be allowed after more than 3X thermal stress.

24.1.2 Acceptance requirements of IPC-6011 Class 2 in IPC-A-600 and IPC-6012 Section 3.3 shall apply, unless otherwise specified herein.

24.1.3 Bow and Twist (reference IPC-TM-650, Section 2.4.22) shall not exceed +/- 0.7 percent (+/- 0.007 inch-per-inch). Bending or baking of finished boards to meet this requirement is not permitted. Any change to glass style or board construction shall require a new process qualification concerning this requirement. Some of these warpage requirements are tighter than industry standards.

- Board flatness (bow and twist) measurement procedure: Board shall be placed on a flat granite table and be free-standing (board shall not be held down at any corner), once with the primary component side up and once with the secondary component side (bottom side) up.
- Board flatness (bow and twist) specification: Unless otherwise specified, no corner of a free-standing board shall have more than 1.78 mm (0.070 inches) clearance from the surface of the flat granite table when either side of the board is up.

24.1.4 All boards with QFN, organic BGA and/or organic LGA device sites shall not exceed +/- 0.5 percent (+/- 0.005 inch per inch) bow and twist. Within each QFN, organic BGA and/or organic LGA device area shall not exceed +/- 0.3 percent (+/- 0.003 inch per inch) bow and twist or maximum 0.20 mm (0.008 inches) coplanarity (example: shadow moiré). Within each ceramic BGA and/or ceramic LGA device area shall not exceed 0.3 percent (+/- 0.003 inch per inch) bow and twist or 0.13 mm (0.005 inches) coplanarity.

- Finished printed wiring boards shall be evaluated against the criteria of UL-94 Standard, and shall have at least 105 C 'maximum continuous use' or 'maximum operating temperature' (MOT) rating as determined by UL-796 standard when not otherwise specified on the fabrication drawing. Rigid boards meeting the above requirements are listed in the `ZPMV2' category of UL's Recognized Plastics Components Directory by manufacturer name and board type. Rigid-flex and flexible circuits meeting the above requirements are listed in the 'ZPXK2' category.

- Finished printed wiring boards shall meet minimum requirements of current carrying parts electrical and mechanical performance criteria as detailed in UL-796 Standard for Safety: Printed Wiring Boards, and as detailed in the 'ZPMV2' category of UL's Recognized Components Directory.
- The acceptability of defective parts or 'x-outs' within an array is determined by the assembly subcontractor (assembly EM) and Oracle's applicable Supplier Sourcing Program Manager.
- All board edges shall be routed and smooth (no burrs). Boards may not be punched, unless specified on the fabrication drawing.

24.2 Selective Electroplated Hard Gold over Nickel

24.2.1 Unless otherwise specified, the following requirements apply to all edge contact fingers, LGA pads, and any associated fiducial or other sites requiring minimum 0.50 micrometers (20 micro-inches) or more of hard gold finish over nickel as identified on the fabrication drawing.

24.2.2 The non-critical contact area for LGA or other selective gold body plated sites extends from the pad perimeter up to 0.08 mm (0.0032 inches) in from the perimeter of the pad. Therefore, from the center area of the pad out to within 0.08 mm (0.0032 inches) of the perimeter is the critical contact area.

24.2.3 In addition to 24.2.2 and for edge contact fingers only, the non-critical contact area shall be 25 percent starting from top of the edge contact finger (side opposite the board edge).

24.2.4 For the critical contact area on all electroplated gold over nickel finished pads and contact fingers;

- Residues are not acceptable if they are not removable with mild detergent aqueous cleaning solution (near-neutral pH, non-abrasive, no builder nor washing soda), and are not electrically conductive.
- Maximum of three electrical test probe marks (exposed nickel sites) are allowed provided there is no exposed copper and maximum dimension across any probe mark does not exceed 0.13 mm (0.005 inches).
- Scratches, pits and dents are not acceptable if nickel is exposed, except for edge contact fingers pits and dents shall also not exceed 0.13 mm (0.005 inches).
- No spots of solder allowed, except on LGA pads on the bottom side since the bottom side LGA pads are not a critical contact area.
- New process and process change qualifications shall require EDX and/or SEM on at least 20 selective hard gold over nickel sites per board, with FTIR analysis of any suspect areas found, to ensure no organic plating resist residue on finished boards.

24.2.5 For fiducials and non-critical contact areas on electroplated gold over nickel finished pads and contact fingers;

- Exposed copper is permitted up to 0.051 mm (0.002 inches) in from the perimeter. Otherwise, scratches, pits and dents are not acceptable if copper is exposed.

- Maximum dimension of any exposed nickel shall not exceed 0.13 mm (0.005 inches). Minimum nickel thickness is 2.5 mm (0.098 inches), unless otherwise specified herein.
- Scratches in non-critical contact area are allowed provided the underlying copper is not exposed.
- Spots of solder on gold pads or associated gold over nickel plated vias are not allowed without prior approval by Oracle's applicable Supplier Sourcing Program Manager, except where otherwise stated herein.

24.2.6 For both critical and non-critical contact areas on all electroplated gold over nickel finished pads and contact fingers;

- Foreign material is not acceptable when the height exceeds 0.051 mm (0.002 inches).
- Nodules in metallization are not acceptable when the height exceeds 0.051 mm (0.002 inches). If the height of a nodule is never more than its width or length, then this visual inspection determination can serve as alternative acceptance criteria.
- No separation between plated layers or between metallization and laminate material is allowed.
- Brush plating rework of gold-finished pads is allowed only for rework of nodules and scratches. Brush plating of gold directly over copper is not allowed.
- Tape test for plated gold over nickel adhesion shall be done on rework sites.
- Brush plating rework for other causes requires prior approval by Oracle Engineering (reference Appendix A).

Brush plating rework process qualification shall include tape test for plated gold over nickel adhesion, porosity test, and surface roughness profile.8. Burrs and other plated gold over nickel protrusions are acceptable if they do not extend more than 0.025 mm (0.001 inches) out from any selectively finished trace or contact land, and do not extend more than 0.051 mm (0.002 inches) out from the copper base of a contact edge finger pad.9. Dark oxidized copper residue may be on the surface of adjacent hard gold finished via pads as long as the via holes are clear of any debris.

25. Reliability Testing and Evaluation

25.1 At any time, multilayer boards may be checked for compliance to this specification and the acceptance requirements of IPC-6011 Class 2 in IPC-6012 for the following reliability tests at a certified independent lab facility, unless otherwise specified herein. On boards with 2.26 mm (0.089 inches) or more overall thickness, a preconditioning bake at 135 C (275 F) to 149 C (300 F) for 4 hours is permitted before regular or quarterly testing. All product sampling shall be zero acceptance (C=0) where a single failure or defect scraps the entire lot, unless additional sampling or 100 percent inspection and testing is done that effectively isolates the problem.

25.2 Minimum 3X Thermal Stress Test (reference IPC TM-650, Section 2.6.8). Each hole type shall be included in the evaluation (examples: blind, buried, and small plated-through holes), and plated-through component holes 1.0 to 1.5 mm (0.040 to 0.060 inches) in diameter shall also be micro sectioned and their cross-sections evaluated. Boards going through lead-free assembly processing shall be thermal stress tested at 288 C using hot oil or a representative reflow alloy that

does not cause excessive copper dissolution. The manufacturer shall regularly evaluate the small via plated-through holes and 1.0 to 1.5 mm component plated-through holes after 6X Thermal Stress Test for delamination and other defects according to section 24.1.1. If this fails the supplier shall perform root cause failure analysis and corrective action. A 3X Thermal Stress Test shall be performed and evaluated to ensure no defects and external layer pad lifting shall not exceed 0.050 mm (0.002 inches) from the laminate surface plane to the bottom edge of the lifted land (whether or not resin appears on the copper land after assembly rework simulation or bond strength testing). Together these constitute the minimum thermal stress test reliability requirement for product acceptance.

25.3 Edge dip solderability (reference IPC-TM-650, Section 2.4.12).

25.4 Plating adhesion according to IPC-TM-650, Section 2.4.1. Acceptance requires no evidence of any metal-to-metal plating separation or gaps.

25.5 Dielectric withstanding voltage (reference IPC-TM-650, Section 2.5.7).

25.6 Insulation resistance (reference IPC-TM-650, Section 2.6.3).

25.7 Thermal shock reliability testing of representative boards (board thickness and layer count) shall be performed when IST test data (reference section 25.12) is not available for process qualification. Oracle has reviewed and approved the APD-Oil-T-Shock and similar tests for this purpose. APD-Oil-T-Shock Reliability Test: Small diameter plated-through holes when subjected to 400 cycles liquid-liquid, -35 C to +125 C, 15 minute dwell time at each temperature, 30 +10/-20 seconds between baths, silicon oil (5 centistoke Dow Corning 200 fluid) medium for both baths, air-driven stirrer to ensure bath uniformity and fast equilibration time, daisy chain test patterns on each of minimum 24 sample boards tested shall include daisy chain of at least 200 of the smallest representative plated-through holes and each net shall not show more than 10 percent increase in resistance (APD-Oil-T-Shock Reliability Test).

25.8 Rework simulation and peel/bond strength testing (reference IPC-TM-650, Section 2.4). Peel strength of external layer copper foil at 125 C shall be minimum 0.70 N/mm (4.0 lbs/inch).

25.9 Copper ductility according to IPC-TM-650, Section 2.4.2.1, Flexural Fatigue and Ductility (for plating line qualification).

25.10 For process qualification, the SMD land and component holes shall meet finished solderability requirement of 0.10 N/m minimum wetting force after 155 C for 4 hours Aging Test (reference IEC 60068-2-54, ANSI J-STD-003).

25.11 Interconnect Stress Testing (IST) shall be required when specified on the fabrication drawing or as required for new manufacturing facility or material qualification testing. The manufacturer shall add each IST coupon specified to the working panel border, fabricate boards and IST coupons, perform testing, and complete data analysis as specified.

26. Manufacturer's Responsibility

26.1 The manufacturer shall employ the measures necessary to assure that printed wiring boards are manufactured to the requirements of this specification. The absence of a specific provision herein shall not excuse failure to provide multilayer boards that meet the highest quality standards of the printed wiring board manufacturing industry.

26.2 Oracle reserves the right to source inspect to any of the criteria specified herein to assure conformance, and may repeat any or all of the inspections and tests contained herein.

26.3 Printed wiring board cross-sections and associated records shall be traceable to the board part number, lot number, week, and year of manufacture, and shall be made available to Oracle upon request.

27. Major PWB Manufacturing Process, Material, and Equipment Changes

27.1 Major printed wiring board (PWB) manufacturing process, material, or equipment changes are changes that can potentially affect end product specifications and include the obsolescence or deletion of current process, material, or product offerings (reference section 3).

27.2 Includes the introduction of new production equipment:

- Drilling (broken drill bit detection, registration capability)
- Electrical Test (equipment, method, density)
- Hi-Pot Test (equipment, method)
- Impedance/TDR Test (equipment, method)

27.3 Includes major refurbishment of existing production equipment:

- Automatic Optical Inspection/AOI (equipment, I/L capability, O/L capability)
- Reference section 27.2.

27.4 Includes change in manufacturing facility location or major rearrangement of existing facilities.

27.5 Includes change in finished materials or sub-components (supplier or composition):

- Any change in laminate material manufacturing facility or change in laminate material composition requires prior approval by Oracle and qualification testing as required.
- Multilayer Board Construction (stack-up, number of plies between layers)
- Soldermask (manufacturing facility, type, application method or any other change in chemistry, material, process or equipment with possible impact on product form, fit, function or reliability).

27.6 Includes change in critical process materials or sub-components (supplier or composition):

- Inner Layers (chemistry, PEP method)
  - Pre-clean quality index including Micro-etch etch rate
- Copper Treatment Prior to Press Lamination (chemistry, supplier, method)
  - Oxide quality index including Micro-etch etch rate, and roughness (Rz, Ra, Rs, RMS) of Hoz after oxide treatment
- Copper Foil (supplier, copper foil type/roughness)
- Plating (process flow/method, chemistry)

- Desmear Process (plasma, sweller, permanganate chemistry, method)
- Electroless Copper Application Process (chemistry, method)
    - Electroless quality index including Micro-etch etch rate and electroless deposit thickness.
- Carbon-based Direct Plating Process (chemistry, method)
    - Quality index including Micro-etch etch rate, and deposit thickness.
- Mass Lamination (masslam)
- Laser Ablation Method (example: CO2)
- Epoxy fill (process flow/method)
- Soldermask pre-treatment (process flow/method)
- Soldermask (equipment, process flow/method)
- Surface finish method, and chemistry
    - Quality index including Micro-etch etch rate, and deposit thickness.
    - Surface Finish (example: OSP surface finish chemistry)

27.7 Includes change in source of any subcontracted components or manufacturing related services.

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PC Design Engineering Issue Report Form & Procedure

For all board PCB Fab design-related issues, and corresponding deviation and waiver requests and instructions, the following issue report information must be sent to, and approved through Oracle's PC Design Engineering department. The PC Design Engineering department contacts appropriate Oracle engineers for resolution. The PC Design Engineering department then provides Oracle's authorized response to the PCB Fab manufacturer.

The following formats are acceptable for attachments: PDF, GIF, BMP, PNG and JPEG.

PC Design Engineering E-Mail: pcbengineering_ww_grp@oracle.com

---------- FABRICATOR DEVIATION / HOLD NOTICE ----------

PCB Fab Manufacturer (Company Name & Facility Location) :

DATE: TIME:

CUSTOMER: ORACLE

PART NUMBER:

PCB FAB MFR. REF./TOOL#:

PCB FABRICATOR Primary Contact:

Phone#: E-Mail:

Alternate Contact:

Phone#: E-Mail:

ILLUSTRATIONS: ( ) NONE ( ) ATTACHED (Please provide before and after graphics)

---------- ASSEMBLER INFORMATION ----------

PC ASSEMBLY EM (Company Name & Facility Location) :

ASSEMBLER Contact Name:

Phone#: E-Mail:

---------- APPROVAL INFORMATION (optional) ----------

ASSEMBLY EM APPROVAL Contact Name: Date:

ASSEMBLY EM APPROVAL (completed as directed by Oracle PCB Fab Engineering):

( ) Not Applicable ( ) YES ( ) NO

---------- STATUS ----------

( ) JOB IS NOT ON HOLD

( ) JOB IS ON HOLD: DATE: TIME:

( ) JOB TAKEN OFF HOLD: DATE: TIME:

DEVIATION (List all part number specific deviation requests with as much detail as possible. Even if just asking for confirmation include a good description and details of the DFM issue, potential assembly issue, and/or other risk involved. The manufacturing facility generating the TQ issues shall identify each item as being either general or potentially specific to the manufacturing facility (proprietary). All attributes of the finished product affected by each deviation should be clearly stated):

1) QTY ____ LAYER(S) AFFECTED _____ XY LOCATIONS _____

2) QTY ____ LAYER(S) AFFECTED _____ XY LOCATIONS _____

3) QTY ____ LAYERS AFFECTED _____ XY LOCATIONS _____

RESOLUTION (List the best resolution to each deviation request with sufficient detail for complete and accurate implementation):

1)

2)

3)

28.Revision History

REV	ECO NO	DESCRIPTION	APPROVAL
50	E0000521	Production Release	Sep 2, 2010
51	E0013201	Production Release	Nov 8, 2012
52	E0035653	Production Release	Jul 25, 2017
53	E0052487	Production Release	Nov 8, 2019
54	E0055600	Production Release	Aug 24, 2021
55	E56377	AQP Reformat	Dec 2, 2021
56	E56475	Fix Beehive References, Add Page Breaks	Jan 18, 2022
57	E59795	Update: 7.1, 8.1.1, 8.1.2, 8.1.3, 9.1.1, 9.1.3, 9.1.4, 10.2, 11.10, 13.6, 13.9, 14.10, 15.6, 16.4, 18.16, 20.1, 22.7, 22.15, 24.1, 27.6	May 10, 2023
58	E61360	Update: 2.15, 7.5, 10.1, 11.9, 13.6, 14.17, 17.4, 19.3, 20.3.4, 27.6, Delete: 9.10, 12.4, 21.5, 22.4,	Oct 13, 2023
59	E63046	New: 8.13, Update: 9.1.4, 14.17	Aug 27, 2024
60	E63286	No content change. Fix numbers on table of contents. Remove redlines from Related Info section	Oct 3, 2024

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