

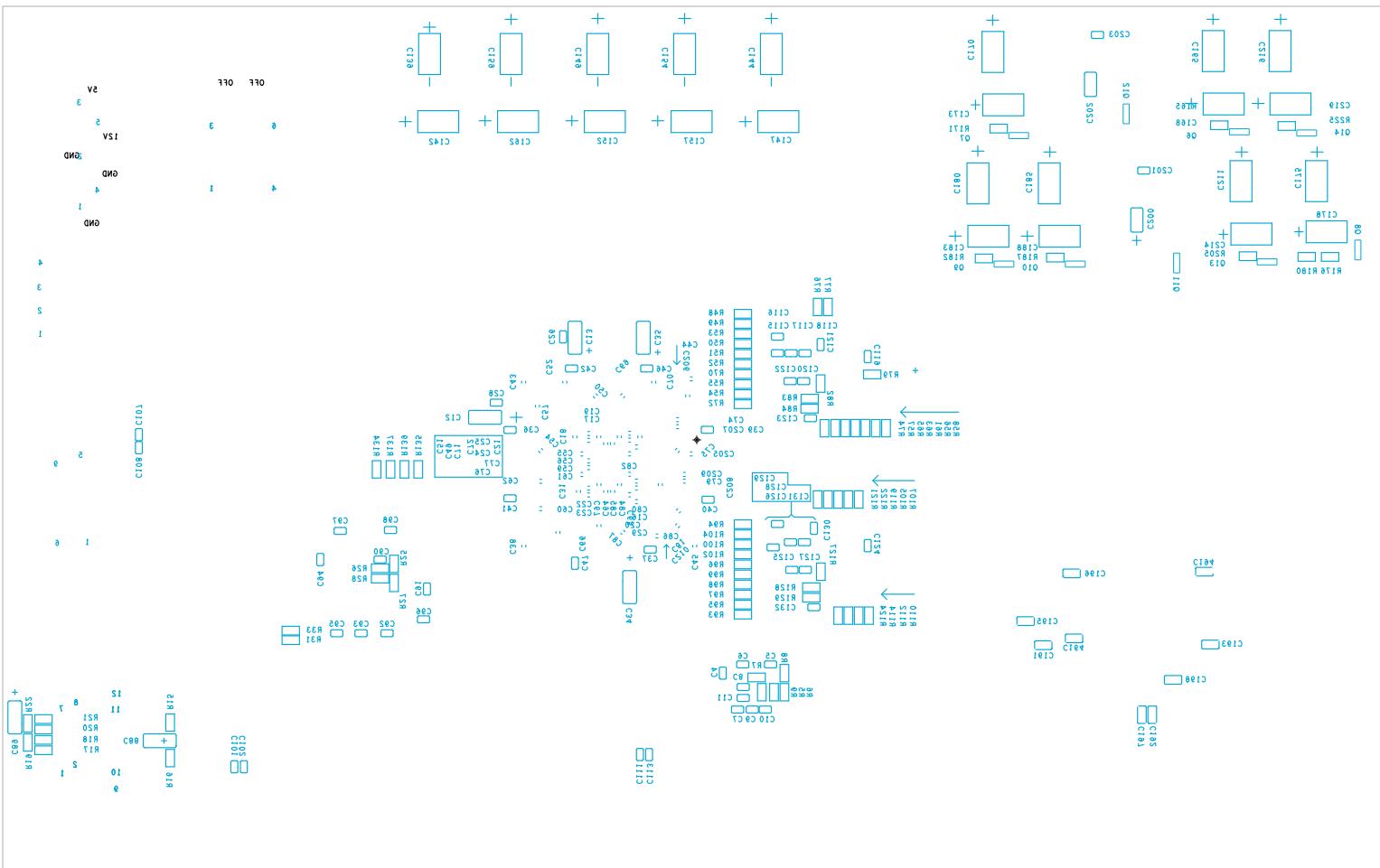
10 of 10

go Inc.

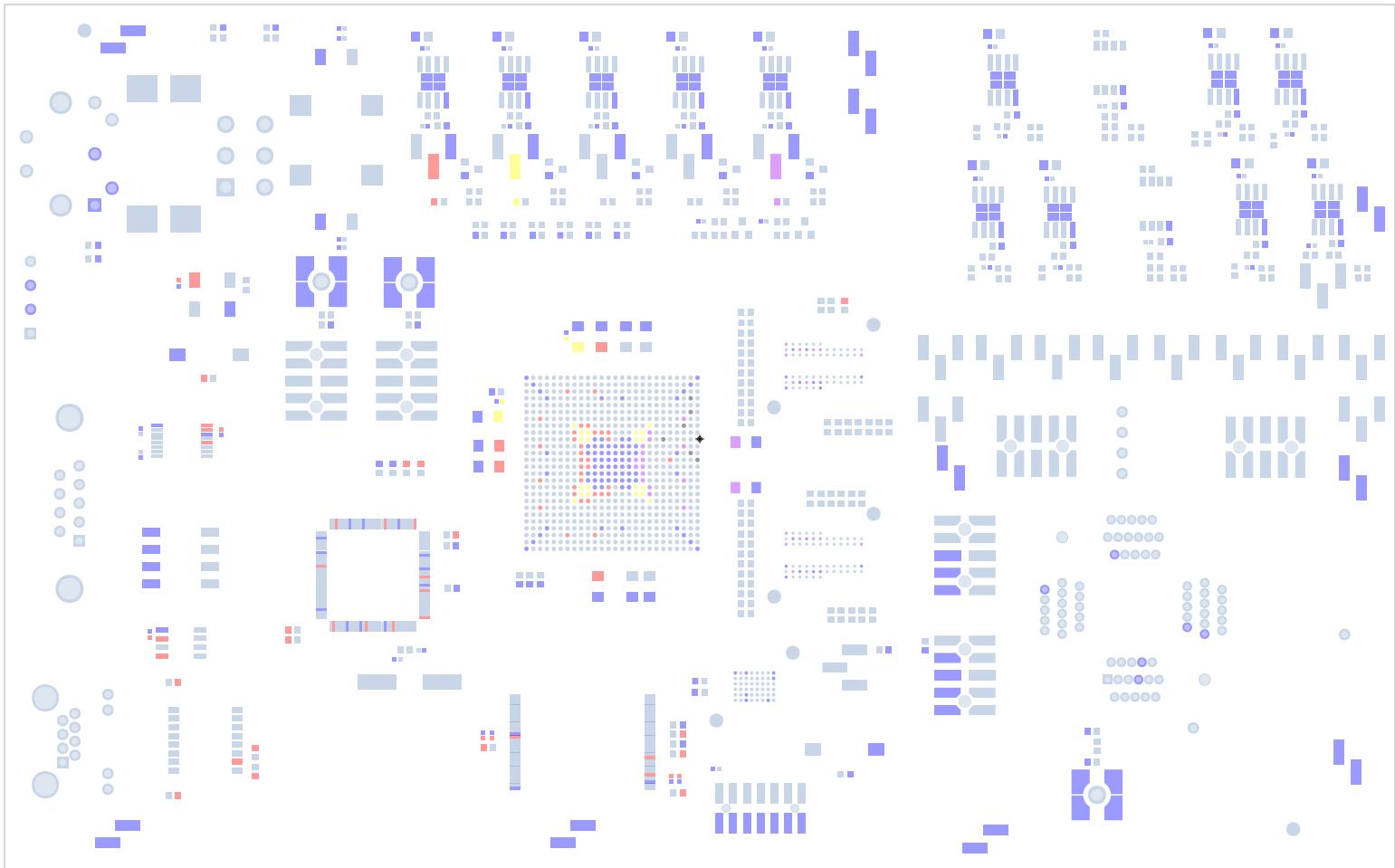
5 Totten Pond Road, Wa

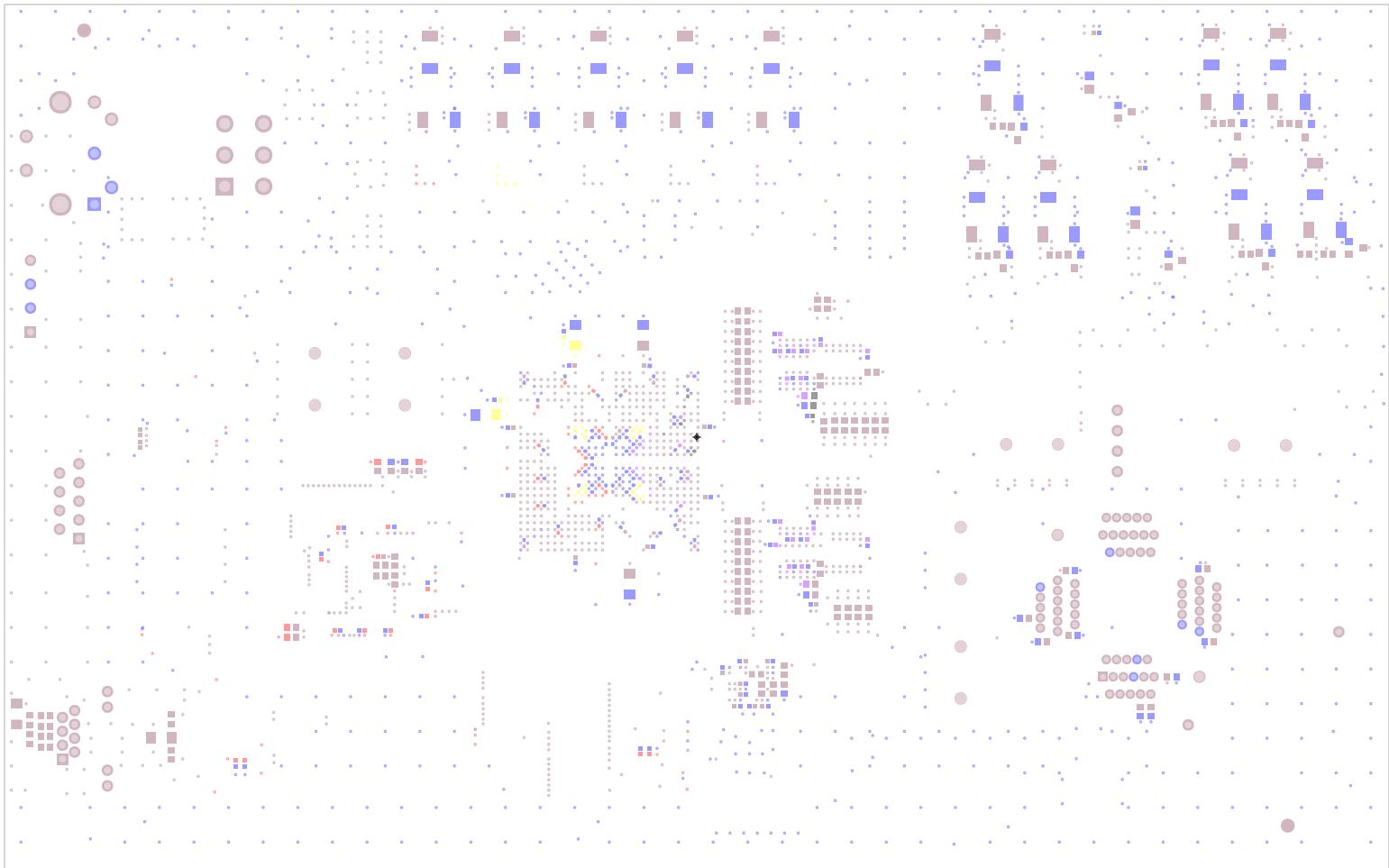
## **Diagnosis Validation/Evaluation**

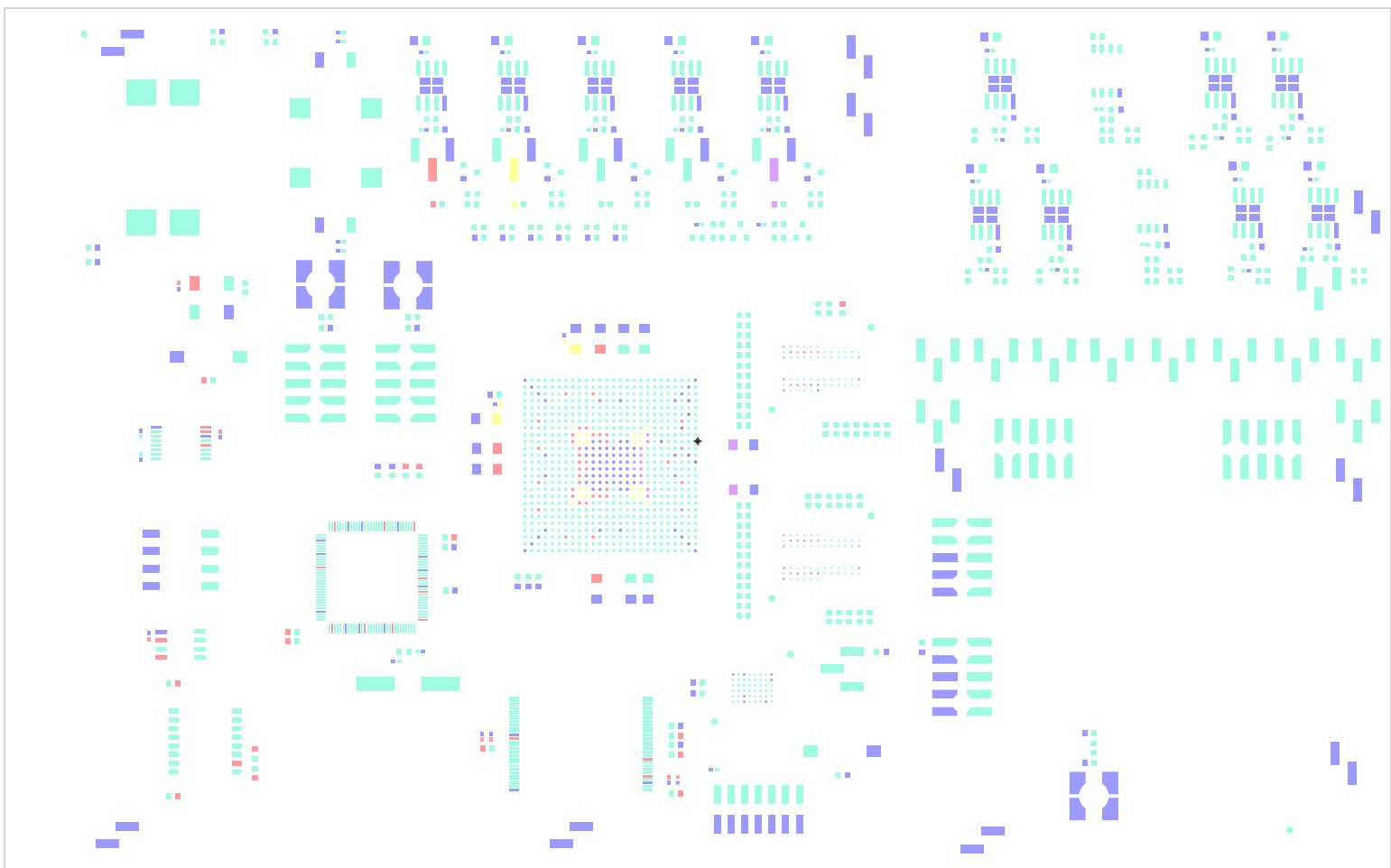
Made in USA, 2008 Tego

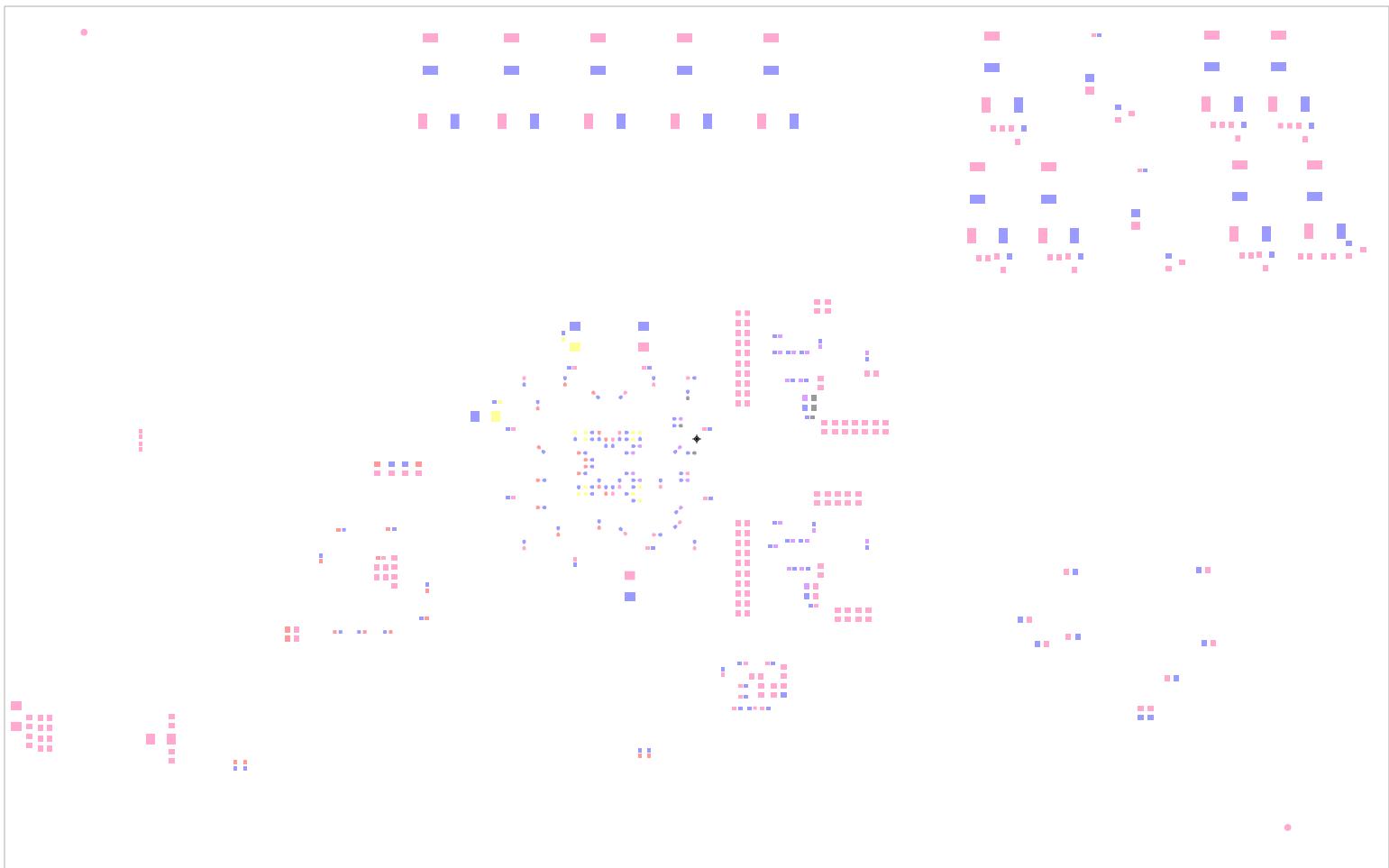


ART FILM - SILK\_BOTTOM









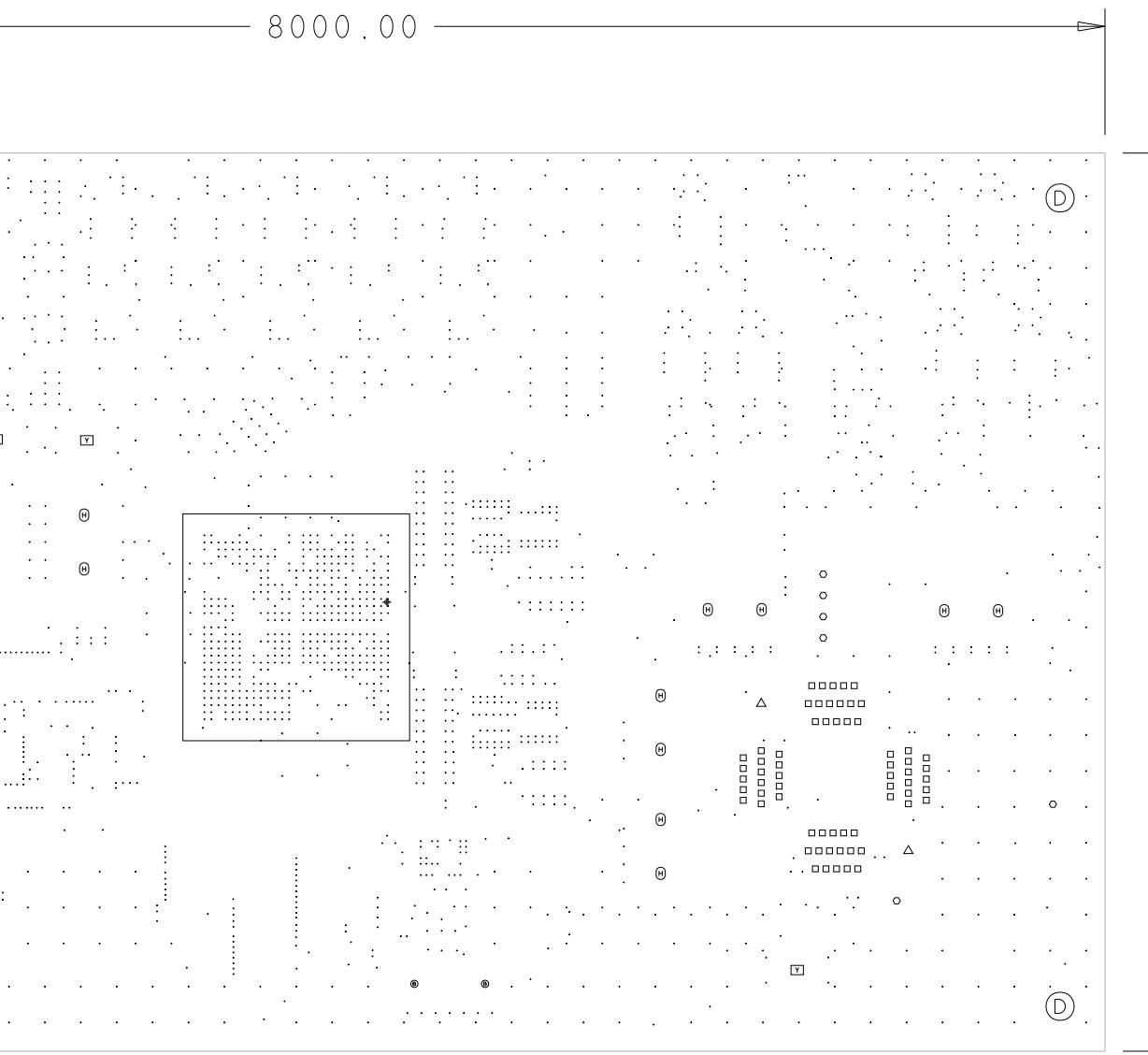
ART FILM - ASSY\_TOP

8000.00 -

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8000.00

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
.	10.0	+ 3.0 / - 3.0	PLATED	2692
□	32.7	+ 3.0 / - 3.0	PLATED	64
○	40.0	+ 3.0 / - 3.0	PLATED	22
○	41.0	+ 3.0 / - 3.0	PLATED	9
◊	52.0	+ 3.0 / - 3.0	PLATED	7
△	59.1	+ 3.0 / - 3.0	PLATED	2
○	65.0	+ 3.0 / - 3.0	PLATED	6
◎	68.0	+ 3.0 / - 3.0	PLATED	12
■	69.0	+ 3.0 / - 3.0	PLATED	3
⊗	95.0	+ 3.0 / - 3.0	PLATED	2
Ⓐ	125.0	+ 3.0 / - 3.0	PLATED	2
◎	40.0	+ 3.0 / - 3.0	NON-PLATED	2
Ⓒ	128.0	+ 3.0 / - 3.0	NON-PLATED	2
Ⓓ	156.0	+ 3.0 / - 3.0	NON-PLATED	4



FAB NOTES:UNLESS OTHERWISE SPECIFIED.

1. THE FINISHED PRINTED CIRCUIT BOARD SHALL MEET THE REQUIREMENTS OF IEC 60068-2-21 CLASS 2 AND 3000 GRADS.
  2. DIMENSIONING ON THE DRAWING SHALL BE CONTROLLED BY THE GERBER DATA.
  3. MATERIAL: .005 INCHES +/-10% THICK, NEMA GRADE GLASS/EPOXY, NATURAL COLOR. THIS PRINTED CIRCUIT BOARD WILL BE X LAYER.
  4. PLATING HOLE SIZES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH .001 INCHES COPPER MINIMUM. COPPER TO BE MEASURED AT THE CENTER OF VIA HOLE.
  5. ALL COPPER HOLES SHALL BE FINISHED WITH IMMERSION GOLD .0002 INCHES MIN.
  6. ALL HOLE'S DIMENSIONS ARE STATED AS FINISHED HOLE SIZES.
  7. FABRICATION TOLERANCES, END PROTRUDENCE, TRACE WIDTHS AND LANDS SHALL NOT VARY FROM THE GERBER DATA.
  8. SOLIDAREAS & PHOTO-MASKED TOTUVES, BOLUSES ON BOTH SIDE OF BOARD IN SOLDER MASK COLOR TO BE GREEN.
  9. COMPONENT MARKING AND TELSCREEN BOTH SIDES WITH WHITE NON CONDUCTIVE INK.
  10. BOW AND TWIST: SHALL NOT EXCEED .007 INCHES PER INCH.
  11. ELECTRICAL TEST: THE PRINTED CIRCUIT BOARD SHALL BE ELECTRICALLY TESTED FOR OPEN AND SHORT CIRCUITS. THE BOARD SHALL BE DOCUMENTED AND DELIVERED ALONG WITH EACH LOT.
  12. DEPICTED ON THE ENDOR LOGO TO BE ETCHED ON THE BOTTOM SIDE. ETCH THE LOGO ON THE TOP SIDE.
  13. THIEVING ALLOW ON OUTER AND INNER LAYERS. THIEVING SHOULD NOT BE OVERLAP READING TRACES AND PADS AT LEAST .25 MILS FROM ANY ADJACENT TRACES.
  14. ALL .001 MILS TRACE (FOR ALL LAYERS) SHOULD BE CONTROLLED TO 50 OHM +/- 10% (IF APPLICABLE).
  15. PLUG ALL VIA HOLES TO THE TOP SIDE OF BGA. (IF APPLICABLE)
  16. THE MINIMUM TRACE WIDTH:xx MILS. THE MINIMUM TRACE GAP:xx MILS.
- \*\*\*\*\*SPECIAL\*\*\*\*\*
17. VIA ON PAD:xx MILS VIA HOLES ON BGA PADS TO BE FILLED WITH CONDUCTIVE EPOXY (IF APPLICABLE)
  18. HARD GOLD IS PRIMARILY USED ON THE EDGE FINGERS. 25 MICRO INCHES MIN TO 30 MICRO INCHES MAX ON THE BGA. GOLD IS PLATED OVER 150 TO 200 MICRO INCHES OF NICKEL. (IF APPLICABLE)
  19. THERE ARE INTENTIONAL SHORT BY DESIGN ON:
  20. EDGE-COUPLE STRIPING 50 OHMS DIFFERENTIAL IMPEDANCE ON USB TRACES X.99 MILS WIDTH AND X.01 MILS SPACING

\*\*\*\*\* NOTE FOR VIAS IN PADS\*\*\*\*\*

- 1) Here is the fab note for via-in-pad.
- 'This design uses via-in-pad technology. The via holes (size = .xxx") shall be filled with conductive epoxy then planarized and plated over.'
- 2) And the note below is for vias inside the BGA but 'not' in pads.
- 'All vias inside the BGA areas, which have a hole size of .xxx", shall be filled with solder mask. Plug height and/or dimples shall not exceed the height of the plated pads.'

