SAED 14nm FinFET EDUCATIONAL DESIGN KIT

SAED_EDK14_FinFET

DATABOOK

Document #: SAED_EDK14_FinFET
Revision : 1.1
Technology : SAED14nm FinFET
Process : SAED14nm FinFET 1P9M 0.8v/1.5v/1.8v

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1. Introduction

This specification describes the basic technical requirements of the SAED_EDK14_FINFET Educational Design Kit (EDK).

1.1. Goal of EDK development

SAED_EDK14_FINFET will be designed to be free from intellectual property restrictions EDK and will be anticipated for the use in educational purposes aimed at training highly qualified specialists in the area of microelectronics in:

- SYNOPSYS Customer Education Services
- SYNOPSYS Global Technical Services
- Universities included in SYNOPSYS University Program

SAED_EDK14_FINFET is foreseen to support the trainees to better master:

- Advanced design methodologies
- Capabilities of SYNOPSYS tools.

For the use of EDK it is assumed that European or North American bundle of SYNOPSYS EDA tools is available to trainees.
SAED_EDK14_FINFET will be anticipated for designing different integrated circuits by the application of 14nm_FinFET technology and SYNOPSYS EDA tools.

1.2. Peculiarities of Low Power Design

During the development of SAED_EDK14_FINFET the possibility to apply state-of-the-art methods of low power design should be considered which are described in the [1,2].

1.3. Content of EDK

The content of SAED_EDK14_FINFET is shown in Table 1.1.

Table 1.1. Content of SAED_EDK14_FINFET

N	Name	Description
2	SAED_EDK14_FINFET_CORE	Digital Standard Cell Library
3	SAED_EDK14_FINFET_IO_STD	I/O Standard Cell Library (Wire-bond and Flip-Chip versions)
4	SAED_EDK14_FINFET_IO_SP	I/O Special Cell Library (Wire-bond and Flip-Chip versions)
5	SAED_EDK14_FINFET_RAM	Set of Memories
6	SAED_EDK14_FINFET_PLL	Phase Locked Loop
7	SAED_EDK14_FINFET_RAM_OS	OpenSPARC Megacells
8	SAED_EDK14_FINFET_ORCA	ORCA processor's reference design
9 10	SAED_EDK14_FINFET_ChipTop SAED_EDK14_FINFET_Leon3	ChipTop processor's reference design Leon3 processor's reference design
11	SAED_EDK14_FINFET_OpenSPARC	OpenSPARC processor's reference design

1.4. Methodology of getting technological files

For design of SAED14nm FinFET Educational Design Kit, abstract technology, simulation models will be generated recalling as a primary model the Predictive Technology Model

(PTM) developed by the Nanoscale Integration and Modeling Group (NIMO) of Arizona State University (ASU) (http://ptm.asu.edu/). The initial version of the model will be specified using FinFET device characteristics of [3, 4] item from open sources.

Layout design rules for SAED14nm_FinFET educational, abstract technology should be obtained by considering lithography requirements and restrictions for 14nm FinFET technology. Parasitics extraction deck will be formed using the models of parasitics estimation developed by NIMO group of ASU. Double patterning rules and also 14nm advanced rules supported by Synopsys IC Compiler Zroute router will be added.

Digital Standard Cell Library SAED_EDK14_FINFET_CORE will be built using SAED14nm FinFET technology. The library will be created aimed at optimizing the main characteristics of designed integrated circuits by its help. The library will include typical miscellaneous combinational and sequential logic cells for different drive strengths. Besides, the library will contain all the cells which are required for different styles of low power designs (multi-voltage,power gating, clock gating, multi-threshold, etc.).

I/O Standard Cell Library SAED_EDK14_FINFET_IO_STD will be built using SAED14nm FinFET technology. The library will include typical I/O cells which are necessary for integrated circuits design for educational purposes.

I/O Special Cell Library SAED_EDK14_FINFET_IO_SP will be built using SAED14nm FinFET technology according to specifications of corresponding special I/Os. The library will include commonly used special I/O cells.

Both Standard and Special I/O Cell Libraries will be developed in both wire-bond and flip chip versions enabling advanced designs in educational environment.

Set of Memories SAED_EDK14_FINFET_RAM will be built using SAED14nm FinFET technology. The set will include several RAMs of not large sizes which are necessary for integrated circuits design for educational purposes.

OpenSPARC Megacells SAED_EDK14_FINFET_RAM_OS will be designed using SAED14nm FinFET technology according to specification of OpenSPARC processor.

Phase Locked Loop SAED_EDK14_FINFET_PLL will be designed using SAED14nm FinFET technology and will be used for integrated circuits design for educational purposes.

ChipTop is a reference processor design which helps to get introduced to Synopsys design flow. It contains both design (.v, .sdc, .tcl, .upf), all setup (.setup) and other files needed to design the processor. ChipTop processor design must be created by all well known low-power techniques (multi voltage, power gating, clock gating, multi threshold, .etc) to be possible to compare all design versions in university enviroment.

ORCA is a reference processor design which helps to get introduced to Synopsys design flow. It contains both design files (.v, .sdc, .tcl, .upf) and all setup files (.setup) needed to design the processor.

Leon3 is a reference processor design which helps to get introduced to Synopsys design flow. It contains both design files (.v, .sdc, .tcl, .upf) and all setup files (.setup) needed to design the processor. Leon3 processor design must be created by all well known low-power

techniques (multi voltage, power gating, clock gating, multi threshold) to be possible to compare all design versions in university enviroment.

OpenSPARC is a reference processor design which helps to get introduced to Synopsys design flow. It contains both design files (.v, .sdc, .tcl, .upf) and all setup files (.setup) needed to design the processor.

2. Set of Memories SAED_EDK14_FINFET_RAM

2.1. Introduction

The SAED_EDK14_FINFET_RAM set of memories will be designed using SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V process. It will represent a set of several static RAMs (SRAMs) with small number of words (word depth – m) and bits in word (data width – n). All SRAMs, included in SAED_EDK14_FINFET_RAM, will represent Synchronous Dual-Port or Single-port SRAM with Write Enable, Output Enable, Chip Select port(s). Each SRAMmxn, included in the set, will have the same architecture and will differ from the rest with its nxm (width x depth) sizes. As SAED_EDK14_FINFET_RAM is anticipated for the use of educational purposes, only SRAMs of the sizes, shown in Table 5.1., will be included in it.

Table 2.1. SRAMmxn Cell List

No	Data width (n)	Word depth (m)	Address width ($k=\log_2 m$)	Cell Name
1	4	4	2	SRAM1RW4x4
2	8	4	2	SRAM1RW4x8
3	4	16	4	SRAM1RW16x4
4	8	16	4	SRAM1RW16x8
5	16	16	4	SRAM1RW16x16
6	32	16	4	SRAM1RW16x32
7	4	32	5	SRAM1RW32x4
8	8	32	5	SRAM1RW32x8
9	16	32	5	SRAM1RW32x16
10	32	32	5	SRAM1RW32x32
11	4	64	6	SRAM1RW64x4
12	8	64	6	SRAM1RW64x8
13	16	64	6	SRAM1RW64x16
14	32	64	6	SRAM1RW64x32
15	128	64	6	SRAM1RW64x128
16	4	128	7	SRAM1RW128x4
17	8	128	7	SRAM1RW128x8
18	16	128	7	SRAM1RW128x16
19	32	128	7	SRAM1RW128x32
20	8	256	8	SRAM1RW256x8
21	32	256	8	SRAM1RW256x32
22	128	256	8	SRAM1RW256x128
23	8	512	9	SRAM1RW512x8
24	32	512	9	SRAM1RW512x32
25	64	512	9	SRAM1RW512x64
26	128	512	9	SRAM1RW512x128
27	4	4	2	SRAM2RW4x4
28	8	4	2	SRAM2RW4x8
29	4	16	4	SRAM2RW16x4
30	8	16	4	SRAM2RW16x8
31	16	16	4	SRAM2RW16x16
32	32	16	4	SRAM2RW16x32
33	4	32	5	SRAM2RW32x4

No	Data width (n)	Word depth (m)	Address width ($k=\log_2 m$)	Cell Name
34	8	32	5	SRAM2RW32x8
35	16	32	5	SRAM2RW32x16
36	32	32	5	SRAM2RW32x32
37	4	64	6	SRAM2RW64x4
38	8	64	6	SRAM2RW64x8
39	16	64	6	SRAM2RW64x16
40	32	64	6	SRAM2RW64x32
41	128	64	6	SRAM2RW64x128
42	4	128	7	SRAM2RW128x4
43	8	128	7	SRAM2RW128x8
44	16	128	7	SRAM2RW128x16
45	32	128	7	SRAM2RW128x32
46	8	256	8	SRAM2RW256x8
47	32	256	8	SRAM2RW256x32
48	128	256	8	SRAM2RW256x128
49	8	512	9	SRAM2RW512x8
50	32	512	9	SRAM2RW512x32
51	64	512	9	SRAM2RW512x64
52	128	512	9	SRAM2RW512x128

2.2. SRAM naming conventions

All memories in the set are named according to the following template (Fig. 3.1):

SRAM***p***RW***nxw***

Figure 2.1. Memories naming template

The template contains symbols denoting specifics of the memory, the descriptions of the symbols are given in Table 3.1.

Table 2.2. Memories naming conventions

Symbol	Description	Values
p	Number of access ports	1,2
n	Number of words	Integer number, 2^n
w	Word size	Integer, various

2.3. General Information

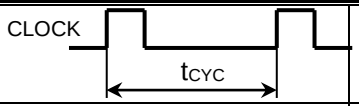
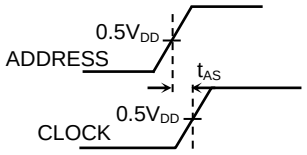
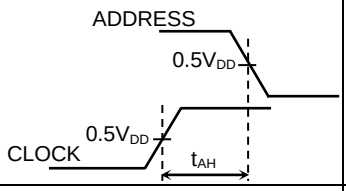
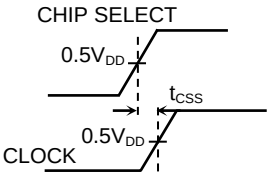
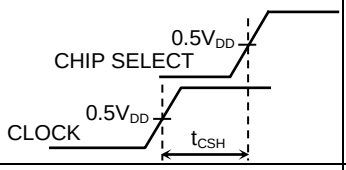
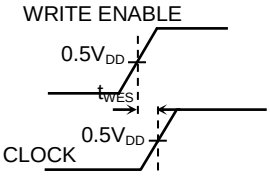
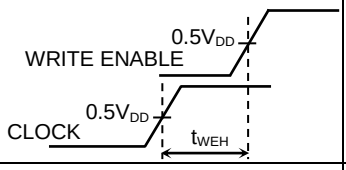
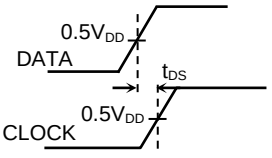
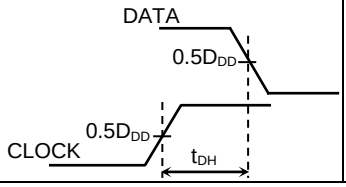
The Synchronous Dual-Port SRAMmxn will have two ports (Primary and Dual) for the same memory location. Both ports can be independently accessed for read or write operations. Single-port cells have only one port.
The used symbols of SRAMpRWnxm states are shown in Table 5.2.

Table 2.3. Symbols of SRAMmxn states

Symbol	State
L (“0”)	LOW Logic Level
H (“1”)	HIG`H Logic Level
Z	High-impedance State
LH (“0”→”1”)	LOW to HIGH Transition
HL (“1”→”0”)	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

Parameters and measurement conditions of SRAMmxn, included in SAED_EDK14_FINFET_RAM set of memories, are shown in Table 6.3.

Table 2.4. Parameters and measurement conditions of SRAMmxn

No	Parameter	Unit	Symbol	Figure	Definition
Timing parameters					
1	Cycle time	ns	t_{CYC}		The amount of time between two sequential active edges of clock signal
2	Access time	ns	t_A	None	The amount of time between applying Write/Read Enable signal and obtaining Access to Data in Memory
3	Address setup	ns	t_{AS}		The minimum amount of time in which the address to a SRAMmxn must be stable before the active edge of the clock occurs
4	Address hold	ns	t_{AH}		The minimum amount of time in which the address to a SRAMmxn must remain stable after the active edge of the clock has occurred
5	Chip select setup	ns	t_{CSS}		The minimum amount of time in which the Chip select signal to a SRAMmxn must be stable before the active edge of the clock occurs
6	Chip select hold	ns	t_{CSH}		The minimum amount of time in which the Chip select signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
7	Write enable setup	ns	t_{WES}		The minimum amount of time in which the Write enable signal to a SRAMmxn must be stable before the active edge of the clock occurs
8	Write enable hold	ns	t_{WEH}		The minimum amount of time in which the Write enable signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
9	Data setup	ns	t_{DS}		The minimum amount of time in which the input data to a SRAMmxn must be stable before the active edge of the clock occurs
10	Data hold	ns	t_{DH}		The minimum amount of time in which the input data to a SRAMmxn must remain stable after the active edge of the clock has occurred

No	Parameter	Unit	Symbol	Figure	Definition
11	Output Z state entry time	ns	t_{OZ}	None	The amount of time that takes the outputs to change to Z state after output enable signal is applied
12	Output Z state exit time	ns	t_{ZO}	None	The amount of time that takes the outputs to exit from Z state after output enable signal is applied
Power parameters					
13	AC current	mA	i_{AC}	None	Average value of dynamic current for read/write operations
14	Read AC current	mA	i_{ACR}	None	Dynamic current for read operation
15	Write AC current	mA	i_{ACW}	None	Dynamic current for write operation
16	Peak current	mA	i_{ACP}	None	Maximum value of dynamic current for read/write operations
17	Deselected current	mA	i_{ACD}	None	The value of current when SRAMmxn is disabled, all addresses switch and 50% of data input switch
18	Standby current	mA	i_{ACS}	None	The value of current in standby mode when all inputs and outputs are stable

2.4. Dual port SRAMs

2.4.1. Basic Pins

The Basic Pins of dual port SRAM2RWmxn are shown in Figure 5.2 and its descriptions are shown in Table5.5.

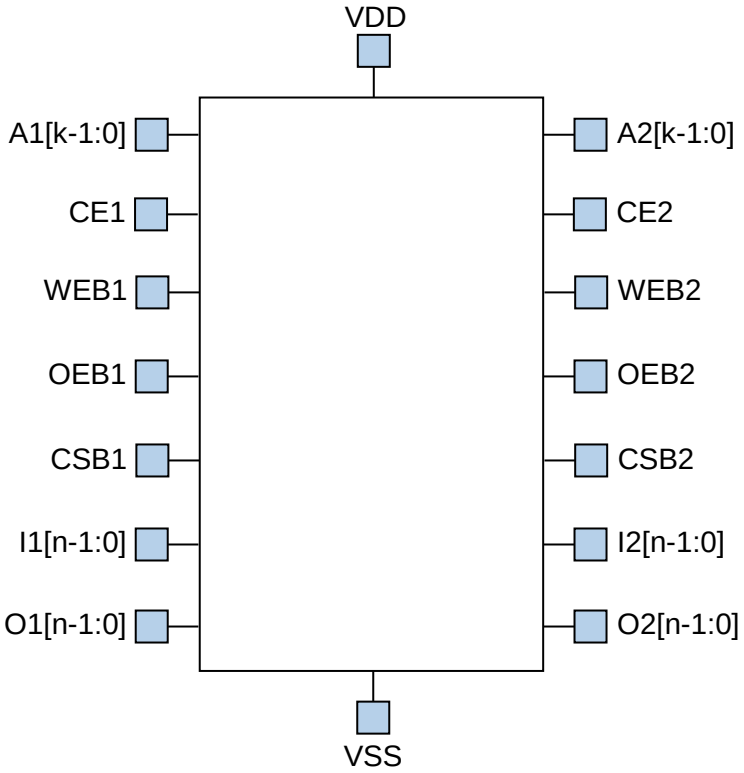


Figure 2.2. Dual port SRAMmxn Basic Pins

Table 2.5. Dual port SRAM2RWmxn Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A1	k	Input	Primary Read/Write Address
CE1	1	Input	Primary Positive-Edge Clock
WEB1	1	Input	Primary Write Enable, Active Low
OEB1	1	Input	Primary Output Enable, Active Low
CSB1	1	Input	Primary Chip Select, Active Low
I1	n	Input	Primary Input data bus
O1	n	Output	Primary Output data bus
A2	k	Input	Dual Read/Write Address
CE2	1	Input	Dual Positive-Edge Clock
WEB2	1	Input	Dual Write Enable, Active Low
OEB2	1	Input	Dual Output Enable, Active Low
CSB2	1	Input	Dual Chip Select, Active Low
I2	n	Input	Dual Input data bus
O2	n	Output	Dual Output data bus
VDD	Power supply		
VSS	Power ground		

2.4.2. Dual port SRAMmxn Description

The general block-diagram of SRAMmxn is shown in Figure 5.2.

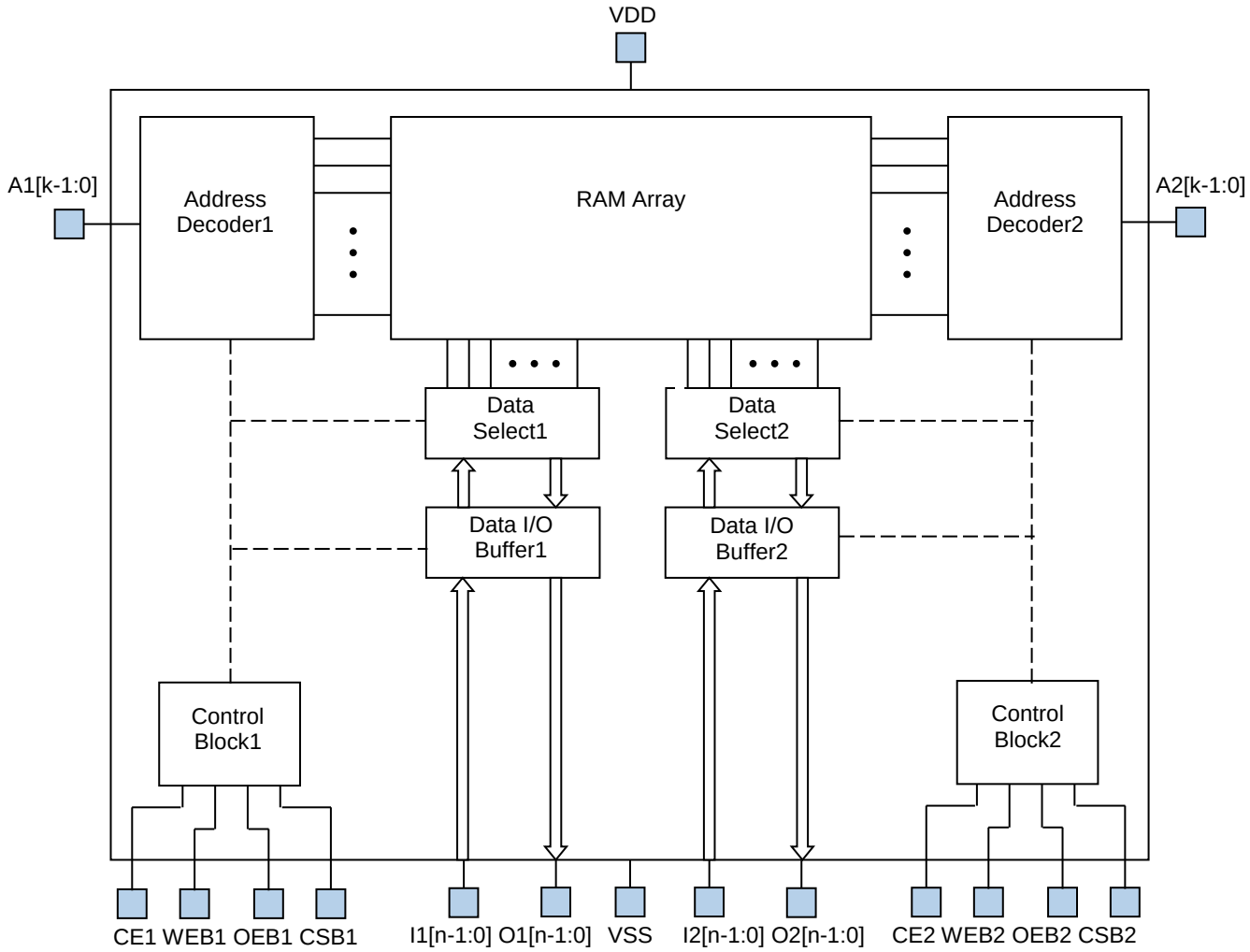


Figure 2.3. Dual port SRAMmxn block diagram

Dual port SRAMmxn Basic Operations is shown in Table 5.6.
Dual port SRAMmxn access is synchronous and triggered by the rising edge of the clock signals (CE1, CE2). Read/Write addresses (A1, A2), Input data (I1, I2), Write enable signals (WEB1, WEB2), and Chip select signals (CSB1, CSB2) are latched by the rising edge of the clocks (CE1, CE2).
The value of Chip Select signal is low (CS1/CS2=0) for read/write operation. The SRAMmxn enter read mode when CS1/CS2=0 and WEB1/WEB2=1. During read operations, data read from the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus I1[n-1:0]/I2[n-1:0] and appear on the data output bus O1[n-1:0]/O2[n-1:0].

Table 2.6. Dual port SRAMmxn Basic Operations

Pins						Data in Memory	Access to Memory	Operation
A1[k-1:0]	WEB1	OEB1	CSB1	I1[n-1:0]	O1[n-1:0] (t+1)	D(A1[k-1:0]) (t+1)		
X	X	0	1	Disabled	O1[n-1:0] (t)	D(A1[k-1:0]) (t)	No	Standby
		1			Z			
X	0	0	0	Enabled	I1[n-1:0]	I1[n-1:0]	Yes	Write
		1			Z			
X	1	0	0	X	D(A1[k-1:0]) (t)	D(A1[k-1:0]) (t)	No	Read
		1			Z			
A2[k-1:0]	WEB2	OEB2	CSB2	I2[n-1:0]	O2[n-1:0] (t+1)	D(A2[k-1:0]) (t+1)		
X	X	0	1	Disabled	O2[n-1:0] (t)	D(A2[k-1:0]) (t)	No	Standby
		1			Z			
X	0	0	0	Enabled	I2[n-1:0]	I2[n-1:0]	Yes	Write
		1			Z			
X	1	0	0	X	D(A2[k-1:0]) (t)	D(A2[k-1:0]) (t)	No	Read
		1			Z			

Note: O1[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O1[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A1[k-1:0]) (t) is the data in the RAM location specified on the address bus A1[k-1:0] in the previous moment of time, and D(A1[k-1:0]) (t+1) in the next moment of time.
O2[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O2[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A2[k-1:0]) (t) is the data in the RAM location specified on the address bus A2[k-1:0] in the previous moment of time, and D(A2[k-1:0]) (t+1) in the next moment of time.

Dual port SRAMmxn enter write mode when CSB1/CSB2=0 and WEB1/WEB2=0. During write mode, data on the data input bus I1[n-1:0]/I2[n-1:0] is writing into the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus I1[n-1:0]/I2[n-2:0].
If OEB1/OEB2=1, data on the output bus O1[n-1:0]/O2[n-1:0] placed in Z state. At that time read/write operation continue. When OEB1/OEB2=0, the data appear on the output bus O1[n-a:0]/O2[n-1:0].
Power dissipation is minimized using static circuit implementations. A standby mode is provided to further reduce power dissipation during periods of non-operation (CCB1/CSB2=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A1[k-1:0])/D(A2[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

Address contention will occur when both ports simultaneously access the same address. In this case, both ports will read the same data.

2.4.3. Dual port SRAMmxn Timing Waveforms

SRAMmxn will function according to the block-diagrams shown in Figures 5.5 – 5.7.

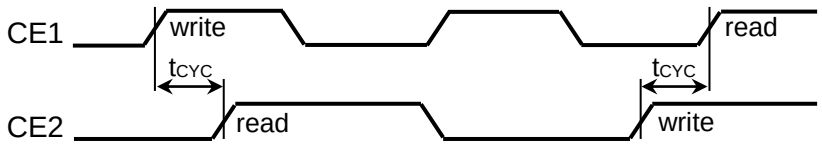


Figure 2.4. Dual port SRAMmxn Write-Read Clock Timing Waveforms

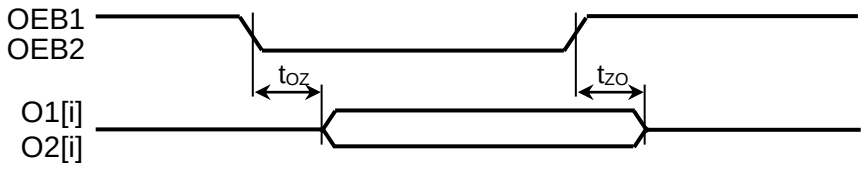


Figure 2.5. Dual port SRAMmxn Output-Enable Timing Waveforms

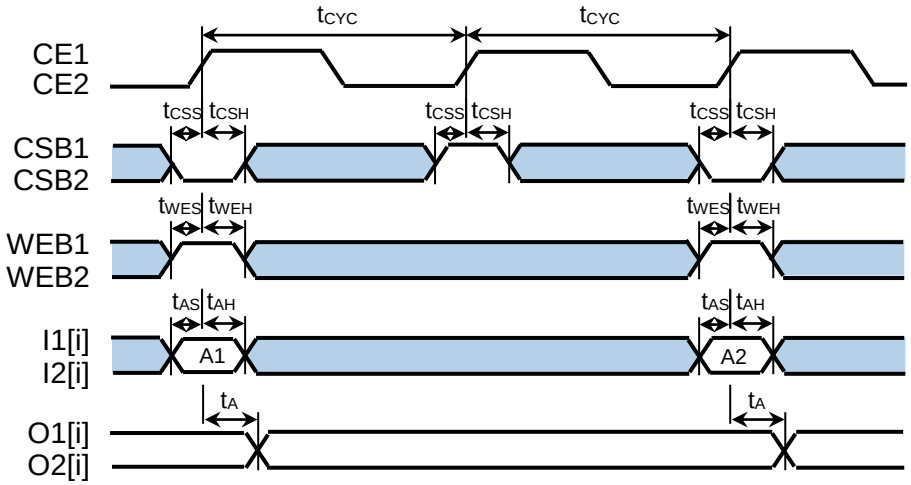


Figure 2.6. Dual port SRAMmxn Read-Cycle Timing Waveforms

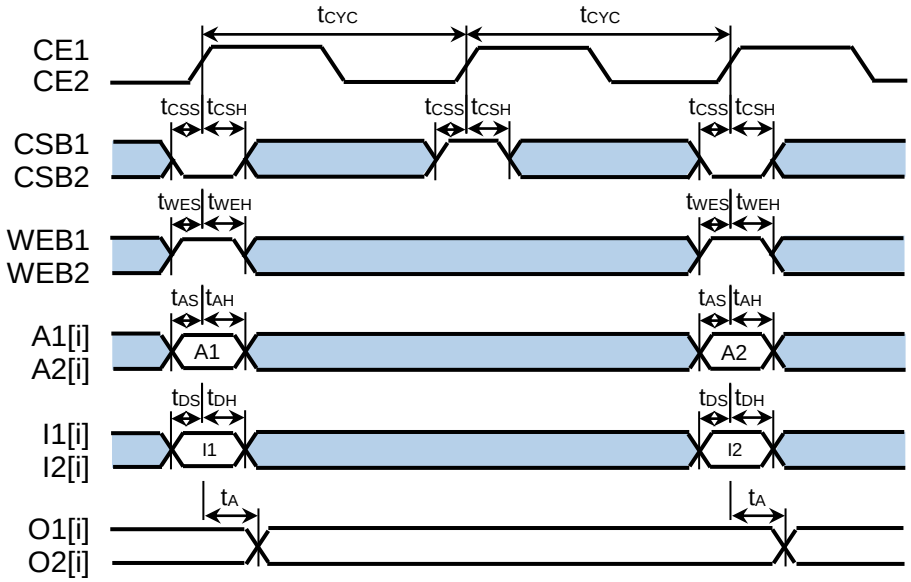


Figure 2.7. Dual port SRAMmxn Write-Cycle Timing Waveforms

2.5. Single port SRAMs

2.5.1. Basic Pins

The Basic Pins of single port SRAM1RWnxm are shown in Figure 5.8 and its descriptions are shown in Table 5.7.

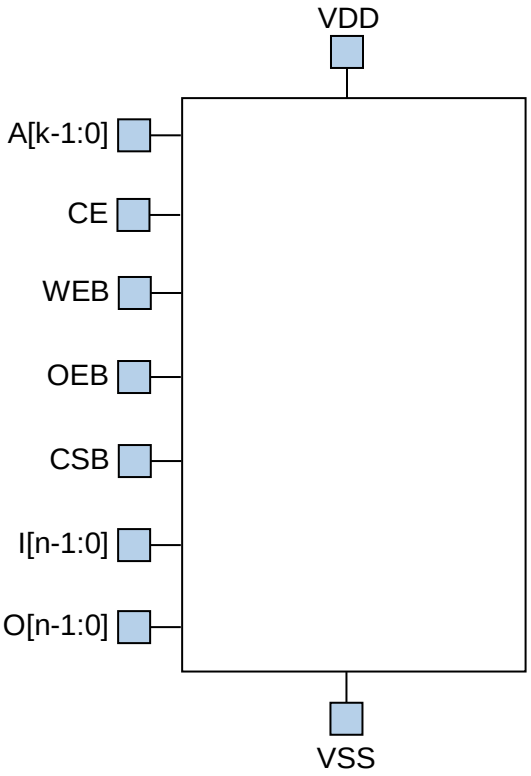


Figure 2.8. Single port SRAM1RWmxn Basic Pins

Table 2.7. Single port SRAM1RWmxn Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A	k	Input	Primary Read/Write Address
CE	1	Input	Primary Positive-Edge Clock
WEB	1	Input	Primary Write Enable, Active Low
OEB	1	Input	Primary Output Enable, Active Low
CSB	1	Input	Primary Chip Select, Active Low
I	n	Input	Primary Input data bus
O	n	Output	Primary Output data bus
VDD	Power supply		
VSS	Power ground		

2.5.2. Single port SRAM1RWmxn Description

The general block-diagram of single port SRAM1RWmxn is shown in Figure 5.9.

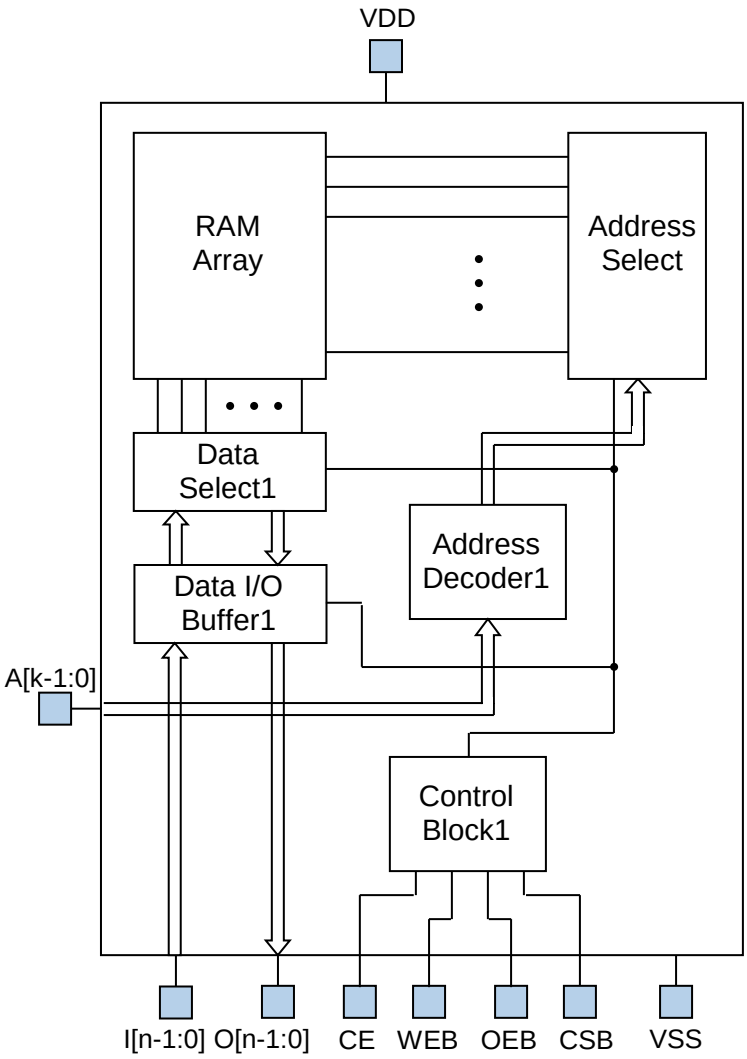


Figure 2.9. Single port SRAM1RWmxn block diagram

Single port SRAM1RWmxn Basic Operations is shown in Table 5.8.

Single port SRAM1RWmxn access is synchronous and triggered by the rising edge of the clock signals (CE). Read/Write addresses (A), Input data (I), Write enable signals (WEB), and Chip select signals (CSB) are latched by the rising edge of the clocks (CE).

The value of Chip Select signal is low (CS=0) for read/write operation. SRAM enter read mode when CS=0 and WEB=1. During read operations, data read from the memory location D(A[k-1:0]) specified on the address bus I[n-1:0] and appear on the data output bus O[n-1:0].

Table 2.8. Single port SRAM1RWmxn Basic Operations

Pins						Data in Memory	Access to Memory	Operation
A[k-1:0]	WEB	OEB	CSB	I[n-1:0]	O[n-1:0] (t+1)	D(A[k-1:0]) (t+1)		
X	X	0	1	Disabled	O[n-1:0] (t)	D(A[k-1:0]) (t)	No	Standby
		1			Z			
X	0	0	0	Enabled	I[n-1:0]	I[n-1:0]	Yes	Write
		1			Z			
X	1	0	0	X	D(A[k-1:0]) (t)	D(A[k-1:0]) (t)	No	Read
		1			Z			

Note: O[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.
O[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.

Single port SRAM1RWmxn enter write mode when CSB=0 and WEB=0. During write mode, data on the data input bus I[n-1:0] is writing into the memory location D(A[k-1:0]) specified on the address bus I[n-1:0].
If OEB=1, data on the output bus O[n-1:0] placed in Z state. At that time read/write operation continue. When OEB=0, the data appear on the output bus O[n-a:0].
Power dissipation is minimized using static circuit implementations. A standby mode is provided to further reduce power dissipation during periods of non-operation (CCB=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

2.5.3. Single port SRAM1RWmxn Timing Waveforms

Single port SRAM1RWmxn functions according to the block-diagrams shown in Figures 5.10 – 5.12.

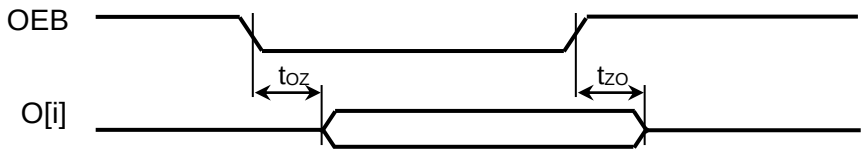


Figure 2.10. Single port SRAM1RWmxn Output-Enable Timing Waveforms

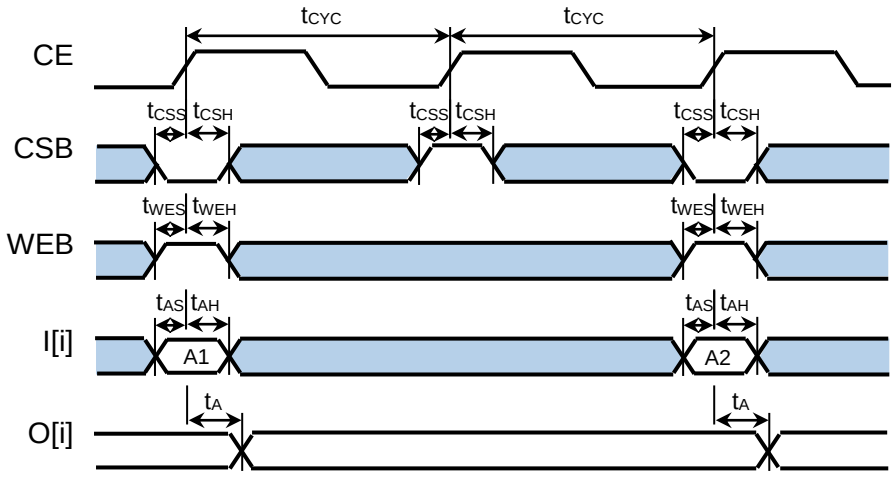


Figure 2.11. Single port SRAM1RWmxn Read-Cycle Timing Waveforms

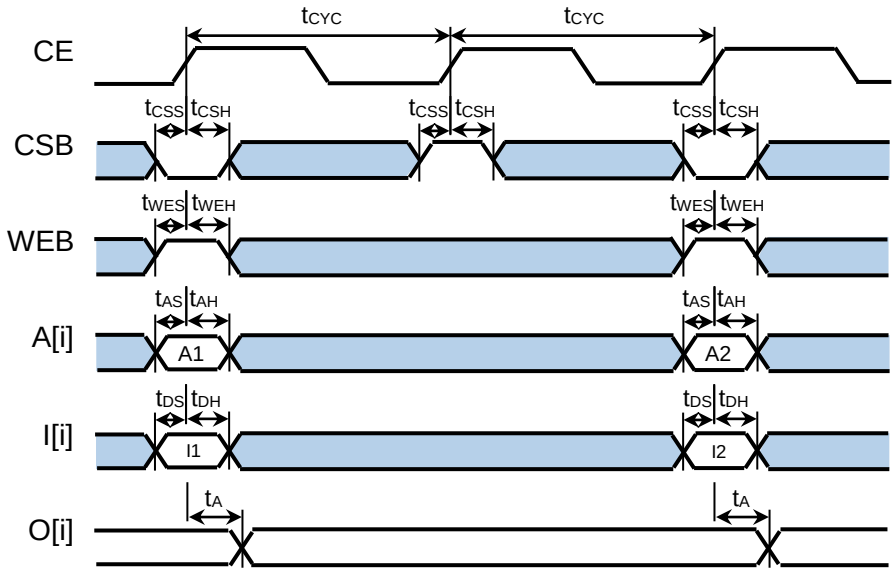


Figure 2.12. Sihgle port SRAM1RWmxn Write-Cycle Timing Waveforms

2.6. Operating conditions

The operating conditions of SAED_EDK14_FINFET_RAM set of memories are shown in Table 5.9..

Table 2.9. Operating conditions

Parameter	Min	Typ	Max	Units
Power supply (VDD) range	0.72	0.8	0.88	V
Operating Temperature	-40	+25	+125	°C
Operating Frequency (F)			1	GHz

2.7. Characterization corners

The timing data will be given only for 3 process/voltage/temperature (PVT) conditions shown in Table 5.11.

Table 2.10. Characterization Corners

Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature(^{0}C)	Power Supply (V)	Library Name Suffix
SS	Fast – Fast	125	0.88	ss0d88v125c
SS	Fast – Fast	25	0.88	ss0d88v25c
SS	Fast – Fast	-40	0.88	ss0d88vm40c
TT	Typical – Typical	125	0.8	tt0d8v125c
TT	Typical – Typical	25	0.8	tt0d8v25c
TT	Typical – Typical	-40	0.8	tt0d8vm40c
FF	Slow – Slow	125	0.72	ff0d72v125c
FF	Slow – Slow	25	0.72	ff0d72v25c
FF	Slow – Slow	-40	0.72	ff0d72vm40c

Critical path, setup and hold analyses will be performed for the mentioned corners.

3. Set of Low Power Memories SAED_EDK14_FINFET_RAM_LP

3.1. Introduction

The SAED_EDK14_FINFET_RAM_LP set of low power memories will be designed using SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V process. It will represent a set of several static RAMs (SRAMs) with small number of words (word depth – m) and bits in word (data width – n). All SRAMs, included in SAED_EDK14_FINFET_RAM_LP, will represent Synchronous Dual-Port or Single-port SRAM with Write Enable, Output Enable, Chip Select port(s). Each SRAMLPscmxn, included in the set, will have the same architecture and will differ from the rest with its nxm (width x depth) sizes. As SAED_EDK14_FINFET_RAM_LP is anticipated for the use of educational purposes, only SRAMs of the sizes, shown in Table 6.1., will be included in it. SAED_EDK14_FINFET_RAM set of memories are intended for use in low power design flow. To achieve low power consumption the following power management techniques are used:

- Reducing the supply voltage of periphery
- Reducing the supply voltage of memory core and shutting down the supply voltage of periphery
- Complete shut down of the memory during the periods of non-operation
- Switched power control (VDD power)
- Switched ground control (Vss ground)

Table 3.1. SRAMmxn Cell List

No	Data width (n)	Word depth (m)	Address width ($k=\log_2 m$)	Cell Name
1	4	4	2	SRAMLP1RWPC4x4
2	8	4	2	SRAMLP1RWPC4x8
3	4	16	4	SRAMLP1RWPC16x4
4	8	16	4	SRAMLP1RWPC16x8
5	16	16	4	SRAMLP1RWPC16x16
6	32	16	4	SRAMLP1RWPC16x32
7	4	32	5	SRAMLP1RWPC32x4
8	8	32	5	SRAMLP1RWPC32x8
9	16	32	5	SRAMLP1RWPC32x16
10	32	32	5	SRAMLP1RWPC32x32
11	4	64	6	SRAMLP1RWPC64x4
12	8	64	6	SRAMLP1RWPC64x8
13	16	64	6	SRAMLP1RWPC64x16
14	32	64	6	SRAMLP1RWPC64x32
15	128	64	6	SRAMLP1RWPC64x128
16	4	128	7	SRAMLP1RWPC128x4
17	8	128	7	SRAMLP1RWPC128x8
18	16	128	7	SRAMLP1RWPC128x16
19	32	128	7	SRAMLP1RWPC128x32
20	8	256	8	SRAMLP1RWPC256x8
21	32	256	8	SRAMLP1RWPC256x32
22	128	256	8	SRAMLP1RWPC256x128
23	8	512	9	SRAMLP1RWPC512x8
24	32	512	9	SRAMLP1RWPC512x32

No	Data width (n)	Word depth (m)	Address width ($k=\log_2 m$)	Cell Name
25	64	512	9	SRAMLP1RWPC512x64
26	128	512	9	SRAMLP1RWGC512x128
27	4	4	2	SRAMLP2RWPC4x4
28	8	4	2	SRAMLP2RWPC4x8
29	4	16	4	SRAMLP2RWPC16x4
30	8	16	4	SRAMLP2RWPC16x8
31	16	16	4	SRAMLP2RWPC16x16
32	32	16	4	SRAMLP2RWPC16x32
33	4	32	5	SRAMLP2RWPC32x4
34	8	32	5	SRAMLP2RWPC32x8
35	16	32	5	SRAMLP2RWPC32x16
36	32	32	5	SRAMLP2RWPC32x32
37	4	64	6	SRAMLP2RWPC64x4
38	8	64	6	SRAMLP2RWPC64x8
39	16	64	6	SRAMLP2RWPC64x16
40	32	64	6	SRAMLP2RWPC64x32
41	128	64	6	SRAMLP2RWPC64x128
42	4	128	7	SRAMLP2RWPC128x4
43	8	128	7	SRAMLP2RWPC128x8
44	16	128	7	SRAMLP2RWPC128x16
45	32	128	7	SRAMLP2RWPC128x32
46	8	256	8	SRAMLP2RWPC256x8
47	32	256	8	SRAMLP2RWPC256x32
48	128	256	8	SRAMLP2RWPC256x128
49	8	512	9	SRAMLP2RWPC512x8
50	32	512	9	SRAMLP2RWPC512x32
51	64	512	9	SRAMLP2RWPC512x64
52	128	512	9	SRAMLP2RWGC512x128

All memories in the set are named according to the following template (Fig. 3.1):

3.1. SRAM naming conventions

SRAMLP***p***RW***scnxw***

Figure 3.1. Memories naming template

The template contains symbols denoting specifics of the memory, the descriptions of the symbols are given in Table 3.1.

Table 3.2. Memories naming conventions

Symbol	Description	Values
p	Number of access ports	1,2
n	Number of words	Integer number, 2^n
w	Word size	Integer, various
sc	Supplay control	pc(power control),gc(ground control)

3.2. General Information

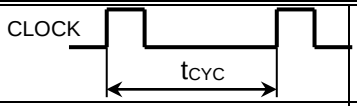
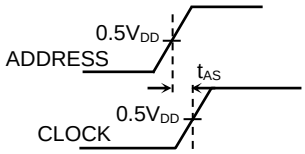
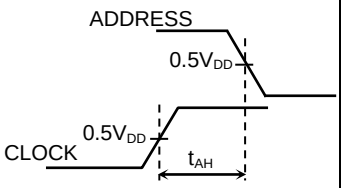
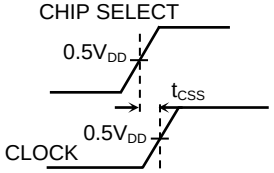
The Synchronous Dual-Port SRAMLPscmxn will have two ports (Primary and Dual) for the same memory location. Both ports can be independently accessed for read or write operations. Single-port cells have only one port.
The used symbols of SRAMLPscmxn states are shown in Table 6.3.

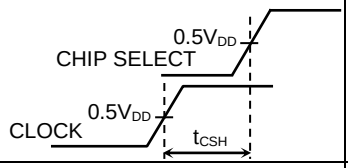
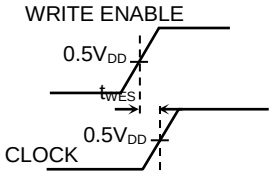
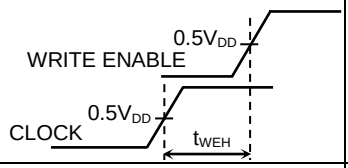
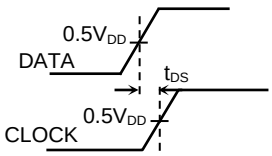
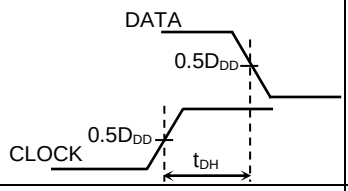
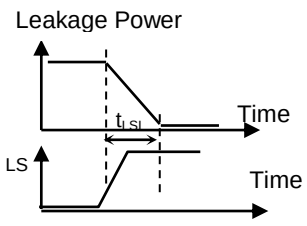
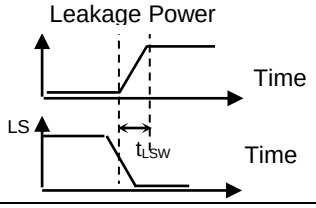
Table 3.3. Symbols of SRAMLPscmxn states

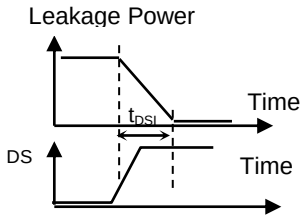
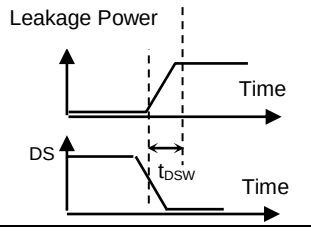
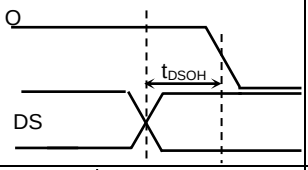
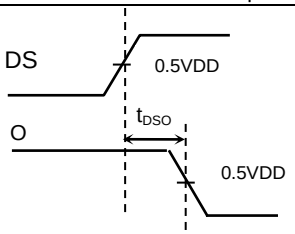
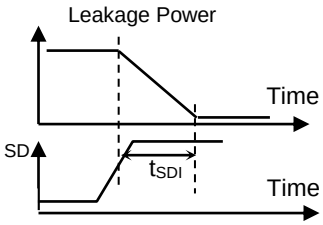
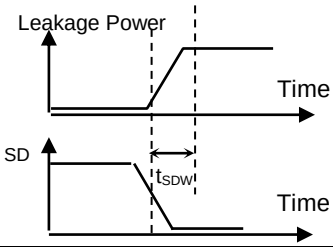
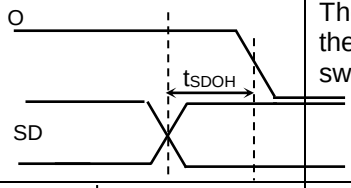
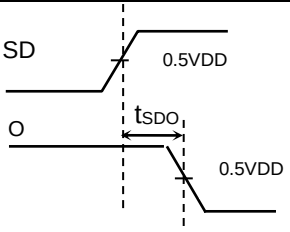
Symbol	State
L (“0”)	LOW Logic Level
H (“1”)	HIGH Logic Level
Z	High-impedance State
LH (“0”→”1”)	LOW to HIGH Transition
HL (“1”→”0”)	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

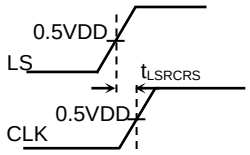
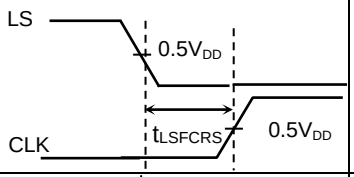
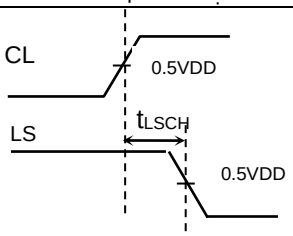
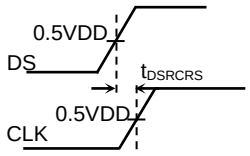
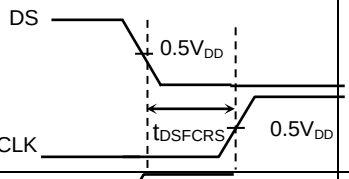
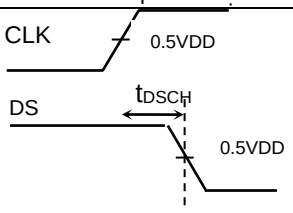
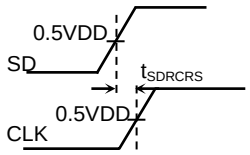
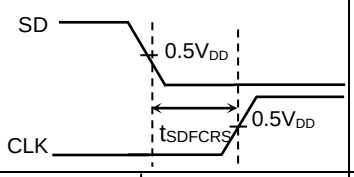
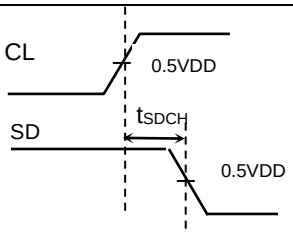
Parameters and measurement conditions of SRAMLPscmxn, included in SAED_EDK14_FINFET_RAM_LP set of memories, are shown in Table 6.4.

Table 3.4. Parameters and measurement conditions of SRAMLPscmxn

No	Parameter	Unit	Symbol	Figure	Definition
Timing parameters					
19	Cycle time	ns	t_{CYC}		The amount of time between two sequential active edges of clock signal
20	Access time	ns	t_A	None	The amount of time between applying Write/Read Enable signal and obtaining Access to Data in Memory
21	Address setup	ns	t_{AS}		The minimum amount of time in which the address to a SRAMmxn must be stable before the active edge of the clock occurs
22	Address hold	ns	t_{AH}		The minimum amount of time in which the address to a SRAMmxn must remain stable after the active edge of the clock has occurred
23	Chip select setup	ns	t_{CSS}		The minimum amount of time in which the Chip select signal to a SRAMmxn must be stable before the active edge of the clock occurs

No	Parameter	Unit	Symbol	Figure	Definition
24	Chip select hold	ns	t_{CSH}		The minimum amount of time in which the Chip select signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
25	Write enable setup	ns	t_{WES}		The minimum amount of time in which the Write enable signal to a SRAMmxn must be stable before the active edge of the clock occurs
26	Write enable hold	ns	t_{WEH}		The minimum amount of time in which the Write enable signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
27	Data setup	ns	t_{DS}		The minimum amount of time in which the input data to a SRAMmxn must be stable before the active edge of the clock occurs
28	Data hold	ns	t_{DH}		The minimum amount of time in which the input data to a SRAMmxn must remain stable after the active edge of the clock has occurred
29	Output Z state entry time	ns	t_{OZ}	None	The amount of time that takes the outputs to change to Z state after output enable signal is applied
30	Output Z state exit time	ns	t_{ZO}	None	The amount of time that takes the outputs to exit from Z state after output enable signal is applied
Low Power control measurments					
31	LS active to memory low leakage state	ns	t_{LSI}		The minimum amount of time LS signal must remain active till memory goes into low leakage mode
32	LS inactive to memory wake up from low leakage state	ns	t_{LSW}		The minimum amount of time LS signal must remain inactive till memory wakes up from low leakage mode.

No	Parameter	Unit	Symbol	Figure	Definition
33	DS active to memory low leakage state	ns	t_{DSI}		The minimum amount of time DS signal must remain active till memory goes into low leakage mode.
34	DS inactive to memory wake up from low leakage state	ns	t_{DSW}		The minimum amount of time DS signal must remain inactive till memory wakes up from low leakage mode.
35	O hold time after DS High/Low	ns	t_{DSOH}		The maximum amount of time the output remains stable after switching of DS signal.
36	DS rise to O falling delay	ns	t_{DSO}		Delay between positive edge of DS and negative edge of output.
37	SD active to memory low leakage state	ns	t_{SDI}		The minimum amount of time SD signal must remain active till memory goes into low leakage mode
38	SD inactive to memory wake up from low leakage state	ns	t_{SDW}		The minimum amount of time SD signal must remain inactive till memory wakes up from low leakage mode.
39	O hold time after SD High/Low	ns	t_{SDOH}		The maximum amount of time the output remains stable after switching of SD signal.
40	SD rise to O falling delay	ns	t_{SDO}		Delay between positive edge of SD and negative edge of output

No	Parameter	Unit	Symbol	Figure	Definition
41	LS rise setup time before CLK rises	ns	t_{LSRCRS}		The minimum amount of time in which the LS signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
42	LS fall setup time before CLK rises	ns	t_{LSFCRS}		The minimum amount of time in which the LS signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
43	LS hold time after CLK rises	ns	t_{LSCH}		The minimum amount of time in which the LS signal to a SRAMLPscmxn must remain stable after the active edge of the clock has occurred
44	DS rise setup time before CLK rises	ns	t_{DSRCRS}		The minimum amount of time in which the DS signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
45	DS fall setup time before CLK rises	ns	t_{DSFCRS}		The minimum amount of time in which the DS signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
46	DS hold time after CLK rises	ns	t_{DSCH}		The minimum amount of time in which the DS signal to a SRAMLPscmxn must remain stable after the active edge of the clock has occurred
47	SD rise setup time before CLK rises	ns	t_{SDRCRS}		The minimum amount of time in which the SD signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
48	SD fall setup time before CLK rises	ns	t_{SDFCRS}		The minimum amount of time in which the SD signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
49	SD hold time after CLK rises	ns	t_{SDCH}		The minimum amount of time in which the SD signal to a SRAMLPscmxn must remain stable after the active edge of the clock has occurred
Power parameters					

No	Parameter	Unit	Symbol	Figure	Definition
50	AC current	mA	i_{AC}	None	Average value of dynamic current for read/write operations
51	Read AC current	mA	i_{ACR}	None	Dynamic current for read operation
52	Write AC current	mA	i_{ACW}	None	Dynamic current for write operation
53	Peak current	mA	i_{ACP}	None	Maximum value of dynamic current for read/write operations
54	Deselected current	mA	i_{ACD}	None	The value of current when SRAMLPscmxn is disabled, all addresses switch and 50% of data input switch
55	Standby current	mA	i_{ACS}	None	The value of current in standby mode when all inputs and outputs are stable

3.3. Dual port SRAMs

3.3.1. Basic Pins

The Basic Pins of dual port SRAMLPscmxn are shown in Figure 6.2 and its descriptions are shown in Table7.4.

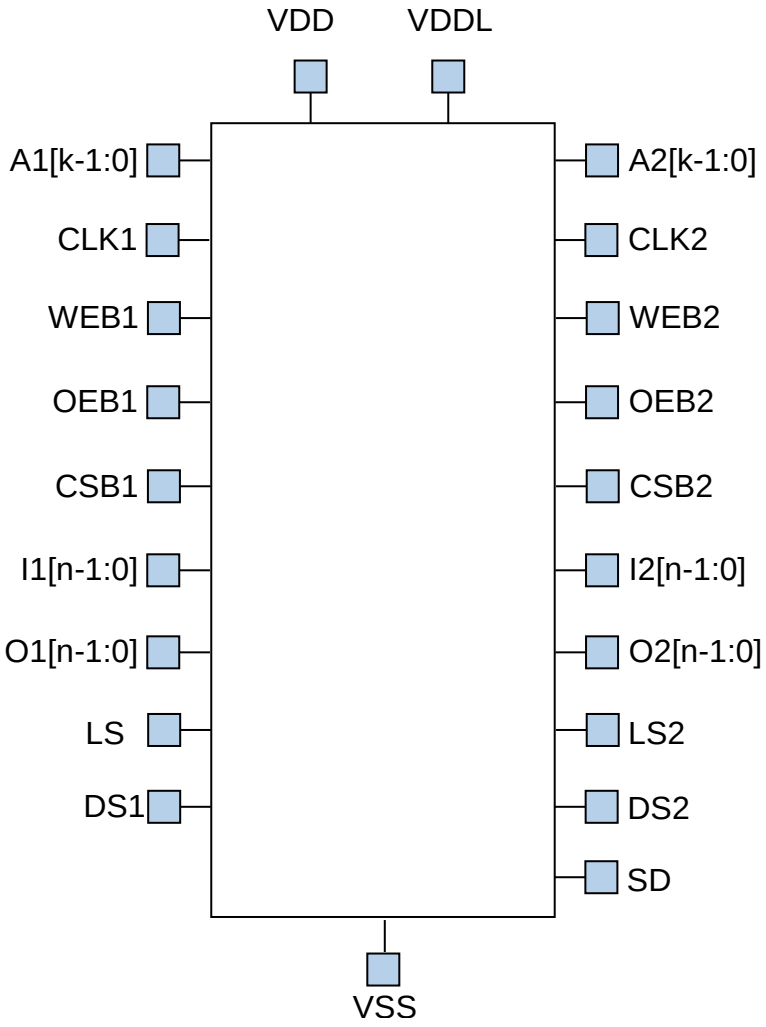


Figure 3.2. Dual port SRAMLPscmxn Basic Pins

Table 3.5. Dual port SRAMLPscmxn Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A1	K	Input	Primary Read/Write Address
CLK1	1	Input	Primary Positive-Edge Clock
WEB1	1	Input	Primary Write Enable, Active Low
OEB1	1	Input	Primary Output Enable, Active Low
CSB1	1	Input	Primary Chip Select, Active Low
I1	N	Input	Primary Input data bus
O1	N	Output	Primary Output data bus
LS1	1	Input	Primary Light Sleep, Active High
DS1	1	Input	Primary Deep Sleep, Active High
SD1	1	Input	Primary Shut Down, Active High
A2	k	Input	Dual Read/Write Address
CLK2	1	Input	Dual Positive-Edge Clock
WEB2	1	Input	Dual Write Enable, Active Low
OEB2	1	Input	Dual Output Enable, Active Low
CSB2	1	Input	Dual Chip Select, Active Low
I2	n	Input	Dual Input data bus
O2	n	Output	Dual Output data bus
LS2	1	Input	Dual Light Sleep, Active High
DS2	1	Input	Dual Deep Sleep, Active High
SD2	1	Input	Dual Shut Down, Active High
VDD	Power supply of the memory array		
VDDL	Power supply of the periphery		
VSS	Power ground		

3.3.2. Dual port SRAMLPscmxn Description

The general block-diagram of SRAMLPscmxn is shown in Figure 6.3.

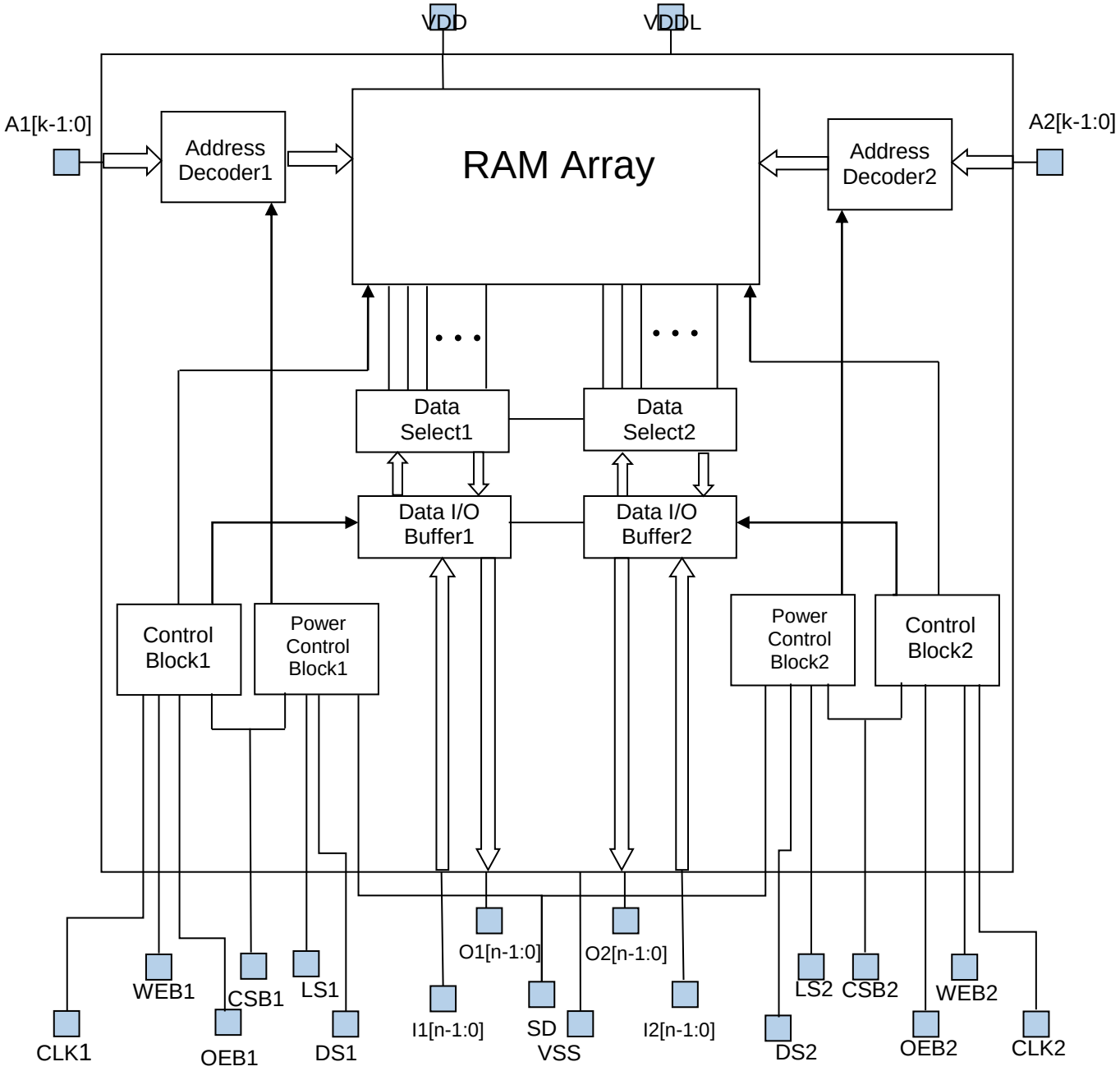


Figure 3.3. Dual port SRAMLPscmxn block diagram

Dual port SRAMLPscmxn Basic Operations is shown in Table 7.5.
Dual port SRAMLPscmxn access is synchronous and triggered by the rising edge of the clock signals (CLK1/CLK2). Read/Write addresses (A1/A2), Input data (I1/I2), Write enable (WEB1/WEB2), Light Sleep (LS1/LS2), Deep Sleep (DS1/DS2), Shut Down (SD1/SD2) and Chip select (CSB1/CSB2) signals are latched by the rising edge of the clocks (CLK1/ CLK2).

Table 3.6. Dual port SRAMLPscmxn Basic Operations

Pins									Data in Memory	Access to Memory	Operation Mode
A1[k-1:0]	WEB1	OEB1	CSB1	LS1	DS1	SD1	I1[n-1:0]	O1[n-1:0] (t+1)	D(A1[k-1:0]) (t+1)		
X	X	0 1	1	0	0	0	Disabled	O1[n-1:0] (t) Z	D(A1[k-1:0]) (t)	No	Stand by
X	0	0 1	0	0	0	0	Enabled	I1[n-1:0] Z	I1[n-1:0]	Yes	Write
X	1	0 1	0	0	0	0	X	D(A1[k-1:0]) (t) Z	D(A1[k-1:0]) (t)	No	Read
X	X	X	1	1	0	0	Disabled	O1[n-1:0] (t)	D(A1[k-1:0]) (t)	No	Light Sleep
X	X	X	1	0	1	0	Disabled	0	D(A1[k-1:0]) (t)	No	Deep Sleep
X	X	X	1	0	0	1	Disabled	0	Z	No	Shut Down
A2[k-1:0]	WEB2	OEB2	CSB2	LS2	DS2	SD2	I2[n-1:0]	O2[n-1:0] (t+1)	D(A2[k-1:0]) (t+1)		
X	X	0 1	1	0	0	0	Disabled	O2[n-1:0] (t) Z	D(A2[k-1:0]) (t)	No	Stand by
X	0	0 1	0	0	0	0	Enabled	I2[n-1:0] Z	I2[n-1:0]	Yes	Write
X	1	0 1	0	0	0	0	X	D(A2[k-1:0]) (t) Z	D(A2[k-1:0]) (t)	No	Read
X	X	X	1	1	0	0	Disabled	O2[n-1:0] (t)	D(A2[k-1:0]) (t)	No	Light Sleep
X	X	X	1	0	1	0	Disabled	0	D(A2[k-1:0]) (t)	No	Deep Sleep
X	X	X	1	0	0	1	Disabled	0	Z	No	Shut Down

Note: O1[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O1[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A1[k-1:0]) (t) is the data in the RAM location specified on the address bus A1[k-1:0] in the previous moment of time, and D(A1[k-1:0]) (t+1) in the next moment of time.
O2[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O2[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A2[k-1:0]) (t) is the data in the RAM location specified on the address bus A2[k-1:0] in the previous moment of time, and D(A2[k-1:0]) (t+1) in the next moment of time.

3.3.3. Operation modes of dual port SRAMLPscmxn

Read Mode: The value of Chip Select signal is low (CSB1/CSB2=0) for read operation. The SRAMmxn enter read mode when CS1/CS2=0 and WEB1/WEB2=1. In this mode the LS1/LS2, DS1/DS2 and SD signals are inactive. During read operations, data read from the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus I1[n-1:0]/I2[n-1:0] and appear on the data output bus O1[n-1:0]/O2[n-1:0].

Write Mode: In Write Mode the value of Chip Select signal is low (CSB1/CSB2=0) Dual port SRAMmxn enter write mode when CSB1/CSB2=0 and WEB1/WEB2=0. In this mode the

LS1/LS2, DS1/DS2 and SD signals are inactive. During write mode, data on the data input bus I1[n-1:0]/I2[n-1:0] is being written into the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus A1[k-1:0])/D(A2[k-1:0]).
If OEB1/OEB2=1, data on the output bus O1[n-1:0]/O2[n-1:0] is placed in Z state. At that time read/write operation continues. When OEB1/OEB2=0, the data appears on the output bus O1[n-a:0]/O2[n-1:0].

Standby Mode: The Standby mode is provided to further reduce power dissipation during periods of non-operation (CSB1/CSB2=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A1[k-1:0])/D(A2[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

Light Sleep Mode: When CSB1/CSB2=1 and the LS1/LS2 pin is active, the memory goes into Light Sleep mode. In this mode VDDL supply voltage of periphery is reduced down to 0.7v. In Light Sleep mode DS1/DS2, SD signals are inactive and the output state doesn't change.

Deep Sleep Mode: In this mode the value of Chip Select signal is high (CSB1/CSB2=1), and LS1/LS2 and SD signals are inactive. If DS1/DS2 pin is set, the power to periphery is shut down completely and the power to the memory core is reduced down to 0.5v. In this mode memory contents is retained, but the outputs of the memory are pulled low.

Shut Down Mode: The SRAMLPscmxn enters this mode, when the value of SD1/SD2 signal is high. When the SD pin is set, there is a complete shutdown (both the periphery and array are power gated), with no data retention, and the memory outputs are pulled low.

Address contention will occur when both ports simultaneously access the same address. In this case, both ports will read the same data.

Mentioned low power techniques differ not only with power consumption efficiency, but also with timing parameters. Table 7.10 shows the differences.

3.3.4. Dual port SRAMLPscmxn Timing Waveforms

SRAMLPscmxn will function according to the block-diagrams shown in Figures 6.5. – 6.7.

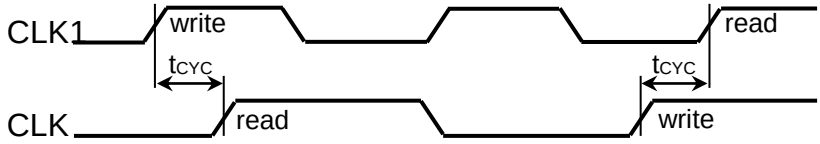


Figure 3.4. Dual port SRAMLPscmxn Write-Read Clock Timing Waveforms

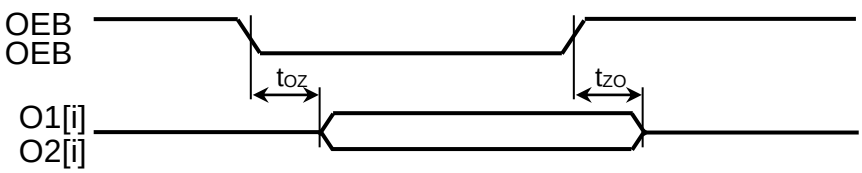


Figure 3.5. Dual port SRAMLPscmxn Output-Enable Timing Waveforms

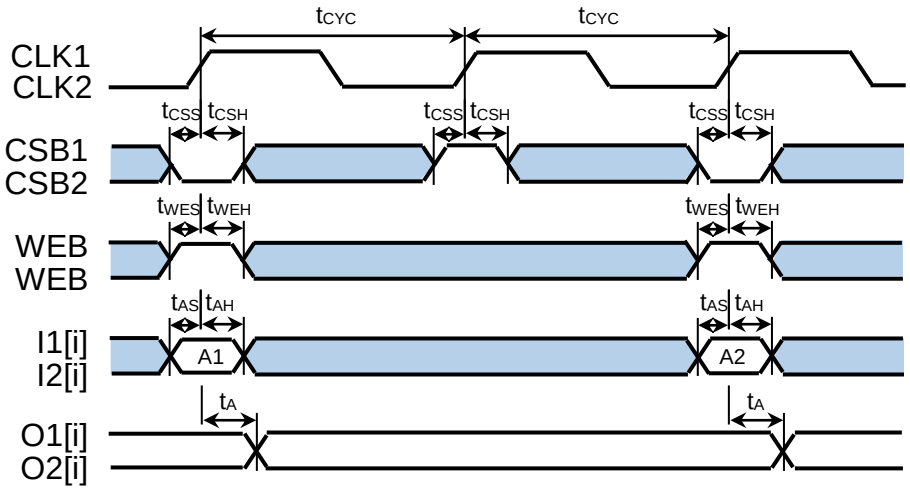


Figure 3.6. Dual port SRAMLPscmxn Read-Cycle Timing Waveforms

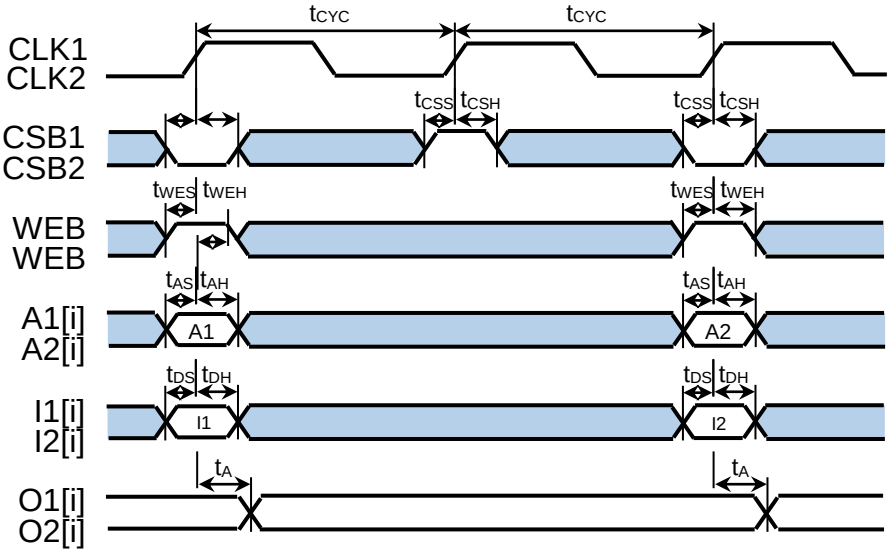


Figure 3.7. Dual port SRAMLPscmxn Write-Cycle Timing Waveforms

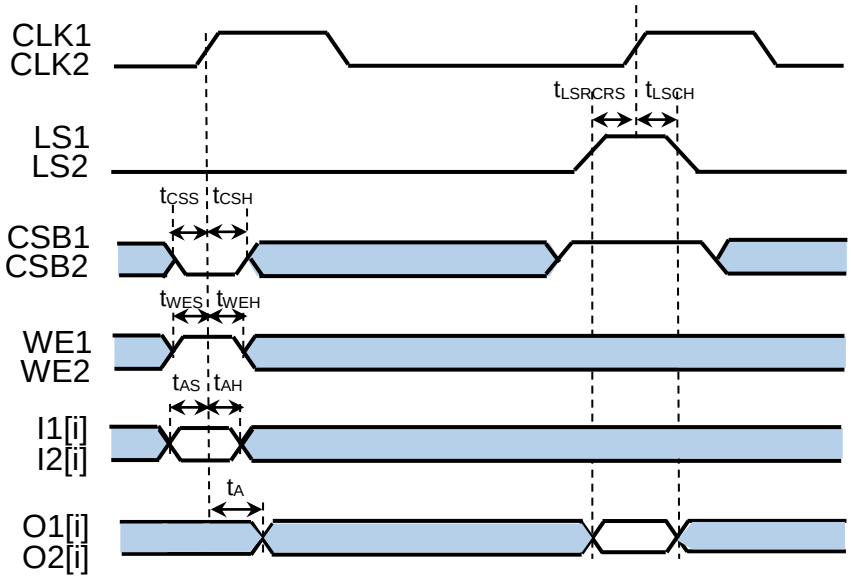


Figure 3.8. Dual port SRAMLPscmxn Write-Cycle Timing Waveforms with Lights Sleep state

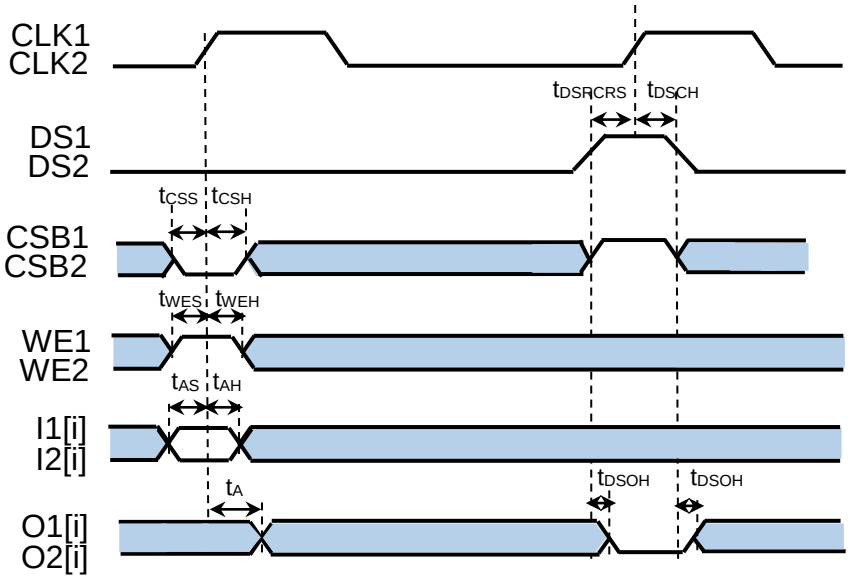


Figure 3.9. Dual port SRAMLPscmxn Write-Cycle Timing Waveforms with Deep Sleep state

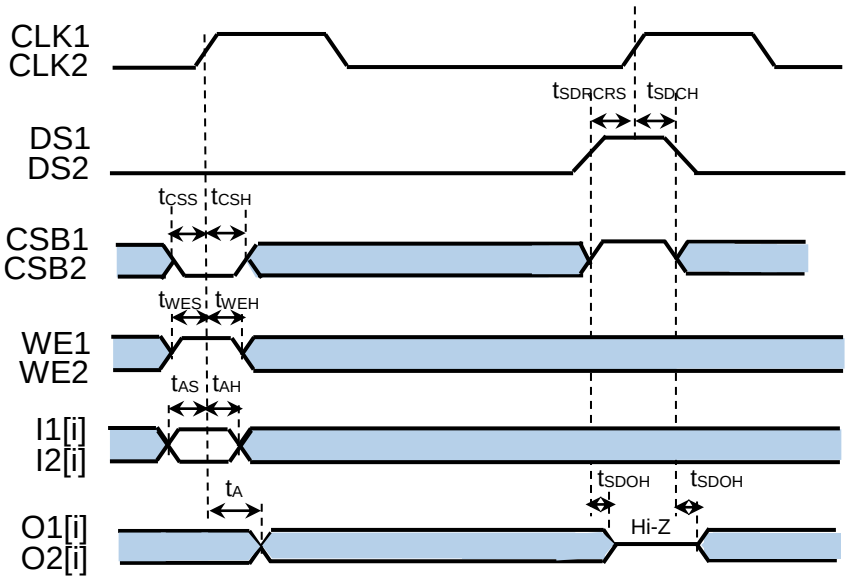


Figure 3.10. Dual port SRAMLPscmxn Write-Cycle Timing Waveforms with Shat Down state

3.4. Single port SRAMs

3.4.1. Basic Pins

The Basic Pins of single port SRAMLPscmxn are shown in Figure 6.11. and their descriptions are shown in Table6.7.

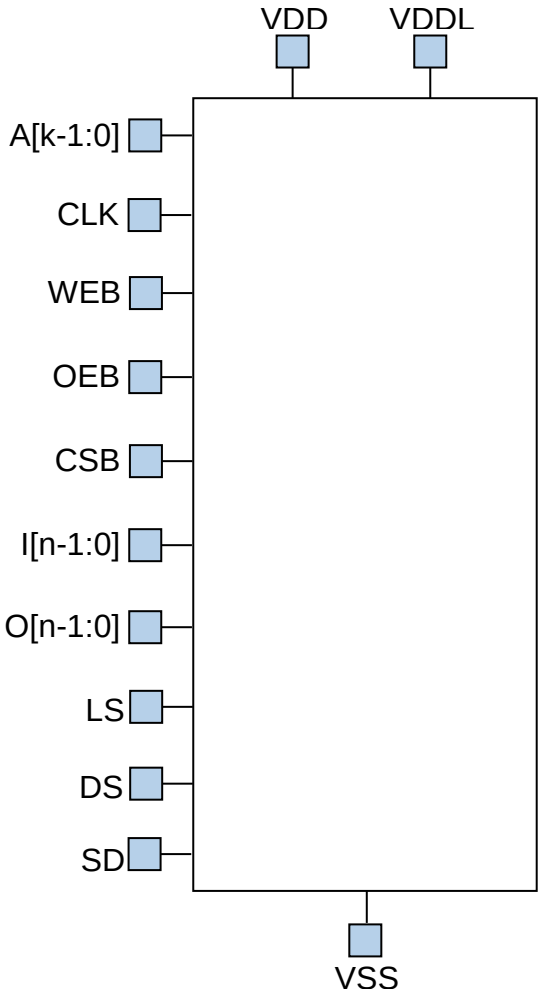


Figure 3.11 Single port SRAMLP1RWscmxn Basic Pins

Table 3.7 Single port SRAMLP1RWscmxn Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A	k	Input	Primary Read/Write Address
CLK	1	Input	Primary Positive-Edge Clock
WEB	1	Input	Primary Write Enable, Active Low
OEB	1	Input	Primary Output Enable, Active Low
CSB	1	Input	Primary Chip Select, Active Low
I	n	Input	Primary Input data bus
O	n	Output	Primary Output data bus
LS	1	Input	Primary Light Sleep, Active High
DS	1	Input	Primary Deep Sleep, Active High
SD	1	Input	Primary Shut Down, Active High
VDD	Power supply of the memory array		
VDDL	Power supply of the periphery		
VSS	Power ground		

3.4.2. Single port SRAMLP1RWscmxn Description

The general block-diagram of single port SRAMLP1RWscmxn is shown in Figure 6.12.

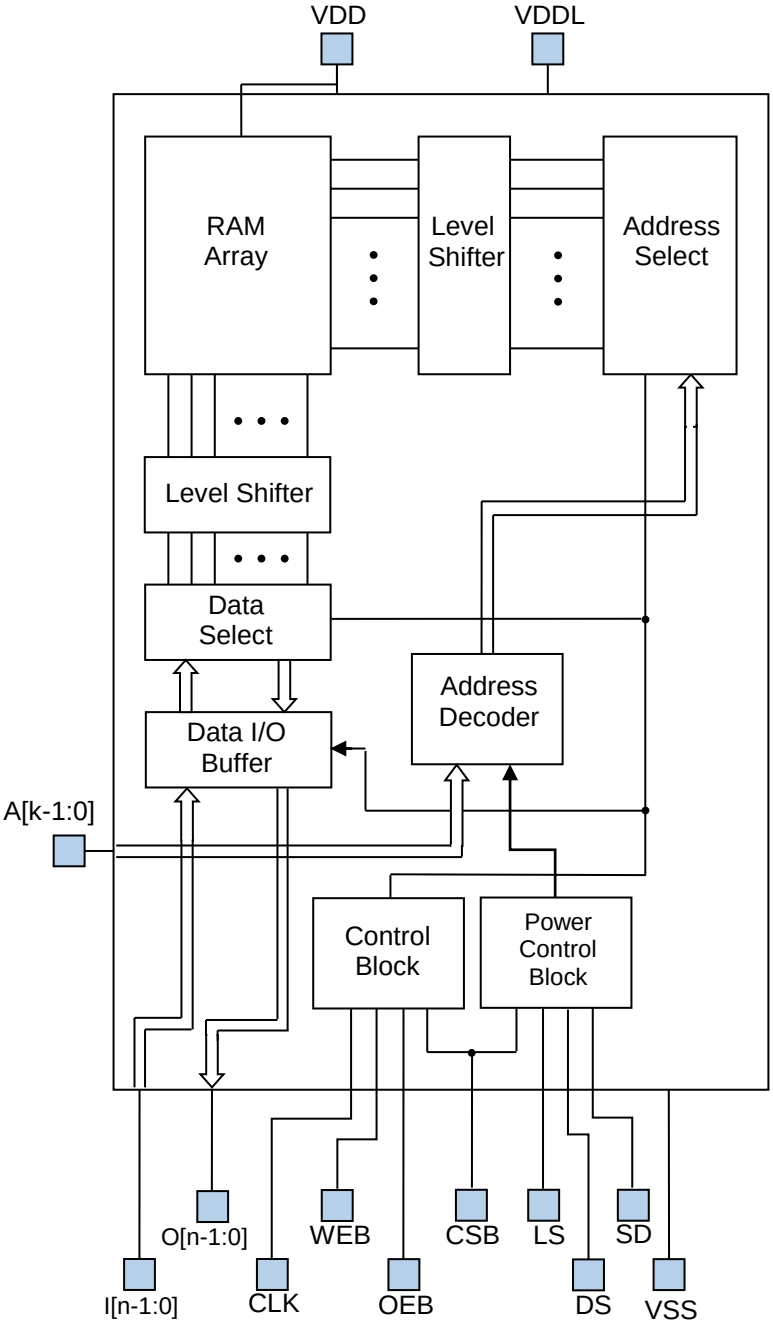


Figure 3.12. Single port SRAMLP1RWscmxn block diagram

Single port SRAMLP1RwscmxnBasic Operations is shown in Table 7.7.
Single port SRAMLP1Rwscmxnaccess is synchronous and triggered by the rising edge of the clock signal (CLK). Read/Write addresses (A), Input data (I), Write enable (WEB), Light Sleep (LS), Deep Sleep (DS), Shut Down (SD) and Chip select (CSB) signals are latched by the rising edge of the clock (CLK).

Table 3.8 Single port SRAMLP1RwscmxnBasic Operations

Pins									Data in Memory	Access to Memory	Operation
A[k-1:0]	WEB	OEB	CSB	LS	DS	SD	I [n-1:0]	O[n-1:0] (t+1)	D(A[k-1:0]) (t+1)		
X	X	0 1	1	0	0	0	Disabled	O[n-1:0] (t) Z	D(A[k-1:0]) (t)	No	Standby
X	0	0 1	0	0	0	0	Enabled	I[n-1:0] Z	I[n-1:0]	Yes	Write
X	1	0 1	0	0	0	0	X	D(A[k-1:0]) (t) Z	D(A[k-1:0]) (t)	No	Read
X	X	X	1	1	0	0	Disabled	O[n-1:0] (t)	D(A[k-1:0]) (t)	No	Light Sleep
X	X	X	1	0	1	0	Disabled	0	D(A[k-1:0]) (t)	No	Deep Sleep
X	X	X	1	0	0	1	Disabled	0	Z	No	Shut Down

Note: O[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.
O[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.

3.4.3. Operation modes of single port SRAMLPscmxn

Read Mode: The value of Chip Select signal is low (CSB=0) for read operation. The SRAMLPscmxn enter read mode when CS=0 and WEB=1. In this mode the LS, DS and SD signals are inactive. During read operations, data read from the memory location D(A[k-1:0]) specified on the address bus I[n-1:0] and appear on the data output bus O[n-1:0].

Normal Write Mode: In Normal Write mode the value of Chip Select signal is low (CSB=0) for write operation. Single port SRAMLPscmxn enter write mode when CSB=0 and WEB=0. In this mode the LS, DS and SD signals are inactive. During write mode, data on the data input bus I[n-1:0] is writing into the memory location D(A[k-1:0]) specified on the address bus I[n-1:0].
If OEB=1, data on the output bus O[n-1:0] placed in Z state. At that time read/write operation continues. When OEB=0, the data appear on the output bus O[n-a:0].

Standby Mode: The standby mode is provided to further reduce power dissipation during periods of non-operation (CSB=1). While in standby mode, address and data inputs are

disabled; data stored in the memory D(A[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

Light Sleep Mode: When the memory is in Stadby mode (CSB=1) and the LS pin is active, then the memory goes into Light Sleep mode. In this mode VDDL supply voltage of periphery is reduced down to 0.7v. In Light Sleep mode DS, SD signals are inactive and the output state doesn't change.

Deep Sleep Mode: In this mode the value of Chip Select signal is high (CSB=1) in this mode, and LS and SD signals are inactive. If DS pin is set, he power to periphery is shut down completely and the power to the memory core is reduced down to 0.5v. In this mode memory contents is retained, but the outputs of the memory are pulled low.

Shut Down Mode: The SRAMLPscmxn enters this mode, when the value of SD signal is high. When the SD pin is set, there is a complete shutdown (both the periphery and array are power gated), with no data retention, and the memory outputs are pulled low.

Mentioned low power techniques differ not only with power consumption efficiency, but also with timing parameters. The timing parameters of low power pins are shown in Table 7.10.

3.4.4. Single port SRAMLP1RwscmxnTiming Waveforms

Single port SRAMLP1Rwmxnfunctions according to the block-diagrams shown in Figures 6.13 – 6.18.

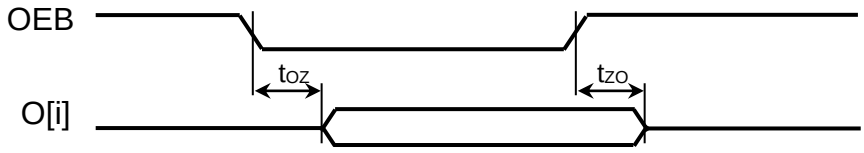


Figure 3.13. Single port SRAMLP1RwscmxnOutput-Enable Timing Waveforms

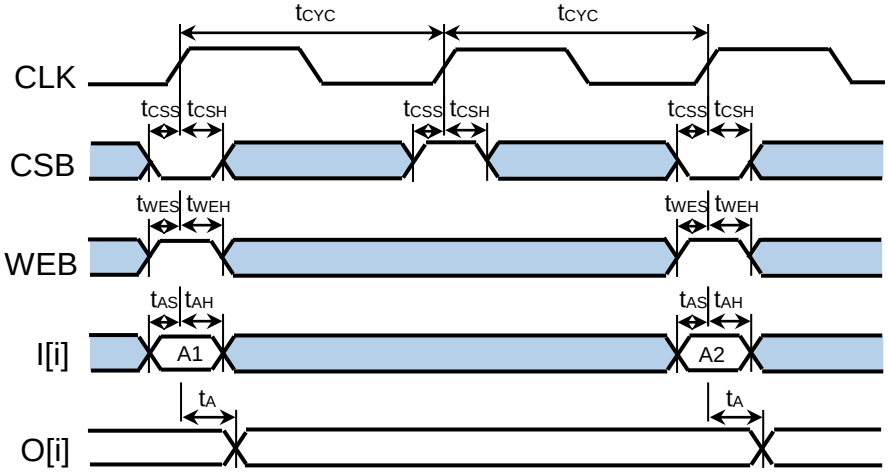


Figure 3.14. Single port SRAMLP1RWscmxn Read-Cycle Timing Waveforms

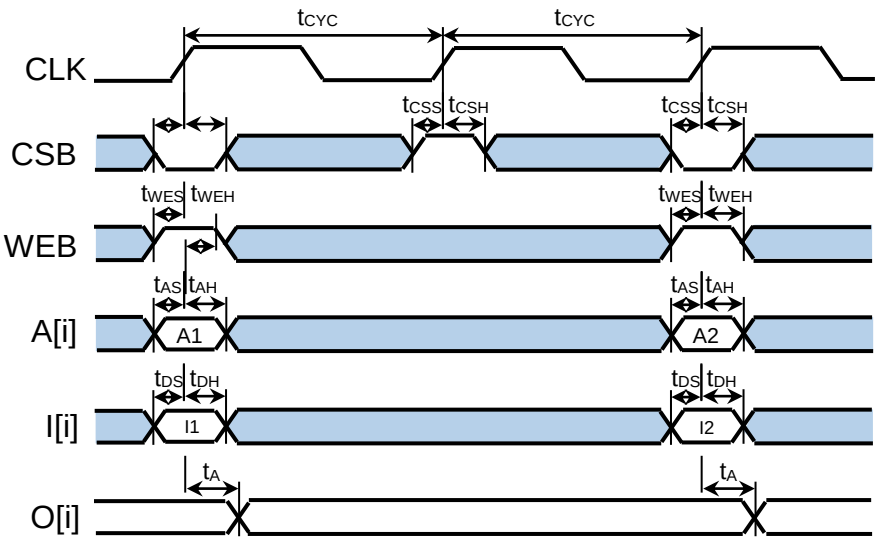


Figure 3.15. Sihgle port SRAMLP1RWscmxn Write-Cycle Timing Waveforms

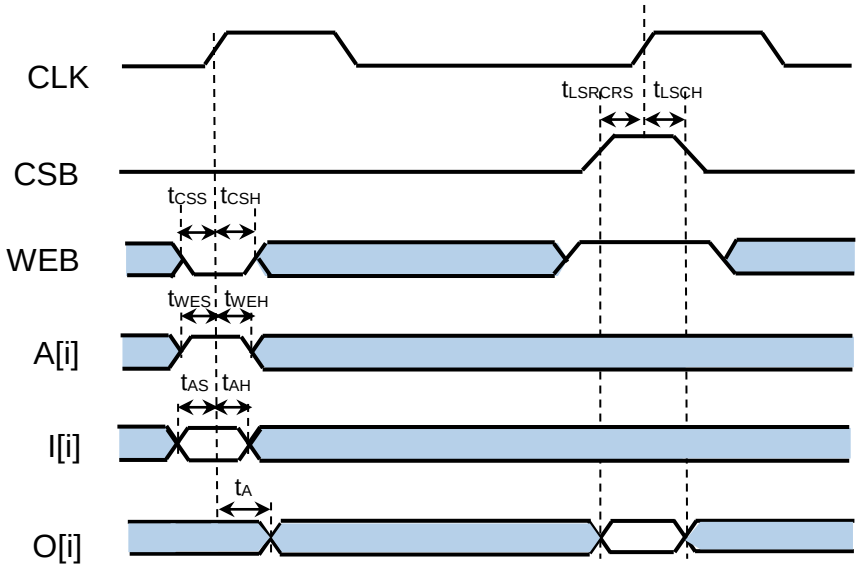


Figure 3.16. Sihgle port SRAMLP1RWscmxn Write-Cycle Timing Waveforms with Lights Sleep state

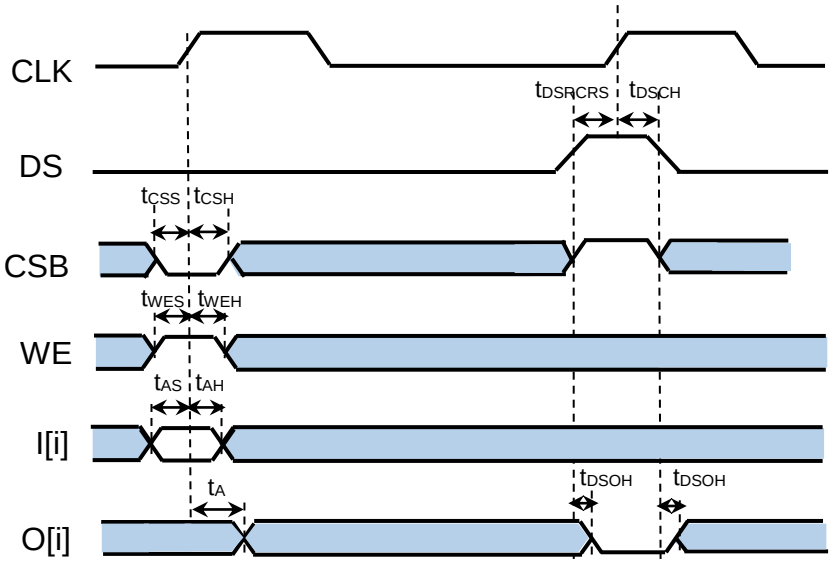


Figure 3.17. Sihgle port SRAMLP1RWscmxn Write-Cycle Timing Waveforms with Deep Sleep state

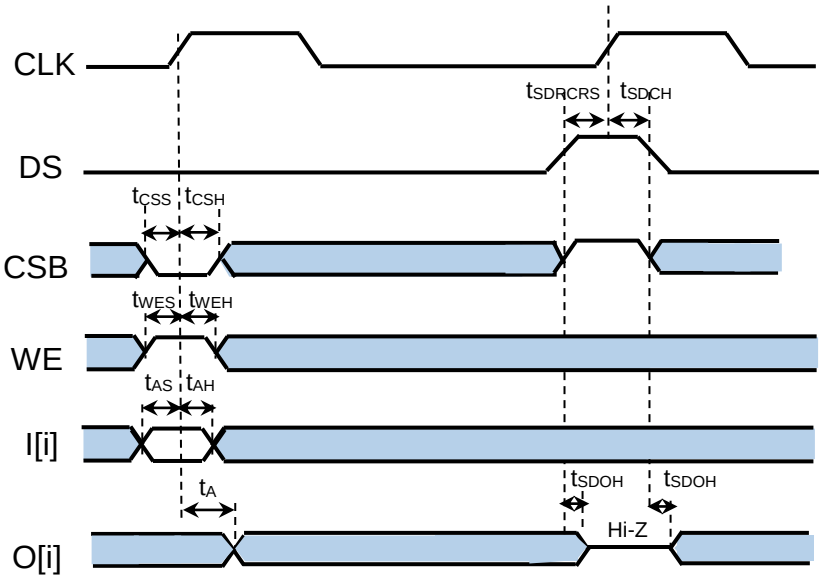


Figure 3.18. Sihgle port SRAMLP1RWscmxn Write-Cycle Timing Waveforms with Shat Down state

3.5. Operating conditions

The operating conditions of SAED_EDK14_FINFET_RAM_LP set of memories are shown in Table 6.9.

Table 3.9 Operating conditions

Parameter	Min	Typ	Max	Units
Power supply range	0.72	0.8	0.88	V
Operating Temperature	-40	+25	+125	°C
Operating Frequency (F)			1	GHz

3.6. Characterization corners

The timing data will be given only for 3 process/voltage/temperature (PVT) conditions shown in Table 6.12.

Table 3.10. Characterization Corners

#	Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (^{0}C)	Power Supply (V)	Power Supply (V)	Library Name Suffix
1	FF	ff0p88v25c_i0p88v	Fast-Fast	0.88	0.88	25
2	FF	ff0p88vm40c_i0p88v	Fast-Fast	0.88	0.88	-40
3	FF	ff0p88v125c_i0p88v	Fast-Fast	0.88	0.88	125
4	FF	ff0p88v25c_i0p72v	Fast-Fast	0.88	0.72	25
5	FF	ff0p88vm40c_i0p72v	Fast-Fast	0.88	0.72	-40
6	FF	ff0p88v125c_i0p72v	Fast-Fast	0.88	0.72	125
7	FF	ff0p88v25c_i0p64v	Fast-Fast	0.88	0.64	25
8	FF	ff0p88vm40c_i0p64v	Fast-Fast	0.88	0.64	-40
9	FF	ff0p88v125c_i0p64v	Fast-Fast	0.88	0.64	125
10	FF	ff0p72v25c_i0p72v	Fast-Fast	0.72	0.72	25
11	FF	ff0p72vm40c_i0p72v	Fast-Fast	0.72	0.72	-40
12	FF	ff0p72v125c_i0p72v	Fast-Fast	0.72	0.72	125
13	TT	tt0p64v25c_i0p64v	Typical-Typical	0.64	0.64	25
14	TT	tt0p64vm40c_i0p64v	Typical-Typical	0.64	0.64	-40
15	TT	tt0p65v125c_i0p65v	Typical-Typical	0.65	0.65	125
16	TT	tt0p59v25c_i0p59v	Typical-Typical	0.59	0.59	25
17	TT	tt0p59vm40c_i0p59v	Typical-Typical	0.59	0.59	-40
18	TT	tt0p59v125c_i0p59v	Typical-Typical	0.59	0.59	125
19	TT	tt0p8v25c_i0p8v	Typical-Typical	0.8	0.8	25
20	TT	tt0p8vm40c_i0p8v	Typical-Typical	0.8	0.8	-40
21	TT	tt0p8v125c_i0p8v	Typical-Typical	0.8	0.8	125
22	TT	tt0p8v25c_i0p59v	Typical-Typical	0.8	0.59	25
23	TT	tt0p8vm40c_i0p59v	Typical-Typical	0.8	0.59	-40
24	TT	tt0p8v125c_i0p59v	Typical-Typical	0.8	0.59	125
25	TT	tt0p8v25c_i0p64v	Typical-Typical	0.8	0.64	25
26	TT	tt0p8vm40c_i0p64v	Typical-Typical	0.8	0.64	-40

#	Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (^{0}C)	Power Supply (V)	Power Supply (V)	Library Name Suffix
27	TT	tt0p8v125c_i0p64v	Typical-Typical	0.8	0.64	125
28	SS	ss0p72v25c_i0p72v	Slow-Slow	0.72	0.72	25
29	SS	ss0p72vm40c_i0p72v	Slow-Slow	0.72	0.72	-40
30	SS	ss0p72v125c_i0p72v	Slow-Slow	0.72	0.72	125
31	SS	ss0p72v25c_i0p57v	Slow-Slow	0.72	0.57	25
32	SS	ss0p72vm40c_i0p57v	Slow-Slow	0.72	0.57	-40
33	SS	ss0p72v125c_i0p57v	Slow-Slow	0.72	0.57	125
34	SS	ss0p72v25c_i0p53v	Slow-Slow	0.72	0.53	25
35	SS	ss0p72vm40c_i0p53v	Slow-Slow	0.72	0.53	-40
36	SS	ss0p72v125c_i0p53v	Slow-Slow	0.72	0.53	125
37	SS	ss0p53v25c_i0p53v	Slow-Slow	0.53	0.53	25
38	SS	ss0p53vm40c_i0p53v	Slow-Slow	0.53	0.53	-40
39	SS	ss0p53v125c_i0p53v	Slow-Slow	0.53	0.53	125
40	SS	ss0p57v25c_i0p57v	Slow-Slow	0.57	0.57	25
41	SS	ss0p57vm40c_i0p57v	Slow-Slow	0.57	0.57	-40
42	SS	ss0p57v125c_i0p57v	Slow-Slow	0.57	0.57	125
43	SS	ss0p64v25c_i0p64v	Slow-Slow	0.64	0.64	25
44	SS	ss0p64vm40c_i0p64v	Slow-Slow	0.64	0.64	-40
45	SS	ss0p64v125c_i0p64v	Slow-Slow	0.64	0.64	125

Critical path, setup and hold analyses will be performed for the mentioned corners.