Lab 5: Static Timing Analysis

Objective

Learn how to use PrimeTime to validate the timing performance of a design by checking all possible paths for timing violations, without using logic simulation or test vectors.

Reports

Please include the results and any problems and findings in the report, especially:

1. Screenshot of design after each step
2. Generated scripts & reports

Introduction

PrimeTime is a full-chip, gate-level static timing analysis tool that is an essential part of the design and analysis flow for today's large chip designs.

Laboratory Tasks

PrimeTime can be used after Design Compiler or IC Compiler. The difference is that after IC Compiler parasitics netlist in SPEF format can be used by PrimeTime for timing calculation. The steps to run PrimeTime with the results from Design Compiler are very similar.

1. Copy lab05 folder and move to the working directory lab05

```
$ cp -a /home/tools/synopsys/m3/lab05 $HOME/icdesign/m3
$ cd $HOME/icdesign/m3/lab05
$ source /home/tools/synopsys/env.sh
```

2. Run the synthesis with the following command

The following command will run the synthesis that we did from the previous lab.

```
$ cd $HOME/icdesign/m3/lab05/syn
$ dc_shell -f scripts/compile.tcl 2>&1 | tee run.log
```

3. Run the floorplan, placement and route with the following command

The following command will run the synthesis that we did from the previous lab.

```
$ cd $HOME/icdesign/m3/lab05/pnr
$ icc2_shell -f scripts/flow.tcl 2>&1 | tee run.log
```

4. Open the cell after Place & Route and write out the necessary file

```
$ icc2_shell -gui
```

Click on “open existing blocks”. Select the library and open the block “11_i2c_master_top_route_finish”

Run the following command to write out necessary files for primetime:

```
icc2_shell> write_parasitics -output ../results/i2c_master_top.max.spef -no_name_mapping \
                -compress -hierarchical -rde_corr -format spef -corner slow
icc2_shell> write_parasitics -output ../results/i2c_master_top.min.spef -no_name_mapping \
                -compress -hierarchical -rde_corr -format spef -corner fast
icc2_shell> write_verilog ../results/i2c_master_top.pnr.v -include all
```

5. Start PrimeTime graphical user interface (GUI) from **sta** directory. To start it enter:

```
$ cd $HOME/icdesign/m3/lab05/sta
$ pt_shell
pt_shell> start_gui
```

This opens the PrimeTime top-level GUI window. (Fig. 1)

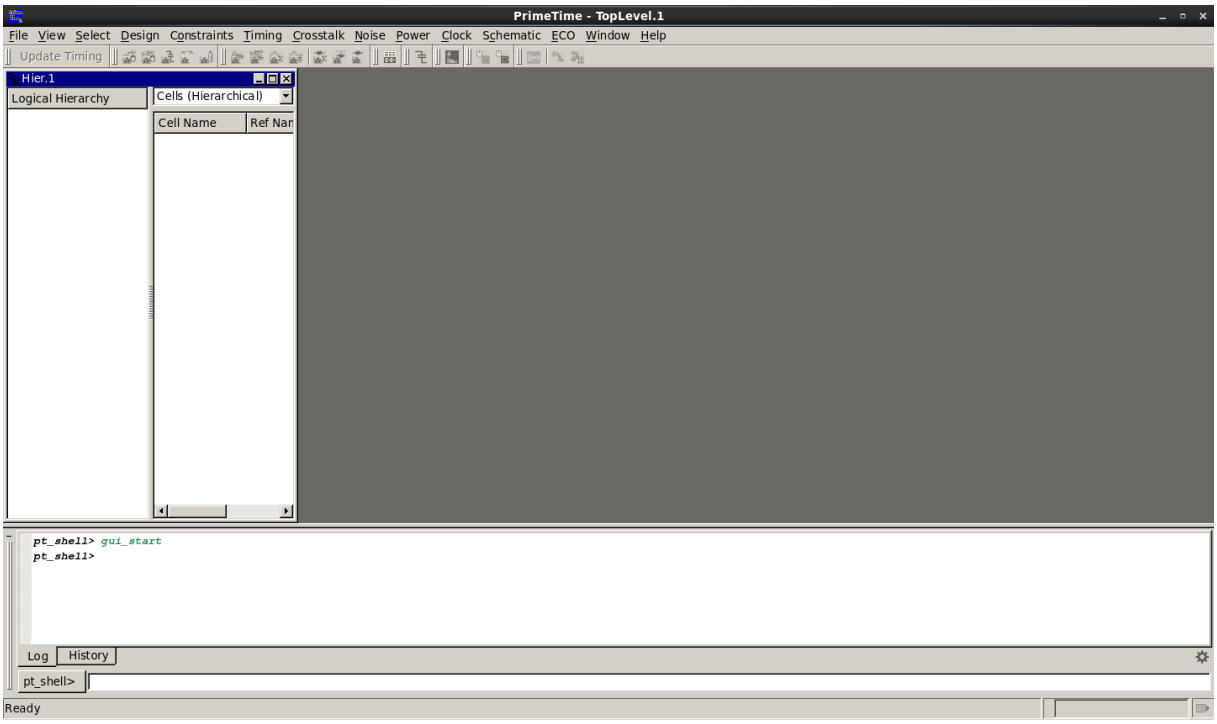

Fig.1. PrimeTime Top-level GUI window

6. The libraries are appended to the search path from .synopsys_pt.setup file located in **work** directory. The setup file includes the following:

```
pt_shell> source ../common/common.tcl
```

7. Setup the library

```
pt_shell> set link_library "* saed14rvt_ss0p6v125c.db"
```

To check hold timing first enter **reset_design** command in command line, then source the **sta_post_min.tcl** script.

Now run the followign step:.

8. Read the design netlist. (Fig. 2) PrimeTime accepts design gate-level netlists in Verilog and VHDL formats. Read design netlist with the following command: read_verilog, read_vhdl.

```
pt_shell> read_verilog [list ../results/i2c_master_top.pnr.v]
pt_shell> current_design i2c_master_top
```

9. For a design to be complete, it needs to be connected to all of the library components and designs it references. So to perform a name-based resolution of design references for the current design use the link command. The references must be located and linked to the current design in order for the design to be functional. The purpose of this command is to locate all of the designs and library components referenced in the current design and connect (link) them to the current design.

```
pt_shell> link
```

10. Read the design constraints and parasitics. Read design constraints using following command:.

```
pt_shell> source -echo -verbose ../inputs/i2c_master_top_icc.sdc
pt_shell> read_parasitics ../results/i2c_master_top.max.spef
```

11. Get a detailed report on all constraint violations in the design with **report_constraint -all_violators**.

```
pt_shell> file mkdir reports
```

```
pt_shell> report_constraint -all_violators -significant_digits 4 > reports/i2c_master_top.max_constr.rpt
```

12. The **report_timing** command is the most flexible and powerful PrimeTime analysis command. The **-delay_type** option specifies the type of timing checks to report. Set the delay type to **max** for setup checks, **min** for hold checks.

```
pt_shell> report_timing -delay_type max -nworst 40 -significant_digits 4 \
                > reports/i2c_master_top.max_timing.rpt
```

In reports it is possible to have violations, for example hold or setup violation. To correct the hold violation, add buffers to the respective port. And for correcting the setup violation increase the area of cells. Here is an example of a report that has no violations.

The report can also be seen in the Timing Analysis Driver Console by remarking one of the rows and clicking the inspector button. See Fig. 2, and Fig.3.

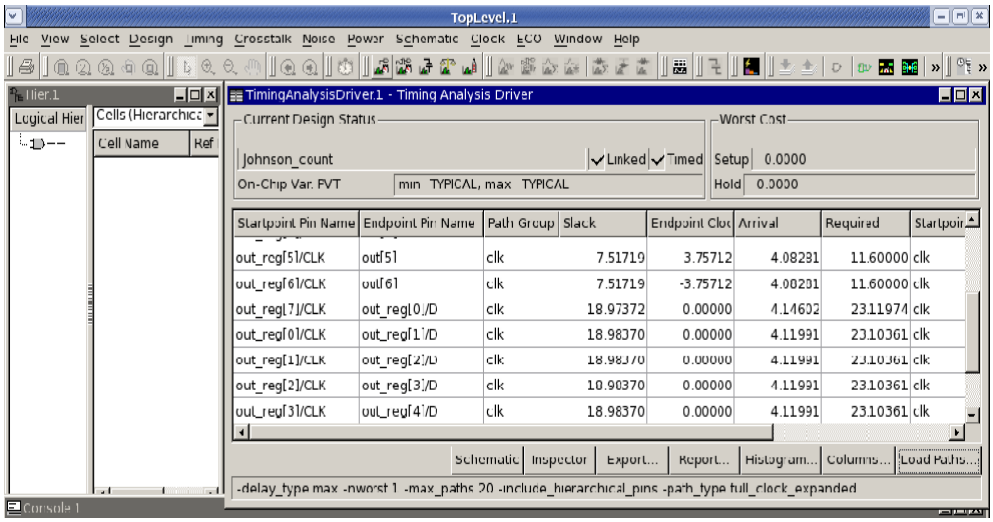

Fig. 2. The Timing Analysis Driver

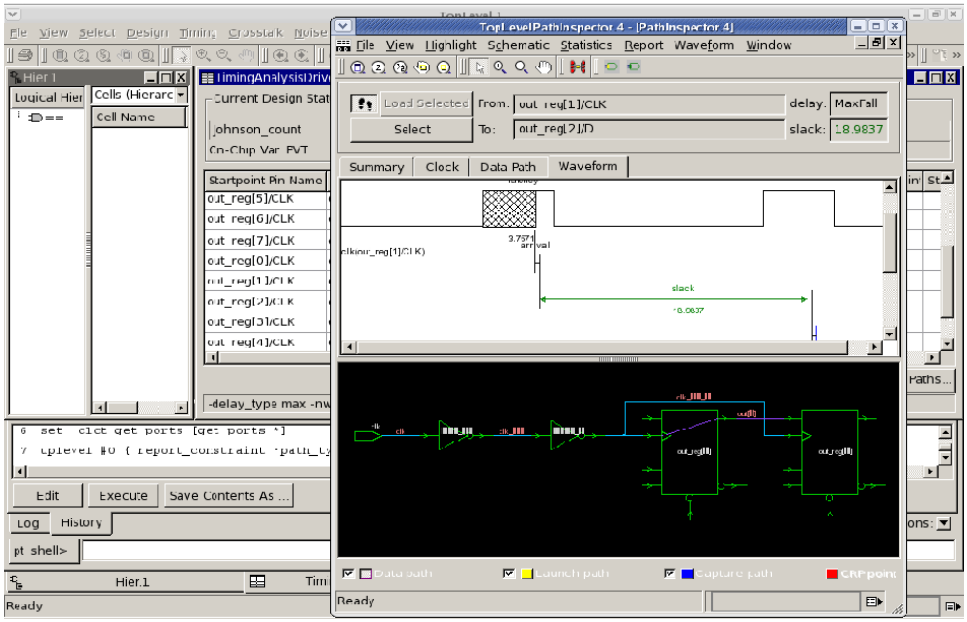

Fig. 3. Path Inspector console

13. The output file of PrimeTime is Standard Delay Format (.sdf) and it includes delay information, such as pin-to-pin cell delays and net delays, and timing checks, such as setup, hold, recovery, and removal times. In the script it was done using the following command:

```
pt_shell> write_sdf ../results/i2c_master_top.max.sdf
```

In this design, output results are stored in ../**results/** directory.

14. Reset the design and run the process above again but now with the hold check

```
pt_shell> reset_design
pt_shell> set link_library "* saed14rvt_ff0p6v125c.db"
pt_shell> read_verilog [list ../results/i2c_master_top.pnr.v]
pt_shell> current_design i2c_master_top
pt_shell> link
pt_shell> source -echo -verbose ../inputs/i2c_master_top_icc.sdc
pt_shell> read_parasitics ../results/i2c_master_top.min.spef
pt_shell> report_constraint -all_violators -significant_digits 4 > reports/i2c_master_top.min_constr.rpt
pt_shell> report_timing -delay_type min -nworst 40 -significant_digits 4 \
                > reports/i2c_master_top.min_timing.rpt
pt_shell> write_sdf ../results/i2c_master_top.max.sdf
```

15. To exit PrimeTime write:

```
pt_shell> exit
```