= Preliminary =

AK4493S

Quality Oriented 32-Bit 2ch DAC

1. General Description

The AK4493S is a new generation Premium 32-bit 2ch DAC with VELVET SOUND™ technology, achieving industry's leading level low distortion characteristics. The newly adopted OSR-Doubler technology establishes wide signal band, low power consumption and low distortion characteristics. Moreover, the AK4493S has six types of 32-bit digital filters, realizing simple and flexible sound tuning in a wide range of applications. The AK4493S accepts up to 768kHz PCM data and 22.4MHz DSD data, ideal for high-resolution audio source playback that is becoming widespread in network audio, USB-DAC, etc.

Application: AV Receivers, CD/SACD Players, Network Audios, USB DACs, USB Headphones, Sound Plates/Bars, Measurement Equipment, Control Systems, IC-Recorder, Bluetooth Headphone, HD Audio/Voice Conference Systems.

2. Features

- **THD+N: -113dB**
- **DR, S/N: 123dB (2Vrms), 125dB (Large Amplitude Mode), 126dB (Mono Mode)**
- **256 Times Over Sampling**
- **Sampling Rate: 8kHz ~ 768kHz**
- **32-bit 8x Digital Filter**
  - **Short Delay Sharp Roll-off, GD = 6.0/fs,**
  - **Short Delay Slow Roll-off, GD = 5.0/fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**
  - **Low Dispersion Short Delay Filter**
  - **Super Slow Roll-off**
- **High Tolerance to Clock Jitter**
- **Low Distortion/ Low Noise High Performance Differential Amplifier Output**
- **Large Amplitude Output Mode**
- **DSD64, DSD128, DSD256, DSD512 Input Support**
  - **Filter1 (fc = 39kHz, DSD64 mode), Filter2 (fc = 76kHz, DSD64 mode)**
- **Digital De-emphasis for 32, 44.1 and 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step + mute)**
- **Mono Mode**
- **External Digital Filter Interface**
- **Audio I/F Format: 24/32 bit MSB justified, 16/20/24/32 bit LSB justified, I²S, DSD, TDM**
- **Master Clock**
  8kHz ~ 32kHz: 256fs or 384fs or 512fs or 768fs or 1152fs
  32kHz ~ 54kHz: 256fs or 384fs or 512fs or 768fs
  54Hz ~ 108kHz: 256fs or 384fs
  108kHz ~ 216kHz: 128fs or 192fs
  216kHz ~ 388kHz: 32fs or 48fs or 64fs or 96fs
  388kHz ~ 776kHz: 16fs or 32fs or 48fs or 64fs
- **3-wire, I²C-bus Register Control Interface, or Pin Control**
- **Power Supply:**
  TVDD = AVDD = 3.0 ~ 3.6V (by internal LDO), VDDL/R = 4.75 ~ 5.25V
  TVDD = AVDD = DVDD ~ 3.6V (by external supply), DVDD = 1.7V ~ 1.98V
  VDDL/R = 4.75 ~ 5.25V

- **Operational Temperature: -40 ~ 85 °C**
- **Digital Input Level: CMOS**
- **Package: 48-pin LQFP**

3. Table of Contents

4. Block Diagram

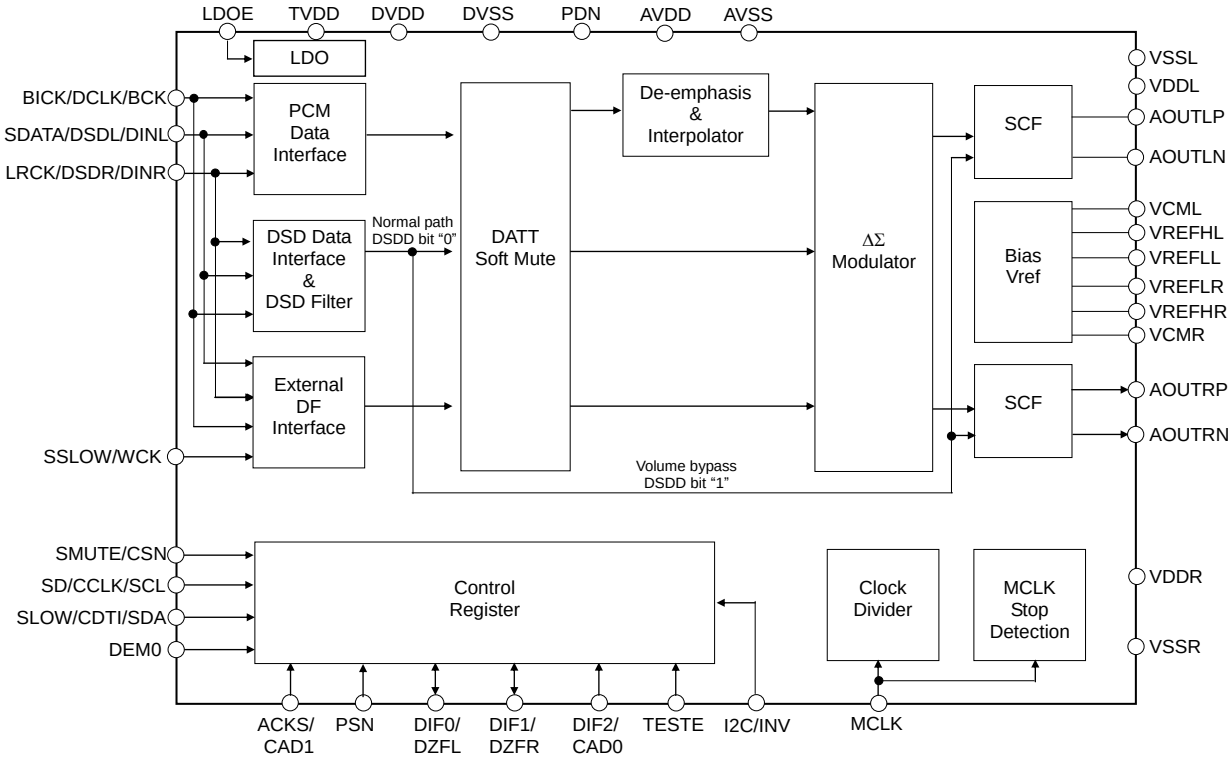


Figure 1. Block Diagram

Block	Function
PCM Data Interface	Execute serial/parallel conversion of SDATA input data by synchronizing with LRCK and BICK and generate TDM output data.
DSD Data Interface	1-bit data that is input from DSDL and DSDR pins is received by synchronizing with DCLK.
DSD Filter	FIR filter that reduces high frequency noise of DSD input data
DATT, Soft Mute	Apply DATT and Soft Mute process to input data.
De-emphasis & Interpolator	A digital filter that applies De-emphasis process to input data and executes over sampling.
ΔΣ Modulator	Output multi-bit data to SCF. This block consists of a third-order digital delta-sigma modulator.
SCF	Convert multi bit output of ΔΣ Modulator into analog signal. This block consists of the switched capacitor DAC.
Control Register	Keep register settings for each mode. Control registers are accessed in 3-wire (CSN, CCLK, CDTI) or I2C-Bus (SCL, SDA) control mode.
Clock Divider	Divide Master Clock In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode, the master clock frequency is set by DCKS bit.
MCLK Stop Detection	It is the detection circuit of MCLK input or no input.
Bias, Vref	It outputs common voltage VCML/R that is generated by reference voltage VREFHL/R and VREFLL/R.
LDO	It is the power supply circuit for internal digital circuit. Its power supply voltage is typical 1.8V.

5. Pin Configurations and Functions

■ Pin Configurations

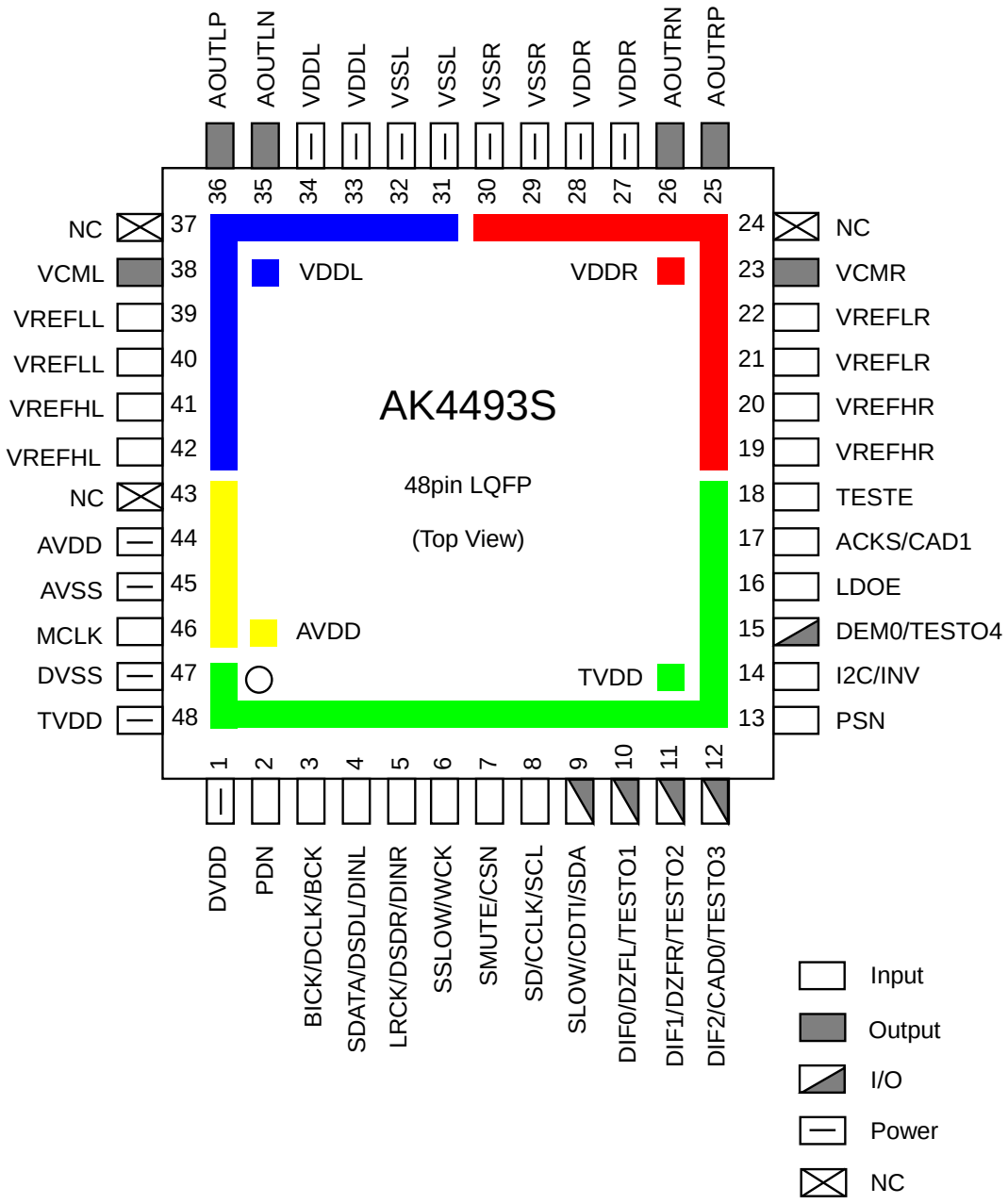


Figure 2. Pin Layout

■ Pin Functions

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
1	DVDD	O	-	(LDOE pin = "H") LDO Output Pin, this pin should be connected to DVSS with 1.0μF (±50%). This pin is inhibited to connect other devices.	Pull-down to DVSS (500Ω)
		-		(LDOE pin = "L") 1.8V Power Input Pin	Hi-Z
2	PDN	I	TVDD/DVSS	Power-Up, Power-Down Pin When at "L", the AK4493S is in power-down mode and is held in reset. The AK4493S must always be reset upon power-up.	Hi-Z (PDN = "L")
3	BICK	I	TVDD/DVSS	Audio Serial Data Clock Pin in PCM Mode	Hi-Z
	BCK	I		Audio Serial Data Clock Pin in EXDF Mode	
	DCLK	I		DSD Clock Pin in DSD Mode	
4	SDATA	I	TVDD/DVSS	Audio Serial Data Input Pin in PCM Mode	Hi-Z
	DINL	I		Lch Audio Serial Data Input Pin in EXDF Mode	
	DSDL	I		DSD Lch Data Input Pin in DSD Mode	
5	LRCK	I	TVDD/DVSS	L/R Clock Pin in PCM Mode	Hi-Z
	DINR	I		Rch Audio Serial Data Input Pin in EXDF Mode	
	DSDR	I		DSD Rch Data Input Pin in DSD Mode	
6	SSLOW	I	TVDD/DVSS	Digital Filter Select Pin in Pin Control Mode	Hi-Z
	WCK	I		Word Clock input pin in EXDF Mode	
7	SMUTE	I	TVDD/DVSS	When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.	Hi-Z
	CSN	I		Chip Select Pin in Register Control Mode	
8	SD	I	ー /DVSS	Digital Filter Select Pin in Pin Control Mode	Hi-Z
	CCLK	I		Control Data Clock Pin in Register Control Mode	
	SCL	I		I2C="H": Control Data Clock Input Pin	
9	SLOW	I	ー /DVSS	Digital Filter Select Pin in Pin Control Mode	Hi-Z
	CDTI	I		Control Data Input Pin in Register Control Mode	
	SDA	I/O		I2C="H": Control Data Input Pin	
10	DIF0	I	TVDD/DVSS	Digital Input Format 0 Pin in Pin Control Mode	Pull-Down to DVSS (100kΩ)
	DZFL	O		Lch Zero Input Detect Pin in Register Control Mode (Internal pull-down pin)	
	TESTO1	O		Test Signal Output Pin in SCAN Test Mode	
11	DIF1	I	TVDD/DVSS	Digital Input Format 1 Pin in Pin Control Mode	Pull-Down to DVSS (100kΩ)
	DZFR	O		Rch Zero Input Detect Pin in Register Control Mode (Internal pull-down pin)	
	TESTO2	O		Test Signal Output Pin in SCAN Test Mode	
12	DIF2	I	TVDD/DVSS	Digital Input Format 2 Pin in Pin Control Mode	Hi-Z
	CAD0	I		Chip Address 0 Pin in Register Control Mode	
	TESTO3	O		Test Signal Output Pin in SCAN test & Pin function test	
13	PSN	I	TVDD/DVSS	Pin Control Mode or Register Control Mode Select Pin (Internal pull-up pin) "L": Register Control Mode, "H": Pin Control Mode	Pull-Up to TVDD (100kΩ)
14	INV	I	TVDD/DVSS	L/Rch Output Polarity Select Pin in Pin Control Mode	Hi-Z
	I2C	I		Resister Control Interface Pin in Register Control Mode	
15	DEM0	I	TVDD/DVSS	De-emphasis Enable 0 Pin in Pin Control Mode	Hi-Z
	TESTO4	O		Test Signal Output Pin in SCAN test & Pin function test	
16	LDOE	I	TVDD/DVSS	Internal LDO Enable Pin. "L": Disable, "H": Enable	Pull-Up to TVDD (100kΩ)

No.	Pin Name	I/O	Protection Diode	Function	PowerDown State
17	ACKS	I	TVDD/DVSS	Auto Setting Mode Select Pin in Pin control mode “L”: Manual Setting Mode, “H”: Auto Setting Mode	Hi-Z
	CAD1	I		Chip Address 1 Pin in Register Control Mode	
18	TESTE	I	TVDD/DVSS	Test Mode Enable Pin (Internal pull-down pin)	Pull-Down to DVSS (100kΩ)
19 20	VREFHR	I	VDDR/VSSR	Rch High Level Voltage Reference Input Pin	Hi-Z
21 22	VREFLR	I	VDDR/VSSR	Rch Low Level Voltage Reference Input Pin	Connected to VCMR (5kΩ)
23	VCMR	-	VDDR/VSSR	Right channel Common Voltage Pin, Normally connected to VREFLR with a 10uF electrolytic cap. This pin is inhibited to connect other devices.	Connected to VREFLR (5kΩ)
24	NC	-	-	No internal bonding.Connect to GND.	-
25	AOUTRP	O	VDDR/VSSR	Rch Positive Analog Output Pin	Connected to AOUTRN (300kΩ)
26	AOUTRN	O	VDDR/VSSR	Rch Negative Analog Output Pin	Connected to AOUTRP (300kΩ)
27 28	VDDR	-	-	Rch Analog Power Supply Pin	-
29 30	VSSR	-	-	Analog Ground Pin	-
31 32	VSSL	-	-	Analog Ground Pin	-
33 34	VDDL	-	-	Lch Analog Power Supply Pin .	-
35	AOUTLN	O	VDDL/VSSL	Lch Negative Analog Output Pin	Connected to AOUTLP (300kΩ)
36	AOUTLP	O	VDDL/VSSL	Lch Positive Analog Output Pin	Connected to AOUTLN (300kΩ)
37	NC	-	-	No internal bonding.Connect to GND.	-
38	VCML	-	VDDL/VSSL	Left channel Common Voltage Pin, Normally connected to VREFLL with a 10uF electrolytic cap. This pin is inhibited to connect other devices.	Connected to VREFLL (5kΩ)
39 40	VREFLL	I	VDDL/VSSL	Lch Low Level Voltage Reference Input Pin	Connected to VCML (5kΩ)
41 42	VREFHL	I	VDDL/VSSL	Lch High Level Voltage Reference Input Pin	Hi-Z
43	NC	-	-	No internal bonding. Connect to GND.	-
44	AVDD	-	-	Analog Power Supply Pin, (LDOE pin = “H”) AVDD=3.0 ~ 3.6V (LDOE pin = “L”) AVDD=DVDD ~ 3.6V	-
45	AVSS	-	-	Analog Ground Pin	-
46	MCLK	I	AVDD/AVSS	Master Clock Input Pin	Hi-Z
47	DVSS	-	-	Digital Ground Pin	-
48	TVDD	-		Digital Power Supply Pin, (LDOE pin = “H”) TVDD=3.0 ~ 3.6V (LDOE pin = “L”) TVDD=DVDD ~ 3.6V	-

Note 1. All input pins except internal pull-up/down pins must not be left floating.

Note 2. The AK4493S must be reset by the PDN pin when changing control mode (Pin Control ⇔ Register Control) by the PSN pin.

Note 3. PCM mode, DSD mode and EXDF mode are controlled by register settings.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

(1) Pin Control Mode (PCM mode only)

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	TESTE	Connect to DVSS or Open

(2) Register Control Mode

1. PCM Mode

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	WCK, DEM0	Connect to DVSS
	TESTE	Connect to DVSS or Open
	DZFL, DZFR	Open

2. DSD Mode

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	WCK, DEM0	Connect to DVSS
	TESTE	Connect to DVSS or Open
	DZFL, DZFR	Open

3. EXDF Mode

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	DEM	Connect to DVSS
	TESTE	Connect to DVSS or Open
	DZFL, DZFR	Open

4. With I2C-Bus

Classification	Pin Name	Status
Digital	CSN	Connect to DVSS

5. Pull-up, Pull-down Pin List

Classification	Pin Name	Internal connection
pull-up pin (typ = 100kΩ)	LDOE, PSN	TVDD
pull-down pin(typ = 100kΩ)	DZFL, DZFR, TESTE	DVSS

6. Absolute Maximum Ratings

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0V; Note 4)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Digital I/O	TVDD	–0.3	4.0	V
	Digital Core	DVDD	–0.3	2.35	V
	Clock Interface	AVDD	–0.3	4.0	V
	Analog	VDDL/R	–0.3	6.0	V
	|AVSS – DVSS| (Note 5)	ΔGND	-	0.3	V
	|AVSS – VSSL| (Note 5)	ΔGND	-	0.3	V
	|AVSS – VSSR| (Note 5)	ΔGND	-	0.3	V
	|DVSS – VSSL| (Note 5)	ΔGND	-	0.3	V
	|DVSS – VSSR| (Note 5)	ΔGND	-	0.3	V
	|VSSL – VSSR| (Note 5)	ΔGND	-	0.3	V
Voltage Reference	"H" voltage reference (Note 6)	VREFHL/R	-0.3	VDDL/R+0.3 Or 6.0	V
	"L" voltage reference	VREFLL/R	-0.3	+0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 7)		VIND	–0.3	TVDD+0.3 or 4.0	V
Ambient Temperature (Power supplied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 4. All voltages with respect to ground.
Note 5. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.
Note 6. Regarding VREFHL/R pins, maximum value which is lower value (VDDL/R+0.3) or 6.0V.
Note 7. Regarding Digital input pins, maximum value which is lower value (VDDL/R+0.3) or 4.0V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0V; Note 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 8)	■ LDOE pin = "L"					
	Digital I/O	TVDD	DVDD	1.8	3.6	V
	Clock Interface	AVDD	DVDD	1.8	3.6	V
	Digital Core	DVDD	1.7	1.8	1.98	V
	Analog	VDDL/R	4.75	5.0	5.25	V
	■ LDOE pin = "H"					
	Digital I/O	TVDD	3.0	3.3	3.6	V
	Clock Interface	AVDD	3.0	3.3	3.6	V
	Analog	VDDL/R	4.75	5.0	5.25	V
Voltage Reference (Note 8)	"H" voltage reference	VREFHL/R	VDDL/R-0.5	-	VDDL/R	V
	"L" voltage reference	VREFLL/R	-	VSSL/R	-	V

Note 4. All voltages with respect to ground.

Note 8. The analog output voltage scales with the voltage of (VREFHL/R – VREFLL/R).

Note 9. TVDD must be powered up before AVDD or at the same time. When not using the internal LDO (LDOE pin = "L"), TVDD must be powered up before DVDD or at the same time.

Note 10. The internal LDO outputs DVDD (1.8V) when the LDOE pin = "H".

*** AKM assumes no responsibility for the usage beyond the conditions in this data sheet.**

8. Electrical Characteristics

■ Analog Characteristics

(Ta = 25°C; LDOE pin = "L", AVDD = TVDD = 3.3V, DVDD = 1.8V; AVSS = DVSS = VSSL/R = 0V; VREFHL/R = VDDL/R = 5.0V, VREFLL/R = 0V; Input data = 24bit; BICK = 64fs; Signal Frequency= 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Example Circuit 3 (Figure 81); SC[1:0] bits = "00"; 2Vrms output mode (GC[2:0] bits = "000"); unless otherwise specified.)

Parameter					Min.	Typ.	Max.	Unit
Resolution					-	-	32	Bit
Dynamic Characteristics (Note 11)								
THD+N	fs=44.1kHz	BW=20kHz	0dBFS	GC[2:0]="000"	-	-113	TBD	dB
				GC[2:0]="100"	-	-110	-	
			–60dBFS		-	-60	-	dB
	fs=96kHz	BW=40kHz	0dBFS		-	-110	-	dB
			–60dBFS		-	-57	-	dB
	fs=192kHz	BW=40kHz	0dBFS		-	-107	-	dB
			–60dBFS		-	-57	-	dB
		BW=80kHz	–60dBFS		-	-54	-	dB
	fs=384kHz	BW=40kHz	0dBFS		-	-107	-	dB
	fs=768kHz	BW=40kHz	0dBFS		-	-107	-	dB
Dynamic Range (–60dBFS with A-weighted) (Note 12)					TBD	123	-	dB
S/N (A-weighted) (Note 13)			GC[2:0] = "000"		TBD	123	-	dB
			GC[2:0] = "100"	Stereo mode	TBD	125	-	dB
				Mono mode (Note 17)	-	126	-	
Inter-channel Isolation					TBD	120	-	dB
DC Accuracy								
Inter-channel Gain Mismatch					-	0.15	TBD	dB
Gain Drift					-	20	-	ppm/°C
Output Voltage	GC[2:0] bits = "000" (Note 14)				TBD	±2.8	TBD	Vpp
	GC[2:0] bits = "100" (Note 15)				TBD	±3.75	TBD	Vpp
Load Resistance (Note 16)					450	-	-	Ω
Load Capacitance (Note 16)					-	-	25	pF

Note 11. Measured by Audio Precision APx555. Averaging mode.

Note 12. 101dB at 16bit data and 118dB at 20bit data.

Note 13. S/N ratio does not depend on input bit length.

Note 14. The analog output voltage with 0dBFS input signal when GC[2:0] bits = "000" is calculated by the following formula:

AOUTL/R (typ. @0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFHL/R – VREFLL/R)/5.

This expression is equivalent to 5.6Vpp and is differential and irrespective of ground reference or the Vcom bias voltage.

Note 15. The analog output voltage with 0dBFS input signal when GC[2:0] bits = "100" is calculated by the following formula:

AOUTL/R (typ. @0dB) = (AOUT+) – (AOUT–) = ±3.75Vpp × (VREFHL/R – VREFLL/R)/5.

This expression is equivalent to 7.5Vpp and is differential and irrespective of ground reference or the Vcom bias voltage.

Note 16. The load resistance value is 450 ohm (Min) against the DC load (No DC cut capacitor) with respect to ground. The load capacitance value with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore, the capacitive load must be minimized.

Note 17. When using the circuit shown in Figure 82

(Ta = 25°C; AVDD = TVDD = 3.3V, DVDD = 1.8V (LDOE pin = “L”), AVSS = DVSS = VSSL/R = 0V; VREFHL/R = VDDL/R = 5.0V, VREFLL/R = 0V; Input data = 24bit; BICK = 64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; SC[1:0] bits = “00”; 2Vrms output mode (GC[2:0] bits = “000”); unless otherwise specified.)

Power Supplies						
Parameter			**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current						
Normal operation (PDN pin = “H”)						
VDDL/R (total)			-	33	TBD	mA
VREFHL/R			-	1	TBD	mA
AVDD			-	1	TBD	mA
TVDD						
	LDOE pin = “H”	fs = 44.1kHz	-	9	TBD	mA
		fs = 96kHz	-	15	TBD	mA
		fs = 192kHz	-	23	TBD	mA
	LDOE pin = “L”		-	1	TBD	mA
DVDD						
	LDOE pin = “L”	fs = 44.1kHz	-	8	TBD	mA
		fs = 96kHz	-	14	TBD	mA
		fs = 192kHz	-	22	TBD	mA
Total IDD (fs = 44.1kHz)			-	44	TBD	mA
Power down (PDN pin = “L”) (Note 18) TVDD + AVDD + VDDL/R + DVDD			-	10	100	μA

Note 18. In power down mode, the PSN pin = TVDD and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held to DVSS.

Note 19. The DVDD pin becomes an output pin when the LDOE pin = “H”.

■ DSD Mode

(Ta = 25°C; AVDD = TVDD = 3.3V, DVDD = 1.8V (LDOE pin = "L"), AVSS = DVSS = VSSL/R = 0V; VREFHL/R = VDDL/R = 5.0V, VREFLL/R = 0V; Signal Frequency = 1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Example Circuit 3 (Figure 81); SC[1:0] bits = "00"; 2Vrms output mode (GC[2:0] bits = "000"); unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Dynamic Characteristics						
THD+N (Note 20)	DSD Datastream: DSD64	0dBFS	-	-113	-	dB
	DSD Datastream: DSD128	0dBFS	-	-113	-	dB
	DSD Datastream: DSD256	0dBFS	-	-113	-	dB
S/N (A-weighted, Normal path) (Note 20)	DSD Datastream: DSD64	Digital "0" (Note 23)	-	123	-	dB
	DSD Datastream: DSD128	Digital "0" (Note 23)	-	123	-	dB
	DSD Datastream: DSD256	Digital "0" (Note 23)	-	123	-	dB
DC Accuracy						
Output Voltage (Normal path)		(Note 14)	TBD	±2.8	TBD	Vpp
Output Voltage (Volume Bypass)		(Note 24)	TBD	±2.5	TBD	Vpp

Note 20. DSD Datastream: Analog characteristics are not guaranteed with DSD512 datastream.

Note 21. The peak level of DSD signal should be in the range of 25% ~ 75% duty according to the SACD format book (Scarlet Book).

Note 22. The output level is assumed as 0dB when a 1kHz 25% ~ 75% duty sine wave is input. Click noise may occur if the input signal exceeds 0dB.

Note 23. Digital "0" is a digital zero code pattern ("01101001") according to the SACD format book (Scarlet Book).

Note 24. When DSDD bit = "1", the analog output voltage at 25% ~ 75% input signal duty is calculated by the following equation:

$$\text{AOUTL/R (typ. @0dB)} = (\text{AOUTLP/RP}) - (\text{AOUTLN/RN})$$
$$= \pm 2.8\text{Vpp} \times (\text{VREFHL/R} - \text{VREFLL/R})/5.0.$$

This expression is equivalent to 5.6Vpp and is differential and irrespective of ground reference or the Vcom bias voltage.

Note 25. When DSDD bit = "1", the analog output voltage at 25% ~ 75% input signal duty is calculated by the following equation:

$$\text{AOUTL/R (typ. @0dB)} = (\text{AOUTLP/RP}) - (\text{AOUTLN/RN})$$
$$= \pm 2.5\text{Vpp} \times (\text{VREFHL/R} - \text{VREFLL/R})/5.0.$$

This expression is equivalent to 5.0Vpp and is differential and irrespective of ground reference or the Vcom bias voltage.

■ Sharp Roll-Off Filter Characteristics

Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7~ 1.98V; Normal Speed Mode; DEM = OFF; SD bit = "0" or SD pin = "L", SLOW bit = "0" or SLOW pin = "L", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	22.05	20.0 -	kHz kHz
Passband	(Note 27)	PB	0		20.0	kHz
Stopband	(Note 27)	SB	24.1			kHz
Passband Ripple	(Note 28)	PR			±0.005	dB
Stopband Attenuation	(Note 26)	SA	100			dB
Group Delay	(Note 296)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 20.0kHz		-	-0.2	-	+0.1	dB

Sharp Roll-Off Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Double Speed Mode; DEM = OFF; SD bit = "0" or SD pin = "L", SLOW bit = "0" or SLOW pin = "L", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	48.0	43.5 -	kHz kHz
Passband	(Note 27)	PB	0		43.5	kHz
Stopband	(Note 27)	SB	52.5			kHz
Passband Ripple	(Note 28)	PR			±0.005	dB
Stopband Attenuation	(Note 26)	SA	100			dB
Group Delay	(Note 296)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 40.0kHz			-0.6	-	+0.1	dB

Sharp Roll-Off Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Quad Speed Mode; DEM = OFF; SD bit = "0" or SD pin = "L", SLOW bit = "0" or SLOW pin = "L", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	96.0	87.0 -	kHz kHz
Passband	(Note 27)	PB	0		87.0	kHz
Stopband	(Note 27)	SB	104.9			kHz
Passband Ripple	(Note 28)	PR			±0.005	dB
Stopband Attenuation	(Note 26)	SA	100			dB
Group Delay	(Note 296)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 80.0kHz			-2.0	-	+0.1	dB

Note 26. Frequency response refers to the output level (0dB) of a 1kHz, 0dB sine wave input. Stopband attenuation band ranges from SB to 4fs.

Note 27. The passband and stopband frequencies scale with fs. For example, PB = 0.4535×fs (@±0.01dB), SB = 0.546×fs.
Note 28. This value is the gain amplitude of first step interpolator which is 4 times oversampling filter in pass band width.
Note 29. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

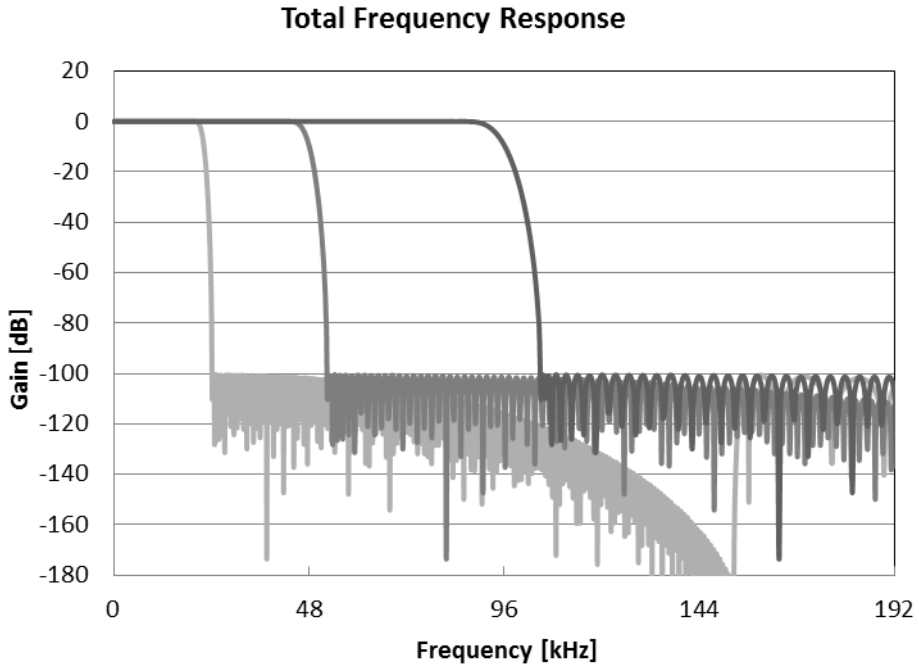


Figure 3. Sharp Roll-off Filter Frequency Response

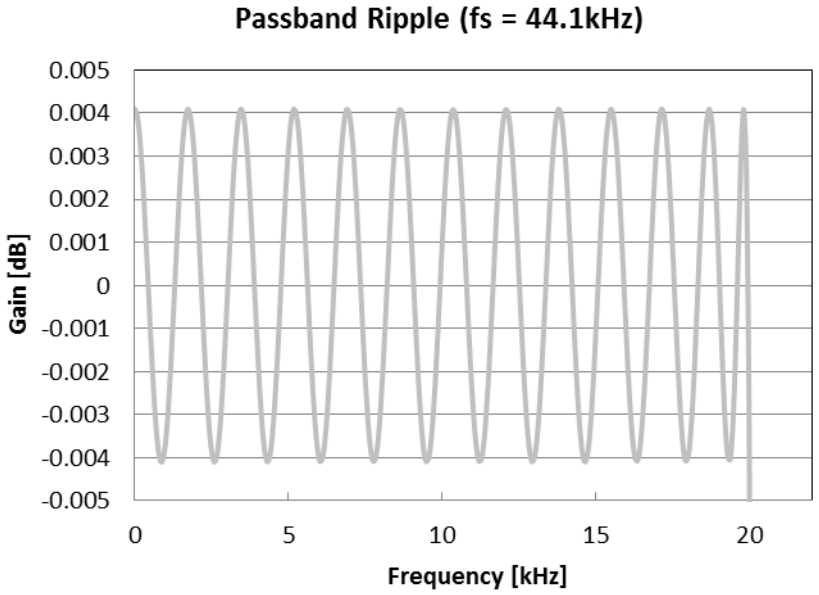


Figure 4. Sharp Roll-off Filter Passband Ripple

■ Slow Roll-Off Filter Characteristics

Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta = -40~85°C; VDDL/R = 4.75~5.25V, AVDD = TVDD = 1.7~3.6V, DVDD = 1.7~1.98V; Normal Speed Mode; DEM = OFF; SD bit = "0" or SD pin = "L", SLOW bit = "1" or SLOW pin = "H", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 21.0	8.0 -	kHz kHz
Passband	(Note 30)	PB	0	-	8.0	kHz
Stopband	(Note 30)	SB	39.2	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 26)	SA	92	-	-	dB
Group Delay	(Note 29)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 20.0kHz			-5.0	-	+0.1	dB

Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta = -40~85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7~3.6V, DVDD = 1.7~1.98V; Double Speed Mode; DEM = OFF; SD bit = "0" or SD pin = "L", SLOW bit = "1" or SLOW pin = "H", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 45.6	17.6 -	kHz kHz
Passband	(Note 30)	PB	0	-	17.6	kHz
Stopband	(Note 30)	SB	85.4	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 26)	SA	92	-	-	dB
Group Delay	(Note 29)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 40.0kHz			-3.8	-	+0.1	dB

Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Quad Speed Mode; DEM = OFF; SD bit = "0" or SD pin = "L", SLOW bit = "1" or SLOW pin = "H", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 91.2	35.2 -	kHz kHz
Passband	(Note 30)	PB	0	-	35.2	kHz
Stopband	(Note 30)	SB	170.7	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 26)	SA	100	-	-	dB
Group Delay	(Note 29)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 80.0kHz			-5.0	-	+0.1	dB

Note 307. The passband and stopband frequencies scale with fs.
For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8889 × fs.

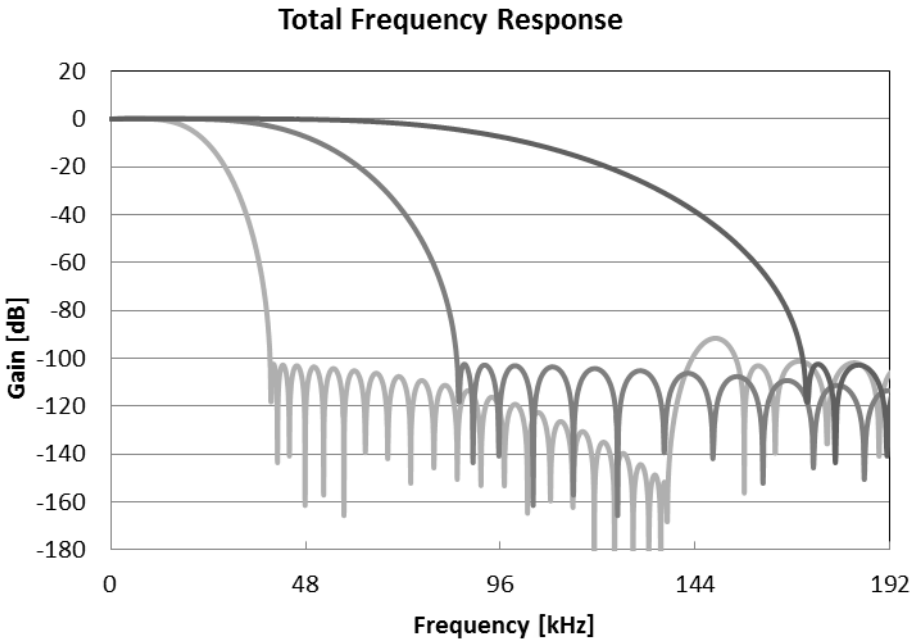


Figure 5. Slow Roll-off Filter Frequency Response

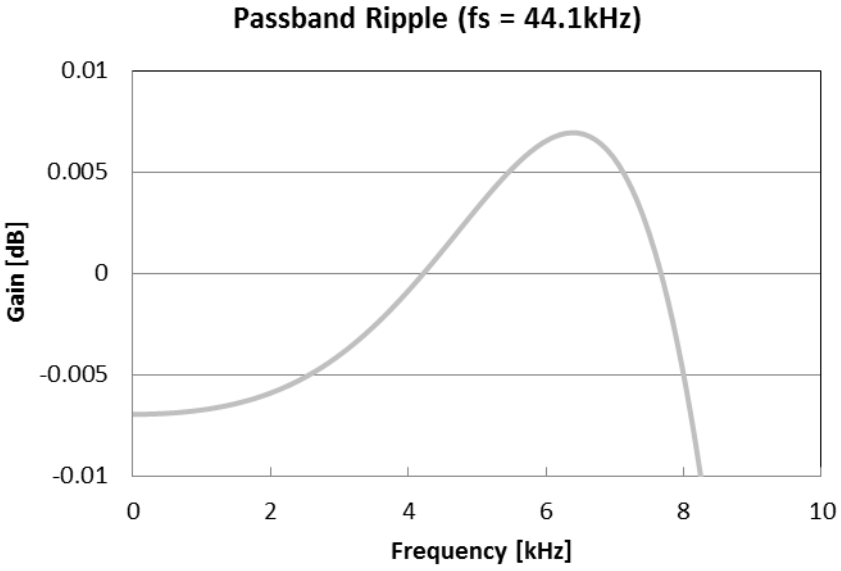


Figure 6. Slow Roll-off Filter Passband Ripple

■ Short Delay Sharp Roll-Off Filter Characteristics

Short Delay Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Normal Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "0" or SLOW pin = "L", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 22.05	20.0 -	kHz kHz
Passband	(Note 31)	PB	0	-	20.0	kHz
Stopband	(Note 31)	SB	24.1	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 26)	SA	100	-	-	dB
Group Delay	(Note 29)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 20.0kHz			-0.2	-	+0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Double Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "0" or SLOW pin = "L", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 48.0	43.5 -	kHz kHz
Passband	(Note 31)	PB	0	-	43.5	kHz
Stopband	(Note 31)	SB	52.5	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 26)	SA	100	-	-	dB
Group Delay	(Note 29)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 40.0kHz			-0.6	-	+0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Quad Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "0" or SLOW pin = "L", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 96.0	87.0 -	kHz kHz
Passband	(Note 31)	PB	0	-	87.0	kHz
Stopband	(Note 31)	SB	104.9	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 26)	SA	100	-	-	dB
Group Delay	(Note 29)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 80.0kHz			-2.0	-	+0.1	dB

Note 318. The passband and stopband frequencies scale with fs.

For example, PB = 0.4535 × fs (@±0.01dB), SB = 0.546 × fs.

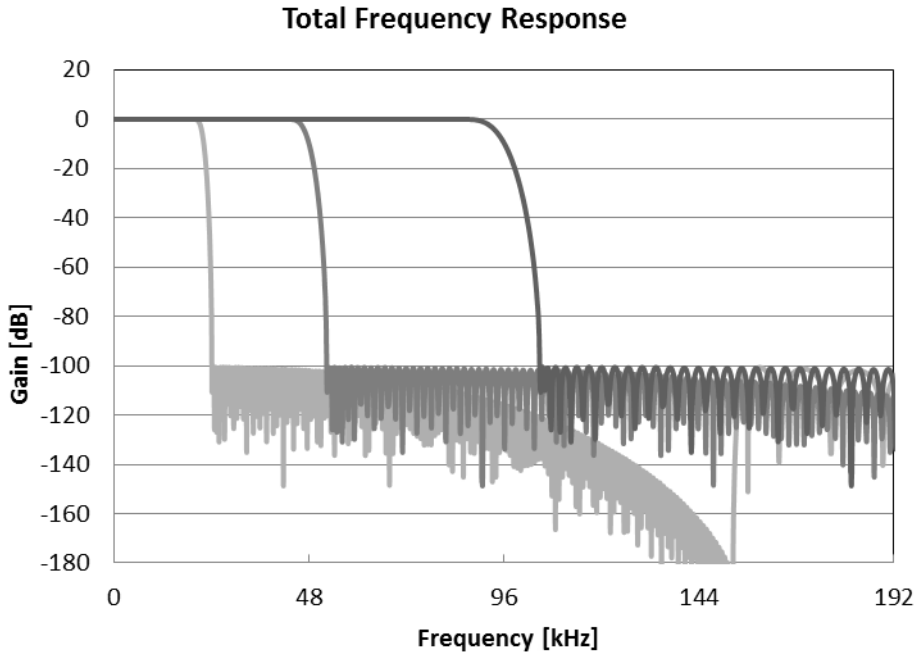


Figure 7. Short Delay Sharp Roll-off Filter Frequency Response

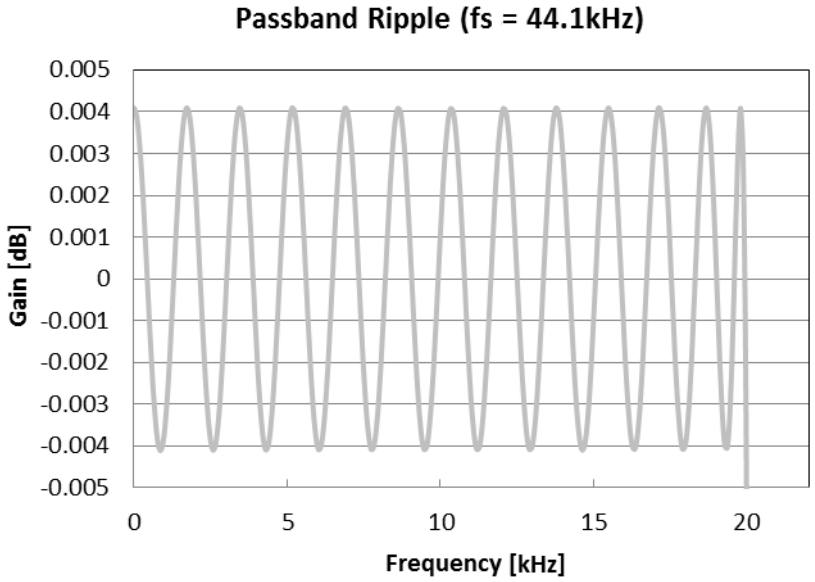


Figure 8. Short Delay Sharp Roll-off Filter Passband Ripple

■ Short Delay Slow Roll-Off Filter Characteristics

Short Delay Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Normal Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "1" or SLOW pin = "H", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 21.0	8.0 -	kHz kHz
Passband	(Note 29)	PB	0	-	8.0	kHz
Stopband	(Note 29)	SB	39.2	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 26)	SA	92	-	-	dB
Group Delay	(Note 29)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 20.0kHz			-5.0	-	+0.1	dB

Short Delay Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Double Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "1" or SLOW pin = "H", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 45.6	17.6 -	kHz kHz
Passband	(Note 29)	PB	0	-	17.6	kHz
Stopband	(Note 29)	SB	85.4	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 26)	SA	100	-	-	dB
Group Delay	(Note 29)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 40.0kHz			-3.8	-	+0.1	dB

Short Delay Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Quad Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "1" or SLOW pin = "H", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.01dB −6.0dB	- -	0 -	- 91.2	35.2 -	kHz kHz
Passband	(Note 29)	PB	0	-	35.2	kHz
Stopband	(Note 29)	SB	170.7	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 26)	SA	100	-	-	dB
Group Delay	(Note 29)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 80.0kHz			-5.0	-	+0.1	dB

Note 29. The passband and stopband frequencies scale with fs.
For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8866 × fs.

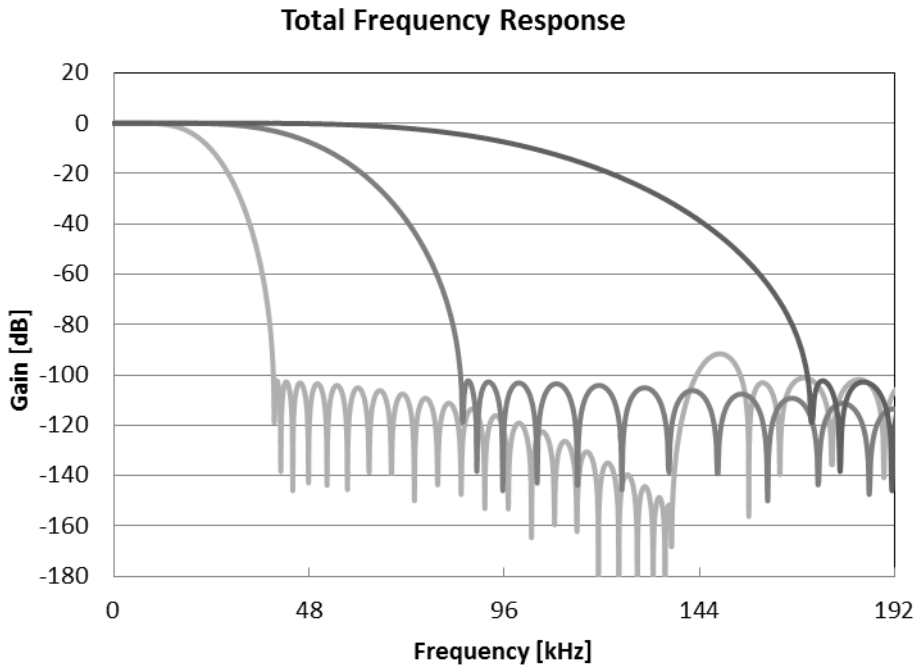


Figure 9. Short Delay Slow Roll-off Filter Frequency Response

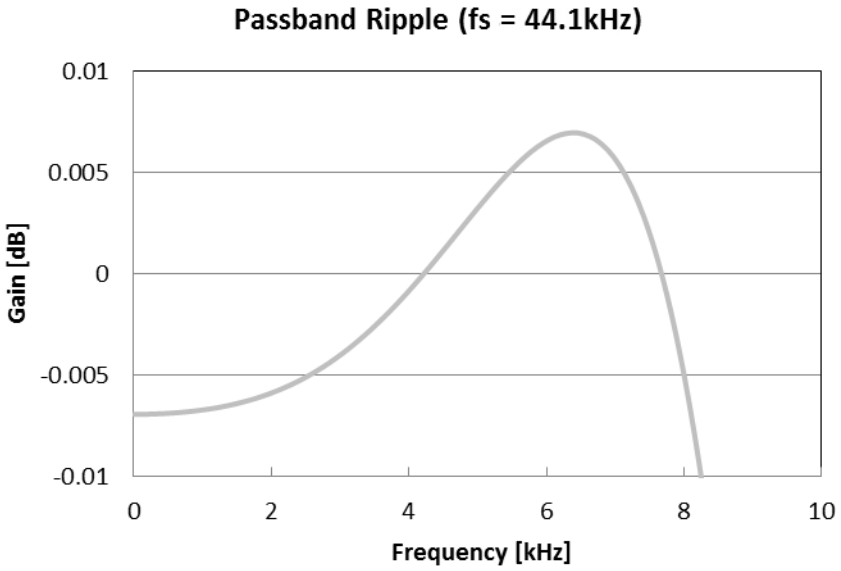


Figure 10. Short Delay Slow Roll-off Filter Passband Ripple

■ Low Dispersion Short Delay Filter Characteristics

Low Dispersion Short Delay Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Normal Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "X" or SLOW pin = "X", SSLOW bit = "1" or SSLOW pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.05dB −6.0dB	- -	0 -	- 22.05	18.4 -	kHz kHz
Passband	(Note 32)	PB	0	-	18.4	kHz
Stopband	(Note 32)	SB	25.7	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 26)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 20.0kHz			-0.8	-	+0.1	dB

Low Dispersion Short Delay Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Double Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "X" or SLOW pin = "X", SSLOW bit = "1" or SSLOW pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.05dB −6.0dB	- -	0 -	- 48.0	40.1 -	kHz kHz
Passband	(Note 32)	PB	0	-	40.1	kHz
Stopband	(Note 32)	SB	55.9	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 26)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 40.0kHz			-0.6	-	+0.1	dB

Low Dispersion Short Delay Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; Quad Speed Mode; DEM = OFF; SD bit = "1" or SD pin = "H", SLOW bit = "X" or SLOW pin = "X", SSLOW bit = "1" or SSLOW pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 26)	±0.05dB −6.0dB	- -	0 -	- 98.0	80.2 -	kHz kHz
Passband	(Note 32)	PB	0	-	80.2	kHz
Stopband	(Note 32)	SB	111.8	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 26)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs
Digital Filter + SCF	(Note 26)					
Frequency Response: 0 ~ 80.0kHz			-2.0	-	+0.1	dB

Note 320. The passband and stopband frequencies scale with fs.
For example, PB = 0.418 × fs (@±0.05dB), SB = 0.582 × fs.

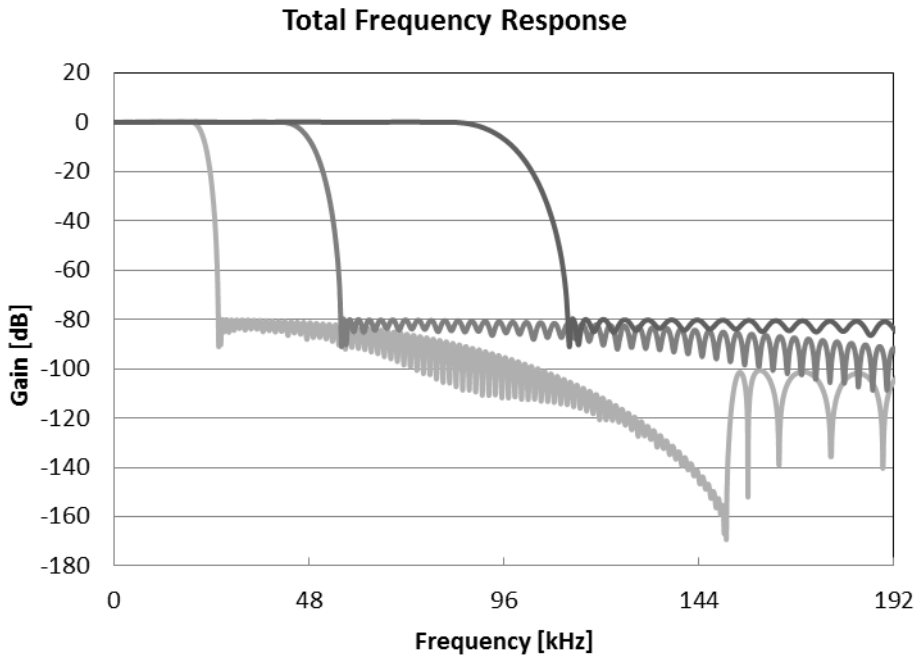


Figure 11. Low Dispersion Short Delay Filter Frequency Response

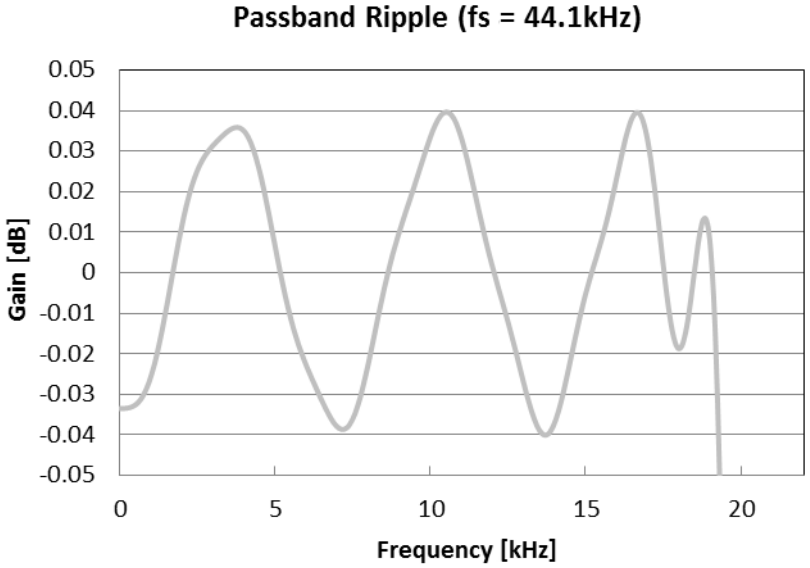


Figure 12. Low Dispersion Short Delay Filter Passband Ripple

■ DSD Filter Characteristics

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; fs = 44.1kHz; DP bit = "1", DSDF bit = "0", DSDSEL[1:0] bits = "00" (Note 34))

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response					
Frequency Response (64fs) (Note 35)	20kHz		-0.77		dB
	50kHz		-5.25		dB
	100kHz		-18.80		dB

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V; fs = 44.1kHz; DP bit = "1", DSDF bit = "1", DSDD bit = "1", DSDSEL[1:0] bits = "00" (Note 34))

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response					
Frequency Response (64fs) (Note 35)	20kHz		-0.19		dB
	100kHz		-5.29		dB
	150kHz		-15.57		dB

Note 33. The peak level of DSD signal should be in the range of 25% ~ 75% duty according to the SACD format book (Scarlet Book).

Note 34. 0dB is the output level when a 1kHz 25% ~ 75% duty sine wave is input.

Note 35. The frequency (20kHz, 50kHz, 100kHz or 150 kHz) is doubled in DSD128 speed (DSDSEL[1:0] bits = "01"), is quadrupled in DSD256 speed (DSDSEL[1:0] bits = "10"), and is 8x in DSD512 speed.

■ DC Characteristics

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = TVDD = 1.7 ~ 3.6V, DVDD = 1.7 ~ 1.98V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD = 1.7 ~ 3.0V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
TVDD = 3.0V ~ 3.6V					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (DZFL, DZFR pins: Iout = -100μA)	VOH	TVDD−0.3	-	-	V
Low-Level Output Voltage					
(except SDA pin: Iout = 100μA)	VOL	-	-	0.3	V
(SDA pin, 2.0V ≤ DVDD ≤ 3.6V: Iout = 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.7V ≤ DVDD ≤ 2.0V: Iout = 3mA)	VOL	-		20%TVDD	V
Input Leakage Current	Iin	-	-	±10	μA

Note 36. The TESTE, DIF0 and DIF1 pins have internal pull-down and the PSN pin has internal pull-up resistors. The resistance is 100 kohm (typ). Therefore, the TESTE, DIF0, DIF1 and PSN pins are not included in this specification.

■ Switching Characteristics

(Ta = -40 ~ 85°C; VDDL/R = 4.75 ~ 5.25V, AVDD = DVDD = 1.7 ~ 3.6V, C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
Frequency	fCLK	2.048	-	49.664	MHz
Duty Cycle	dCLK	40	-	60	%
Minimum Pulse Width	tCLKH	9.05	-	-	nsec
	tCLKL	9.05	-	-	nsec
LRCK Clock Timing (Note 37)					
Normal Mode (TDM[1:0] bits = "00")					
Normal Speed Mode	fsn	8	-	54	kHz
Double Speed Mode	fsd	54	-	108	kHz
Quad Speed Mode	fsq	108	-	216	kHz
Oct speed mode	fso	216	-	388	kHz
Hex speed mode	fsh	388	-	776	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 mode (TDM[1:0] bits = "01")					
Normal Speed Mode	fsn	8	-	54	kHz
Double Speed Mode	fsd	54	-	108	kHz
Quad Speed Mode	fsq	108	-	216	kHz
High time	tLRH	1/128fs	-	-	nsec
Low time	tLRL	1/128fs	-	-	nsec
TDM256 mode (TDM[1:0] bits = "10")					
Normal Speed Mode High time	fsn	8	-	54	kHz
Double Speed Mode	fsd	54	-	108	kHz
High time	tLRH	1/256fs	-	-	nsec
Low time	tLRL	1/256fs	-	-	nsec
TDM512 mode (TDM[1:0] bits = "11")					
Normal Speed Mode	fsn	8	-	54	kHz
High time	tLRH	1/512fs	-	-	nsec
Low time	tLRL	1/512fs	-	-	nsec

Note 37. The MCLK frequency must be changed while the AK4493S is in reset state by setting the PDN pin = "L" or RSTN bit = "0".

Parameter		Symbol	Min.	Typ.	Max.	Unit
PCM Audio Interface Timing						
Normal Mode (TDM[1:0] bits = "00")						
BICK Period						
Normal Speed Mode		tBCK	1/256fsn			nsec
Double Speed Mode		tBCK	1/128fsd			nsec
Quad Speed Mode		tBCK	1/64fsq			nsec
Oct speed mode		tBCK	1/64fso			nsec
Hex speed mode		tBCK	1/64fsh			nsec
BICK Pulse Width Low		tBCKL	9			nsec
BICK Pulse Width High		tBCKH	9			nsec
BICK "↑" to LRCK Edge	(Note 38)	tBLR	5			nsec
LRCK Edge to BICK "↑"	(Note 38)	tLRB	5			nsec
SDATA Hold Time		tSDH	5			nsec
SDATA Setup Time		tSDS	5			nsec
TDM128 mode (TDM[1:0] bits = "01")						
BICK Period						
Normal Speed Mode		tBCK	1/128fsn			nsec
Double Speed Mode		tBCK	1/128fsd			nsec
Quad Speed Mode		tBCK	1/128fsq			nsec
BICK Pulse Width Low		tBCKL	14			nsec
BICK Pulse Width High		tBCKH	14			nsec
BICK "↑" to LRCK Edge	(Note 38)	tBLR	14			nsec
LRCK Edge to BICK "↑"	(Note 38)	tLRB	14			nsec
SDATA Hold Time		tSDH	5			nsec
SDATA Setup Time		tSDS	5			nsec
TDM256 mode (TDM[1:0] bits = "10")						
BICK Period						
Normal Speed Mode		tBCK	1/256fsn			nsec
Double Speed Mode		tBCK	1/256fsd			nsec
BICK Pulse Width Low		tBCKL	14			nsec
BICK Pulse Width High		tBCKH	14			nsec
BICK "↑" to LRCK Edge	(Note 38)	tBLR	14			nsec
LRCK Edge to BICK "↑"	(Note 38)	tLRB	14			nsec
SDATA Hold Time		tSDH	5			nsec
SDATA Setup Time		tSDS	5			nsec
TDM512 mode (TDM[1:0] bits = "11")						
BICK Period						
Normal Speed Mode		tBCK	1/512fsn			nsec
BICK Pulse Width Low		tBCKL	14			nsec
BICK Pulse Width High		tBCKH	14			nsec
BICK "↑" to LRCK Edge	(Note 38)	tBLR	14			nsec
LRCK Edge to BICK "↑"	(Note 38)	tLRB	14			nsec
SDATA Hold Time		tSDH	5			nsec
SDATA Setup Time		tSDS	5			nsec

Note 38. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
PCM Audio Interface Timing					
External Digital Filter Mode					
BCK Period	tB	27	-	-	nsec
BCK Pulse Width Low	tBL	10	-	-	nsec
BCK Pulse Width High	tBH	10	-	-	nsec
BCK "↑" to WCK Edge	tBW	5	-	-	nsec
WCK Period	tWCK	1.3	-	-	usec
WCK Edge to BCK "↑"	tWB	5	-	-	nsec
WCK Pulse Width Low	tWCKL	54	-	-	nsec
WCK Pulse Width High	tWCKH	54	-	-	nsec
DINL/R Hold Time	tDH	5	-	-	nsec
DINL/R Setup Time	tDS	5	-	-	nsec
DSD Audio Interface Timing					
Sampling Frequency	fs	30	-	48	kHz
(DSD64, DSDSEL [1:0] bits = "00")					
DCLK Period	tDCK	-	1/64fs	-	nsec
DCLK Pulse Width Low	tDCKL	144	-	-	nsec
DCLK Pulse Width High	tDCKH	144	-	-	nsec
DCLK Edge to DSDL/R (Note 39)	tDDD	–20	-	20	nsec
(DSD128, DSDSEL [1:0] bits = "01")					
DCLK Period	tDCK	-	1/128fs	-	nsec
DCLK Pulse Width Low	tDCKL	72	-	-	nsec
DCLK Pulse Width High	tDCKH	72	-	-	nsec
DCLK Edge to DSDL/R (Note 39)	tDDD	–10	-	10	nsec
(DSD256, DSDSEL [1:0] bits = "10")					
DCLK Period	tDCK	-	1/256fs	-	nsec
DCLK Pulse Width Low	tDCKL	36	-	-	nsec
DCLK Pulse Width High	tDCKH	36	-	-	nsec
DCLK Edge to DSDL/R (Note 39)	tDDD	–5	-	5	nsec
(DSD512, DSDSEL [1:0] bit = "11")					
DCLK Period	tDCK	-	1/512fs	-	nsec
DCLK Pulse Width Low	tDCKL	18	-	-	nsec
DCLK Pulse Width High	tDCKH	18	-	-	nsec
DSDL/R Setup Time	tDDS	5	-	-	nsec
DSDL/R Hold Time	tDDH	5	-	-	nsec

Note 39. DSD data transmitting device must meet this time. "tDDD" is defined from DCLK "↓" until DSDL/R edge when DCKB bit = "0" (default), "tDDD" is defined from DCLK "↑" until DSDL/R edge when DCKB bit = "1". If the audio data format is in phase modulation mode, "tDDD" is defined from DCLK edge "↓" or "↑" until DSDL/R edge regardless of DCKB bit setting.

Note 40. The AK4493S does not support Phase Modulation Mode in DSD512 Mode.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire I/F mode):					
CCLK Period	tCCK	200	-	-	nsec
CCLK Pulse Width Low	tCCKL	80	-	-	nsec
CCLK Pulse Width High	tCCKH	80	-	-	nsec
CDTI Setup Time	tCDS	40	-	-	nsec
CDTI Hold Time	tCDH	40	-	-	nsec
CSN "H" Time	tCSW	150	-	-	nsec
CSN "↓" to CCLK "↑"	tCSS	50	-	-	nsec
CCLK "↑" to CSN "↑"	tCSH	50	-	-	nsec
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	usec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	usec
Clock Low Time	tLOW	1.3	-	-	usec
Clock High Time	tHIGH	0.6	-	-	usec
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	usec
SDA Hold Time from SCL Falling (Note 41)	tHD:DAT	0	-	-	usec
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	usec
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	usec
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	usec
Setup Time for Stop Condition	tSU:STO	0.6	-	-	usec
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	nsec
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing (Note 42)					
PDN Accept Pulse Width	tAPD	150	-	-	nsec
PDN Reject Pulse Width	tRPD	-	-	30	nsec

Note 41. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 42. The AK4493S can be reset by bringing the PDN pin "H" upon power-up.
Note 43. I^2C -bus is a trademark of NXP B.V.

■ **Timing Diagram**

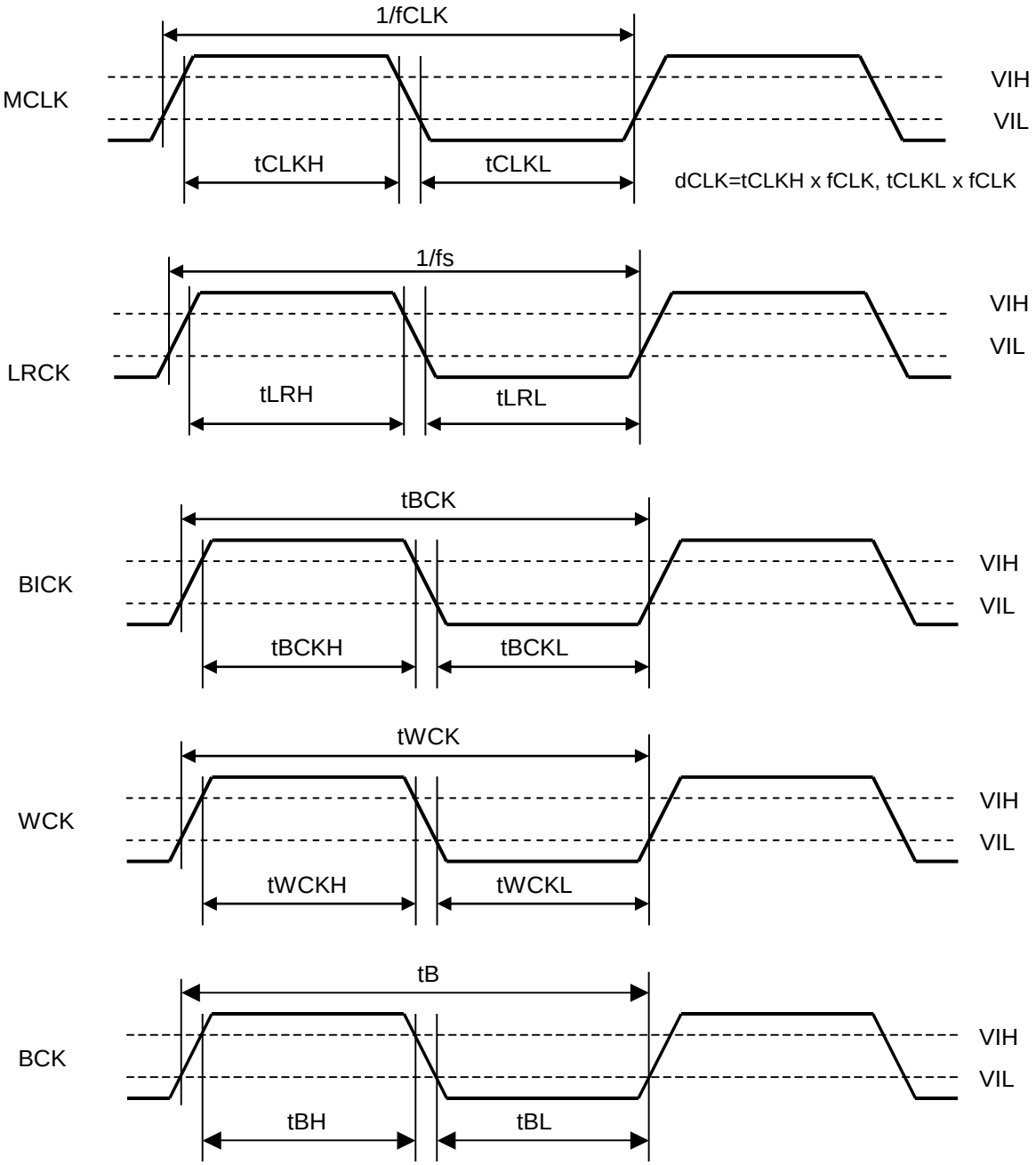


Figure 13. Clock Timing

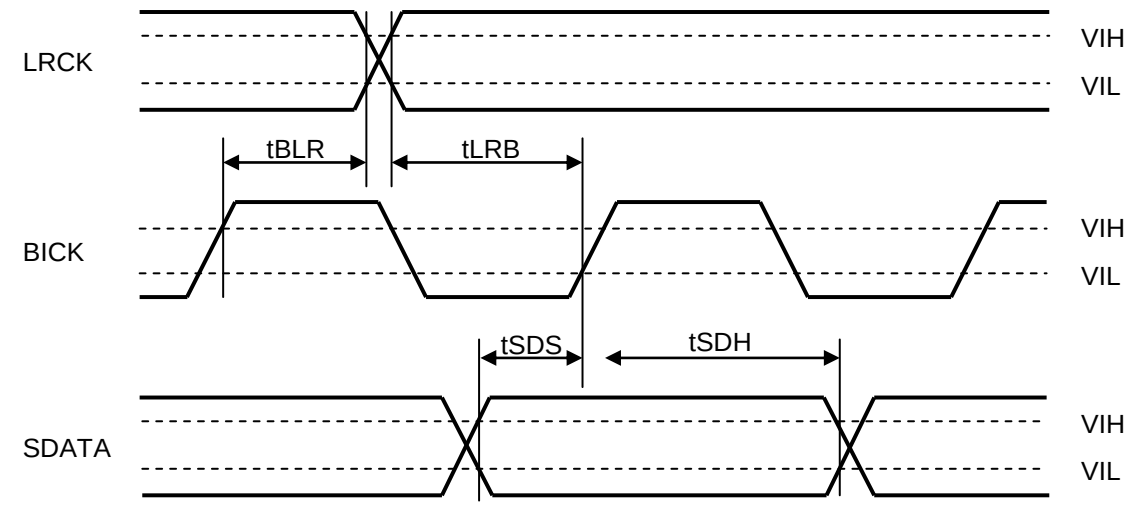


Figure 14. Audio Interface Timing (PCM Mode)

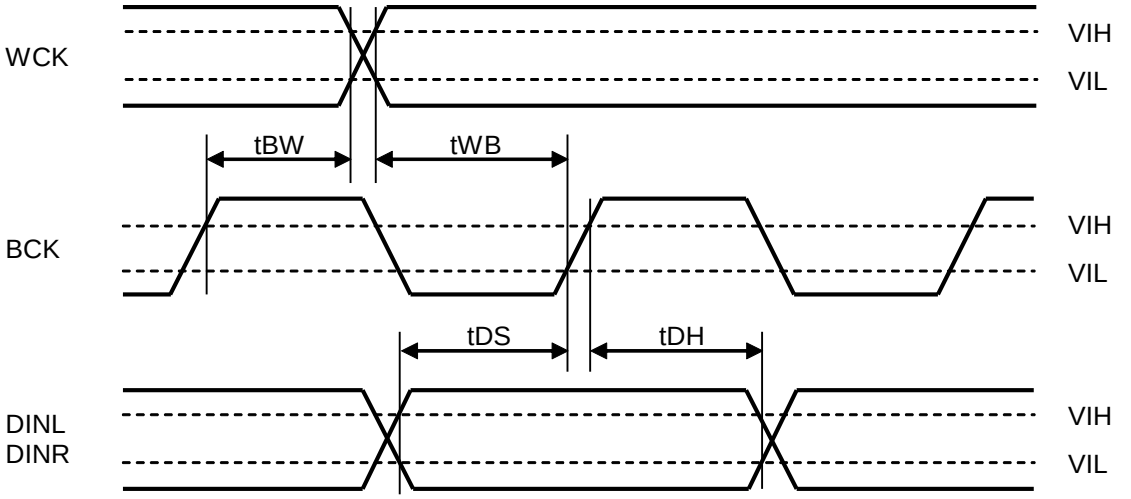
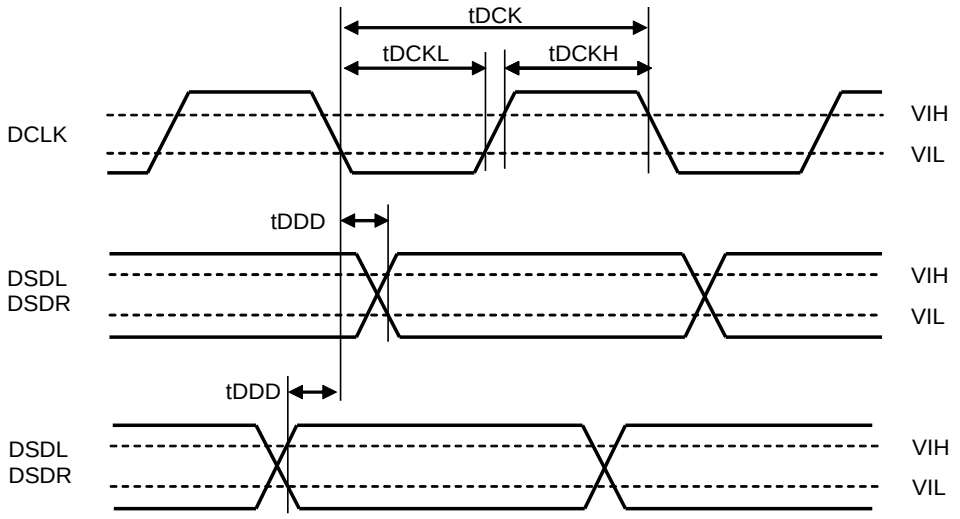
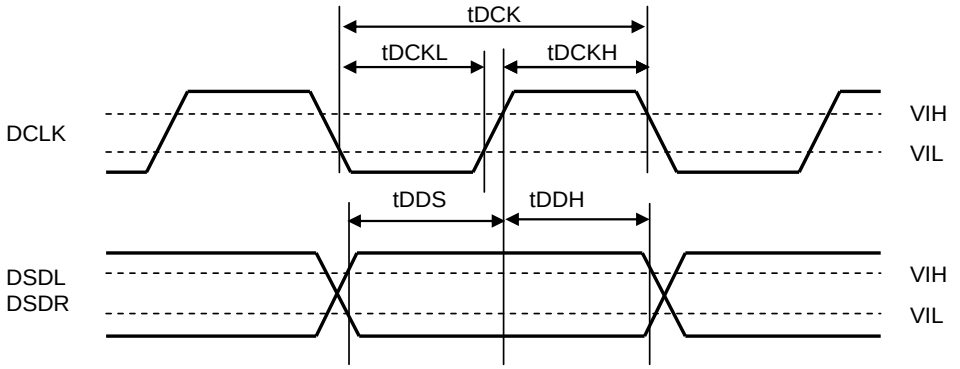


Figure 15. Audio Interface Timing (External Digital Filter I/F Mode)



DSD Audio Interface Timing (DSD64, DSD128, DSD256 Mode)



DSD Audio Interface Timing (DSD512 Mode)

Figure 16. Audio Interface Timing (DSD Normal Mode, DCKB bit = “0”)

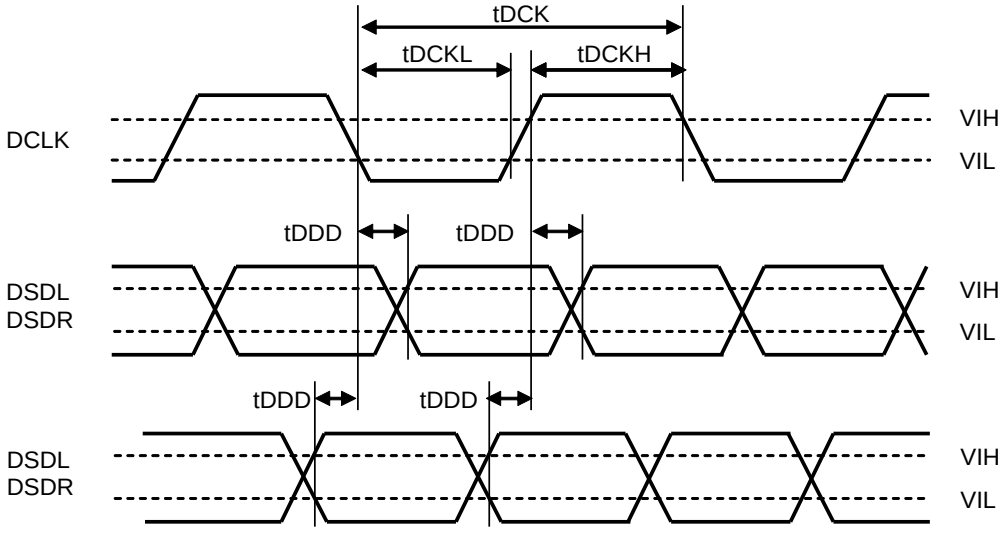


Figure 17. Audio Interface Timing (DSD Phase Modulation Mode, DCKB bit = “0”)

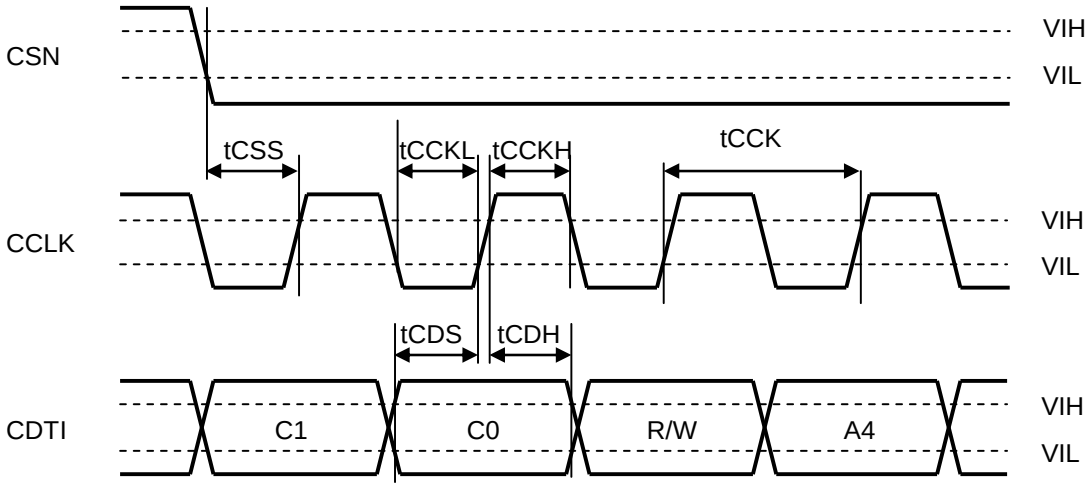


Figure 18. WRITE Command Input Timing

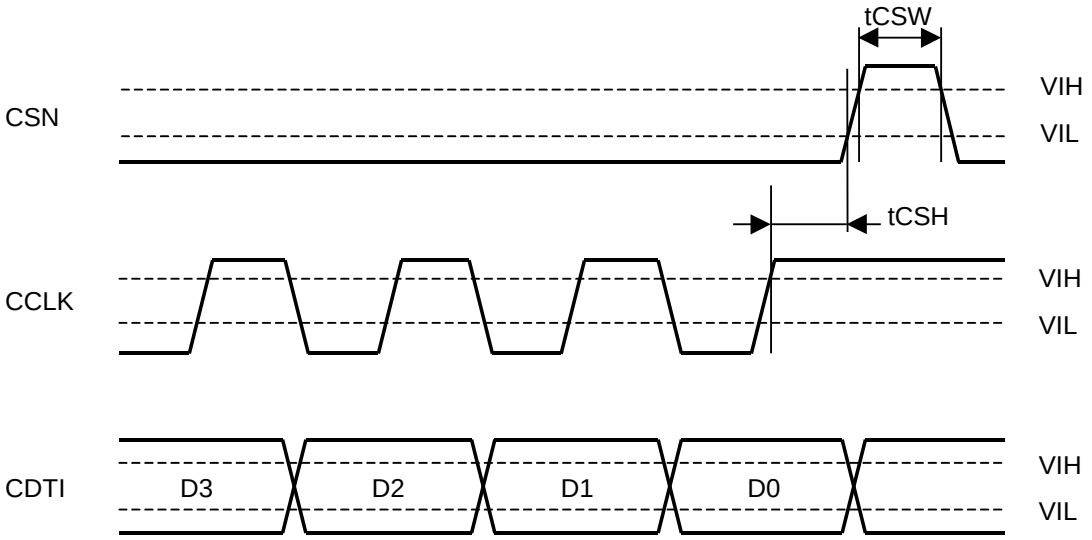


Figure 19. WRITE Data Input Timing

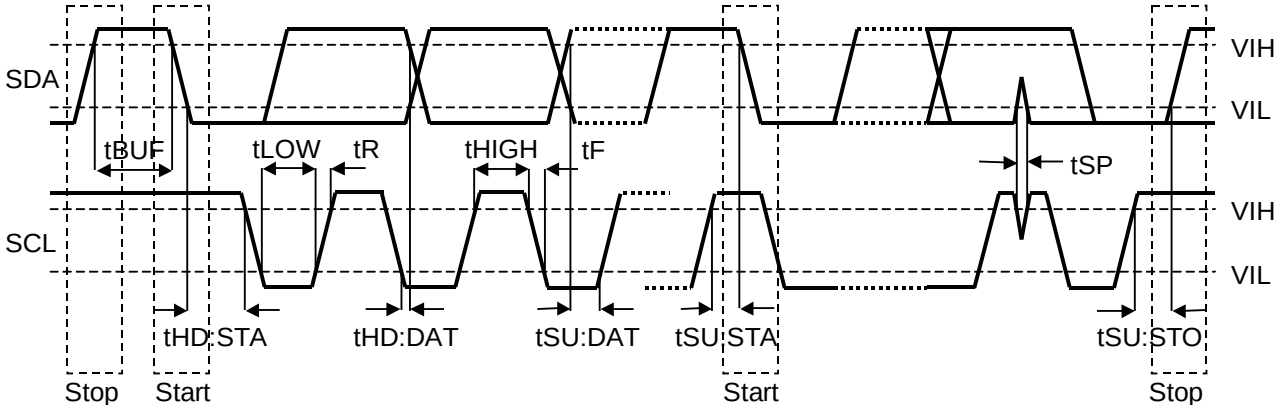


Figure 20. I²C Bus Mode Timing

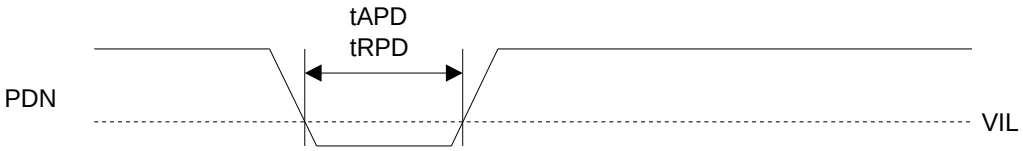


Figure 21. Power Down & Reset Timing

9. Functional Descriptions

Each function of the AK4493S is controlled by pins (Pin Control Mode) or registers (Register Control Mode) (Table 1). Select the control mode by setting the PSN pin. The AK4493S must be powered down by the PDN pin when changing the PSN pin setting. There is a possibility of malfunction if the device is not powered down when changing the control mode since the previous setting is not reinitialized. Register settings are invalid in Pin Control Mode, and pin settings are invalid in Register Control Mode.

Table 2 shows available functions of each control mode and Table 3 shows available functions in PCM/DSD/EXDF mode.

Table 1. Pin/Register Control Mode Select

PSN pin	Control Mode
L	Register Control Mode
H	Pin Control Mode

Table 2. Function List in Pin/Register Control Mode

Function	Pin Control Mode	Register Control Mode
DSD/EXDF Mode Select	-	Y
System Clock Setting Select	Y	Y
Audio Format Select	Y	Y
TDM Mode	-	Y
Digital Filter Select	Y	Y
De-emphasis Filter Select	Y (44.1kHz only)	Y
Digital Attenuator	-	Y
Zero Detection	-	Y
Mono Mode	-	Y
Output signal select (Monaural Channel select)	-	Y
Output signal polarity select (Inverting)	Y	Y
Sound Quality Select	-	Y
DSD Full-scale Detect	-	Y
Soft Mute	Y	Y
Register Reset	-	Y
Clock Synchronization Function	-	Y
Register Control	-	Y
Gain Control	-	Y

(Y: Available, -: Not Available)

Table 3. Function List of PCM/EXDF/DSD Mode in Register Control Mode

Function	Default	Address	Bit	PCM	EXDF	DSD
PCM/DSD /EXDF Mode Select	PCM mode	00H 02H	EXDF DP	Y	Y	Y
System Clock Setting in DSD Mode	DSD512	02H	DCKS	-	-	Y
System Clock Setting in EXDF Mode	16fs	00H	ECS	-	Y	-
Digital Filter Select in DSD Mode	39kHz filter	09H	DSDF	-	-	Y
Digital Filter Select in PCM Mode	Short Delay Sharp Roll-off filter	01-02-05H	SD SLOW SSLOW	Y	-	-
De-emphasis Response	OFF	01H	DEM[1:0]	Y	-	-
Path Select in DSD Mode	Normal Path	06H	DSDD	-	-	Y
Audio Data Interface Format in PCM Mode	32bit MSB	00H	DIF[2:0]	Y	-	-
Audio Data Interface Format in EXDF Mode	32bit LSB	00H	DIF[2:0]	-	Y	-
TDM Interface Format	Normal Mode	0AH	TDM[1:0]	Y	-	-
Attenuation Level	0dB	03-04H	ATTL/R[7:0]	Y	Y	Y
Data Zero Detect Enable	Disable	01H	DZFE	Y	Y	Y
Inverting Enable of DZF	“H” active	02H	DZFB	Y	Y	Y
Mono/Stereo mode select	Stereo	02H	MONO	Y	Y	Y
Data Invert Mode Select	OFF	05H	INVL/R	Y	Y	Y
Data Selection of L-channel and R-channel	R-channel	02H	SELLR	Y	Y	Y
Sound Quality Select	Off	08H	SC[2:0]	Y	Y	Y
DSD Mute Function @Full-scale Detected	Disable	06H	DDM	-	-	Y
Soft Mute Enable	Normal Operation	01H	SMUTE	Y	Y	Y
RSTN	RST	00H	RSTN	Y	Y	Y
Clock Synchronization Function	Enable	07H	SYNCE	Y	Y	-
Gain Control	Different Gain on DSDD bit=“1”	07H	GC[2:0]	Y	Y	Y

(Y: Available, N/A: Not Available)

■ D/A Conversion Mode (PCM Mode, DSD Mode, EXDF Mode)

The AK4493S is able to convert either PCM or DSD data to an analog signal, and an external digital filter I/F can also be selected. In PCM mode, PCM data can be input from the BICK, LRCK and SDATA pins. In DSD mode, DSD data can be input from the DCLK, DSDL and DSDR pins. In EXDF mode, EXDF data can be input from the BCK, DINL, DINR and WCK pins. The AK4493S only supports PCM mode in Pin Control Mode.

Switching to DSD mode, manual and automatic settings are selectable. The AK4493S is in Manual Setting Mode when ADPE bit = "0" and it is in Automatic Setting Mode when ADPE bit = "1". However, EXDF mode and PCM mode can only be set manually.

In manual setting mode (ADPE bit = "0"), D/A conversion mode switching between PCM and DSD is executed by DP bit. Switching PCM/DSD mode must be executed during reset state by setting RSTN bit = "0". RSTN bit should not be changed for 4/fs after switching these modes. It takes 2/fs ~ 3/fs for data mode switching.

External digital filter I/F can be selected by setting DP bit = "0" and EXDF bit = "1". EXDF bit controls EXDF I/F modes. Internal/external digital filter switching by EXDF bit must be executed during reset by RSTN bit = "0". Digital filter switching takes 2~3k/fs. The AK4493S is in DSD mode when setting DP bit = "1" and EXDF bit = "1".

In Auto Setting Mode (ADPE bit = "1"), DP bit setting is ignored. The AK4493S monitors input signals of the number 4 pin to select PCM or DSD mode when EXDF bit = "0", and it monitors input signals of the number 6 pin to select EXDF or DSD mode when EXDF bit = "1".

Table 4. PCM/DSD/EXDF Mode Control, in Register Control Mode

ADPE	DP	EXDF	D/A Conv. Mode	Pin Assignment				
				#3 pin	#4 pin	#5 pin	#6 pin	
0	0	0	PCM	BICK	SDATA	LRCK	L	(default)
	1	*	DSD	DCLK	DSDL	DSDR	L	
	0	1	EXDF	BCK	DINL	DINR	WCK	
1	*	0	Auto (PCM or DSD)	BCK/ DCLK	SDATA/ DSDL	LRCK/ DSDR	L	
		1	Auto (EXDF or DSD)	BCK/ DCLK	DINL/ DSDL	DINR/ DSDL	WCK/ L	

(*: Do not care)

■ D/A Conversion Mode Switching Timing

Figure 22 and Figure 23 show switching timing of PCM/EXDF and DSD modes. To prevent noise caused by excessive input, DSD signal should be input 4/fs after setting RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to DSD mode from PCM/EXDF mode. DSD signal should be stopped 4/fs after setting RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to PCM/EXDF from DSD mode.

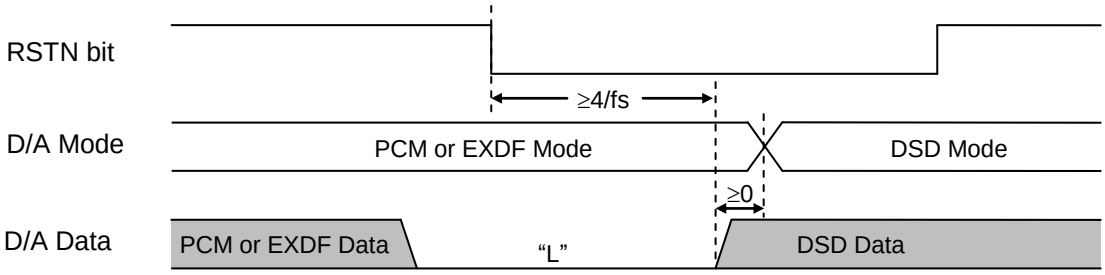


Figure 22. D/A Mode Switching Timing (from PCM/EXDF to DSD)

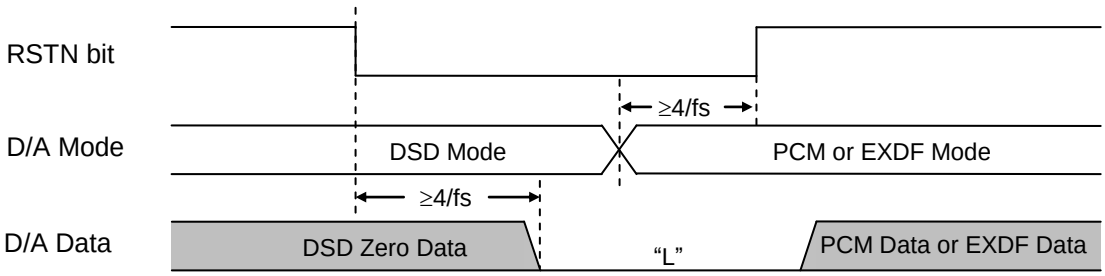


Figure 23. D/A Mode Switching Timing (from DSD to PCM/EXDF)

Figure 24 shows switching timing of PCM and EXDF modes. Set EXDF bit 4/fs after setting RSTN bit = "0" until the device is completely reset internally when changing the conversion mode.

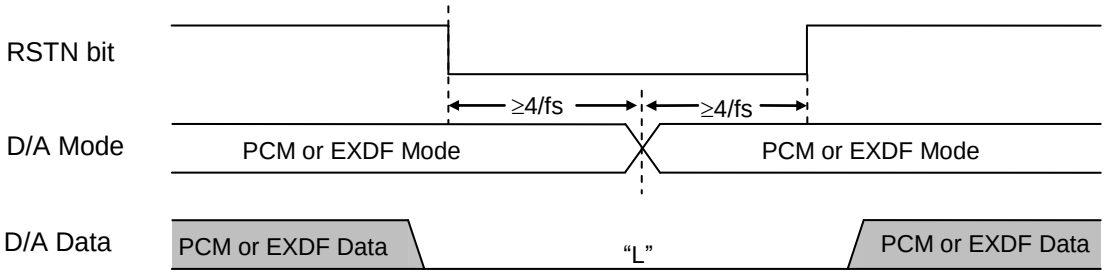


Figure 24. D/A Mode Switching Timing (from PCM to EXDF or from EXDF to PCM)

■ System Clock

[1] PCM Mode

The external clocks, which are required to operate the AK4493S, are MCLK, BICK and LRCK. MCLK, BICK and LRCK should be synchronized but the phase of MCLK is not critical. MCLK is used to operate the digital interpolation filter, the delta sigma modulator and SCF.
There are Manual Setting Mode and Auto Setting Mode (fs auto detection) for MCLK frequency setting (Table 5). In Manual Setting Mode (ACKS pin = "L" or ACKS bit = "0"), MCLK frequency is set automatically but the sampling speed (LRCK frequency) is set by DFS[2:0] bits (Table 6). The sampling frequency is fixed to Normal Speed Mode in Pin Control Mode (PSN pin = "H"), and it is set by DFS[2:0] bits in Register Control Mode (PSN pin = "L"). In Register Control Mode, the AK4493S is in Manual Setting Mode when power-down is released (PDN pin = "L" → "H").
In Auto Setting Mode (ACKS pin = "H" or ACKS bit = "1"), sampling speed and MCLK frequency are detected automatically (Table 7, Table 11) and then the initial master clock is set to the appropriate frequency (Table 8, Table 15, Table 16).

All circuits except control registers, bias generation circuit and internal LDO (if LDOE pin = "H") of the AK4493S are automatically placed in power-down state when MCLK is stopped for more than 1us during normal operation (PDN pin = "H"), and the analog output becomes Hi-z state. When MCLK is input again, the AK4493S exits this power-down state and starts operation again. In this case, register settings are not initialized. The AK4493S is in power-down mode until MCLK, BICK and LRCK are supplied and the analog output is floating state.

Table 5. System Clock Setting Mode

ACKS bit	Mode	
0	Manual Setting Mode	(default)
1	Auto Setting Mode	

(1) Pin Control Mode (PSN pin = "H")

1-1. Manual Setting Mode (ACKS pin = "L")

The MCLK frequency corresponding to each sampling speed should be provided externally (Table 6). The sampling frequency is fixed to Normal Speed Mode in Pin Control Mode. In this mode, Hex, Octal, Quad and Double Speed Modes are not available.

Table 6. System Clock Example (Manual Setting Mode in Pin Control Mode) (N/A: Not Available)

LRCK	MCLK (MHz)							BICK
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	3.0720MHz

1-2. Auto Setting Mode (ACKS pin = “H”)

Auto Setting Mode is a function that enables to playback 44.1kHz, 96kHz and 192kHz audio data without setting registers if an MCLK about 22.5792MHz is input to the AK4493S. The AK4493S can operate with an MCLK about 11.2896MHz, however the characteristics will degrade since it is not an intended speed.

In Auto Setting Mode, the MCLK and LRCK frequency ratio is detected to automatically set the Sampling Speed Mode (Table 7). The frequencies of MCLK and LRCK corresponding to each Sampling Speed Mode should be input externally (Table 8, Table 9).

Table 7. Sampling Speed (Auto Setting Mode in Pin Control Mode)

MCLK		Sampling Speed
1152fs		Normal (fs ≤ 32kHz)
512fs/256fs	768fs/384fs	Normal
256fs	384fs	Double
128fs	192fs	Quad
64fs	96fs	Oct
32fs	48fs	Hex

Table 8. System Clock Example (Auto Setting Mode in Pin Control Mode) (N/A: Not Available)

LRCK	MCLK (MHz)						Sampling Speed
Fs	32fs	48fs	64fs	96fs	128fs	192fs	
32.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal
44.1kHz	N/A	N/A	N/A	N/A	N/A	N/A	
48.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	Quad
192.0kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	
384kHz	N/A	N/A	24.576	36.864	N/A	N/A	Oct
768kHz	24.576	36.864	N/A	N/A	N/A	N/A	Hex

Table 9. System Clock Example (Auto Setting Mode in Pin Control Mode) (N/A: Not Available)

LRCK	MCLK (MHz)						Sampling Speed
Fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0kHz	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal
44.1kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	
48.0kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Double
96.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
384kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

When MCLK = 256fs/384fs, Auto Setting Mode supports sampling rates of 8kHz ~ 96kHz (Table 10). However, the DR and S/N performances will degrade approximately 3dB if the sampling rate is 44.1kHz due to the internal oversampling ratio being reduced by one half.

Table 10. DR and S/N Relationship with MCLK Frequency (fs = 44.1kHz)

ACKS pin	MCLK	DR, S/N (A-weighted)
L	256fs/384fs/512fs/768fs	123dB
H	256fs/384fs	120dB

H	512fs/768fs	123dB

(2) Register Control Mode (PSN pin = "L")

2-1. Manual Setting Mode (ACKS bit = "0")

MCLK frequency is detected automatically and the sampling speed is set by DFS[2:0] bits (Table 11). The MCLK frequency corresponding to each sampling speed that should be provided externally (Table 12, Table 13). The AK4493S is set to Manual Setting Mode at power-up (PDN pin = "L"→"H"). When DFS2-0 bits are changed, the AK4493S should be reset by RSTN bit.

Table 11. Sampling Speed (Manual Setting Mode in Register Control Mode)

DFS2	DFS1	DFS0	Sampling Rate (fs)		
0	0	0	Normal Speed Mode	8kHz ~ 54kHz	(default)
0	0	1	Double Speed Mode	54kHz ~ 108kHz	
0	1	0	Quad Speed Mode	108kHz ~ 216kHz	
0	1	1	Quad Speed Mode	108kHz ~ 216kHz	
1	0	0	Oct Speed Mode	216kHz ~ 388kHz	
1	0	1	Hex Speed Mode	388kHz ~ 776kHz	
1	1	0	Oct Speed Mode	216kHz ~ 388kHz	
1	1	1	Hex Speed Mode	388kHz ~ 776kHz	

Table 12. System Clock Example (Manual Setting Mode in Register Control Mode)

LRCK	MCLK (MHz)						Sampling Speed
Fs	16fs	32fs	48fs	64fs	96fs	128fs	
32.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal
44.1kHz	N/A	N/A	N/A	N/A	N/A	N/A	
48.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	N/A	22.5792	Quad
192.0kHz	N/A	N/A	N/A	N/A	N/A	24.5760	
384kHz	N/A	12.288	18.432	24.576	36.864	N/A	Oct
768kHz	12.288	24.576	36.864	49.152	N/A	N/A	Hex

(N/A: Not Available)

Table 13. System Clock Example (Manual Setting Mode in Register Control Mode)

LRCK	MCLK (MHz)							Sampling Speed
fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0kHz	N/A	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal
44.1kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	
48.0kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2kHz	N/A	22.5792	33.8688	45.1584	N/A	N/A	N/A	Double
96.0kHz	N/A	24.5760	36.8640	49.152	N/A	N/A	N/A	
176.4kHz	33.8688	45.1584	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	36.8640	49.152	N/A	N/A	N/A	N/A	N/A	
384kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex

(N/A: Not Available)

2-2. Auto Setting Mode (AFSD bit = “0”, ACKS bit = “1”)

MCLK frequency and the sampling speed are detected automatically (Table 14) and DFS[2:0] bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 15, Table 16).

Table 14. Sampling Speed (Auto Setting Mode in Register Control Mode)

MCLK		Sampling Speed
1152fs		Normal (fs ≤ 32kHz)
512fs/256fs	768fs/384fs	Normal
256fs	384fs	Double
128fs	192fs	Quad
64fs	96fs	Oct
32fs	48fs	Hex

Table 15. System Clock Example (Auto Setting Mode in Register Control Mode)

LRCK	MCLK (MHz)					Sampling Speed
fs	32fs	48fs	64fs	96fs	128fs	
32.0kHz	N/A	N/A	N/A	N/A	N/A	Normal
44.1kHz	N/A	N/A	N/A	N/A	N/A	
48.0kHz	N/A	N/A	N/A	N/A	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	22.5792	Quad
192.0kHz	N/A	N/A	N/A	N/A	24.5760	
384kHz	N/A	N/A	24.576	36.864	N/A	Oct
768kHz	24.576	36.864	N/A	N/A	N/A	Hex

Table 16. System Clock Example (Auto Setting Mode in Register Control Mode)

LRCK	MCLK (MHz)						Sampling Speed
fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	Normal
44.1kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	
48.0kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	
88.2kHz	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	36.8640	N/A	N/A	N/A	N/A	N/A	
384kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

When MCLK= 256fs/384fs, auto setting mode supports sampling rate from 8kHz to 96kHz (Table 17). However, the DR and S/N performances will degrade approximately 3dB if the sampling rate is 44.1kHz due to the internal oversampling ratio being reduced by one half.

Table 17. DR and S/N Relationship with MCLK Frequency (fs = 44.1kHz)

ACKS bit	MCLK	DR, S/N (A-weighted)
0	256fs/384fs/512fs/768fs	123dB
1	256fs/384fs	120dB
1	512fs/768fs	123dB

[2] DSD Mode (Register Control Mode only)

The AK4493S has a DSD playback function. The external clocks that are required in DSD mode are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit (Table 18).
The AK4493S is automatically placed in power-down state when MCLK is stopped during normal operation (PDN pin = "H"), and the analog output becomes Hi-z state. When the reset is released (PDN pin = "L"→ "H"), the AK4493S is in power-down state until MCLK and DCLK are input.

Table 18. System Clock (DSD Mode, fs = 32kHz, 44.1kHz, 48kHz)

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fs	64fs/128fs/256fs/512fs	(default)
1	768fs	64fs/128fs/256fs/512fs	

The AK4493S supports DSD data stream rates of 2.8224MHz (64fs), 5.6448MHz (128fs), 11.2896MHz (256fs), and 22.5792MHz (512fs) for 44.1kHz base rates. Any base rate in the range 30kHz ~ 48kHz is supported. The data sampling speed is selected by DSDSEL[1:0] bits (Table 19).

Table 19. DSD Data Stream Selection

DSD mode	DSDSEL1	DSDSEL0	DCLK Frequency	DSD data stream			
				fs=32kHz	fs=44.1kHz	fs=48kHz	
DSD64	0	0	64fs	2.048MHz	2.8224MHz	3.072MHz	(default)
DSD128	0	1	128fs	4.096MHz	5.6448MHz	6.144MHz	
DSD256	1	0	256fs	8.192MHz	11.2896MHz	12.288MHz	
DSD512	1	1	512fs	16.384MHz	22.5792MHz	24.576MHz	

The AK4493S has a Volume bypass function for play backing DSD signal. Two modes are selectable by DSDD bit (Table 20). When setting DSDD bit = "1", the output volume control and zero detect functions are not available.

Table 20. DSD Play Back Path Selection

DSDD	Mode	
0	Normal Path	(default)
1	Volume Bypass	

[3] External Digital Filter Mode (EXDF Mode; Register Control mode only)

The external clocks that are required in EXDF mode are MCLK, BCK and WCK. The BCK and MCLK clocks must be the same frequency and continuous, not burst mode. BCK and MCLK frequencies for each sampling speed are shown in Table 21. ECS bit selects WCK frequency from 384kHz and 768kHz.

All circuits except control registers, bias generation circuit and internal LDO (if LDOE pin = "H") of the AK4493S are automatically placed in power-down state when MCLK edge is not detected for more than 1us during normal operation (PDN pin = "H"), and the analog output becomes Hi-Z state. The power-down state is released and the AK4493S starts operation by inputting MCLK again. In this case, register settings are not initialized.
When the reset is released (PDN pin = "L" → "H"), the AK4493S is in power-down state until MCLK, BCK and WCK are input.

Table 21. System Clock Example (EXDF Mode)

Sampling Speed[kHz]	MCLK&BCK [MHz]				ECS bit	
	32fs	48fs	64fs	96fs		
352.8	11.2896	16.9344	22.5792	33.8688	1	
384	12.288	18.432	24.576	36.864	1	

Sampling Speed[kHz]	MCLK&BCK [MHz]				ECS bit	
	8fs	16fs	32fs	48fs		
705.6	N/A	N/A	22.5792	33.8688	0	(default)
768	N/A	N/A	24.576	36.864	0	

■ Audio Interface Format

[1] PCM Mode

(1) Input Data Format
Data is shifted in via the SDATA pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 pins (Pin Control Mode) or DIF[2:0] bits (Register Control Mode) as shown in Table 22. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Mode 2 can be used for 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs.

Normal Mode (TDM[1:0] bits = "00" in Register Control mode, fixed configuration in Pin Control mode)
2ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 pins (Pin Control Mode) or DIF[2:0] bits (Register Control Mode) as shown in Table 22. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Mode 6 can be used for 24-bit, 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs.

TDM128 Mode (TDM[1:0] bits = "01", Register Control Mode only)
4ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Data slot can be selected by SDS[2:0] bits (Table 23). BICK is fixed to 128fs. Six data formats are supported and selected by the DIF[2:0] bits, as shown in Table 22. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

TDM256 Mode (TDM[1:0] bits = "10", Register Control Mode only)
8ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Data slot can be selected by SDS[2:0] bits (Table 23). BICK is fixed to 256fs. Six data formats are supported and selected by the DIF[2:0] bits, as shown in Table 22. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

TDM512 Mode (TDM[1:0] bits = "11", Register Control Mode only)
16ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Data slot can be selected by SDS[2:0] bits (Table 23). BICK is fixed to 512fs. Six data formats are supported and selected by the DIF[2:0] bits, as shown in Table 22. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

Table 22. Audio Interface Format (PCM mode)

Mode		TDM1 bit	TDM0 bit	DIF2	DIF1	DIF0	SDATA Format	LRCK	BICK	Figure	
Normal (Note 44)	0	0	0	0	0	0	16-bit LSB justified	H/L	≥32fs	Figure 25	
	1			0	0	1	20-bit LSB justified	H/L	≥40fs	Figure 26	
	2			0	1	0	24-bit MSB justified	H/L	≥48fs	Figure 27	
	3			0	1	1	16-bit I²S compatible	L/H	32fs	Figure 28	
							24-bit I²S compatible	L/H	≥48fs		
	4			1	0	0	24-bit LSB justified	H/L	≥48fs	Figure 26	
	5			1	0	1	32-bit LSB justified	H/L	≥64fs	Figure 29	
	6			1	1	0	32-bit MSB justified	H/L	≥64fs	Figure 30	(default)
	7			1	1	1	32-bit I²S compatible	L/H	≥64fs	Figure 31	
TDM128	8	0	1	0	1	0	24-bit MSB justified	H/L	128fs	Figure 32	
	9			0	1	1	24-bit I²S compatible	L/H	128fs	Figure 33	
	10			1	0	0	24-bit LSB justified	H/L	128fs	Figure 34	
	11			1	0	1	32-bit LSB justified	H/L	128fs	Figure 32	
	12			1	1	0	32-bit MSB justified	H/L	128fs	Figure 32	
	13			1	1	1	32-bit I²S compatible	L/H	128fs	Figure 33	
TDM256	14	1	0	0	1	0	24-bit MSB justified	H/L	256fs	Figure 35	
	15			0	1	1	24-bit I²S compatible	L/H	256fs	Figure 36	
	16			1	0	0	24-bit LSB justified	H/L	256fs	Figure 37	
	17			1	0	1	32-bit LSB justified	H/L	256fs	Figure 35	
	18			1	1	0	32-bit MSB justified	H/L	256fs	Figure 35	
	19			1	1	1	32-bit I²S compatible	L/H	256fs	Figure 36	
TDM512	20	1	1	0	1	0	24-bit MSB justified	H/L	512fs	Figure 38	
	21			0	1	1	24-bit I²S compatible	L/H	512fs	Figure 39	
	22			1	0	0	24-bit LSB justified	H/L	512fs	Figure 40	
	23			1	0	1	32-bit LSB justified	H/L	512fs	Figure 38	
	24			1	1	0	32-bit MSB justified	H/L	512fs	Figure 38	
	25			1	1	1	32-bit I²S compatible	L/H	512fs	Figure 39	

Note 44. The number of BICK cycles per frame allowed is a min. of 2x the data resolution set by DIF[2:0] (e.g. – 32fs for 16-bit data) or any number of additional BICK cycles up to the max. per the Switching Characteristics tBCK Min. Settings of the DIF[2:0] pins are valid in Normal mode only.

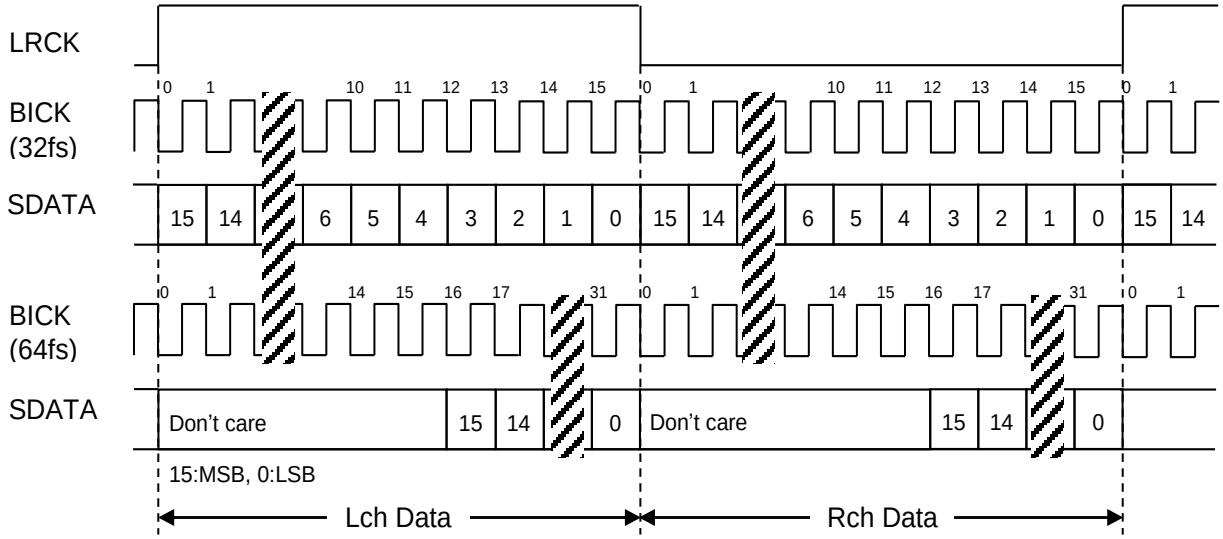


Figure 25. Mode 0 Timing

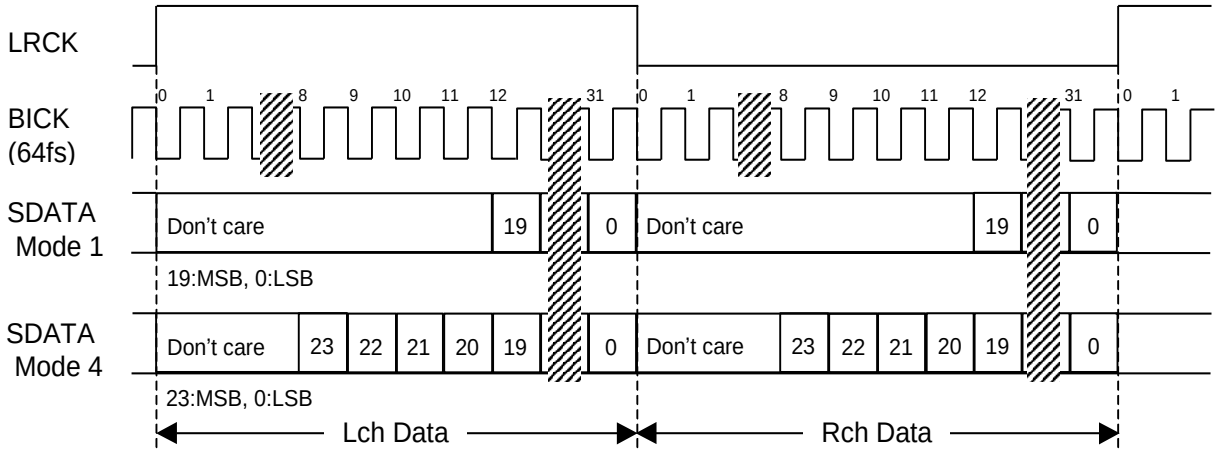


Figure 26. Mode 1, 4 Timing

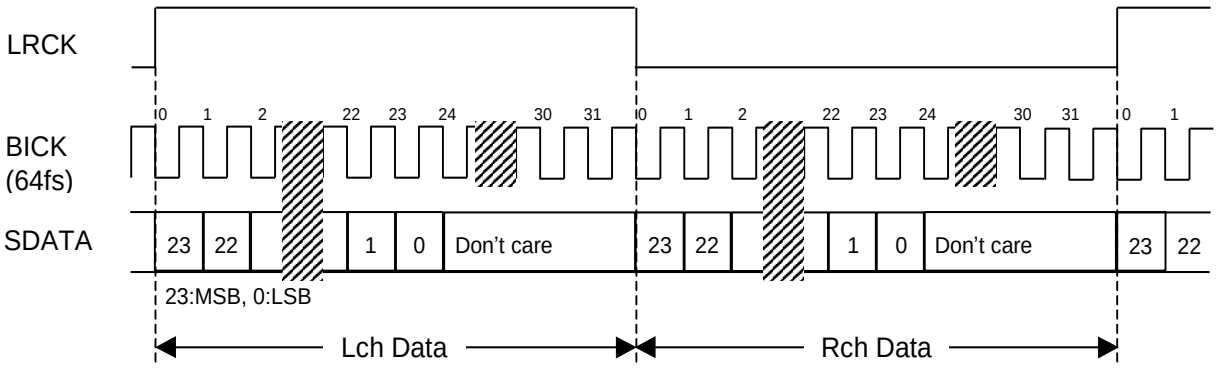


Figure 27. Mode 2 Timing

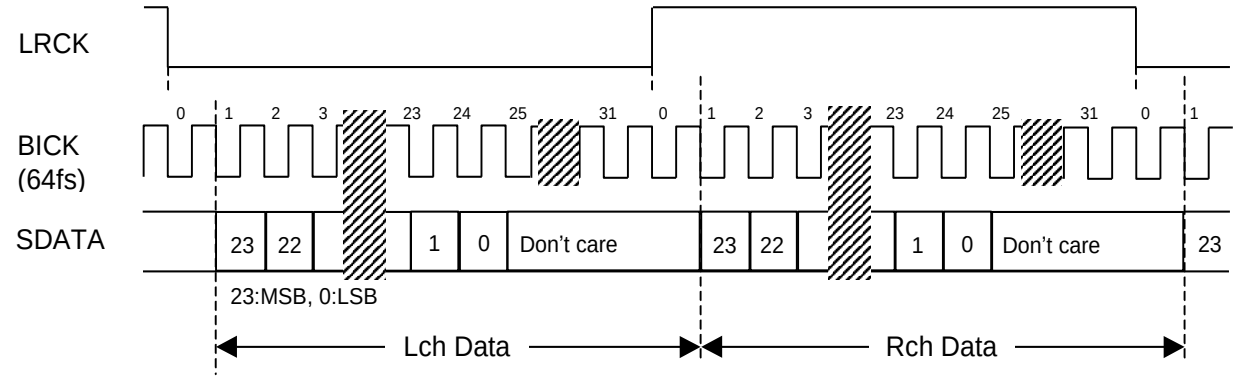


Figure 28. Mode 3 Timing

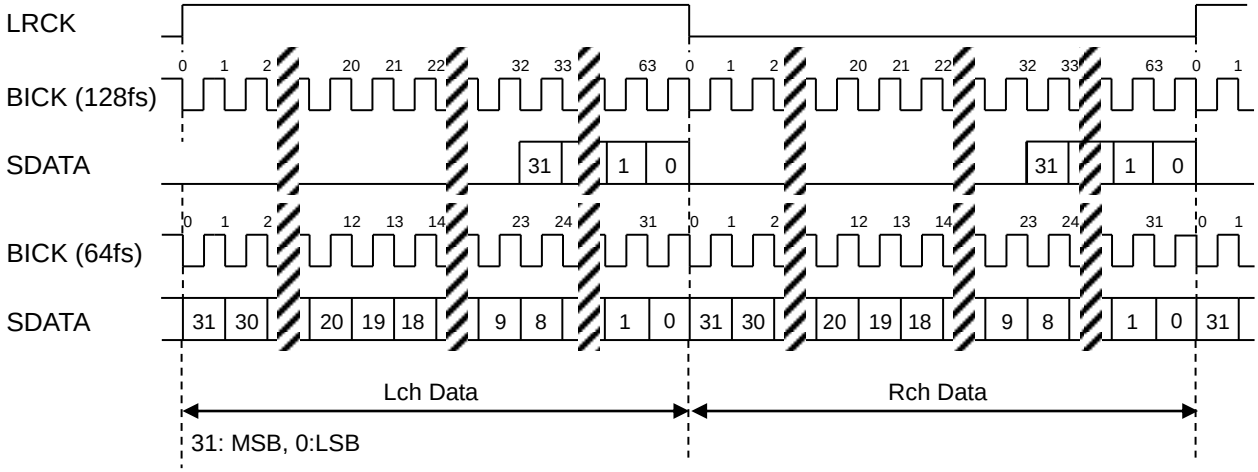


Figure 29. Mode 5 Timing

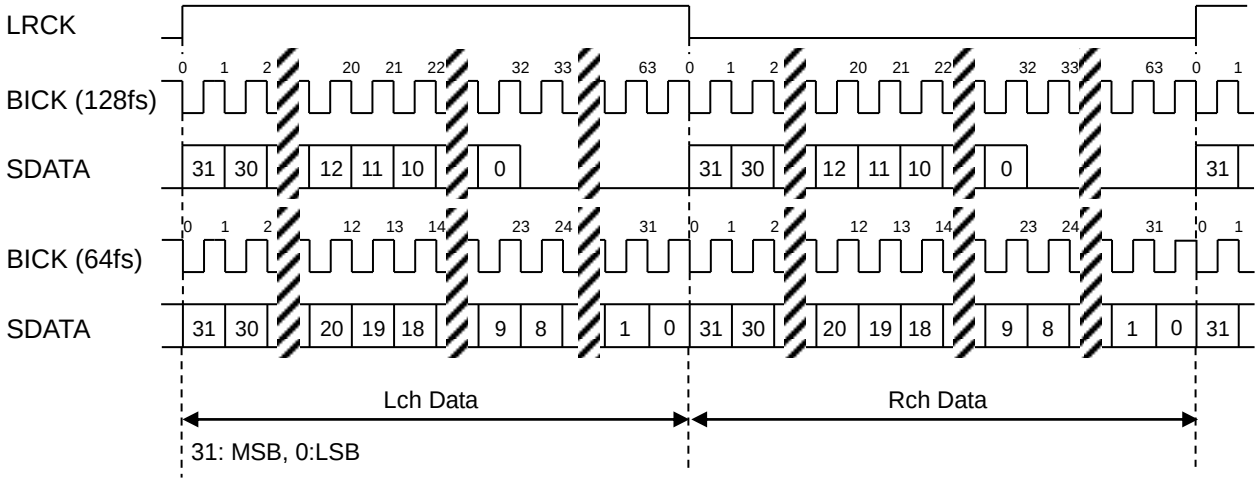


Figure 30. Mode 6 Timing

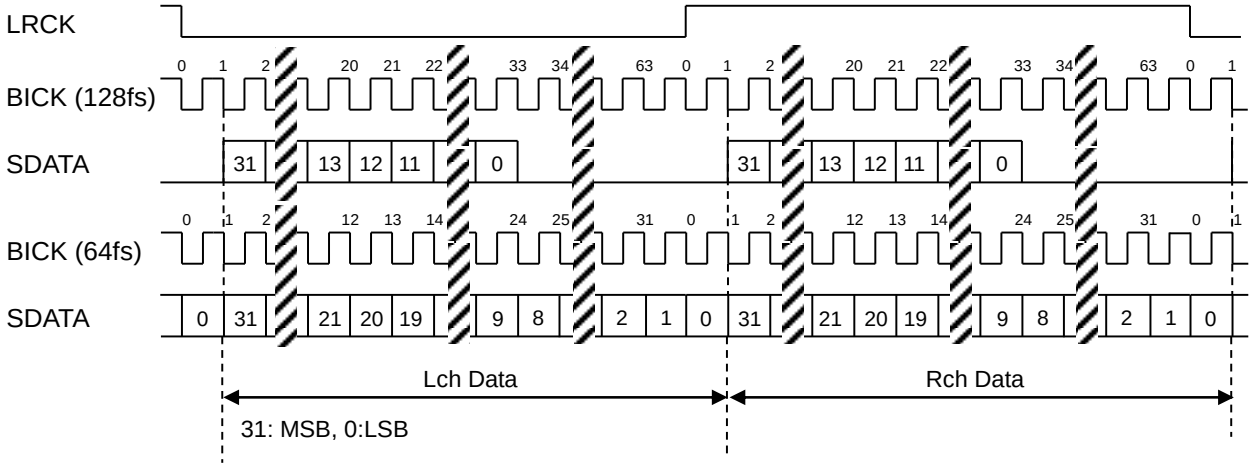


Figure 31. Mode 7 Timing

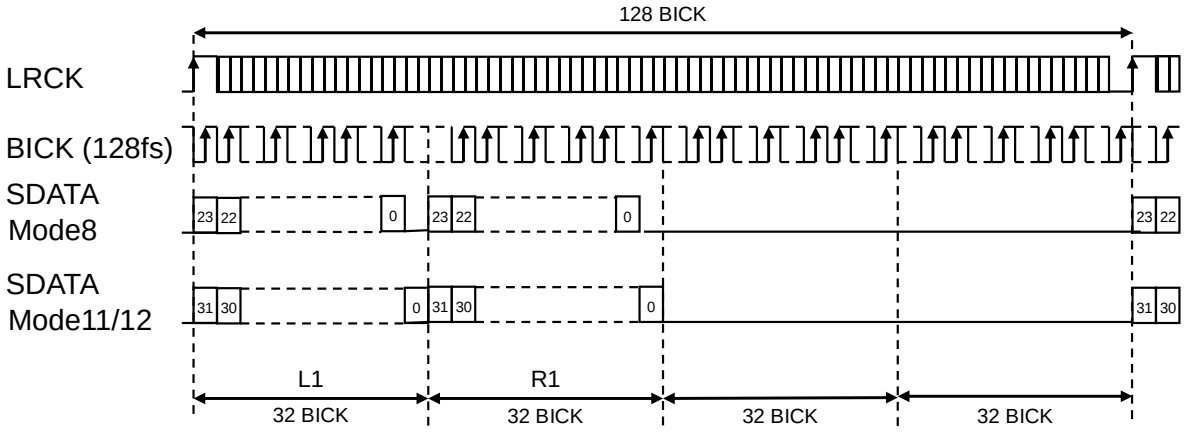


Figure 32. Mode 8/11/12 Timing

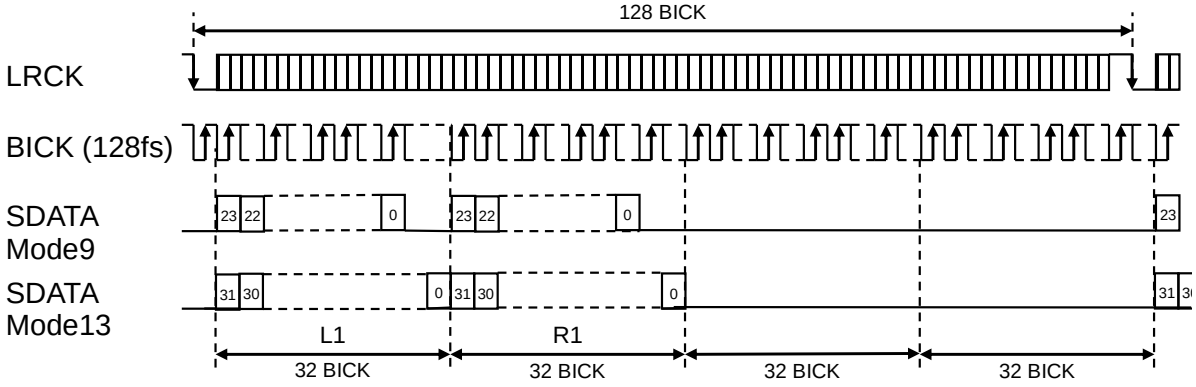


Figure 33. Mode 9/13 Timing

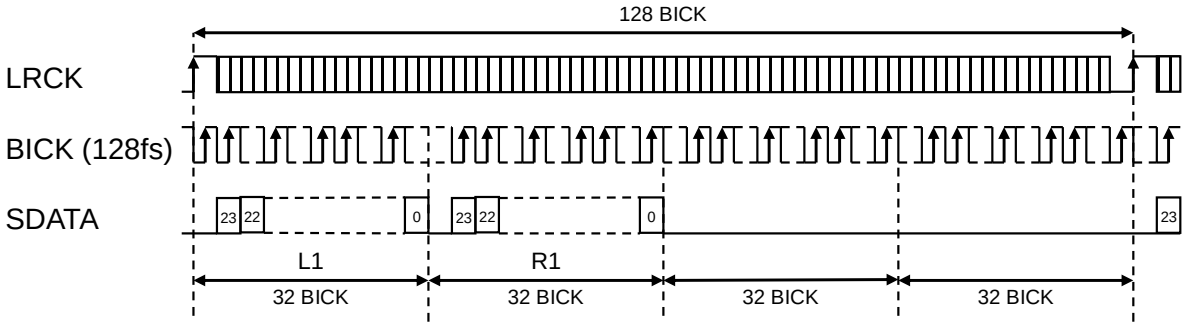


Figure 34. Mode 10 Timing

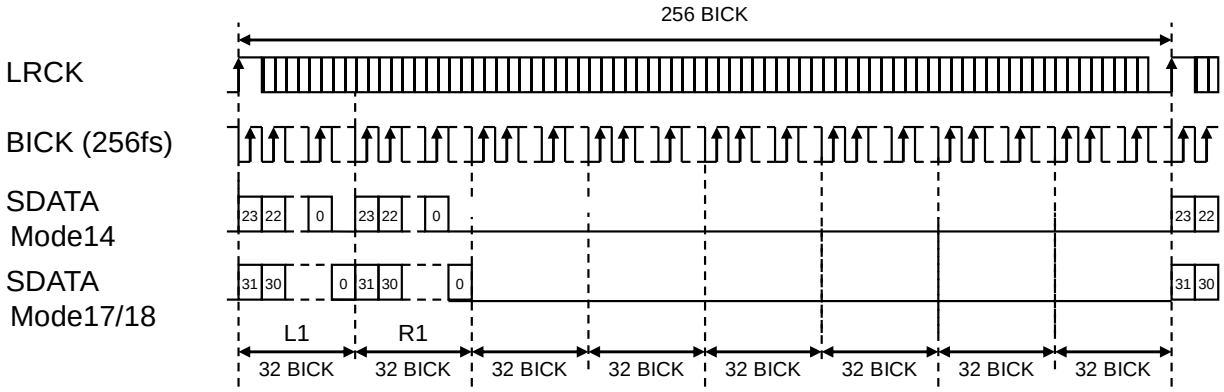


Figure 35. Mode 14/17/18 Timing

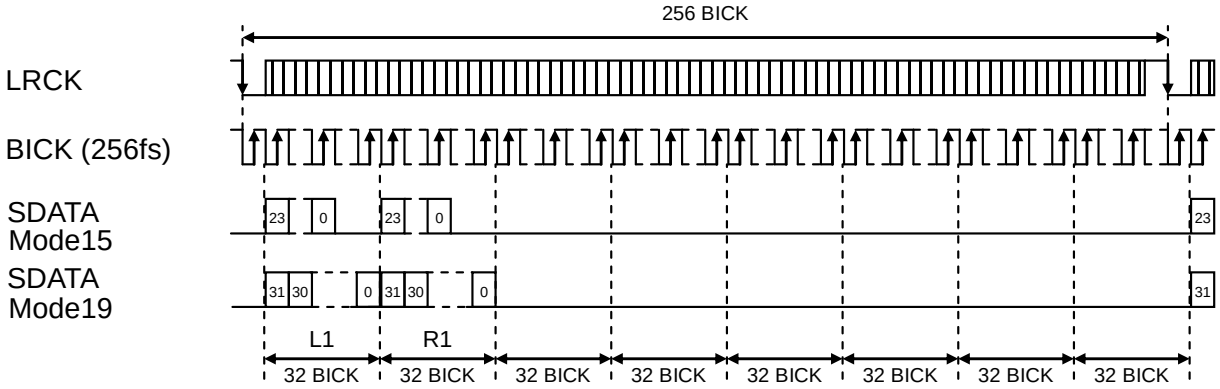


Figure 36. Mode 15/19 Timing

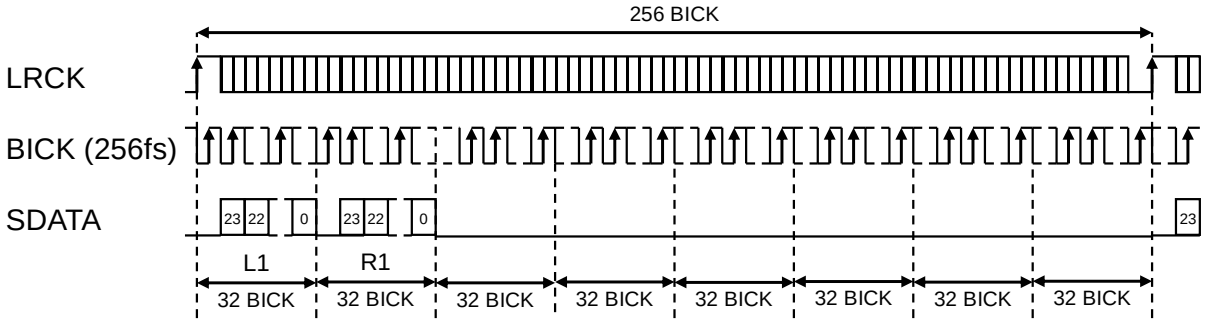


Figure 37. Mode 16 Timing

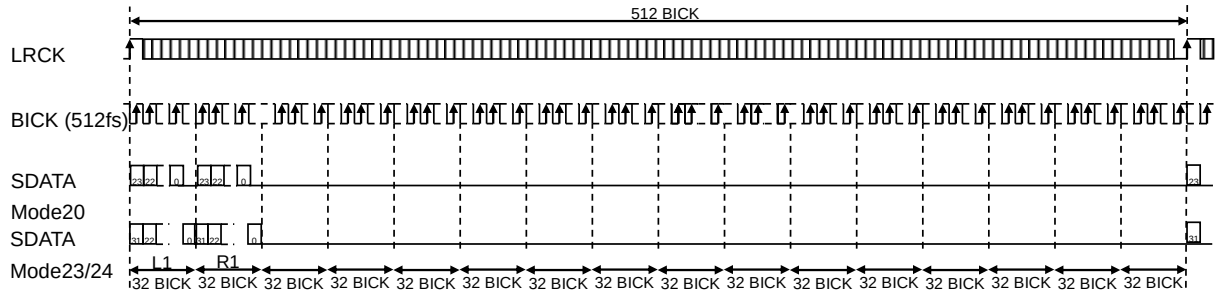


Figure 38. Mode 20/23/24 Timing

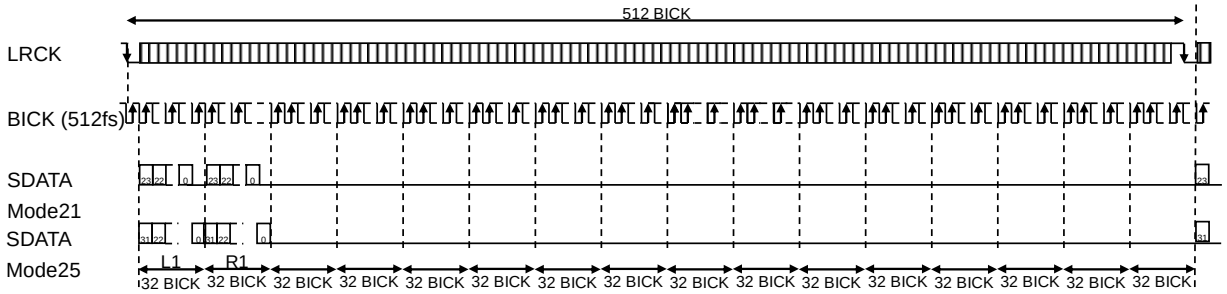


Figure 39. Mode 21/25 Timing

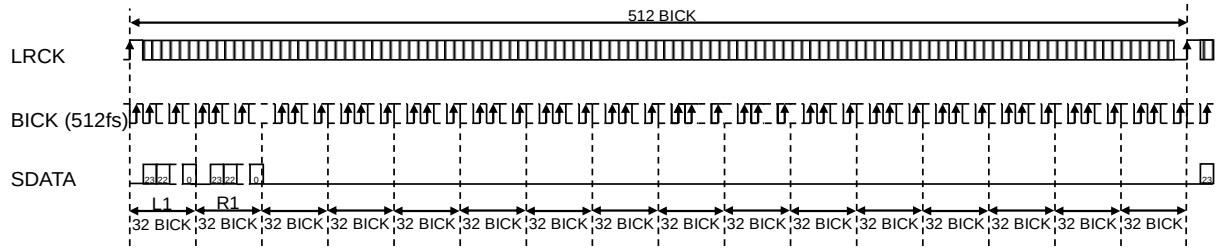


Figure 40. Mode 22 Timing

(2) Data Slot Selection Function

Data slot of 1cycle LRCK for each audio data format is defined as Figure 41 ~ Figure 44. DAC output data can be selected by SDS[2:0] bits (Register Control Mode only), as shown in Table 23.

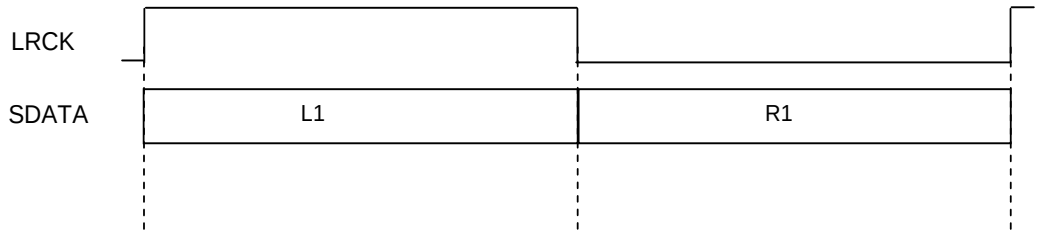


Figure 41. Data Slot in Normal Mode

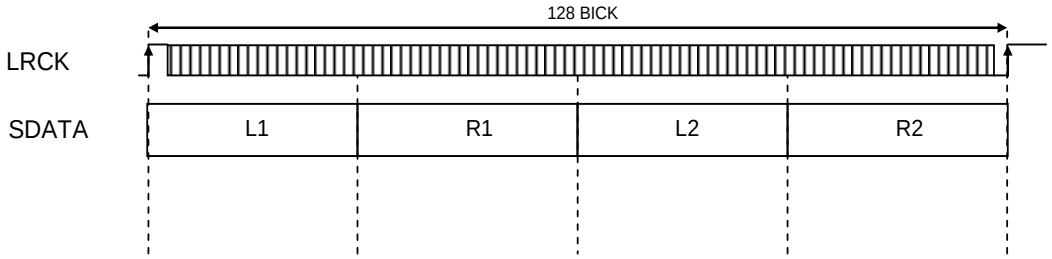


Figure 42. Data Slot in TDM128 Mode

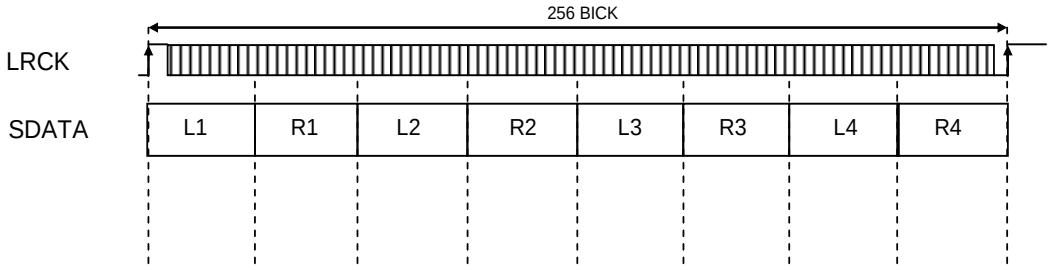


Figure 43. Data Slot in TDM256 Mode

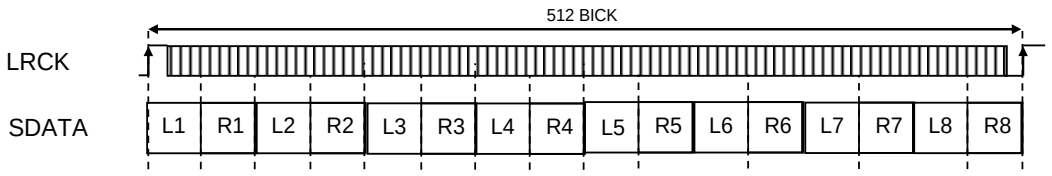


Figure 44. Data Slot in TDM512 Mode

Table 23. Data Select

	TDM1	TDM0	SDS2	SDS1	SDS0	DAC	
						Lch	Rch
Normal	0	0	*	*	*	L1	R1
TDM128	0	1	*	*	0	L1	R1
			*	*	1	L2	R2
TDM256	1	0	*	0	0	L1	R1
			*	0	1	L2	R2
			*	1	0	L3	R3
			*	1	1	L4	R4
TDM512	1	1	0	0	0	L1	R1
			0	0	1	L2	R2
			0	1	0	L3	R3
			0	1	1	L4	R4
			1	0	0	L5	R5
			1	0	1	L6	R6
			1	1	0	L7	R7
			1	1	1	L8	R8

(*: Do not care)

[2] DSD Mode (Register Control Mode only)

In DSD mode, L channel data and R channel data must be input to the DSDL pin and the DSDR pin, respectively by synchronizing to DCLK. In case of DSD mode, the settings of DIF2-0 pins and DIF[2:0] bits are ignored. The frequency of DCLK is selected among 64fs, 128fs, 256fs and 512fs by DSDSEL[1:0] bits. Polarity of DCLK is possible to invert by DCKB bit. The AK4493S does not support phase modulation when DCLK is 512fs (DSDSEL[1:0] bits = “11”).

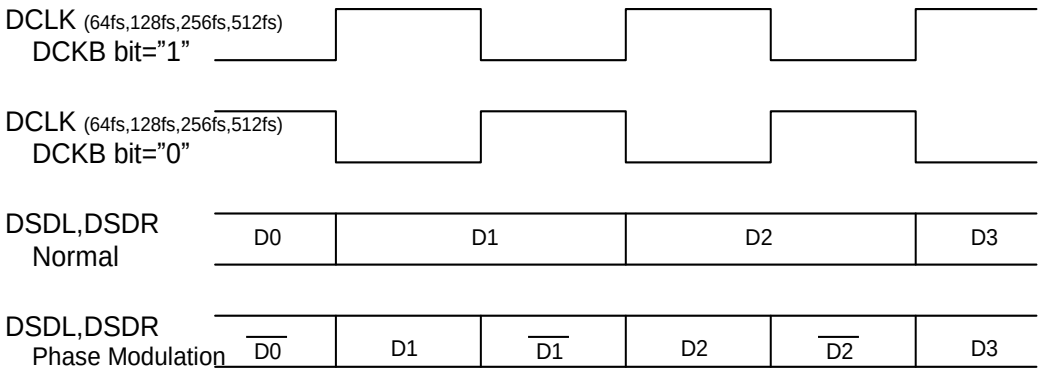


Figure 45. DSD Mode Timing

[3] External Digital Filter Mode (EXDF mode; Register Control Mode only)

The audio data is input by MCLK, BCK and WCK from the DINL and DINR pins. Three formats are available (Table 24) by DIF2-0 bits setting. The data is latched on the rising edge of BCK. The BCK and MCLK clocks must not burst.

Table 24. Audio Interface Format (EXDF mode) (N/A: Not Available)

Mode	DIF2	DIF1	DIF0	Input Format	
0	0	0	0	16-bit LSB justified	
1	0	0	1	N/A	
2	0	1	0	16-bit LSB justified	
3	0	1	1	N/A	
4	1	0	0	24-bit LSB justified	
5	1	0	1	32-bit LSB justified	
6	1	1	0	24-bit LSB justified	(default)
7	1	1	1	32-bit LSB justified	

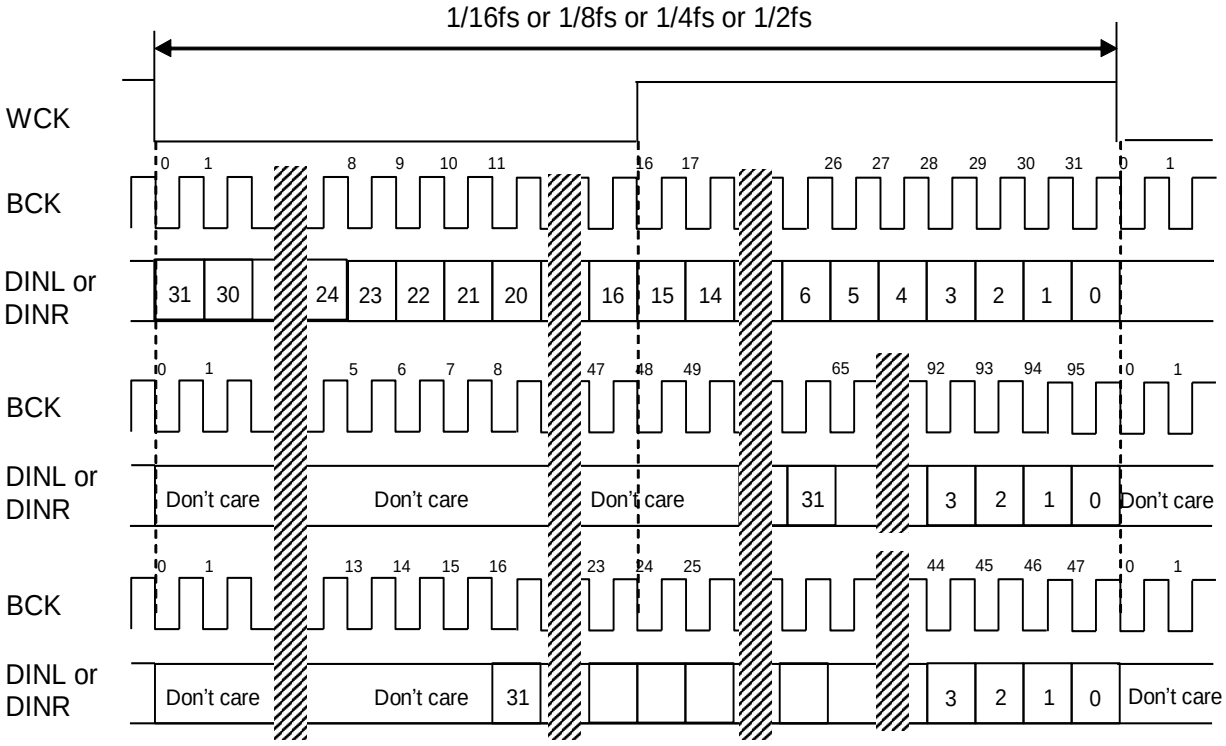


Figure 46. EXDF Mode Timing

■ Digital Filter

Six types of digital filter in PCM mode and two types of digital filter in DSD mode are available in the AK4493S for sound color selection of music playback.

In PCM mode, the digital filter can be selected by the SD, SLOW and SSLOW pins if the AK4493S is in Pin Control Mode, and it can be selected by the SD, SLOW and SSLOW bits in Register Control Mode (Table 25).

Table 25. Digital Filter Setting

SSLOW	SD	SLOW	Mode	
0	0	0	Sharp Roll-off filter	
0	0	1	Slow Roll-off filter	
0	1	0	Short Delay Sharp Roll-off filter	(default)
0	1	1	Short Delay Slow Roll-off filter	
1	0	*	Super Slow Roll-off filter	
1	1	*	Low Dispersion Short Delay filter	

(*: Do not care)

In DSD mode, the cutoff frequency of digital filter can be switched by the DSDF bit. Table 26 shows the cutoff frequency @fs = 44.1 kHz. The cutoff frequency tracks the sampling frequency (fs). Do not set GC[2:0] bits to “100” when DSDD bit = “0” and DSDF bit = “1”. Otherwise a pop noise may occur.

Table 26. DSD Filter Select

DSDF bit	Cut Off Frequency @fs=44.1kHz				
	DSD64	DSD128	DSD256	DSD512	
0	39kHz	78kHz	156kHz	312kHz	(default)
1	76kHz	152kHz	304kHz	608kHz	

■ De-emphasis Filter (PCM)

A digital de-emphasis filter is available for 32kHz*, 44.1kHz or 48kHz* sampling rates (tc = 50/15µs) and is enabled or disabled by the DEM pin or DEM1-0 bits. DEM1-0 bits are ignored in DSD and EXDF modes. DEM setting value is held even if the data mode is switched among PCM, DSD and EXDF modes. *(32kHz and 48kHz de-emphasis are supported in Register Control Mode only.)

Table 27. De-emphasis Control (Register Control Mode)

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 28. De-emphasis Control (Pin Control Mode)

DEM Pin	Mode	
L	44.1kHz	
H	OFF	(default)

■ Output ATT (PCM, DSD and EXDF Modes; Register Control Mode only)

The AK4493S includes channel independent digital output volumes (ATTL/R) with 256 levels at 0.5dB step including MUTE. When changing output levels, it is executed in soft transition, thus no switching noise occurs during these transitions. It can attenuate the input data from 0dB to -127dB and MUTE when assuming the output signal level is 0dB when ATTL/R[7:0] bits = “FFH”.

Table 29. Attenuation Level of Digital Attenuator

ATTL/R[7:0]bits (register 03-04H)	Attenuation Level	
FFH	+0dB	(default)
FEH	-0.5dB	
FDH	-1.0dB	
:	:	
:	:	
02H	-126.5dB	
01H	-127.0dB	
00H	MUTE (-∞)	

The transition time of digital output volume is set by ATS[1:0] bits (Table 29). When changing output levels between Mode0-3, it is executed in soft transition thus no switching noise occurs during these transitions. Register setting values will be kept even switching the PCM and DSD modes.

Table 30. Transition Time between Set Values of ATTL/R[7:0] bits

Mode	ATS1	ATS0	ATT speed			
			EXDF bit= “0”, DP bit= “0”	EXDF bit= “1” DP bit= “0”	DP bit= “1”	
0	0	0	4080/fs	4080*WCK cycle	4080/(2*fs)	(default)
1	0	1	2040/fs	2040*WCK cycle	2040/(2*fs)	
2	1	0	510/fs	510*WCK cycle	510/(2*fs)	
3	1	1	255/fs	255*WCK cycle	255/(2*fs)	

It takes 4080/fs (92.5ms @fs=44.1kHz) from “FFH” (0dB) to “00H” (MUTE) in Mode 0. The attenuation level is initialized to “FFH” (0dB) by setting the PDN pin = “L”.

If the volume is changed during reset period, the output volume will become a setting value after releasing the reset. It will change to a setting value immediately if the volume is changed within 10/fs after releasing reset.

■ Gain Adjustment Function (PCM, DSD and EXDF Modes; Register Control Mode only)

The AK4493S has the gain adjustment function. The analog output amplitude can be adjusted by GC [2:0] bits.

Table 31. Output Level between Set Values of GC [2:0] bit

GC2	GC1	GC0	AOUTLP/LN/RP/RN Output Level			
			PCM	DSD: Normal Path	DSD: Volume Bypass	
0	0	0	2.8Vpp	2.8Vpp	2.5Vpp	(default)
0	0	1	2.8Vpp	2.5Vpp	2.5Vpp	
0	1	0	2.5Vpp	2.5Vpp	2.5Vpp	
0	1	1	2.5Vpp	2.5Vpp	2.5Vpp	
1	0	0	3.75Vpp	3.75Vpp	2.5Vpp	
1	0	1	3.75Vpp	2.5Vpp	2.5Vpp	
1	1	0	2.5Vpp	2.5Vpp	2.5Vpp	
1	1	1	2.5Vpp	2.5Vpp	2.5Vpp	

Note 45. DSDF bit must be set to “0” if GC [2:0] bits are set to “100” when using DSD Normal Path. Click noise may occur if DSDF bit is set to “1”.

■ Zero Detection (PCM, DSD and EXDF Modes; Register Control Mode only)

The AK4493S has a channel-independent zero detection function and zero detection flag is output from the DZFL/R pin when setting DZFE bit = “1” and DDMOE bit = “0”. When the input data at each channel is continuously zeros for 8192 LRCK cycles, the DZF pin of each channel outputs zero detection flag independently. Polarity of the detection flag of the DZFL/R pin can be selected by DZFB bit. The DZFL/R pin goes “H” for zero detection when DZFB bit = “0”, the DZFL/R pin goes “L” when DZFB bit = “1”.

When DZFB bit = “0”, the DZFL/R pin immediately returns to “L” if the input data of each channel is not zero after going to “H”. If the RSTN bit is “0”, the DZF pins of both L and R channels go to “H”. The DZFL/R pin returns to “L” in 4 ~ 5/fs after the input data of each channel becomes “1” when RSTN bit is set to “1”.

If DZFM bit is set to “1” while DZFB bit = “0”, the DZF pins of both L and R channels go to “H” only when the input data for both channels are continuously zeros for 8192 LRCK cycles (16384 times in DSD 512fs mode). The zero detect function can be disabled by setting DZFE bit = “0”. In this case, DZF pins of both channels are always “L”. The zero detect function is also disabled when Volume Bypass is selected in DSD mode.

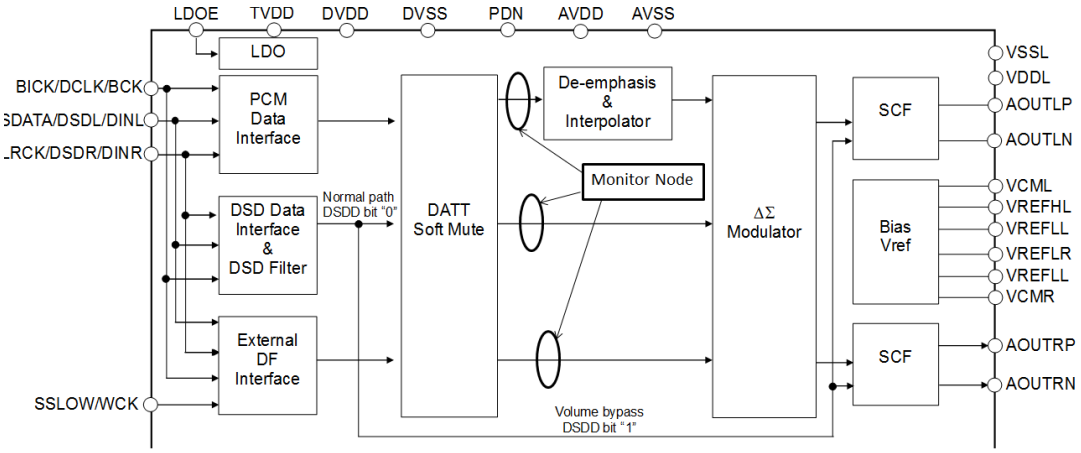


Figure 47. Zero Detection Monitor Node

Table 32. Zero Detect Selection

DZFE	DZFB	RSTN	Data	DZF-pin	
0	0	*	*	L	(default)
	1	*	*	H	
1	0	0	*	H	
		1	not zero	L	
			zero detect	H	
	1	0	-	L	
		1	not zero	H	
			zero detect	L	

(*: Do not care)

The DZFL/R pin also has DSD full-scale detection output function. DSD full-scale detection signal (DMR, DML) is output from the DZFL/R pin when DDMOE bit = "1". The output signal setting of the DZFL/R pin is shown in Table 33. The output polarity is inverted when DZFB bit = "1".

Table 33. Output Signal Setting of the DZFL/DZFR Pin

DDMOE	DZFE	DZFM	DZFL pin	DZFR pin	
0	0	*	L	L	(default)
	1	0	Lch Zero Detection Flag	Rch Zero Detection Flag	
		1	AND Signal of Lch and Rch Zero Detection Flags	AND Signal of Lch and Rch Zero Detection Flags	
1	*	0	DML	DMR	
	0	1	L	OR Signal of DML and DMR	
	1	1	AND Signal of Lch and Rch Zero Detection Flags		

(*: Do not care)

■ LR Channel Output Signal Select, Phase Inversion Function (PCM, DSD and EXDF Modes)

In register control mode, input and output combination of the AK4493S can be changed by MONO bit and SELLR bit. In addition, the output signal phase can be inverted by INVL bit and INVR bit. These functions are available on all audio formats. In pin control mode, the phase of R channel output can be inverted by setting the INVR pin.

Table 34. Output Select (Register Control Mode)

MONO bit	SELLR bit	INVL bit	INVR bit	Lch Out	Rch Out
0	0	0	0	Lch In	Rch In
		0	1	Lch In	Rch In Invert
		1	0	Lch In Invert	Rch In
		1	1	Lch In Invert	Rch In Invert
0	1	0	0	Rch In	Lch In
		0	1	Rch In	Lch In Invert
		1	0	Rch In Invert	Lch In
		1	1	Rch In Invert	Lch In Invert
1	0	0	0	Lch In	Lch In
		0	1	Lch In	Lch In Invert
		1	0	Lch In Invert	Lch In
		1	1	Lch In Invert	Lch In Invert
1	1	0	0	Rch In	Rch In
		0	1	Rch In	Rch In Invert
		1	0	Rch In Invert	Rch In
		1	1	Rch In Invert	Rch In Invert

Table 35. Output Select (Pin Control Mode)

INVR pin	Lch Out	Rch Out
L	Lch In	Rch In
H	Lch In Invert	Rch In Invert

* With the INV function, it is assumed that the AK4493S is connected to the AK4205 without crossing the signal lines.

■ Sound Quality Adjustment Function (PCM, DSD, EXDF; Register Control Mode only)

Sound quality of the AK4493S can be controlled by setting SC[2:0] bits. The Analog Characteristics are specified and only guaranteed in Setting 1 and Setting 3 combined.

Table 36. Sound Quality Select Mode

SC1	SC0	Sound	
0	×	Analog internal current, maximum (Setting1)	(default)
1	×	Analog internal current, medium (Setting2)	

Table 37. Sound Quality Select Mode

SC2	Sound	
0	Sound Setting 3	(default)
1	Sound Setting 4	

■ DSD Signal Full-Scale (FS) Detection

The AK4493S has independent full-scale detection function for each channel in DSD mode.
Mute function of analog output signal becomes enabled after detecting full-scale signal by setting DDM bit = “1”. Figure 48 shows a block diagram of DSD signal playback. Input data of each channel pin (DSDL or DSDR) is received via the DSD_IF block and full-scale detection is executed at the DSD full-scale detection block. The AK4493S mutes the analog output when either L or R channel full-scale signal becomes “1” when DDM bit = “1”. To prevent click noise, DSD_IF block output signal is delayed for “DDMT[1:0] bits setting + 8DCLK cycles” by register block until the signal is muted completely, thus the analog output also delays.

If the input data of either Lch or Rch is continuously “H” or “L” for the time set by DDMT[1:0] bits, the AK4493S is in full-scale detection state (Table 38) and corresponding DML or DMR bit becomes “1” independently. These bits only indicate “1” while full-scale data is input. DML/DMR bit is “0” if the input data is not full-scale in PCM/EXDF mode. Full-scale detection signal can also be output from the DZFL or DZFR pin by setting DDMOE bit = “1”. Refer to Table 32 for details. The AK4493S mutes the analog output when full-scale data is input to either L or R channel. This analog output mute transition is depending on the setting of DSDD bit that selects DSD playback path (Table 39).

When DSDD bit = “1” (Volume Bypass), the output data of DSD filter is changed to Zero data if the AK4493S is in full-scale state. When DSDD bit = “0” (Normal Path), the output data of DSD filter is changed to Zero data and the data is soft muted by DATT block if the AK4493S is in full-scale state. Mute transition time is set by ATS[1:0] bits from 255/2fs to 4080/2fs (fs = 30~48kHz in DSD mode). However, output signal is muted to zero immediately after the AK4493S becomes full-scale detection state since it is much depending on the DSD filter output data transition time.

Full-scale detection state is released when the input data of the full-scale input channel is toggled. The operation after full-scale detection is released is according to DSDD bit setting that selects DSD playback path (Table 39).

If DSDD bit = “1” (Volume Bypass), the AK4493S returns to normal operation as DSD filter output signal is output and the output data is changed immediately when the full-scale detection state is released.
If DSDD bit = “0” (Normal Path), the AK4493S returns to normal operation as DSD filter output signal is output and the soft mute by the DATT block is released. The transition time until the output data returns to normal after releasing full-scale detection state is according to the setting of ATS[1:0] bits since it is much depending on the transition time of attenuating coefficient of DATT block.

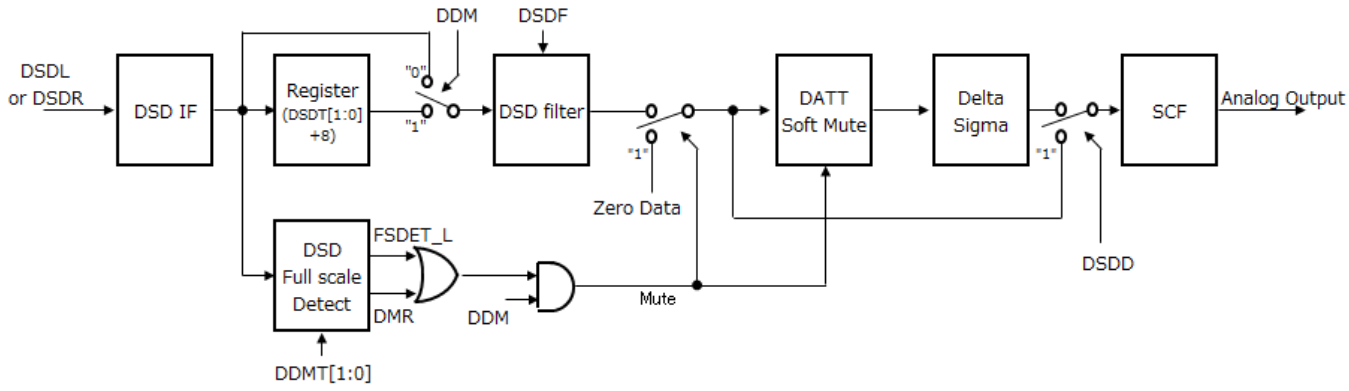


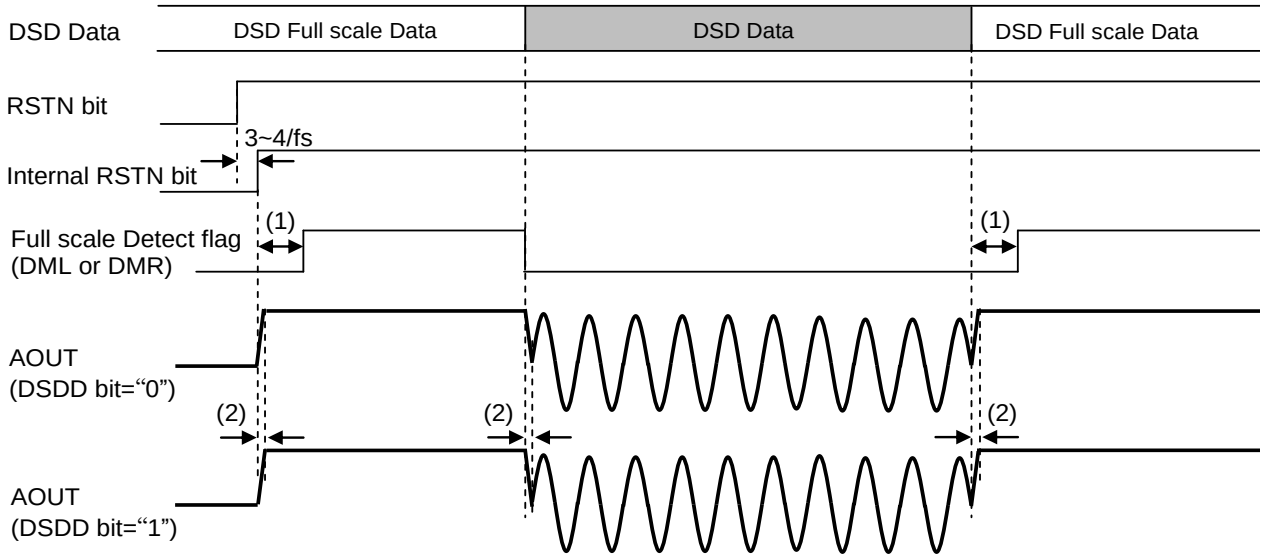
Figure 48. DSD Block Diagram

Table 38. DSD Signal Full-scale Detection Time Setting

DDMT1	DDMT0	Detection Time	Register Delay	
0	0	256 DCLK Cycles	264 DCLK Cycles	(default)
0	1	512 DCLK Cycles	520 DCLK Cycles	
1	0	1024 DCLK Cycles	1032 DCLK Cycles	
1	1	128 DCLK Cycles	136 DCLK Cycles	

Table 39. DSD Mode and Device Status after Full-Scale Detection (DDM bit = “1”)

DSDD	Mode	Mute Transition time	Mute Release time	
0	Normal Path	Rapidly	As ATS[1:0]	(default)
1	Volume Bypass	Rapidly		

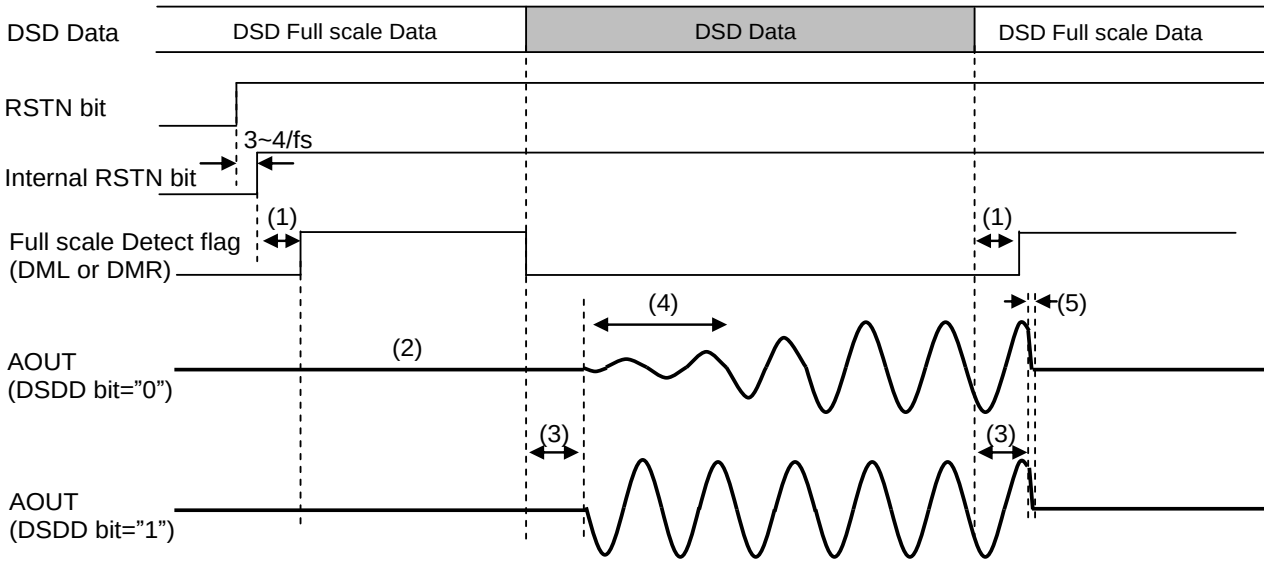


Note:

(1) Internal reset is released after 3~4/fs by setting RSTN bit = “0”. The internal detection flag becomes “1” if full-scale data is input for a period set by DDMT[1:0] bits after releasing internal reset. In this case, excessive signals will be output from the analog output if the DSD input data is full-scale.

(2) Transition time of analog output data to full-scale is set by DSDF bit.

Figure 49. Analog Output Waveform with DSD Full-scale Input (DDM bit = “0”)



Notes:

(1) Internal reset is released after 3~4/fs by setting RSTN bit="0". The internal detection flag becomes "1" if the input data is full-scale for a period set by DDMT[1:0] bits after releasing internal reset.
(2) Analog output is forced to zero (VCML/R level) when the AK4493S detects full-scale data.
(3) Analog output delays for the period set by DDMT[1:0] bits + 8DCLK cycles when setting DDM bit = "1".
(4) The time to return to normal output state from full-scale state is controlled by transition time setting of internal DATT circuit by ATS[1:0] bits.
(5) Analog output is forced to zero (VCML/R level) immediately when it becomes full-scale status during data input.

Figure 50. Analog Output Waveform with DSD Full-scale Input (DDM bit = "1")

■ Automatic Mode Switching Function (PCM/EXDF ⇔ DSD Mode; Register Control Mode only)

The AK4493S has automatic mode switching function that determines DSD or PCM/EXDF mode from input signals of the BICK/BCK/DCLK pin (#3), LRCK/DSDR pin (#4) and WCK pin (#6). This function is available by setting ADPE bit = "1" when the PDN pin = "H" and the PSN pin = "L". ADPE bit must be set while PW bit or RSTN bit = "0". DP bit is for manual setting. It will be ignored when ADPE bit is "1". The result of automatic mode detection can be readout by ADP bit. This readout function of ADP bit is invalid and "0" data is readout when ADPE bit = "0". Group delay will be 18/fs longer in PCM/EXDF mode and 136~1032DCLK cycle longer according to full-scale detection time setting by DDMT[1:0] bits in DSD mode when setting ADPE bit = "1" (Table 38). PCM mode and EXDF mode are not distinguished. This function does not support DSD phase modulation format and edge inversion function of DSD receiving data (DCKB bit = "1"). EXDF bit must be set while PW bit or RSTN bit = "0".

If one of the five conditions shown below is satisfied, the AK4493S executes mode detection. The AK4493S keeps previous mode instead of executing mode detection if any condition is not satisfied.

1. Input data of both channels are zero for a period set by ADPT[1:0] bits (Table 40)
2. Output data of both channels are zero for a period set by ADPT[1:0] bits because of attenuation. (Table 40)
3. Input data of both channels are full-scale for a period set by DDMT[1:0] bits in DSD mode.
4. PW bit = "0"
5. RSTN bit = "0"

Table 40. Time Until Mode Detection when Input Data Becomes Zero

ADPT1	ADPT0	Waiting time for Zero Data	
0	0	8192/fs + 18/fs	(default)
0	1	4096/fs + 18/fs	
1	0	2048/fs + 18/fs	
1	1	1024/fs + 18/fs	

Note: fs=30~48kHz in DSD mode

■PCM/EXDF ⇔ DSD Mode; EXDF bit = "0"

When EXDF bit = "0", the AK4493S execute mode detection by comparing the input signal to the LRCK/DSDR pin (#4) to fixed code patterns. There are five fixed code patterns: "01101001 01101001", "01010101 01010101", "00110011 00110011", "00000000 00000000" and "11111111 11111111". The AK4493S detects DSD mode when the input data is matched with one of "01101001 01101001", "01010101 01010101" and "00110011 00110011" codes twice continuously. The AK4493S detects PCM mode when the input data is matched with either "00000000 00000000" or "11111111 11111111" code twice continuously. After detecting the data mode, ADP bit is changed according to detected mode and it is reflected to the operation on a rising edge of the LRCK/DSDR pin (#5) input data. The data mode is kept if the input data does not match to any of the fixed codes.

Table 41. Mode Detection Conditions when EXDF bit = "0"

#5 LRCK/DSDR Input Signal	Detection Result
One of zero code pattern below is input twice continuously "01101001 01101001" or "01010101 01010101" or "00110011 00110011"	DSD Mode
One of zero code pattern below is input twice continuously "00000000 00000000" or "11111111 11111111"	PCM Mode

Input one of “01101001 01101001”, “01010101 01010101”, “00110011 00110011” code continuously to the DSDR pin to transition to DSD mode from PCM mode. Input a clock toggles in N*16BICK cycles (N must be an integral number greater than or equal to one) or a clock that keeps “L” or “H” for 32BICK cycles to the LRCK/DSDR pin (#5). Refer to Figure 51 and Figure 52 for the operation sequence.

Table 42. Input Signal when Switching PCM⇔DSD Modes (EXDF bit = “0”)

Mode	#5 LRCK/DSDR Pin Input
DSD Mode	One of zero code pattern below is input “01101001 01101001” or “01010101 01010101” or “00110011 00110011”
PCM Mode	Clock toggles in N*16BICK cycles (N ≥ 1) or Clock that keeps “L” or “H” for 32BICK cycles

When EXDF bit = “1”, the AK4493S detects DSD mode immediately and ADP bit becomes “1” to reflect the detection if an input clock to the BCK/DCLK pin (#3) has rising edges more than 256 times during one rising edge cycle of the input clock of the WCK pin (#6). The AK4493S detects EXDF mode if an input clock to the BCK/DCLK pin (#3) has rising edge less than or equal to 256 times for two rising edge cycles of the input clock of the WCK pin (#6) continuously. ADP bit becomes “0” on a rising edge of the input clock to the WCP pin (#6) when detecting EXDF mode. Input “L” to the WCK pin (#6) to playback DSD signal when setting EXDF bit = “1”. Refer to Figure 54 and Figure 55 for the operation sequence.

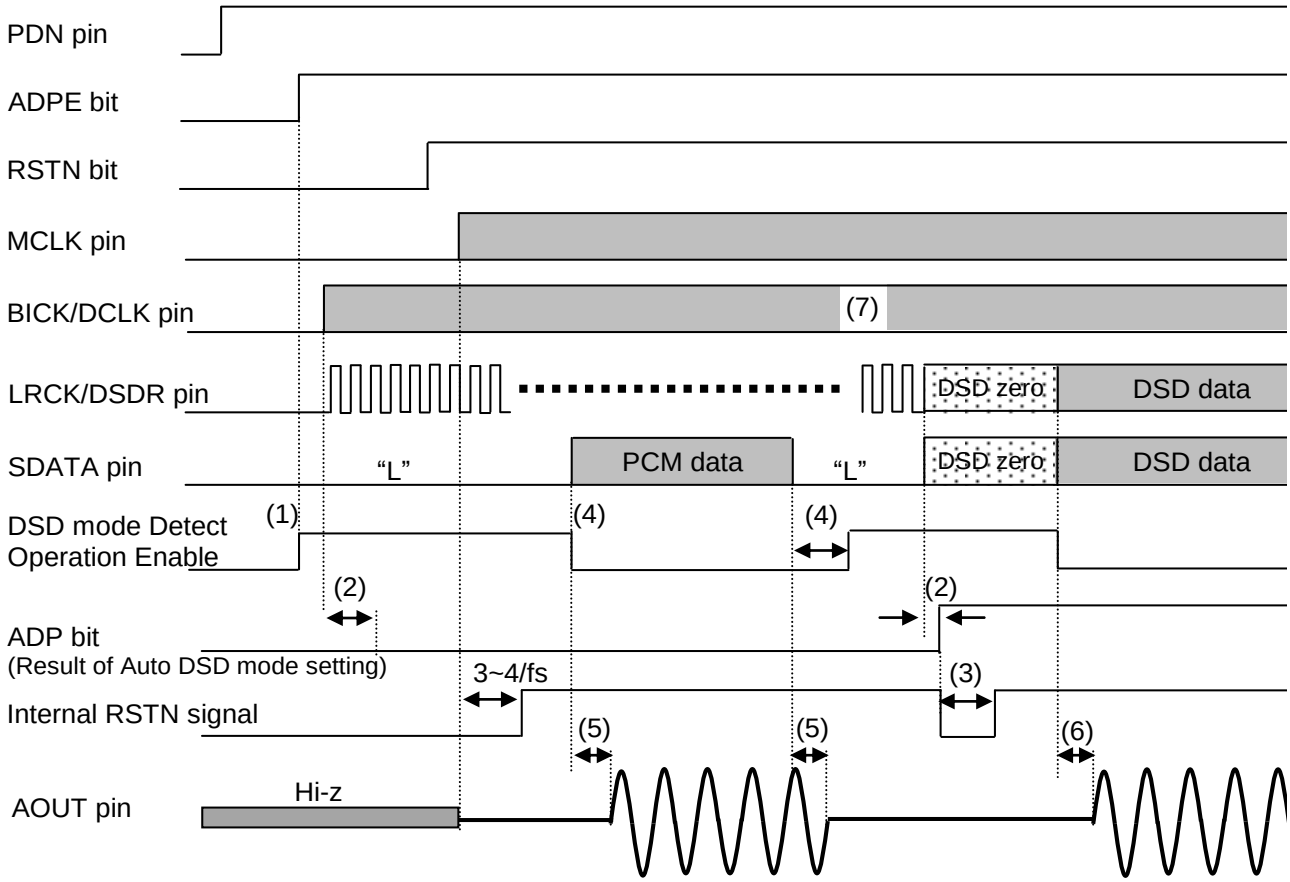
Table 43. Mode Detection Conditions when EXDF bit = “1”

Number of Pulse of BCK/DCLK (#3) In WCK (#6) Cycle	Detection Result
256 < BCK/DCLK pulse number	DSD Mode
BCK/DCLK pulse number ≤ 256, Twice Continuously	EXDF Mode

The AK4493S executes data mode detection even if there is no MCLK input when RSTN bit = “0”. However, the analog output becomes Hi-Z and the AK4493S enters power-off mode when MCLK is stopped. The AK4493S resumes operation according to a data mode that is detected when MCLK is input again. The data mode will be maintained if the input clock to the BICK/BCK/DCLK pin (#3) is stopped. The AK4493S executes internal reset for 3~4/fs automatically when transition the data mode from DSD mode and resumes operation.

Table 44. Input Signal when Switching DSD⇔EXDF Mode (EXDF bit = “1”)

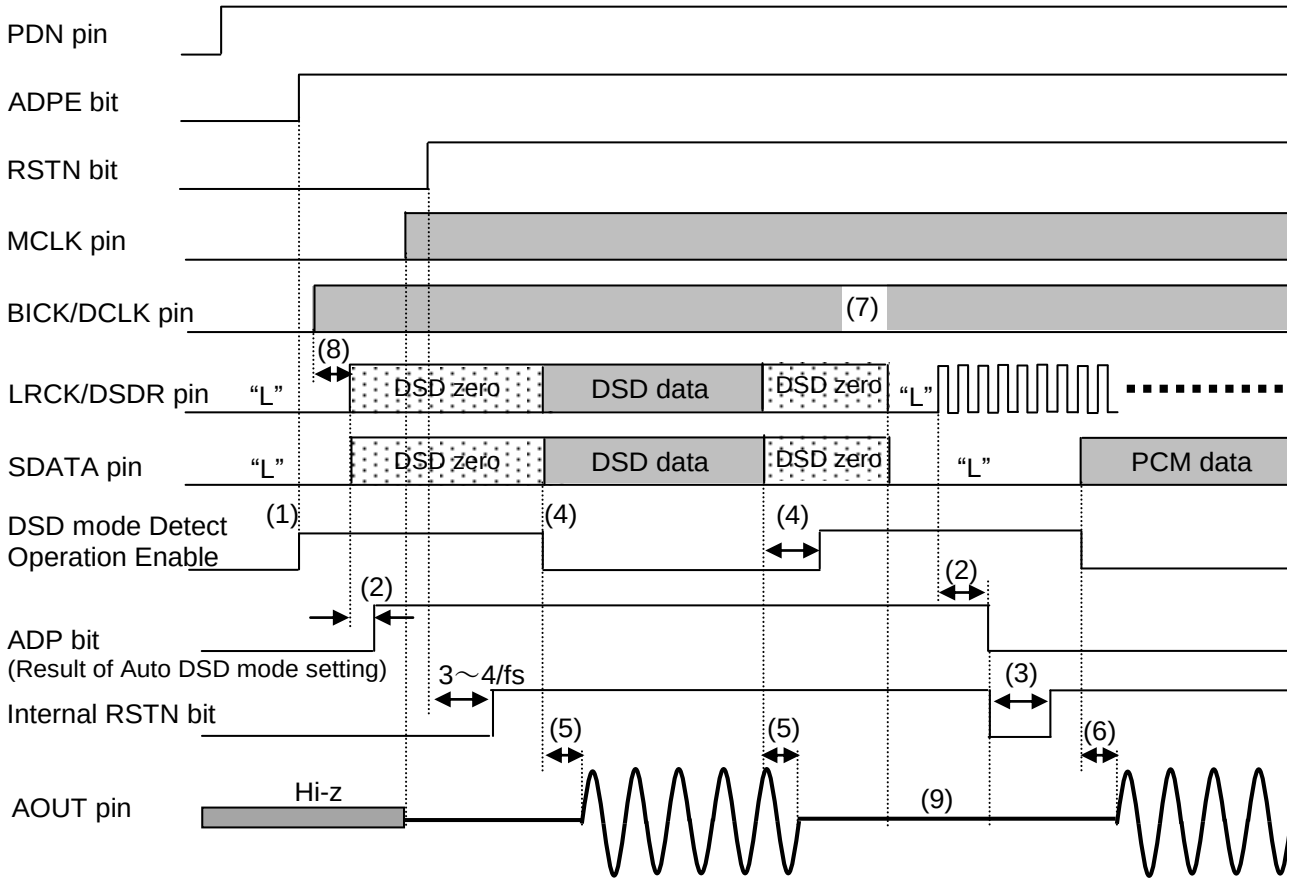
Mode	#6 WCK Pin Input
DSD Mode	L
EXDF Mode	Clock in 32~96BCK Cycles



Note:

(1) Automatic mode switching between PCM/EXDF and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.
(2) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDR pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDR pin. Mode detection is executed even when there is no MCLK input.
(3) When DSD mode is changed, the AK4493S executes internal reset for 3~4/fs automatically.
(4) The AK4493S starts mode detection when input data of both channels are continuously zero for the period set by ADPT[1:0] bits, and it finishes mode detection when a data that is not zero is input.
(5) In PCM mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".
(6) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT[1:0] bits setting.
(7) If BICK input is stopped in PCM mode, the AK4493S stays in PCM mode and continues operation.

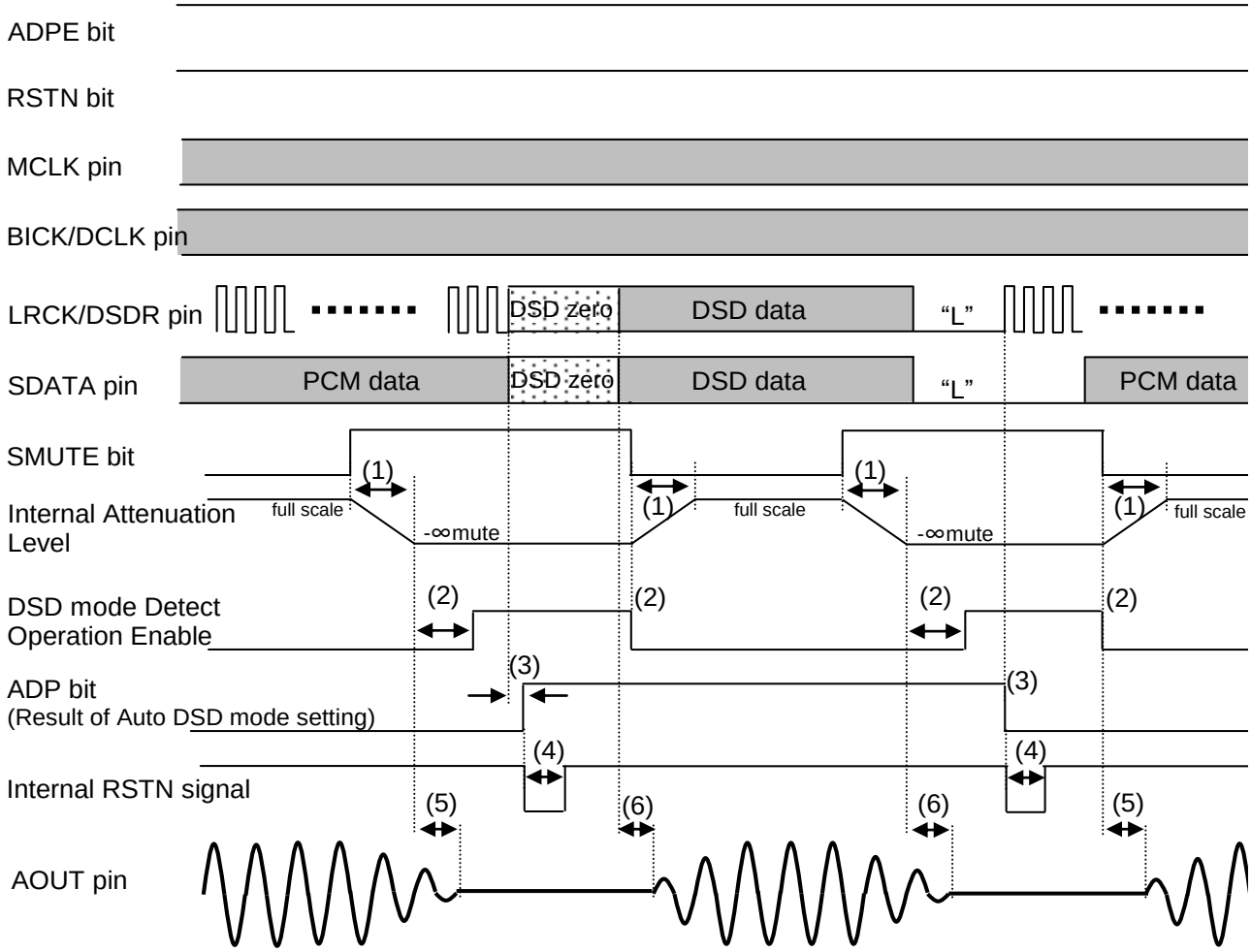
Figure 51. Changing to DSD Mode after Power-up In PCM Mode (EXDF bit = "0")



Note:

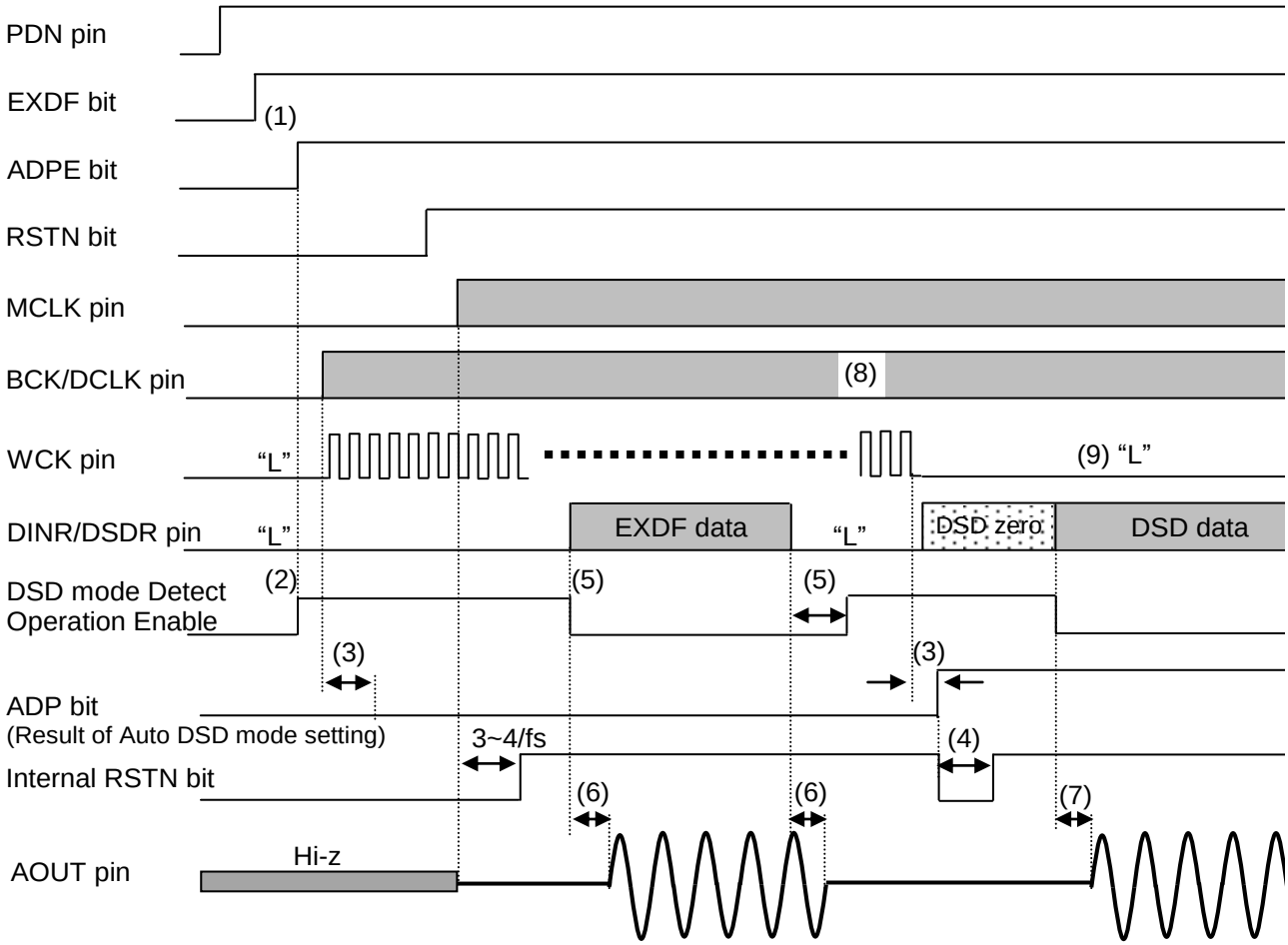
(1) Automatic mode switching between PCM/EXDF and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.
(2) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDR pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDR pin. Mode detection is executed even when there is no MCLK input.
(3) When DSD mode is changed, the AK4493S executes internal reset for 3~4/fs automatically.
(4) The AK4493S starts mode detection when input data of both channels are continuously zero for the period set by ADPT[1:0] bits, and it finishes mode detection when a data that is not zero is input.
(5) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT[1:0] bits setting.
(6) In PCM mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".
(7) If DCLK input is stopped in DSD mode, the AK4493S stays in DSD mode and continues operation.
(8) Upon power up the AK4493S, the AK4493S operates in PCM mode if DCLK is input and DSDR is not input.
(9) If DCLK or DSD data input is stopped in DSD mode, the AK4493S stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4493S. Excessive signal output can be avoided by setting DDM bit = "1" enabling automatic mute function works when detecting DSD full-scale input.

Figure 52. Changing to PCM Mode after Power-up In DSD Mode (EXDF bit = "0")



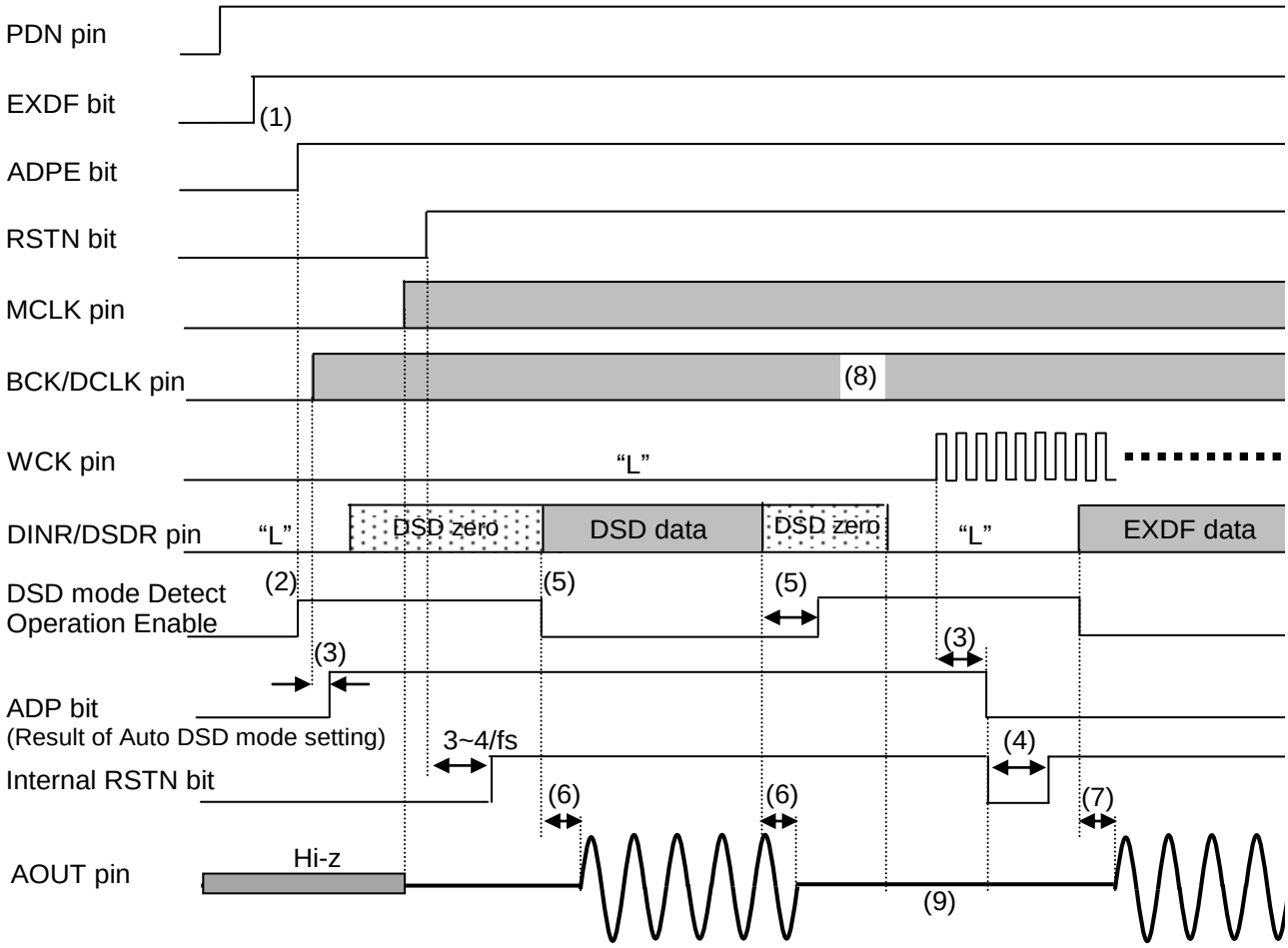
Note:
(1) The transition time to mute completely by setting SMUTE bit = "1" is set by ATS[1:0] bits.
(2) The AK4493S starts mode detection when input data of both channels are continuously zero for the period set by ADPT[1:0] bits, and it finishes mode detection when a data that is not zero is input.
(3) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDR pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDR pin. Mode detection is executed even when there is no MCLK input.
(4) When DSD mode is changed, the AK4493S executes internal reset for 3~4/fs automatically.
(5) In PCM mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".
(6) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT[1:0] bits setting.

Figure 53. Changing to DSD Mode after Power-up In PCM Mode (EXDF bit = "0")



Note:
(1) Automatic mode switching between PCM/EXDF and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". EXDF bit must be set before ADPE bit if setting EXDF bit = "1".
(2) If RSTN bit is in default value "0", mode detection will start by setting ADPE bit = "1".
(3) Mode detection is performed by monitoring input clock of the WCK and BCK/DCLK pins. It takes 256DCLK cycles for mode switching from EXDF to DSD mode, and takes 2WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.
(4) When DSD mode is changed, the AK4493S executes internal reset for 3~4/fs automatically.
(5) The AK4493S starts mode detection when input data of both channels are continuously zero for the period set by ADPT[1:0] bits, and it finishes mode detection when a data that is not zero is input.
(6) In EXDF mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".
(7) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT[1:0] bits setting.
(8) If BICK input is stopped in EXDF mode, the AK4493S stays in EXDF mode and continues operation.
(9) WCK input should be "L" when using DSD mode since DSD mode detection is performed by monitoring presence or absence of the WCK input clock.

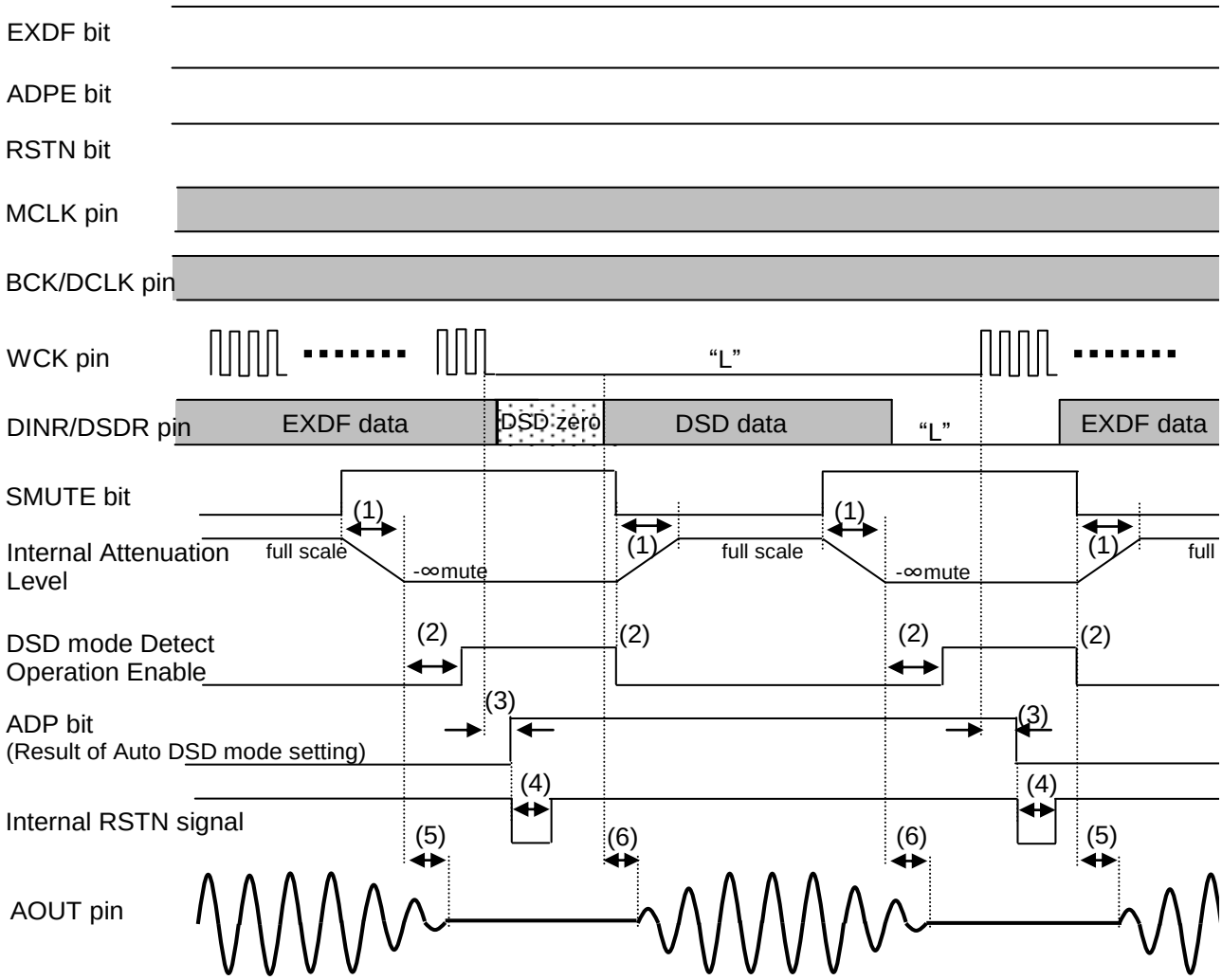
Figure 54. Changing to DSD Mode after Power-up In EXDF Mode (EXDF bit = "1")



Note :

(1) Automatic mode switching between PCM/EXDF and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". EXDF bit must be set before ADPE bit if setting EXDF bit = "1".
(2) If RSTN bit is in default value "0", mode detection will start by setting ADPE bit = "1".
(3) Mode detection is performed by monitoring input clock of the WCK and BCK/DCLK pins. It takes 256DCLK cycles for mode switching from EXDF to DSD mode, and takes 2WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.
(4) According to power-up sequence, reset is released when MCLK is input after setting RSTN bit="1".
(5) The AK4493S starts mode detection when input data of both channels are continuously zero for the period set by ADPT[1:0] bits, and it finishes mode detection when a data that is not zero is input.
(6) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT[1:0] bits setting.
(7) In EXDF mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".
(8) If DCLK input is stopped in DSD mode, the AK4493S stays in DSD mode and continues operation.
(9) If DSDR input is stopped in DSD mode, the AK4493S stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4493S. Excessive signal output can be avoided by setting DDM bit = "1" enabling automatic mute function works when detecting DSD full-scale input.

Figure 55. Changing to EXDF Mode after Power-up In DSD Mode (EXDF bit = "1")

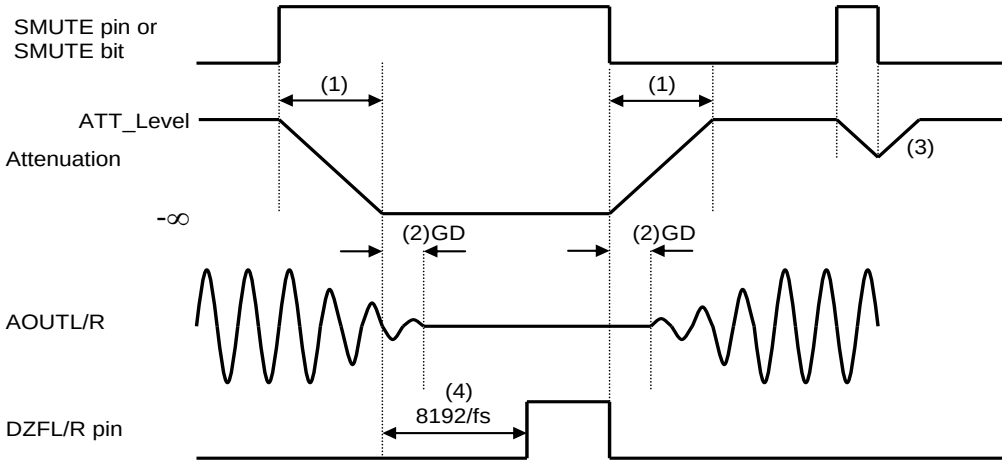


(1) The transition time to mute completely by setting SMUTE bit = "1" is set by ATS[1:0] bits.
(2) The AK4493S starts mode detection when input data of both channels are continuously zero for the period set by ADPT[1:0] bits, and it finishes mode detection when a data that is not zero is input.
(3) Mode detection is performed by monitoring input clock of the WCK and BCK/DCLK pins. It takes 256DCLK cycles for mode switching from EXDF to DSD mode, and takes 2WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.
(4) When DSD mode is changed, the AK4493S executes internal reset for 3~4/fs automatically.
(5) In EDF mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".
(6) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT[1:0] bits setting.

Figure 56. Changing to DSD Mode after Power-up In PCM Mode (EXDF bit = "0")

■ Soft Mute Operation (PCM, DSD, EXDF)

The soft mute operation is performed at digital domain. When setting the SMUTE pin to “H” or SMUTE bit to “1”, the output signal is attenuated by −∞ during ATT_DATA × ATT transition time from the current ATT level.
When setting back the SMUTE pin to “L” or SMUTE bit to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time (Refer to Table 30 for ATT). If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Note:

(1) ATT_DATA × ATT transition time. For example, this time is 4080LRCK cycles at ATT_DATA = 255 in PCM Normal Speed Mode.
(2) The analog output corresponding to the digital input has group delay (GD).
(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.
(4) When the input data for each channel is continuously zeros for 8192 LRCK cycles, the DZFL/R pin for each channel goes to “H”. The DZFL/R pin immediately returns to “L” if the input data is not zero.

Figure 57. Soft Mute Function

■ LDO

When TVDD = 3.0 ~ 3.6V, the power for digital core circuit (DVDD) is supplied by the internal LDO by setting the LDOE pin to “H”. Table 45 shows the DVDD pin statuses with the PDN and LDOE pins setting. The internal LDO is powered up by setting the PDN pin from “L” to “H” (power-down release) and it starts supplying 1.8V DVDD. Connect a 1uF (±50%) capacitor to the DVDD pin when using the LDO. It takes 0.1ms (max.) to power-up the internal LDO.

Table 45. LDO Select Mode (* = Do not care)

PDN	LDOE	TVDD	DVDD
*	L	1.7~3.6V	LDO OFF: Supply 1.7 ~ 1.98V to the DVDD pin externally
L	H	3.0~3.6V	500 ohm Pull-down
H	H	3.0~3.6V	LDO ON: LDO outputs 1.8V. (Do not connect DVDD with other device loads)

The AK4493S has error detect function, as shown in Table 46 for LDO operation (LDOE pin = “H”). The internal LDO will be powered down and stop supplying the power to the digital core when an error is detected. In this case, the analog signal output and the PDA pin becomes Hi-z state (In I^2C mode, ACK is not output). The AK4493S must be reset by setting the PDN pin = “L” → “H” to recover from the error detection status.

Table 46. Error Detection

No	Error Detection	Error Detection Conditions
1	LDO Overvoltage Detection	The AK4493S detects an error when the output voltage of the LDO pin exceeds overvoltage threshold. Threshold: 2.35V (typ)
2	LDO Overcurrent Detection	The AK4493S detects an error when the current flows PMOS from LDO output exceeds overcurrent threshold. Threshold: 58mA (typ)

■ Analog Output Overcurrent Protection

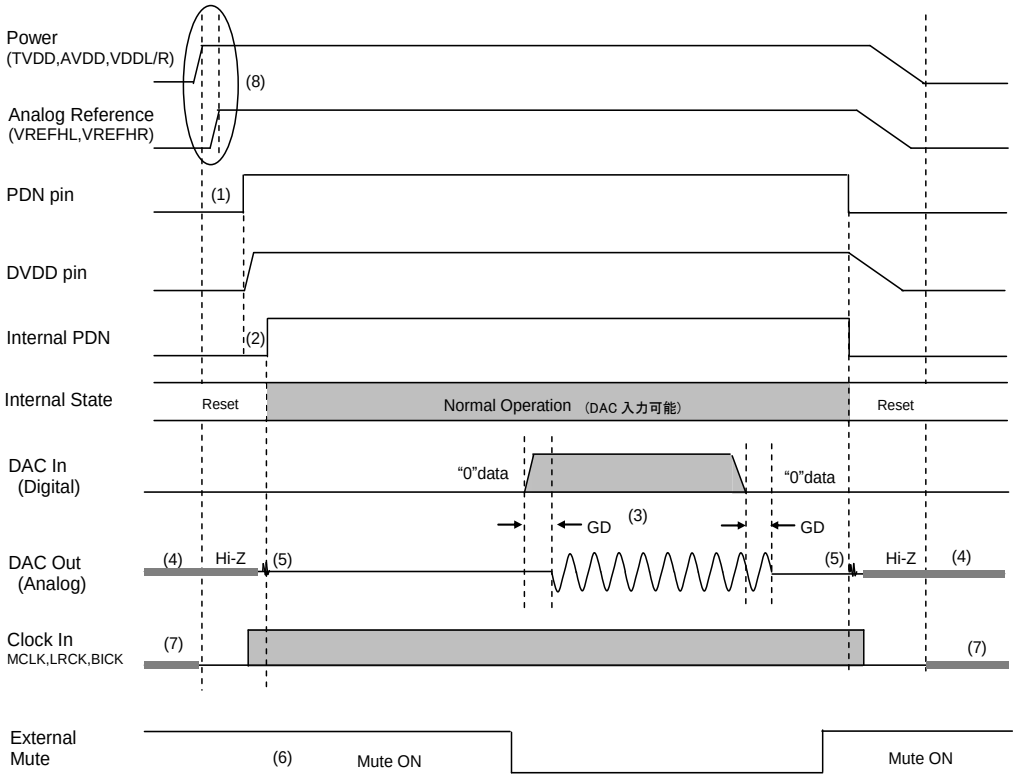
Analog output pins AOUTLP/LN and AOUTRP/RN have channel independent overcurrent protection. When a current that exceeds 85mA (typ.) is output from analog output pins, this function limits the output not to exceed 85mA. This overcurrent protection is invalid if the PDN pin = “L”, PW bit = “0” or MCLK is stopped.

■ Power Up/Down Function

The AK4493S is powered down when the PDN pin is “L”. In power-down state, all circuits stop operation and initialized, and the analog output becomes floating (Hi-z) state. The PDN pin must held “L” for more than 150ns for a certain reset after all power supplies are on. There is a possibility of malfunctions with the “L” pulse less than 150ns. Power-down is released by setting the PDN pin to “H” from “L”. The analog output becomes floating (Hi-z) state until all clocks are input.

[1] Pin Control Mode (PSN pin = “H”)

All circuits will be powered up by inputting MCLK, LRCK and BICK clocks after the PDN pin = “H”. Figure 58 shows system timing example of power down/up when using the internal LDO (LDOE pin “H”).

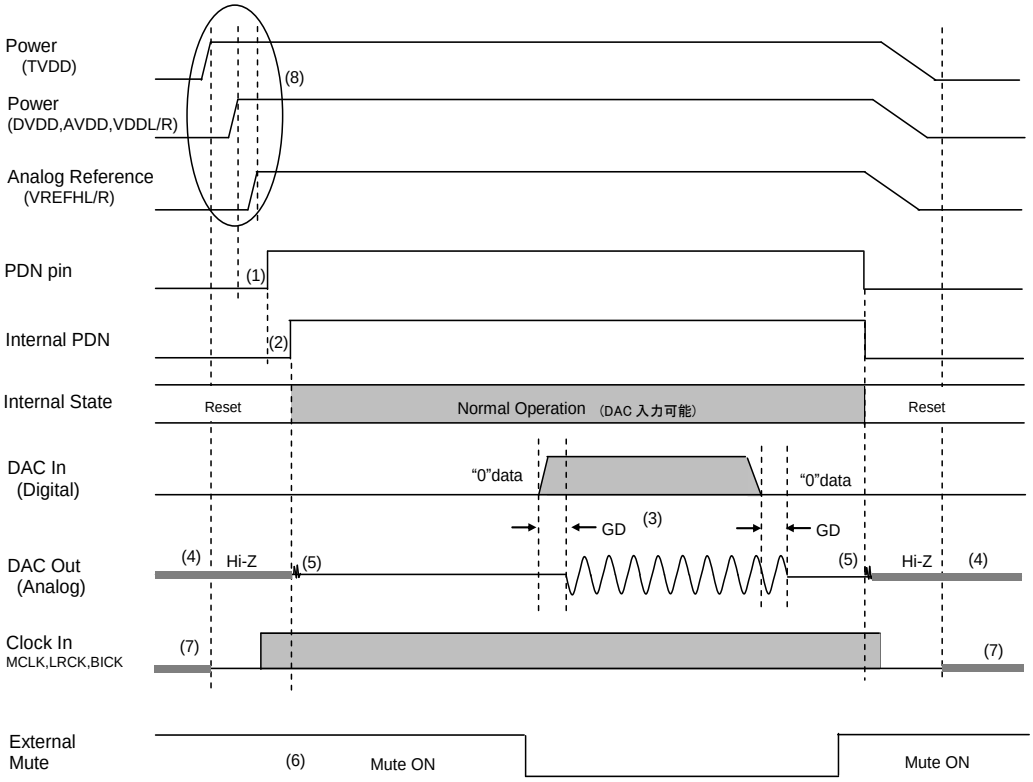


Notes:

(1) The PDN pin must be “L” when start supplying AVDD, TVDD and VDDL/R. It must be held “L” for more than 150ns after AVDD, TVDD and VDDL/R are powered up.
(2) Internal LDO is powered up after the PDN pin = “H” if the LDOE pin = “H”. The internal circuit will start operation after the shutdown switch is ON (max. 2ms) following the internal oscillator count up.
(3) The analog output corresponding to the digital input has group delay (GD).
(4) Analog outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(6) Mute the analog output externally if click noise (5) adversely affect system performance.
(7) Do not input clocks (MCLK, BICK and LRCK) until after the power supplies are turned on.
(8) VREFH/L must be powered up after or at the same time of VDDL/R.

Figure 58. Power-down/up Sequence Example (Pin Control Mode, LDOE pin = “H”)

The timing example when not using the internal LDO (LDOE pin = “L”) is shown in Figure 59.
When the LDOE pin = “L”, TVDD must be powered up before or at the same time of the DVDD.



Notes:

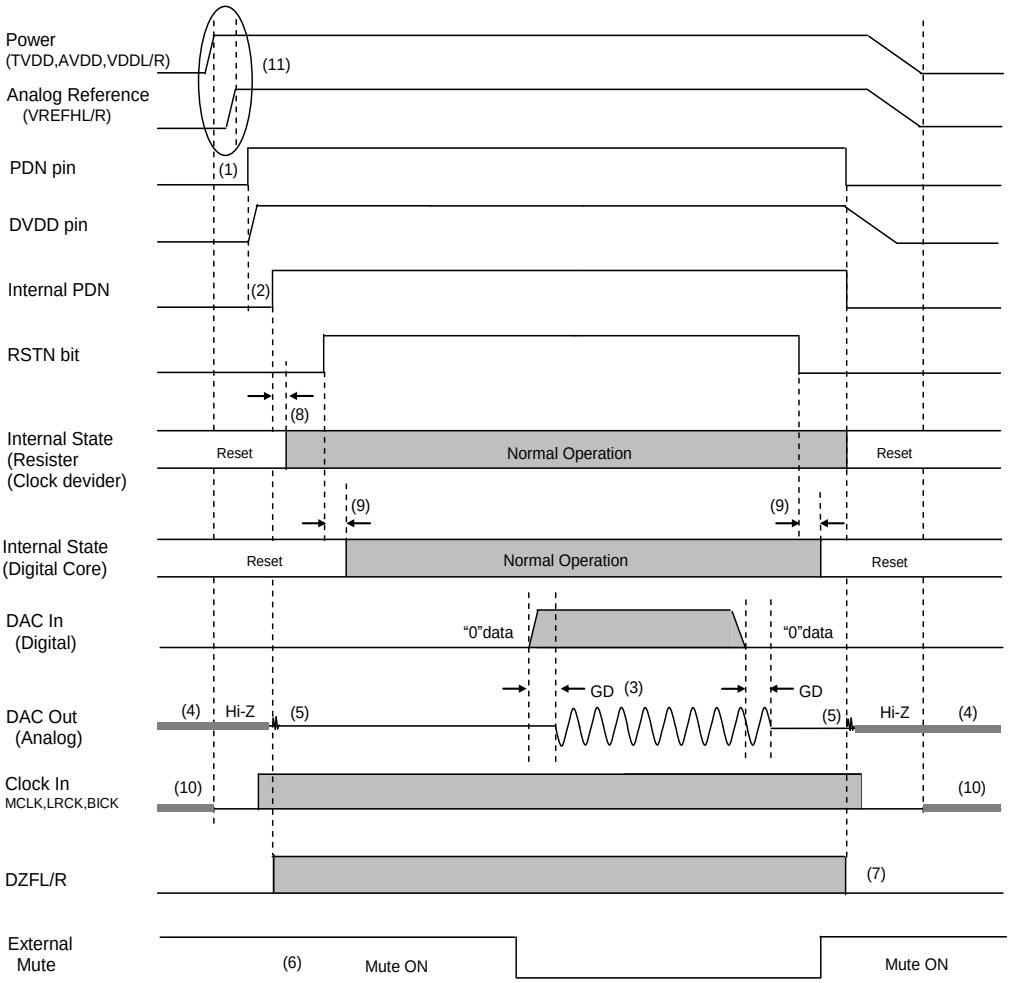
(1) The PDN pin must be “L” when start supplying AVDD, TVDD, DVDD and VDDL/R. It must be held “L” for more than 150ns after AVDD, TVDD, DVDD and VDDL/R are powered up.
(2) Internal shutdown switch is on after power-up if the LDOE pin = “L”. The internal circuit will start operation in 1us (max.) after the shutdown switch is ON.
(3) The analog output corresponding to the digital input has group delay (GD).
(4) Analog outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(6) Mute the analog output externally if click noise (5) adversely affect system performance.
(7) Do not input clocks (MCLK, BICK and LRCK) until after the power supplies are turned on.
(8) TVDD must be powered up before or at the same time of DVDD. VREFH/L must be powered up after or at the same time of VDDL/R.
(9) TVDD must be powered down after or at the same time of DVDD. Power-down sequences of other power supplies are not critical.

Figure 59. Power-down/up Sequence Example (Pin Control Mode, LDOE pin = “L”)

(b) Register Control Mode (PSN pin = “L”)

Figure 60 shows system timing example of power down/up when using the internal LDO (LDOE pin = “H”).

Register access becomes available and internal LDO is powered up after setting the PDN pin = “H”. The analog circuit starts operation by supplying necessary clocks (MCLK, LRCK and BICK for PCM mode, MCLK and DCLK for DSD mode, MCLK, BCK and WCK for EXDF mode) and the clock divider is powered up about after 4/fs. In this time, the analog output pins output analog common voltages (VCML, VCMR). Then the AK4493S transitions to normal operation by setting RSTN bit = “1”.



Notes:

(1) The PDN pin must be “L” when start supplying AVDD, TVDD and VDDL/R. It must be held “L” for more than 150ns after AVDD, TVDD and VDDL/R are powered up.

(2) Internal shutdown switch is on after power-up if the LDOE pin = “L”. The internal circuit will start operation in 1us (max.) after the shutdown switch is ON.

(3) The analog output corresponding to the digital input has group delay (GD).

(4) Analog outputs are floating (Hi-Z) in power down mode.

(5) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.

(6) Mute the analog output externally if click noise (5) adversely affect system performance.

(7) The DZFL/R pin is “L” in power-down mode (PDN pin = “L”).

(8) The clock divider is powered up in about 4/fs after the internal PDN is released.

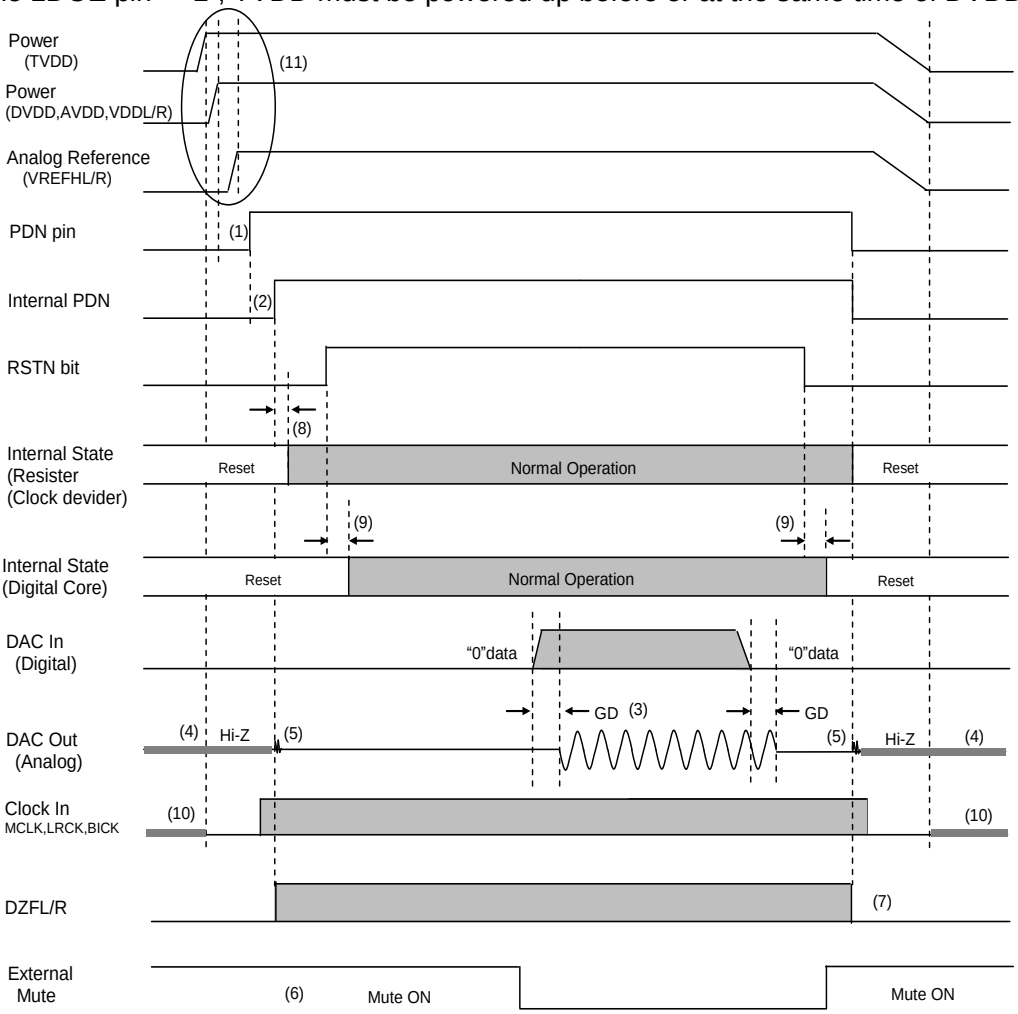
(9) It takes 3~4/fs until a reset instruction is valid when writing RSTN bit to “0” and it takes 2~3/fs when releasing the reset.

(10) Do not input clocks (MCLK, BICK and LRCK) during power down state.

(11) TVDD must be powered up before or at the same time of DVDD. VREFH/L must be powered up after or at the same time of VDDL/R.

Figure 60. Power-down/up Sequence Example (Register Control Mode, LDOE pin = “H”)

The system timing example of power up/down when not using LDO (LODE pin = “L”) is shown in Figure 61. When the LDOE pin = “L”, TVDD must be powered up before or at the same time of DVDD.



Notes:

(1) The PDN pin must be “L” when start supplying AVDD, TVDD, DVDD and VDDL/R. It must be held “L” for more than 150ns after AVDD, TVDD, DVDD and VDDL/R are powered up.
(2) Internal shutdown switch is turned on after power-up if the LDOE pin = “L”. The internal circuit will start operation in 1us (max.) after the shutdown switch is ON.
(3) The analog output corresponding to the digital input has group delay (GD).
(4) Analog outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(6) Mute the analog output externally if click noise (5) adversely affect system performance.
(7) The DZFL/R pin is “L” in power-down mode (PDN pin = “L”).
(8) The clock divider is powered up in about 4/fs after the internal PDN is released.
(9) It takes 3~4/fs until the internal RSTN is changed when changing RSTN bit to “0” and it takes 2~3/fs when changing RSTN bit to “1”.
(10) Do not input clocks (MCLK, BICK and LRCK) during power down state.
(11) TVDD must be powered up before or at the same time of DVDD. VREFH/L must be powered up after or at the same time of VDDL/R. Power up sequence of other power supplies are not critical.
(12) TVDD must be powered down after or at the same time of DVDD. Power-down sequences of other power supplies are not critical.

Figure 61. Power-down/up sequence example (Register Control Mode, LDOE pin = “L”)

■ Power-OFF/Reset Function

Power Down, Stand by and Reset function of the AK4493S are controlled by PW bit, RSTN bit and MCLK (Table 47).

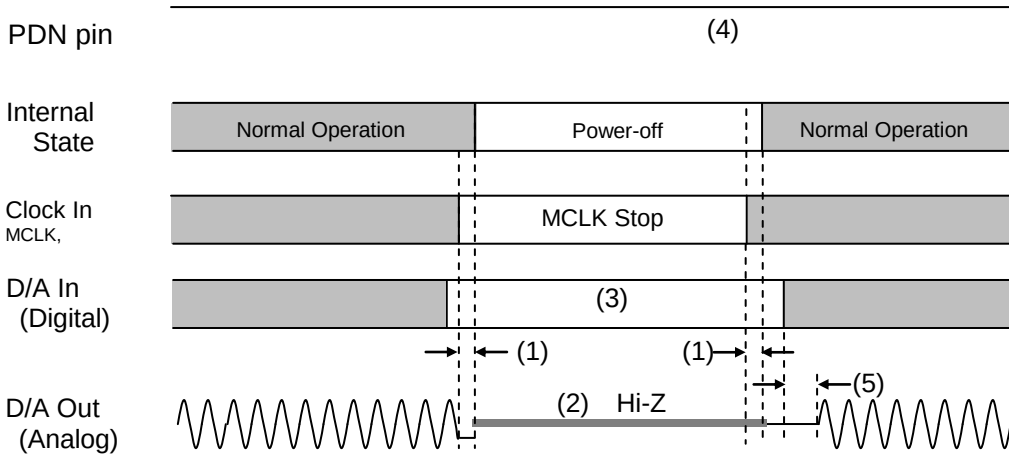
Table 47. Power Off, Reset Function

Mode	PDN Pin	MCLK Supply	PW bit	RSTN bit	DIGITAL Block	ANALOG Block	LDO Register	Analog Output
Power Down	L	–	–	–	OFF	OFF	OFF	Hi-Z
Standby (MCLK Stop) (Note 46)	H	No	–	–	OFF	OFF	ON	Hi-Z
Standby (PW bit = "0")	H	Yes	0	–	OFF	OFF	ON	Hi-Z
Reset	H	Yes	1	0	OFF	ON	ON	VCML/R
Normal Operation	H	Yes	1	1	ON	ON	ON	Signal output

Note 46. This standby mode is valid in case MSTBN bit = "0". This standby mode is set by the condition of PDN pin, PW bit and RSTN bit in case MSTBN bit = "1".

[1] Standby mode by MCLK Clock

The AK4493S detects a clock stop and all circuits except MCLK stop detection circuit, control register, bias generation circuit and LDO (only when the LDOE pin = "H") stop operation if MCLK is not input for 1us (min.) during operation (PDN pin = "H"). In this case, the analog output goes floating state (Hi-Z). The AK4493S returns to normal operation if PW bit and RSTN bit are "1" after starting to supply MCLK again. The zero detect function is disabled when MCLK is stopped.



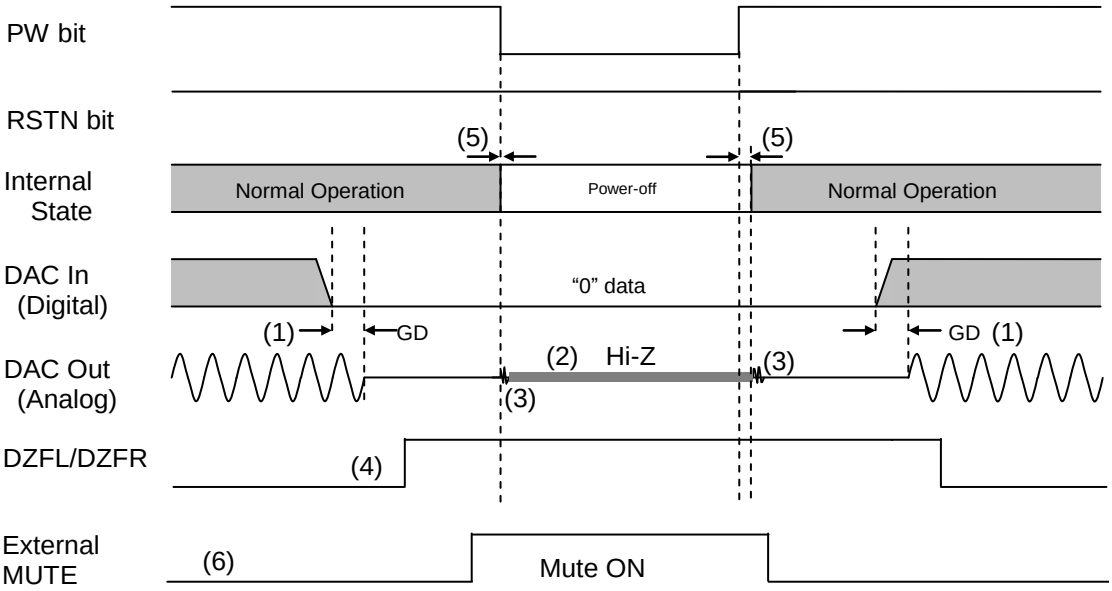
Notes:

(1) The AK4493S detects MCLK stop and becomes power off state when MCLK edge is not detected for 1us (min.) during operation.
(2) The analog output goes to floating state (Hi-Z).
(3) Click noise can be reduced by inputting "0" data when stopping and resuming MCLK supply.
(4) Resume MCLK input to release the power-off state by MCLK. In this case, power-up sequence by the PDN pin or PW bit is not necessary.
(5) The analog output corresponding to the digital input has group delay (GD).

Figure 62. Standby MCLK Clock

[2] Standby mode by PW bit

All circuits except control register, bias generation circuit and LDO (only when the LDOE pin = “H”) stop operation by setting PW bit to “0”. In this case, control register access is available. The analog output goes to floating state (Hi-Z). Figure 63 shows power ON/OFF sequence by PW bit.



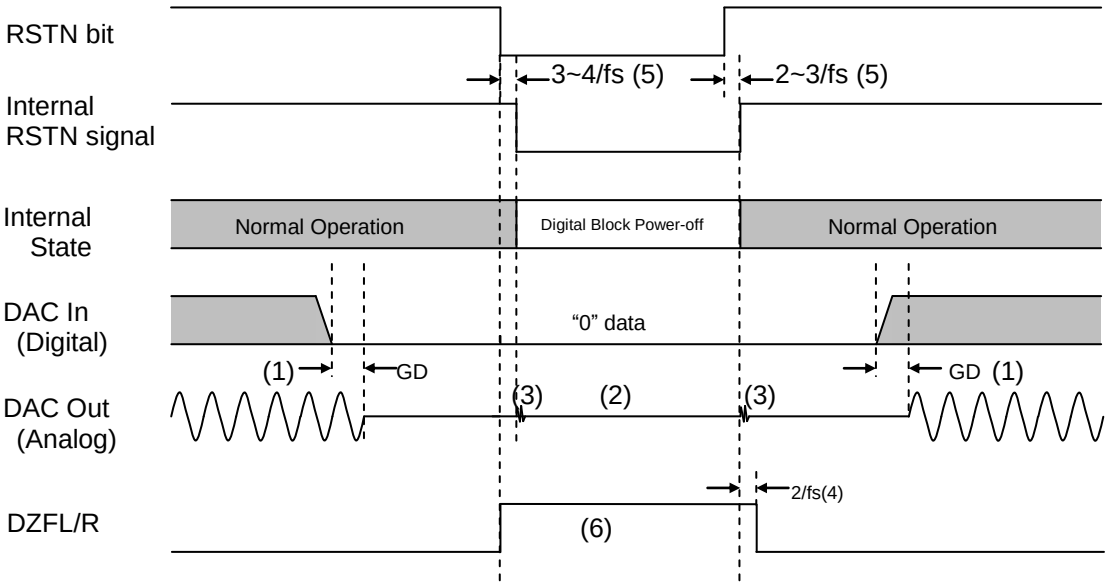
Note:

(1) The analog output corresponding to the digital input has group delay (GD).
(2) The analog output is floating (Hi-Z) state when PW bit = “0”.
(3) Click noise occurs on an edge of PW bit. This noise is output even if “0” data is input.
(4) The zero detect function is enable when the AK4493S is power off (PW bit = “0”). This figure shows the seuqnece when DZFE bit = “1”, DZFB bit = “0” and DZFM bit = “0”.
(5) It takes 4~5/fs until a power down instruction is valid when writing PW bit and it takes 1~2/fs when releasing the power down.
(6) Mute the analog output externally if click noise (3) or Hi-z output (2) adversely affect system performance.

Figure 63. Power ON/OFF Timing Example

[3] Reset mode by RSTN bit

Digital circuits except control registers and clock divider are reset by setting RSTN bit to “0”. In this case, control register settings are held, the analog output becomes VCML/R voltage and the DZFL/R pin outputs “H”. Figure 64 shows power ON/OFF sequence by RSTN bit.



Notes:

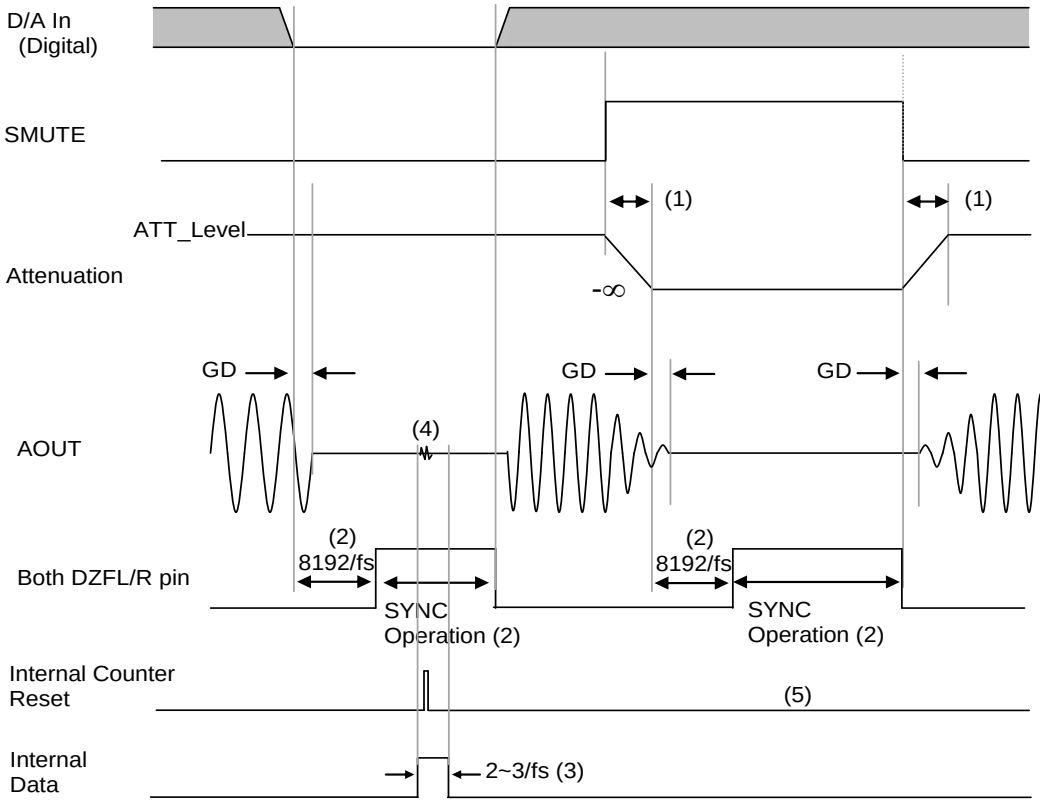
(1) The analog output corresponding to the digital input has group delay (GD).
(2) The analog output is VCML/R voltage when RSTN bit = “0”.
(3) Click noise occurs on an edge of internal RSTN signal. This noise is output even if “0” data is input.
(4) This figure shows the seuqnece when DZFE bit= “1”, DZFB bit = “0” and DZFM bit = “0”. The DZFL/R pin goes “H” on a falling edge of RSTN bit and goes “L” 2/fs after a rising edge of internal RSTN bit.
(5) It takes 3~4/fs until the internal RSTN is changed when changing RSTN bit to “0” and it takes 2~3/fs when changing RSTN bit to “1”.
(6) Mute the analog output externally if click noise (3) adversely affect system performance.

Figure 64. Reset Timing Example

■ Synchronize Function (PCM, EXDF)

The AK4493S has a function that resets the internal counter to keep the timing of falling edge of the internal clock CLK1 and the external clock edge in a certain range. With this synchronize function, group delays between each device can be kept within 4/256fs when using multiple AK4493S's.
Clock synchronize function becomes valid when input data of both L and R channels are "0" for 8192 times continuously in PCM mode or EXDF mode, when both L and R channels become "0" and kept for 8192 times continuously by attenuation or when RSTN bit = "0". In PCM mode, the internal counter is synchronized with a rising edged of LRCK (falling edge of LRCK in I_2S mode), and it is synchronized with a rising edge of WCK in EXDF mode. In this case, the analog output has the same voltage as VCML/R.

This function is disabled by setting SYNCE bit = "0" in register control mode. Figure 65 shows a synchronizing sequence when the input data is "0" for 8192 times continuously. Figure 66 shows a synchronizing sequence by RSTN bit.

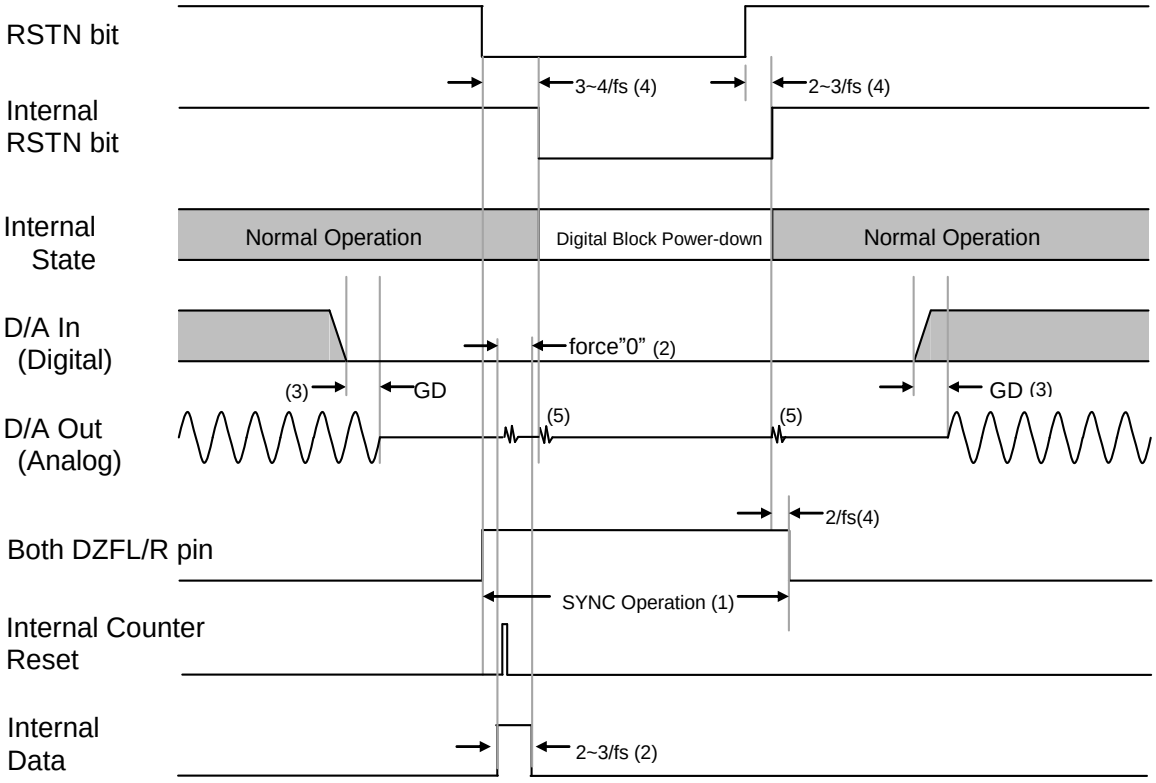


Note:

(1) Regarding ATT Transition time, refer to ■ Output ATT (PCM, DSD and EXDF Modes; Register Control Mode only).
(2) When both L and R channels data are "0" for 8192 times continuously, the DZFL and DZFR pins become "H" and the synchronize function is valid.
(3) Internal data is fixed to "0" forcibly for 2 to 3/fs when internal counter is reset.
(4) Click noise may occur when the internal counter is reset. This noise is output even if "0" data is input. Mute the analog output externally if this click noise affects the system performance.
(5) When the internal clock and external clock are in synchronization, the internal counter is not reset even if the synchronize function is valid.

Figure 65. Synchronizing Sequence by Continuous "0" Data Input for 8192 Times

If RSTN bit is set to “0”, the output signal of the DZFL/R pin becomes “H”. Then, the DAC is reset after 3~4/fs and the analog output becomes the same voltage as VCML/R. The synchronize function becomes valid when both of the DZFL and the DZFR pins output “H”.



Note:

(1) The DZFL and the DZFR pins become “H” by a falling edge of RSTN bit, and becomes “L” in 2/fs after a rising edge of internal signal of RSTN bit. The synchronize function is valid During the DZFL/R pin = “H”.

(2) Internal data is fixed to “0” forcibly for 2 to 3/fs when the internal counter is reset.

(3) Since the analog output corresponding to digital input has group delay (GD), it is recommended to have a no-input period longer than the group delay before writing “0” to RSTN bit.

(4) It takes 3~4/fs until the internal RSTN is changed when changing RSTN bit to “0” and it takes 2~3/fs when changing RSTN bit to “1”. The synchronization function becomes valid immediately when writing “0” to RSTN bit. Therefore, there is a case that the internal counter is reset before internal RSTN signal of the LSI is changed.

(5) Click noise occurs on rising and falling edges of the internal RSTN signal and when the internal counter is reset. This noise is output even if “0” data is input. Mute the analog output externally if this click noise affects the system performance.

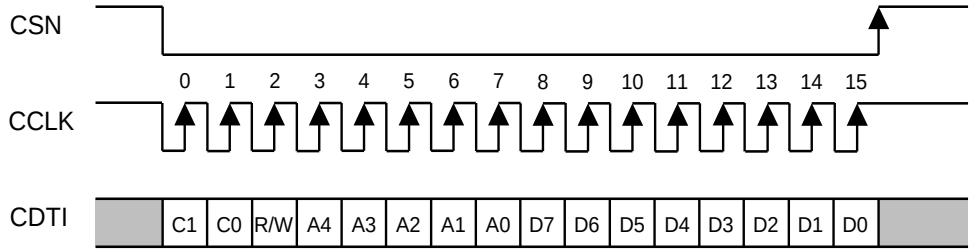
Figure 66. Synchronization Sequence by RSTN Bit

■ Register Control Interface

(1) 3-wire Serial Control Mode (I2C pin = “L”)

Pins (pin control mode) or registers (register control mode) can control the functions of the AK4493S. In pin control mode, the register setting is ignored, and in register control mode the pin settings are ignored. When the state of the PSN pin is changed, the AK4493S should be powered down by the PDN pin. Otherwise, malfunctions may occur since previous settings are not initialized. The register control interface is enabled by setting the PSN pin = “L”. Internal registers may be written to through 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2 bits, C1/0), Read/Write (1 bit; fixed to “1”, write only), Register address (MSB first, 5 bits) and Control data (MSB first, 8 bits). The data is output on a falling edge of CCLK and the data is received on a rising edge of CCLK. The writing of data is valid when CSN “↑”. The clock speed of CCLK is 5MHz (max).

Setting the PDN pin to “L” resets the registers to their default values. In register control mode, the digital block except control registers and clock divider is reset by setting RSTN bit to “0”. In this case, the register values are not initialized.



C1-C0: Chip Address (C1 bit =CAD1 pin, C0 bit =CAD0 pin)
R/W: READ/WRITE (Fixed to “1”, Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 67. Control I/F Timing

* The AK4493S does not support read commands in 3-wire serial control mode.
* When the AK4493S is in power down mode (PDN pin = “L”), writing into control registers is prohibited.
* The control data cannot be written when the CCLK rising edge is 15 times or less, or 17 times or more during CSN is “L”.

(2) I²C-bus Control Mode (I2C pin = “H”)

The AK4493S supports the fast-mode I²C-bus (max: 400kHz, Ver. 1.0).

(2)-1. WRITE Operation

Figure 68 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 74). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as “00100”. The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1 pin, CAD0 pin) sets these device address bits (Figure 69). If the slave address matches that of the AK4493S, the AK4493S generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 75). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4493S and the format is MSB first. The most significant three bits are fixed as “000” (Figure 70). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 71). The AK4493S generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 74).

The AK4493S can perform more than one byte write operation per sequence. After receipt of the third byte the AK4493S generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating a stop condition, the address counter will “roll over” to “00H” and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 76) except for the START and STOP conditions.

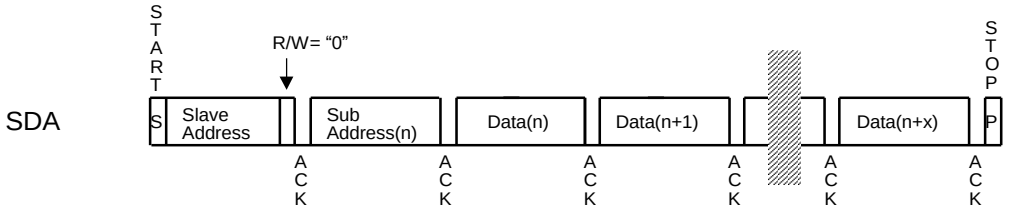


Figure 68. Data Transfer Sequence in I²C Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD0 is set by pin)

Figure 69. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 70. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 71. Byte Structure after The Second Byte

(2)-2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK4493S. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK4493S supports two basic read operations: Current Address Read and Random Address Read.

(2)-2-1. Current Address Read

The AK4493S has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4493S generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4493S ceases the transmission.

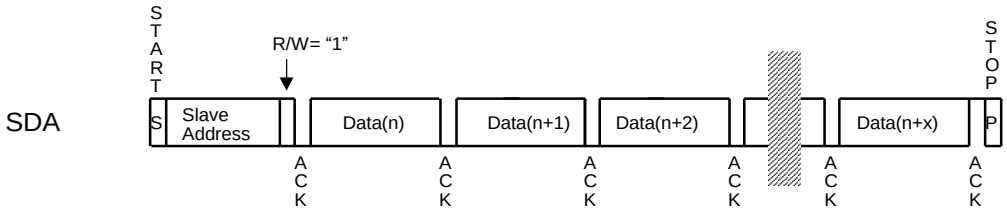


Figure 72. Current Address Read

(2)-2-2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4493S then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4493S ceases the transmission.

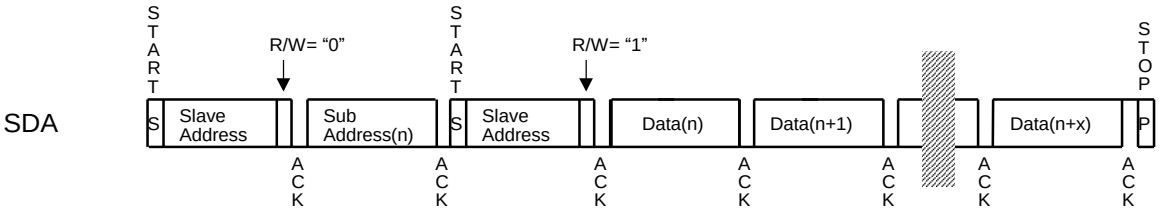


Figure 73. Random Address Read

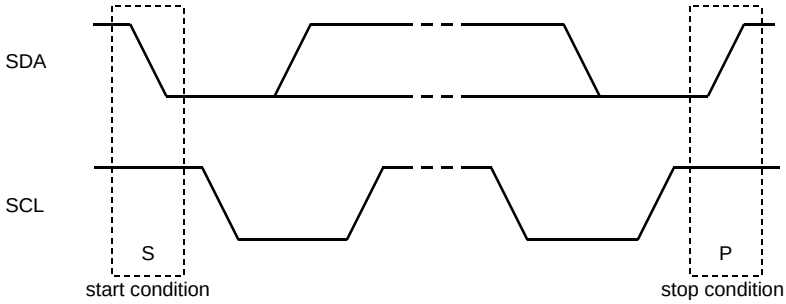


Figure 74. Start Condition and Stop Condition

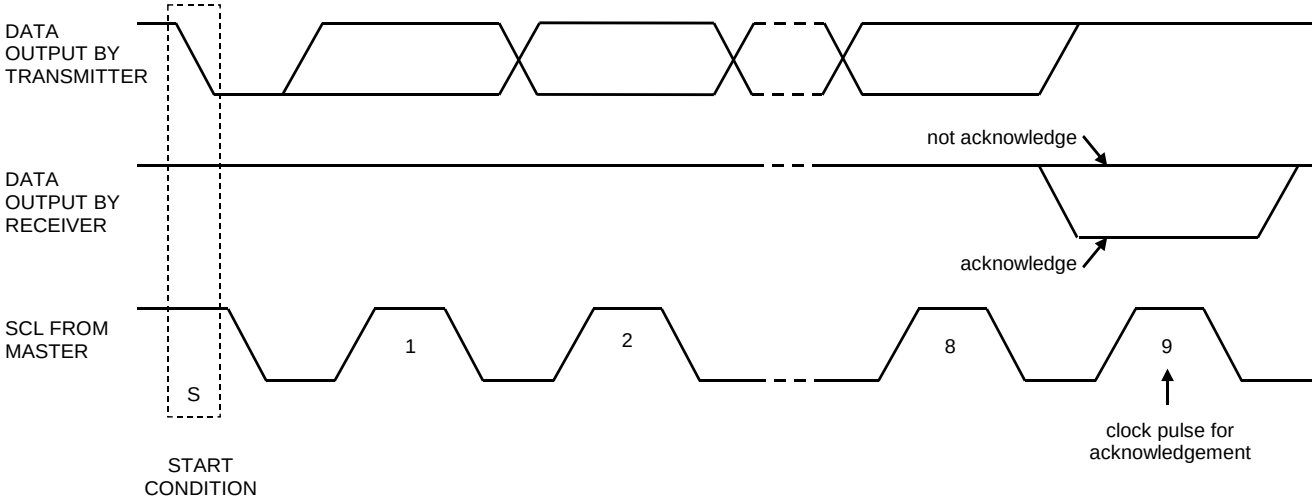


Figure 75. Acknowledge (I^2C Bus)

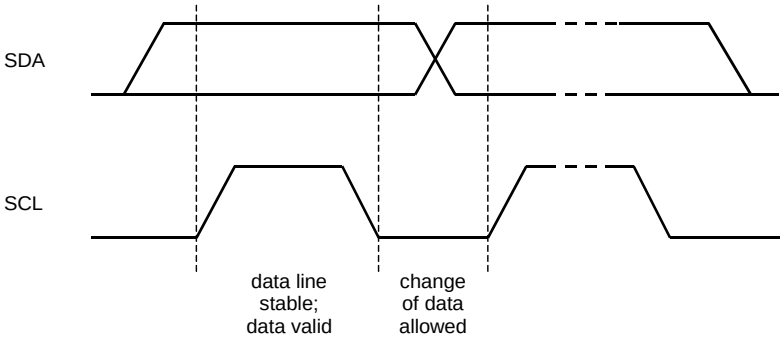


Figure 76. Bit Transfer (I^2C Bus)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
04H	Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
05H	Control 4	INVL	INVR	0	0	0	0	DFS2	SSLOW
06H	DSD1	DDM	DML	DMR	DDMOE	DDMT1	DDMT0	DSDD	DSDSEL0
07H	Control 5	MSTBN	0	0	0	GC2	GC1	GC0	SYNCE
08H	Sound Control	0	0	0	0	0	SC2	SC1	SC0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL1
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	0	PW	0	0
0BH	Control 7	ATS1	ATS0	0	SDS0	0	0	0	TEST
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	Reserved	0	0	0	0	0	0	0	0
0EH	Reserved	0	0	0	0	0	0	0	0
0FH	Reserved	0	0	0	0	0	0	0	0
10H	Reserved	0	0	0	0	0	0	0	0
11H	Reserved	0	0	0	0	0	0	0	0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
15H	Control 8	ADPE	ADPT1	ADPT0	0	0	0	0	0

Notes:

- In 3-wire serial control mode, the AK4493S does not support read commands.
- The AK4493S supports read command in I2C-bus control mode.
- If the address exceeds “15H”, the address counter will “roll over” to “00H” and the next write/read address will be “00H” by automatic increment function in I^2C-Bus mode.
- TEST bit on the address 0BH (D0) and bits indicated as 0 in each address must contain a “0” value except addresses from 0CH to 14H. Malfunctions may occur if writing “1” value to these bits.
- Writing after 16H is forbidden. Malfunctions may also occur by this action.
- When the PDN pin goes to “L”, the registers are initialized to their default values.
- When RSTN bit is set to “0”, the digital block except control registers and clock divider is reset, and the registers are not initialized to their default values.
- When the PSN pin status is changed, the AK4493S should be reset by the PDN pin.

(*) The AK4493S is a register compatible device with the AK4490, the AK4495S and the AK4497.

AK4493 Register Map (Reference)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
04H	Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
05H	Control 4	INVL	INVR	0	0	0	0	DFS2	SSLOW
06H	DSD1	DDM	DML	DMR	DDMOE	DDMT1	DDMT0	DSDD	DSDSEL0
07H	Control 5	0	0	0	0	GC2	GC1	GC0	SYNCE
08H	Sound Control	0	0	0	0	0	SC2	SC1	SC0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL1
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	0	PW	0	0
0BH	Control 7	ATS1	ATS0	0	SDS0	0	0	0	TEST
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	Reserved	0	0	0	0	0	0	0	0
0EH	Reserved	0	0	0	0	0	0	0	0
0FH	Reserved	0	0	0	0	0	0	0	0
10H	Reserved	0	0	0	0	0	0	0	0
11H	Reserved	0	0	0	0	0	0	0	0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
15H	Control 8	ADPE	ADPT1	ADPT0	0	0	0	0	0

AK4490 Register Map (Reference)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control4	INVL	INVR	0	0	0	0	DFS2	DFTHR
06H	DSD1	DDM	DML	DMR	DMC	DMRE	0	DSDD	DSDSEL0
07H	Control5	0	0	0	0	0	0	0	SYNCE
08H	Sound Control	0	0	0	0	0	0	SC1	SC0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL1

AK4495 Register Map (Reference)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control4	INVL	INVR	0	0	0	0	DFS2	DFTHR
06H	Control5	DDM	DML	DMR	DMC	DMRE	DSDD1	DSDD0	DSDSEL
07H	Control6	0	0	0	0	0	0	0	SYNCE
08H	Sound Control	0	0	0	0	0	SC2	SC1	SC0
09H	Reserved	0	0	0	0	0	0	0	0

AK4497 Register Map (Reference)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	AFSD	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control4	INVL	INVR	0	0	0	**0**	DFS2	SSLOW
06H	DSD1	DDM	DML	DMR	DMC	DMRE	0	DSDD	DSDSEL0
07H	Control5	0	0	0	0	GC2	GC1	GC0	SYNCE
08H	Sound Control	0	0	0	0	HLOAD	SC2	SC1	SC0
09H	DSD2	0	0	0	0	0	DSDPATH	DSDF	DSDSEL1
0AH	Control 7	TDM1	TDM0	SDS1	SDS2	0	PW	0	0
0BH	Control 8	ATS1	ATS0	0	SDS0	0	0	DCHAIN	TEST
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	Reserved	0	0	0	0	0	0	0	0
0EH	Reserved	0	0	0	0	0	0	0	0
0FH	Reserved	0	0	0	0	0	0	0	0
10H	Reserved	0	0	0	0	0	0	0	0
11H	Reserved	0	0	0	0	0	0	0	0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
15H	DFS read	0	0	0	0	0	ADFS2	ADFS1	ADFS0

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

RSTN: Internal Timing Reset
0: Reset. All registers are not initialized. (default)
1: Normal Operation

DIF[2:0]: Audio Data Interface Modes (Table 22)
Initial value is “110” (Mode6: 32bit MSB justified).

ECS: EXDF mode clock setting (Table 21)
0: WCK = 768kHz mode(default)
1: WCK = 384kHz mode

EXDF: External Digital Filter I/F Mode (Register Control Mode only)
0: Disable: Internal Digital Filter mode (default)
1: Enable: External Digital Filter mode

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM & EXDF mode only). (Table 14, Table 5)
0: Disable: Manual Setting Mode (default)
1: Enable: Auto Setting Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM[1:0]: De-emphasis Filter Control (Table 28)
Initial value is “01” (OFF).

DFS[1:0]: Sampling Speed Control. (Table 7, Table 11)
Initial value is “000” (Normal Speed). Click noise occurs when DFS[2:0] bits are changed.

SD: Short Delay Filter Enable. (Table 25)
0: Traditional filter (SSLOW = 0)
Super Slow Roll-off (SSLOW = 1, SD = 0)
1: Short delay filter (default, SSLOW = 0)
Low Dispersion Filter (SSLOW = 1, SD = 1)

DZFM: Data Zero Detect Mode
0: Channel Separated Mode (default)
1: Channel ANDed Mode
If the DZFM bit is set to “1”, the DZF pins of both L and R channels go to “H” only when the input data at both channels are continuously zeros for 8192 LRCK cycles.

DZFE: Data Zero Detect Enable
0: Disable (default)
1: Enable
Zero detect function can be disabled by DZFE bit “0”. In this case, the DZF pins of both channels are always “L”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable. (Table 25)
0: Slow Roll-off filter disable (default)
1: Slow Roll-off filter

SELLR: The data selection of L channel and R channel to analog outputs, when MONO mode
0: All channel output L channel data, when MONO mode. (default)
L channel output L channel data, R channel data output R channel data (default)
1: All channel output R channel data, when MONO mode.
L channel output R channel data, R channel data output L channel data

DZFB: Inverting Enable of DZF. (Table 32)
0: DZF pin goes “H” at Zero Detection (default)
1: DZF pin goes “L” at Zero Detection

MONO: MONO mode Stereo mode select
0: Stereo mode (default)
1: MONO mode

DCKB: Polarity of DCLK (DSD Only)
0: DSD data is output from DCLK falling edge. (default)
1: DSD data is output from DCLK rising edge.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0: 512fs (default)
1: 768fs

ADP: Read Back register for internal operation mode. This bit is valid when ADRE bit = “1”.
It is invalid when ADPE bit = “0” and readouts “0” when read.
0: PCM Mode/EXDF Mode
1: DSD Mode

DP: DSD/PCM Mode Select
0: PCM Mode (default)
1: DSD Mode
When DP bit is changed, the AK4493S should be reset by RSTN bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
04H	Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL[7:0]: Attenuation Level
ATTR[7:0]: Attenuation Level

255 levels 0.5dB step + mute

Data	Attenuation
FFH	0dB (default)
FEH	-0.5dB
FDH	-1.0dB
:	:
:	:
02H	-126.5dB
01H	-127.0dB
00H	MUTE (-∞)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL	INVR	0	0	0	0	DFS2	SSLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SSLOW: Super Slow Roll Off (Digital Filter bypass mode) or Low Dispersion Filter Enable. (Table 25)
0: Disable (default)
1: Enable (see also SD)

DFS2: Sampling Speed Control. (Table 11)

INVR: AOUTR Output Phase Inverting
0: Disable (default)
1: Enable

INVL: AOUTL Output Phase Inverting
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DSD1	DDM	DML	DMR	DDMODE	DDMT1	DDMT0	DSDD	DSDSEL0
R/W		R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL [1:0]: DSD Sampling Speed Control
00: DSD64
01: DSD128
10: DSD256
11: DSD512

DSDD: DSD Playback Path Control
0: Normal Path (default)
1: Volume Bypass

DDMT[1:0]: DSD Signal Full-scale Detection Time Setting (Table 38)

DDMOE: Output Setting of the DMR/L Pins for DSD Full-scale Detection (Table 33)

DMR/DML: This register outputs detection flag when a full-scale signal is detected at DSDR/L channel.

DDM: DSD Data Mute
The AK4493S has an internal mute function that mutes the output when DSD input data becomes all “1” or all “0” for 2048 samples (1/fs) continuously. DDM bit controls this function.
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 5	MSTBN	0	0	0	GC2	GC1	GC0	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

SYNCE: SYNC Mode Enable
0: SYNC Mode Disable
1: SYNC Mode Enable (default)

GC[2:0]: PCM, DSD mode Gain Control (Table 31)

MSTBN: Automatic Stand-by mode enable when MCLK is stopped.
0: Enable (default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Sound Control	0	0	0	0	0	SC2	SC1	SC0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SC [2:0]: Sound Control. (Table 36,

SC1	SC0	Sound	
0	×	Analog internal current, maximum (Setting1)	(default)
1	×	Analog internal current, medium (Setting2)	

Table 37)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL1: DSD Sampling Speed Control.

DSDF: Cut-off Frequency of DSD Filter Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	0	PW	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

PW: Power ON/OFF Control
0: Power off
1: Power on (default)

SDS [2:0]: Output Data Slot Selection of Each Channel
0: Normal Operation
1: Output Data of Other Slot (Table 23)
The default value is “000”.

TDM [1:0]: TDM Mode Select
00: Normal (default)
01: TDM128
10: TDM256

11: TDM512

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Control 7	ATS1	ATS0	0	SDS0	0	0	0	TEST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

TEST: “0” value must be written to this bit. Otherwise malfunctions may occur.

SDS[2:0]: Output Data Slot Selection for Each Channel
0: Normal
1: Output Data of Other Slot (Table 23)

ATS[1:0]: Transition Time between Set Values of ATTL/R[7:0] bits (Table 30)
The default value is “00”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	Reserved	0	0	0	0	0	0	0	0
0EH	Reserved	0	0	0	0	0	0	0	0
0FH	Reserved	0	0	0	0	0	0	0	0
10H	Reserved	0	0	0	0	0	0	0	0
11H	Reserved	0	0	0	0	0	0	0	0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

0CH: Reserved

0DH: Reserved

0EH: Reserved

0FH: Reserved

10H: Reserved

11H: Reserved

12H: Reserved

13H: Reserved

14H: Reserved

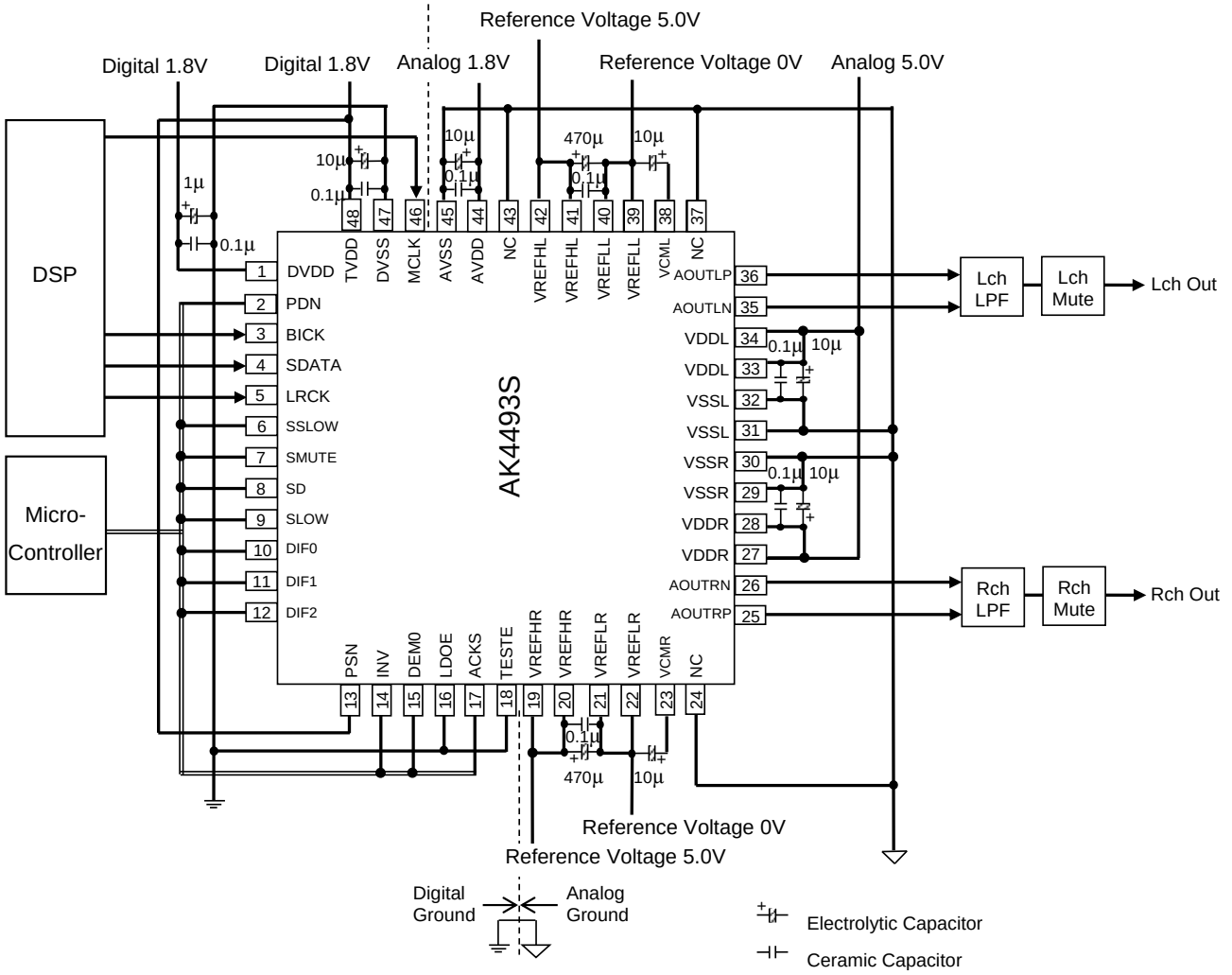
Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	Control 8	ADPE	ADPT1	ADPT0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ADPT[1:0]: Time until PCM/DSD mode detection when input data becomes zero (PCM/EXDF⇔DSD modes)
(Table 40).

ADPE: Automatic Mode Switching Function Enable Bit for PCM/EXDF and DSD Modes
0: Disable (default)
1: Enable

10. Recommended External Circuits

10.1 pin control mode, LDO disable.

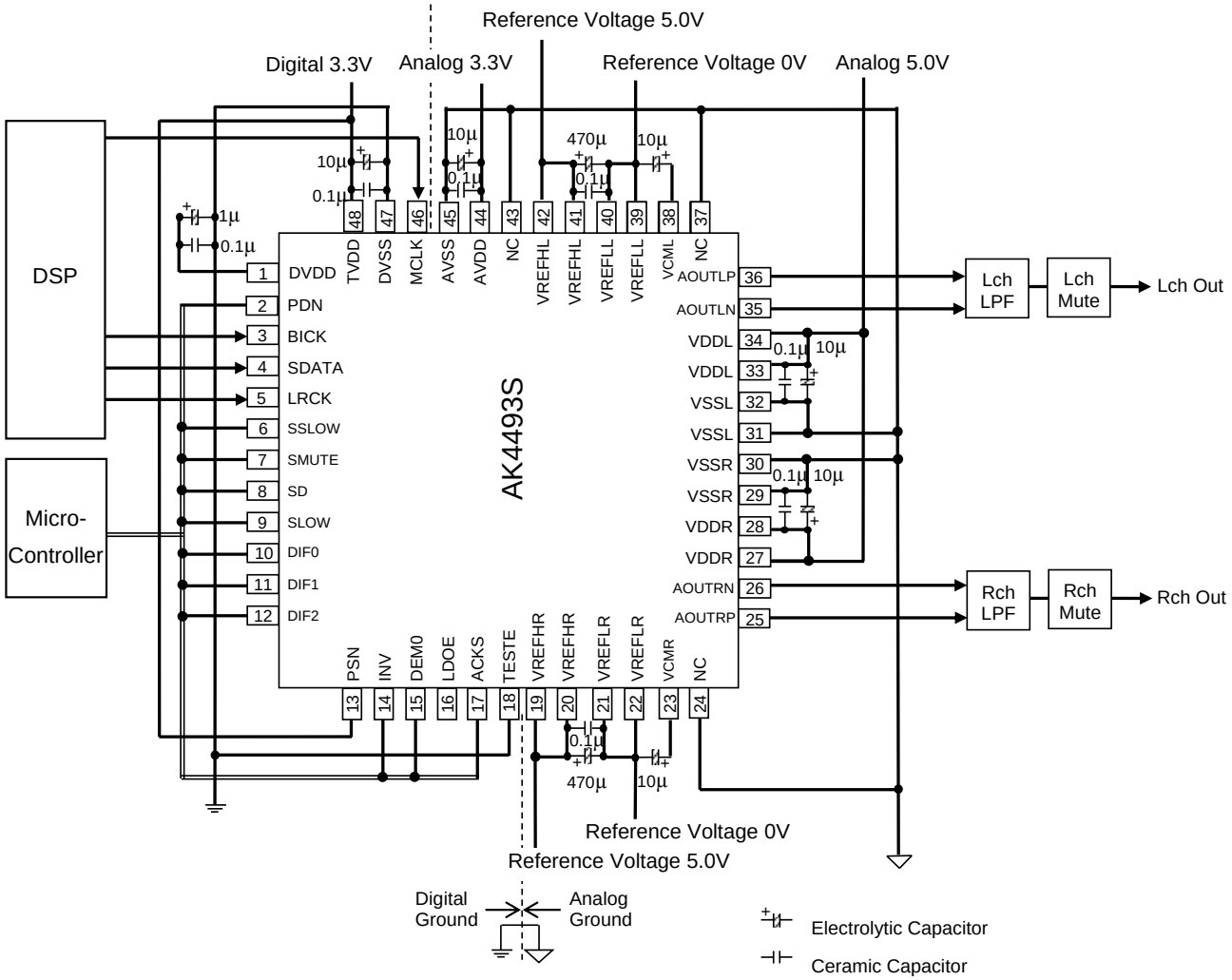


Note:

- BICK = 64fs, LRCK = fs
- Power lines of AVDD, TVDD, VDDL and VDDR should be distributed separately with low impedance of regulators, etc. maintained.
- AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane. (Analog ground should have low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)
- It is recommended to input MCLK via a damping resistor. Without the resistor, there is a possibility that THD+N characteristic degrades because of high-frequency noise of MCLK.
- All input pins except pull-down/pull-up pins should not be allowed to float.

Figure 77. Typical Connection Diagram
(AVDD = TVDD = 3.3V, VDDL/R = VREFHL/R = 5.0V, DVDD = 1.8V, LDOE pin = “L”, Pin Control Mode)

10.2 pin control mode, LDO enable.



Note:

- BICK = 64fs, LRCK = fs
- Power lines of AVDD, TVDD, VDDL and VDDR should be distributed separately with low impedance of regulators, etc. maintained.
- AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane. (Analog ground should have low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)
- It is recommended to input MCLK via a damping resistor. Without the resistor, there is a possibility that THD+N characteristic degrades because of high-frequency noise of MCLK.
- All input pins except pull-down/pull-up pins should not be allowed to float.
- For DVDD pin, 1µF capacitor(±50%, including temperature characteristics) should be connected.

Figure 78. Typical Connection Diagram
(AVDD = TVDD = 3.3V, VDDL/R = VREFHL/R = 5.0V, LDOE pin = “H”, Pin Control Mode)

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, TVDD, DVDD, VDDL and VDDR. AVDD and VDDL/R are supplied from analog supply in system, and TVDD and DVDD are supplied from digital supply in system. Power lines of VDDL/R should be distributed separately, from the point with low impedance of regulators or other parts.

AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane. Decoupling capacitors for high frequency should be placed as near as possible to the AK4493S.

2. Reference Voltage

The differential voltage between VREFHL and VREFLL, and VREFHR and VREFLR set the full-scale of the analog output range. The VREFHL/R pin is normally connected to 5.0V reference voltage, and the VREFLL/R pin is normally connected to the 0V reference voltage. Connect a 0.1µF ceramic capacitor and 470µF (min. value depends upon power supply quality) electrolytic capacitor between VREFHL and VREFLL, and VREFHR and VREFLR. Especially the ceramic capacitors should be connected as near as possible to the pin.
The VREFHL, VREFHR, VREFLL and VREFLR pins should avoid noises from other power supplies. Connect the VREFHL/R pin to the analog 5.0V via a 10Ω resistor, and the VREFLL/R pin to the analog ground via a 10Ω resistor when it is difficult to obtain expected analog characteristics because of noises from other power supplies (A low pass filter of fc=17Hz will be composed with the 470µF capacitor and the 10Ω resistor. It removes signal frequency noise from other power supply lines). No load current may be drawn from the VCML/R pin since VCML/R is a common voltage of analog signals. All digital signals, especially clocks, should be kept away from the VREFHL/R and VREFLL/R pins in order to avoid unwanted coupling into the AK4493S.

3. Analog Output

The analog outputs are full differential outputs. The differential outputs are summed externally, V_{AOUT} = (AOUT+) – (AOUT–) between AOUTL/R+ and AOUTL/R–. When the summing gain is 1 and VREFHL/R – VREFLL/R = 5V, the output range is 2.8Vpp (typ.) centered around VCML and VCMR voltages if GC2 bit = “0”. In this case, the output range after summing will be 5.6V (typ.). The output range is 3.75Vpp (typ.) centered around VCML and VCMR if GC2 bit = “1”, and the output range after summing will be 7.5Vpp (typ.). The bias voltage of the external summing circuit is supplied externally.

The input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full-scale for 7FFFFFFFH (@32bit) and a negative full-scale for 80000000H (@32bit). The ideal V_{AOUT} is 0V for 00000000H (@32bit). The internal switched capacitor filters attenuate the noise generated by the delta sigma modulator beyond the audio passband.

Figure 79 and Figure 80 shows examples of external LPF circuit summing the differential outputs by a single op-amp. Figure 81 shows an example of external LPF with two op-amps and differential output circuits. Figure 82 shows an example of external LPF with two op-amps and the circuit when setting MONO bit = “1”. A resistor that has 1% or less absolute error must be used for external LPFs.

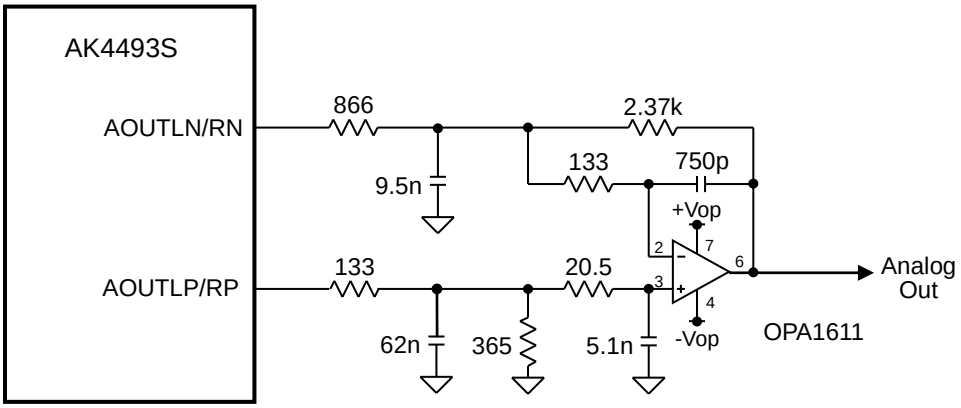


Figure 79. External LPF Circuit Example 1 (fc = 104kHz(typ), Q=0.690(typ))

Table 48. Frequency Response of External LPF Circuit Example 1

Gain (1kHz, Typ)		+8.75 dB
Frequency Response (ref:1kHz, Typ)	20kHz	-0.02 dB
	40kHz	-0.13 dB
	80kHz	-1.34 dB

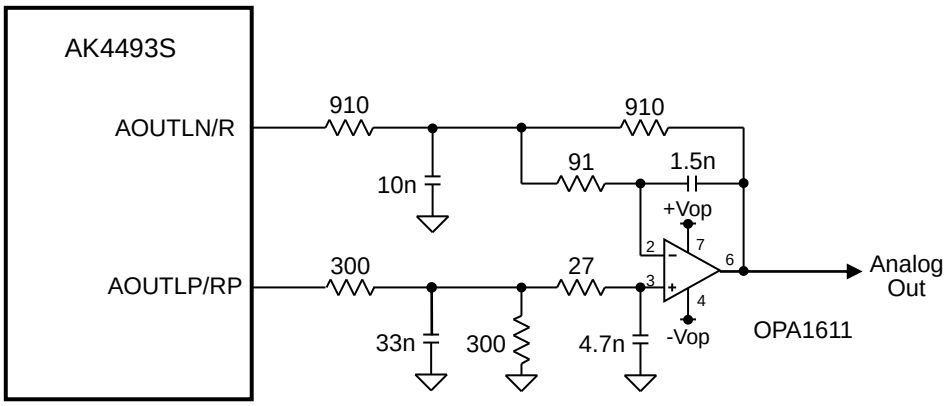


Figure 80. External LPF Circuit Example 2 (fc = 133kHz(typ), Q=0.677(typ))

Table 49. Frequency Response of External LPF Circuit Example 2

Gain (1kHz, Typ)		+0.00 dB
Frequency Response (ref:1kHz, Typ)	20kHz	-0.12 dB
	40kHz	-0.22 dB
	80kHz	-0.75 dB

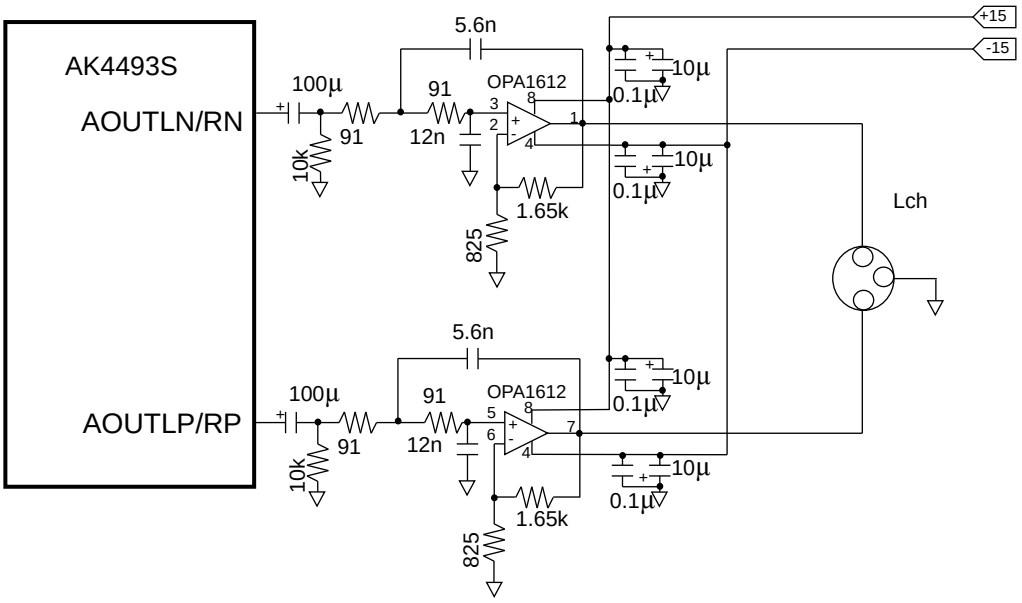


Figure 81. External LPF Circuit Example 3 (fc = 178kHz(typ), Q=0.67(typ))

Table 50. Frequency Response of External LPF Circuit Example 3

Gain (1kHz, Typ)		+9.54 dB
Frequency Response (ref:1kHz, Typ)	20kHz	-0.01 dB
	40kHz	-0.07 dB
	80kHz	-0.34 dB

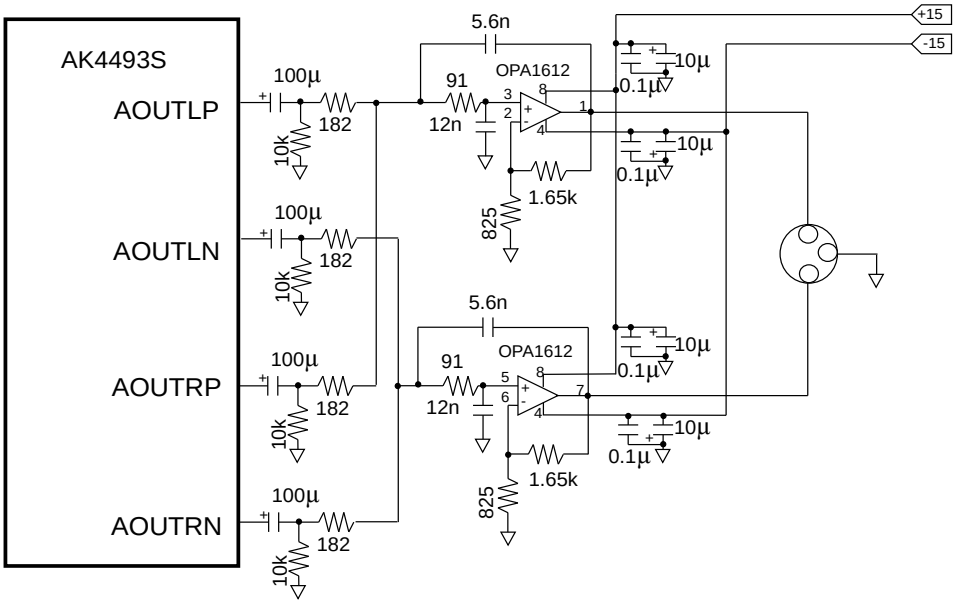
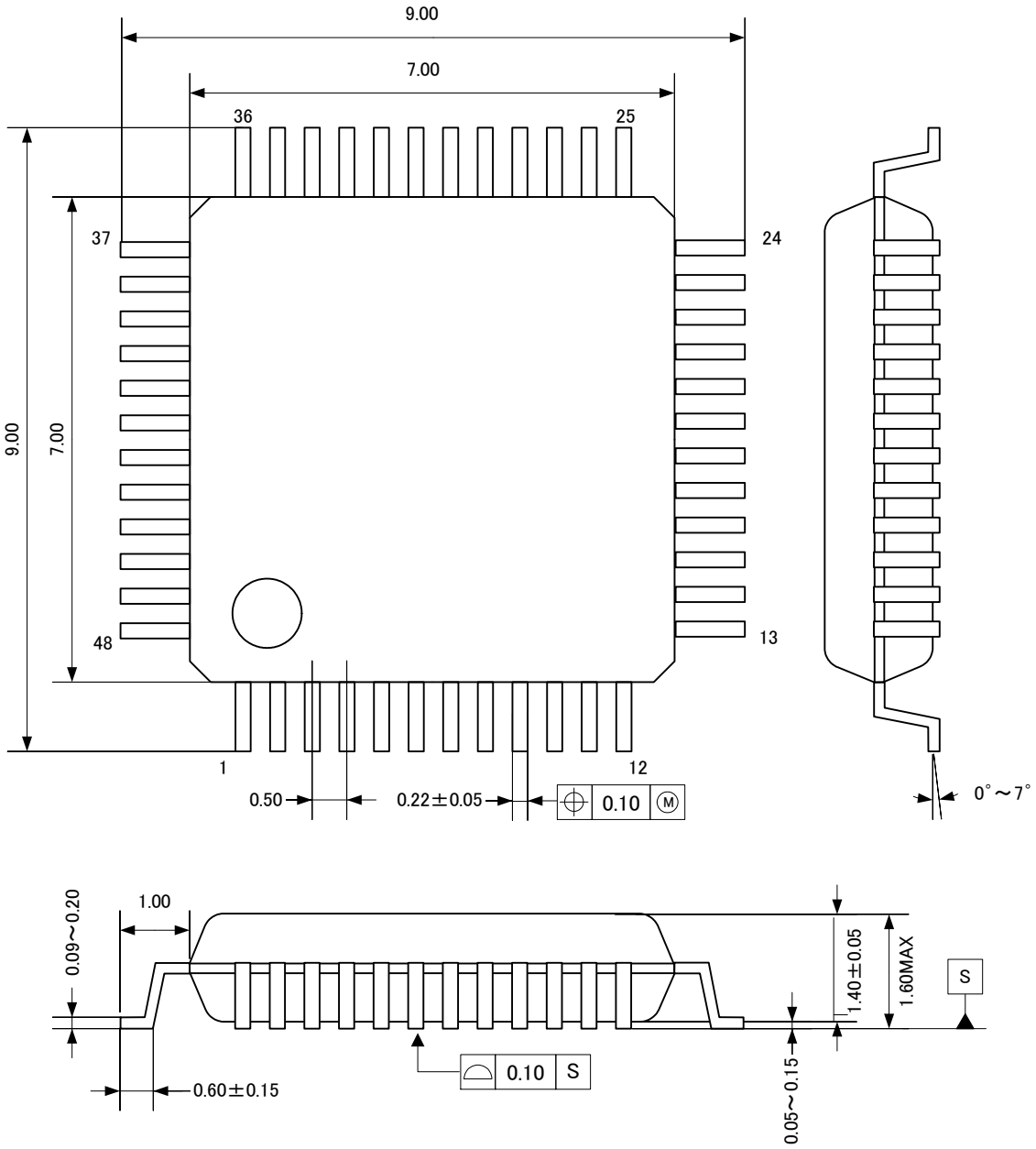


Figure 82. External LPF Circuit Example for mono mode (fc = 178kHz(typ), Q=0.67(typ))

11. Package

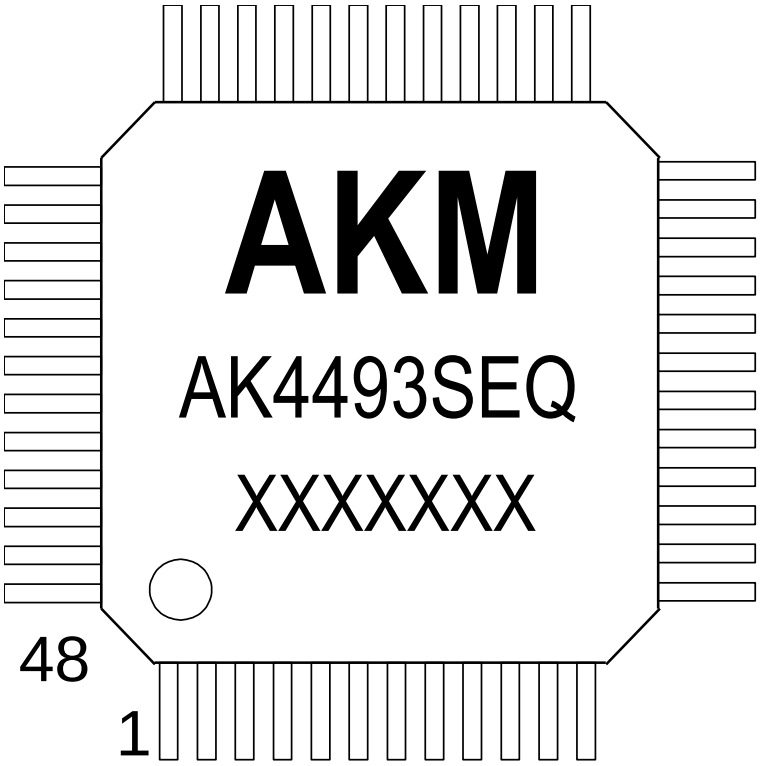
■ Outline Dimensions (48-pin LQFP)



■ Material & Terminal Finish

Package Molding Compound:	Epoxy, Halogen (Br and Cl) free
Lead Frame Material:	EFTEC-64T
Terminal Surface Treatment:	Solder (Pb free) plate

■ **Marking**



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4493SEQ
4) AKM Logo

12. Ordering Guide

■ Ordering Guide

AK4493SEQ	–40 ~ +85°C	48-pin LQFP (0.5mm pitch)
AKD4493S	Evaluation Board for AK4493S	

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