HUSB238A

Register Information

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REVISION HISTORY

Version	Date	Descriptions
Rev. 0.1	05/2023	Initial version

REGISTERS

USER CONFIGURATION REGISTERS

Table 1. CONTROL (Address: 0x01)

Bit	Field	Type	Description	Default
[7:1]	Reserved	R/W		0b
[0]	INT_MASK	R/W	This bit is the global interruption mask for all of interruptions. 1b: Mask all of interruptions 0b: Mask is controlled by MASK and MASK1 registers	1b

Table 2. CONTROL1 (Address: 0x02)

Bit	Field	Type	Description	Default
[7]	Reserved	R/W		0b
[5]	EN_DPM_HIZ	R/W	This bit controls whether the D+ and D- removed away if the DCP is not detected. 0b: Keep D+ and D- connected to internal circuitry 1b: Disconnect D+ and D- away from internal circuitry	0b
[4]	VDM_RESPOND	R/W	This bit controls the response for the received VDM SOP messages. 0b: NAK for all of received valid VDM SOP messages (not include Attention) 1b: ACK for all of received valid VDM SOP messages (not include Attention)	0b
[3]	ENABLE	R/W	This bit is only valid when HUSB238A is in I2C mode. It can be configured via I2C during normal operation. When I2C mode, writing 0b to this bit push the main state machine to I2CDisable State 1b: Enable the HUSB238A in I2C mode 0b: Disable the HUSB238A in I2C mode	0b
[2:0]	TCCDEB	R/W	Debounce time for attaching a device 000b: 120ms 001b: 130ms 010b: 140ms 011b: 150ms 100b: 160ms 101b: 170ms 110b: 180ms 111b: Reserved Note: this time is 0 ms in Attachwait.SNK if $V_{DD} < V_{DD\_UVLO}$	011b

The MANUAL register can force the HUSB238A switching to the type-C state per the configuration bit. Only bit[1] in this register is R/W which controlled freely by I²C master. The rest bits are all write one self-clearing (WC), that is these bits can be written 1b by I²C master but will clear to 0b after the execution. When these bits are written by multiple 1b, the bit[1] has the highest priority. The write action of other bits should be ignore. While for the rest bits, the priority is ERROR_REC> UNATT_SNK>FORCE_DPM_HIZ. For instance, the I²C master writes 0xFF to this register. Only the bit[1] is written successfully and the returned value is 0x02. If the I²C master writes 0xF0 to this register, the bit of FORCE_SNK has high priority and is written successfully. The HUSB238A may start Force Function. Then, the returned value is 0x00.

Table 3. MANUAL (Address: 0x03)

Bit	Field	Type	Description	Default
[7:6]	Reserved	R/W		00b
[5]	FORCE_DPM_HIZ	R/W	1b: Disconnect D+ and D- pin from internal circuitry 0b: No any action	0b

Bit	Field	Type	Description	Default
[4]	Reserved			
[3]	UNATT_SNK	WC	1b: Jump to Unattached.SNK state forcedly 0b: No any action	0b
[2]	Reserved			
[1]	DISABLED	R/W	1b: Jump to Disabled state forcedly 0b: Exit Disabled state and enter ErrorRecovery state	0b
[0]	ERROR_REC	WC	1b: Jump to ErrorRecovery state forcedly 0b: No any action	0b

The RESET register is only a command register to execute a reset action for HUSB238A. When a write action of 1b to this RESET[0], HUSB238A jumps to initialization state. After the reset action, the return value of this register bit[0] is 0b.

Table 4. RESET (Address: 0x04)

Bit	Field	Type	Description	Default
[7:1]	Reserved	R/W		00b
[0]	SW_RES	WC	Chip reset. Return to Initialization State 1b: Jump to Initialization state forcedly 0b: No any action	0b

The MASK and MASK1 registers are control registers which can set the INT_N pin low to request the I2C master's attention. Please note that, even an interruption is masked in the MASK and MASK1 registers, this interruption bit in INTERRUPT and INTERRUPT1 registers is also set.

Table 5. MASK (Address: 0x05)

Bit	Field	Type	Description	Default
[7]	M_FLGIN	R/W	1b: Mask the I_FLGIN interruption to assert INT_N pin 0b: DO NOT mask the FLGIN interruption to assert INT_N pin	0b
[6]	M_ORIENT	R/W	1b: Mask the I_ORIENT interruption to assert INT_N pin 0b: DO NOT mask the I_ORIENT interruption to assert INT_N pin	0b
[5]	M_FAULT	R/W	1b: Mask the I_FAULT interruption to assert INT_N pin 0b: DO NOT mask the I_FAULT interruption to assert INT_N pin	0b
[4]	M_VBUS_CHG	R/W	1b: Mask the I_VBUS interruption to assert INT_N pin 0b: DO NOT mask the I_VBUS interruption to assert INT_N pin	0b
[3]	M_VBUS_OV	R/W	1b: Mask the I_VBUS_OV interruption to assert INT_N pin 0b: DO NOT mask the I_VBUS_OV interruption to assert INT_N pin	0b
[2]	M_BC_LVL	R/W	1b: Mask the I_ BC_LVL interruption to assert INT_N pin 0b: DO NOT mask the I_BC_LVL interruption to assert INT_N pin	0b
[1]	M_DETACH	R/W	1b: Mask the I_ DETACH interruption to assert INT_N pin 0b: DO NOT mask the I_ DETACH interruption to assert INT_N pin	0b
[0]	M_ATTACH	R/W	1b: Mask the I_ ATTACH interruption to assert INT_N pin 0b: DO NOT mask the I_ ATTACH interruption to assert INT_N pin	0b

Table 6. MASK1 (Address: 0x06)

Bit	Field	Type	Description	Default
[7]	M_TSD	R/W	1b: Mask the I_TSD interruption to assert INT_N pin 0b: DO NOT mask the I_TSD interruption to assert INT_N pin	0b
[6]	M_VBUS_UV	R/W	1b: Mask the I_VBUS_UV interruption to assert INT_N pin 0b: DO NOT mask the I_VBUS_UV interruption to assert INT_N pin	0b
[5]	M_DR_ROLE	R/W	1b: Mask the I_DR_ROLE interruption to assert INT_N pin	0b

Bit	Field	Type	Description	Default
			0b: DO NOT mask the I_DR_ROLE interruption to assert INT_N pin	
[4]	Reserved			
[3]	M_SRC_ALERT	R/W	1b: Mask the I_SRC_ALERT interruption to assert INT_N pin 0b: DO NOT mask the I_SRC_ALERT interruption to assert INT_N pin	0b
[2]	M_FRC_FAIL	R/W	1b: Mask the I_FRC_FAIL interruption to assert INT_N pin 0b: DO NOT mask the I_FRC_FAIL interruption to assert INT_N pin	0b
[1]	M_FRC_SUCC	R/W	1b: Mask the I_ FRC_SUCC interruption to assert INT_N pin 0b: DO NOT mask the I_ FRC_SUCC interruption to assert INT_N pin	0b
[0]	M_VDM_MSG	R/W	1b: Mask the I_VDM_MSG interruption to assert INT_N pin 0b: DO NOT mask the I_VDM_MSG interruption to assert INT_N pin	0b

Table 7. MASK1 (Address: 0x07)

Bit	Field	Type	Description	Default
[7:4]	Reserved			
[3]	M_Exit_EPR	R/W	1b: Mask the I_Exit_EPR interruption to assert INT_N pin 0b: DO NOT mask the I_AMS_SUCC interruption to assert INT_N pin	
[2]	M_Go_Fail	R/W	1b: Mask the I_Go_FAIL interruption to assert INT_N pin 0b: DO NOT mask the I_AMS_SUCC interruption to assert INT_N pin	0b
[1]	M_EPR_MDOE	R/W	1b: Mask the I_ VDM_MODE interruption to assert INT_N pin 0b: DO NOT mask the I_ VDM_MODE interruption to assert INT_N pin	0b
[0]	M_PD_HV	R/W	1b: Mask the I_PD_HV interruption to assert INT_N pin 0b: DO NOT mask the I_PD_HV interruption to assert INT_N pin	0b

The INTERRUPT, INTERRUPT1 and INTERRUPT2 registers indicate one or some of the interruption are triggered. Once the interruption bit is set, it is latched until the I2C master writes 1b to this bit to clear it. If any interruptions list below is triggered, the corresponding bit is set, but this bit can be set by MASK and MASK1 registers to determine whether this interruption can assert the INT_N low to request the I2C master's attention.

Table 8. INTERRUPT (Address: 0x09)

Bit	Field	Type	Description	Default
[7:4]	Reserved			
[3]	I_Exit_EPR	R/W	1b: Exit EPR interruption occurs 0b: No such interruption occurs	
[2]	I_Go_Fail	R/W	1b: Go fail interruption occurs 0b: No such interruption occurs	0b
[1]	I_EPR_MODE	R/W	1b: EPR mode has been entered 0b: No such interruption occurs	0b
[0]	I_PD_HV	R/W	1b: PD High Voltage Request is done 0b: No such interruption occurs	0b

Table 9. INTERRUPT1 (Address: 0x0A)

Bit	Field	Type	Description	Default
[7]	I_FLGIN	R/W	1b: FLGIN in STATUS1 has changed from 0b to 1b 0b: No such interruption occurs	0b

Bit	Field	Type	Description	Default
[6]	I_ORIENT	R/W	1b: ORIENT in STATUS has changed from 00b to 01b, or 00b to 10b 0b: No such interruption occurs	0b
[5]	I_FAULT	R/W	1b: FAULT1 or FAULT2 is set 0b: No such interruption occurs	0b
[4]	I_VBUS_CHG	R/W	1b: VBUS_OK transitions from 0b to 1b or 1b to 0b 0b: No such interruption occurs	0b
[3]	I_VBUS_OV	R/W	1b: VBUS_OV fault is set 0b: No VBUS_OV	0b
[2]	I_BC_LVL	R/W	1b: BC_LVL in STATUS is changed 0b: No such interruption occurs	0b
[1]	I_DETACH	R/W	1b: One of exit of Attached.SNK/ DebugAccessory.SNK states happens 0b: No such interruption occurs	0b
[0]	I_ATTACH	R/W	1b: One of entry of Attached.SNK/ DebugAccessory.SNK states happens 0b: No such interruption occurs	0b

Table 10. INTERRUPT2 (Address: 0x0B)

Bit	Field	Type	Description	Default
[7]	I_TSD	R/W	1b: TSD is set 0b: No TSD flag	0b
[6]	I_VBUS_UV	R/W	1b: Valid VBUS_UV fault is set 0b: No valid VBUS_UV	0b
[5]	I_DR_ROLE	R/W	1b: Data Role is changed 0b: Data Role is NOT changed	0b
[4]	Reserved			
[3]	I_SRC_ALERT	R/W	1b: Alert Message is received from Connected source 0b: Alert Message is received from Connected source	0b
[2]	I_FRC_FAIL	R/W	1b: FORCE_SNK has failed 0b: No such interruption occurs	0b
[1]	I_FRC_SUCC	R/W	1b: FORCE_SNK has been done 0b: No such interruption occurs	0b
[0]	I_VDM_MSG	R/W	1b: A VDM message is received 0b: No VDM message is received	0b

Table 11. USER CFG0 (Address: 0x0C)

Bit	Field	Type	Description	Default
[7:6]	TSNKDSCNT	R/W	Debounce time for transition from Attached.SNK to Unattached.SNK 00b:0ms 01b:5ms 10b:15ms 11b: 30ms	10b
[5]	CC_DSCNTEN	R/W	In Attached.SNK, connected CC is used to monitor the disconnection 0b:Disabled 1b:Enabled	
[4]	TFAUL	R/W	Debounce time for detect a valid Fault 0b:10 μs 1b:1 ms	0b

Bit	Field	Type	Description	Default
[3:2]	TVBDSGTIMEOUT	R/W	Max conduction time of VBUS_DSG=1b 00b: Disable VBUS_DSG always 01b: 50ms 10b: 100ms 11b: 200ms	
[1:0]	TBC_LEVEL	R/W	Debounce time of BC_LVL change 00b: 3ms 01b: 12ms 10b: 15ms 11b: 18ms	

Table 12. USER CFG1 (Address: 0x0D)

Bit	Field	Type	Description	Default
[7]	Reserved	R/W	Reserved	0b
[6]	EN_HVDCP	R/W	HVDCP Detection enable control when attached as a Sink. This bit is updated after initialization automatically. It can be configured via I^2C during normal operation. 0b: Only perform BC1.2 CDP,SDP and DCP detection 1b: Perform HVDCP detection after BC1.2 detection	EN_HVDCP/OUT1
[5:4]	Reserved			
[3]	EN_VB_UV	R/W	VBUS UV detection enable control: 0b: Disable VBUS UV detection 1b: Enable VBUS UV detection	0b
[2]	EN_SVID3	R/W	Enable the 3rd SVID info in Discover SVIDs ACK message: 0b: NOT respond VID as the 3rd SVID in the Discover SVIDs ACK 1b: Respond VID as the 3rd SVID in the Discover SVIDs ACK	0b
[1:0]	OUT2_SEL	R/W	FAULT/OUT2 pin function selection: 00b: Fault Indication 01b: ID Indication 10b: Controlled by EN_OUT2 11b: Reserved	

Table 13. USER CFG2 (Address: 0x0E)

Bit	Field	Type	Description	Default
[7]	EN_OUT2	R/W	OUT2 output control when OUT2_SEL=10b. 0b: Drive Low 1b: Drive High	0b
[6]	FLG_ POLARITY	R/W	FAULT/OUT2 output polarity selection. 0b: NOT reverse the output of this pin 1b: Reverse the output of this pin	0b
[5]	EN_FAULTIN	R/W	FLGIN input action selection. 0b: NOT turn off GATE pin 1b: Turn off GATE pin (Hi-Z) immediately	1b
[4]	EN_OUT1	R/W	OUT1 output control. 0b: Drive Low 1b: Drive High	0b

Bit	Field	Type	Description	Default
[3]	Reserved			
[2]	PD_PRIOR	R/W	PD Protocol Priority Control 0b: PD has low Priority and delayed 3s to run the PD PE 1b: PD has high Priority and run the PD PE after connection is successful	
[1]	EN_DRS	R/W	DR_Swap Message Response 0b: Reject DR_Swap 1b: Accept DR_Swap	1b
[0]	Reserved			

Table 14. USER CFG3 (Address: 0x0F)

Bit	Field	Type	Description	Default
[7]	Reserved	R/W		
[6]	PPS_CAP_SNK	R/W	PPS Sink Capability Support Control 0b: PPS Capability is NOT supported 1b: PPS Capability is supported	0b
[5]	AVS_CAP_SNK	R/W	AVS Sink Capability Support Control 0b: AVS Capability is NOT supported 1b: AVS Capability is supported	0b
[4]	MODAL_OPERATION	R/W	SOP Discover Identity ID Header VDO [26]. Modal Operation Supported as UFP: 0b: Respond SOP NAK for Discover SVIDs, Discover Modes, Enter Mode, Exit Mode 1b: Respond SOP ACK for Discover SVIDs, Discover Modes, Enter Mode, Exit Mode	0b
[3]	EPR_AVS_CAP_SNK	R/W	EPR AVS Sink Capability Support Control 0b: EPR AVS Capability is NOT supported 1b: EPR AVS Capability is supported	0b
[2]	SNK_CAP_MIN_VOLTAGE	R/W	Min Voltage in Sink_Capabilities PDO2 0b: 5 V 1b: 3.3 V	0b
[1:0]	SNK_PDO1_CURRENT	R/W	PDO1 current in Sink_Capabilities. 00b: 3 A 01b: 2.4 A 10b: 2.1 A 11b: 1.5 A	00b

Table 15. SVID0_MSB (Address: 0x10)

Bit	Field	Type	Description	Default
[7:0]	SVID0_MSB	R/W	Discover SVIDs VDO1 [31…24]	0x00

Table 16. SVID0_LSB (Address: 0x11)

Bit	Field	Type	Description	Default
[7:0]	SVID0_LSB	R/W	Discover SVIDs VDO1 [23…16]	0x00

Table 17. SVID1_MSB (Address: 0x12)

Bit	Field	Type	Description	Default
[7:0]	SVID1_MSB	R/W	Discover SVIDs VDO1 [16…8]	0x00

Table 18. SVID1_LSB (Address: 0x13)

Bit	Field	Type	Description	Default
[7:0]	SVID1_LSB	R/W	Discover SVIDs VDO1 [7…0]	0x00

Table 19. MODE0_MSB (Address: 0x14)

Bit	Field	Type	Description	Default
[7:0]	MODE0_MSB	R/W	Discover Modes VDO1 [23…16]	0x00

Table 20. MODE0_LSB (Address: 0x15)

Bit	Field	Type	Description	Default
[7:0]	MODE0_LSB	R/W	Discover Modes VDO1 [7…0]	0x00

Table 21. MODE1_MSB (Address: 0x16)

Bit	Field	Type	Description	Default
[7:0]	MODE1_MSB	R/W	Discover Modes VDO1 [23…16]	0x00

Table 22. MODE1_LSB (Address: 0x17)

Bit	Field	Type	Description	Default
[7:0]	MODE1_LSB	R/W	Discover Modes VDO1 [7…0]	0x00

Table 23. GO_COMMAND (Address: 0x18)

Bit	Field	Type	Description	Default
[7:5]	Reserved	R/W	Reserved	000b
[4:0]	GO	R/W	00000b: None 00001b: HUSB238A sets PDO_SELECT and GO to select the target PDO. The action is not limited by the VSET and SNK_PDO2 setting 00010b: bist data mode test 00011b: bist carrier mode test 00100b: Send out Get_SRC_Cap command 00101b: Send out DR_Swap command 00111b: Send out Get_PPS_Status command 01000b: Send out Get_Manufacturer_Info command 01001b: Send out Discover Identity command 01010b: Send out Discover SVIDs command 01011b: Send out Discover Modes (SVID0) command 01100b: Send out Discover Modes (SVID1) command 01101b: Send out Enter Mode (SVID0 & MODE0) command 01110b: Send out Enter Mode (SVID1 & MODE1) command 01111b: Send out Exit Mode (SVID0 & MODE0) command 10000b: Send out Exit Mode (SVID1 & MODE1) command 11000b: Send out EPR_Get_Source_Cap 11001b: Send out EPR_Mode Enter command 11010b: Send out EPR_Mode Exit command 11101b: Send out Soft Reset command 11110b: Send out Hard Reset command	00000b

Table 24. SRC_PDO (Address: 0x19)

Bit	Field	Type	Description	Default
[7:3]	PDO_SELECT	R/W	Select the target SRC_PDO as RDO in PD_MODE. Request ISRC_PDO as operating current in RDO message. 00000b: Not selected 00001b: SRC_PDO_5V 00010b: SRC_PDO_9V 00011b: SRC_PDO_12V 00100b: SRC_PDO_15V 00101b: SRC_PDO_20V	00000b

Bit	Field	Type	Description	Default
			00110b: SRC_PDO_PPS1 00111b: SRC_PDO_PPS2 01000b SRC_PDO_PPS3 01001b: SRC_PDO_AVS 10000b: QC2_5V 10001b: QC2_9V 10010b: QC2_12V 11000b: SRC_PDO_28V 11010b: SRC_PDO_36V 11100b: SRC_PDO_48V 11110b: SRC_EPR_AVS	
[2]	Reserved	R/W	Reserved	0b
[1:0]	SNK_PPS_VOL_M	R/W	Combined with SNK_PPS_VOL_L as the low 8 bits. The request output voltage for GO_COMMAND (SRC_PDO_PPS1, SRC_PDO_PPS2, SRC_PDO_PPS3)	0b

Table 25. SNK_PPS_VOLTAGE (Address: 0x1A)

Bit	Field	Type	Description	Default
[7:0]	SNK_PPS_VOL_L	R/W	Combined with SNK_PPS_VOL_M as the highest 2 bits. The request output voltage for GO_COMMAND (SRC_PDO_PPS1, SRC_PDO_PPS2, SRC_PDO_PPS3). 20 mV per LSB. Offset is 3 V. 0x000: 3.00 V 0x001: 3.02 V … 0x3FF: 23.46 V	00000000b

Table 26. SNK_PPS_CURRENT (Address: 0x1B)

Bit	Field	Type	Description	Default
[7]	Reserved	R/W		0b
[6:0]	SNK_PPS_CURRENT	R/W	The request operating current for GO_COMMAND (SRC_PDO_PPS1, SRC_PDO_PPS2, SRC_PDO_PPS3). 50 mA per LSB. 0x00: 0.0 A 0x01: 0.05 A … 0x7F: 6.35 A	0000000b

Table 27. SNK_AVS_VOLTAGE (Address: 0x1C)

Bit	Field	Type	Description	Default
[7:0]	SNK_AVS_VOL_L	R/W	The request output voltage for GO_COMMAND (SRC_PDO_AVS). 100 mV per LSB. 0x00: 0.0 V 0x01: 0.1 V … 0xFF: 25.5 V	00000000b

Table 28. SNK_AVS_CURRENT (Address: 0x1D)

Bit	Field	Type	Description	Default
[7]	SNK_AVS_VOL_M	R/W	Combined with SNK_AVS_VOL_L as the low 8 bits. The request output voltage for GO_COMMAND (SRC_PDO_AVS). 100 mV per LSB.	0b

Bit	Field	Type	Description	Default
[6:0]	SNK_AVS_CURRENT	R/W	The request operating current for GO_COMMAND (SRC_PDO_AVS). 50 mA per LSB. 0x00: 0.0 A 0x01: 0.05 A … 0x7F: 6.35 A	0000000b

Table 29. EPR_AVS_VOLTAGE (Address: 0x1E)

Bit	Field	Type	Description	Default
[7:0]	EPR_AVS_VOL_L	R/W	Combined with EPR_AVS_VOL_M as the highest 1 bit. The request output voltage for GO_COMMAND (SRC_EPR_AVS). 100 mV per LSB. 0x000: 0.0 V 0x001: 0.1 V … 0x1FF: 51.1 V	00000000b

Table 30. EPR_AVS_CURRENT (Address: 0x20)

Bit	Field	Type	Description	Default
[7]	EPR_AVS_VOL_M	R/W	Combined with EPR_AVS_VOL_L as the low 8 bits. The request output voltage for GO_COMMAND (SRC_EPR_AVS). 100 mV per LSB.	0b
[6:0]	EPR_AVS_CURRENT	R/W	The request operating current for GO_COMMAND (SRC_EPR_AVS). 50 mA per LSB. 0x00: 0.0 A 0x01: 0.05 A … 0x7F: 6.35 A	0000000b

Table 31. SNK_PDP (Address: 0x21)

Bit	Field	Type	Description	Default
[7]	Reserved	R/W		0b
[6:0]	SNK_PDP	R/W	Sink PDP value. 1 W per LSB	0000000b

Table 32. EPR_PDP (Address: 0x22)

Bit	Field	Type	Description	Default
[7:0]	SNK_EPR_PDP	R/W	Sink EPR PDP value. 1 W per LSB	00000000b

STATUS REGISTERS

The STATUS and STATUS1 registers are read-only registers that show the status of functions.

Table 33. STATUS (Address: 0x63)

Bit	Field	Type	Description	Default
[7]	AMS_PROCESS	R	1b: The HUSB238A is in a AMS process 0b: The HUSB238A is NOT in an AMS process. The PD PE stays in PE_SRC_READY or PE_SNK_Ready	0b
[6]	PD_EPR_SNK	R	1b: EPR Mode is entered successfully 0b: NOT in EPR Mode	0b
[5:4]	Reserved	R	Reserved	00b
[3]	TSD	R	1b: TSD is set 0b: TSD is NOT set	0b
[2]	BC_LVL	R	In Attached.SNK State, Connected CC line voltage level status: **Values DEF_COMP 1P5_COMP 3P0_COMP State**	00b

Bit	Field	Type	Description					Default
			00b	0	0	0	In Attached.SNK	
			00b	X	X	X	Not in Attahced.SNK	
			01b	1	0	0	In Attached.SNK	
			10b	1	1	0	In Attached.SNK	
			11b	1	1	1	In Attached.SNK	
[0]	ATTACH	R	1b: In the Attached.SNK/ DebugAccessory.SNK states 0b: DO NOT in the Attached.SNK/ DebugAccessory.SNK states					0b

Table 34. STATUS1 (Address: 0x64)

Bit	Field	Type	Description	Default
[7]	FLGIN	R	1b: FLGIN is High 0b: FLGIN is Low	0b
[6]	Reserved	R		0b
[5]	PD_HV	R	1b: An non-PDO1 PD contract is established 0b: PDO1 contract is established or no PD contract established	0b
[4]	PD_COMM	R	The PD communication is detected when a valid PD message (received a Source_Capabilities in Sink mode, or received a HardReset or GoodCRC for Source_Capabilities sent in Source mode) is detected by HUSB238A 1b: PD communication is detected 0b: PD communication is NOT detected	0b
[3]	SRC_ALERT	R	Alert message reception status from Source 0b: Alert message from source is NOT received 1b: Alert message from source is received	0b
[2]	AMS_SUCC	R	The status of a GO_COMMAND 1b: GO_COMMAND is executed successfully 0b: GO_COMMAND is NOT executed due to it is in a AMS procedure	0b
[1]	FAULT	R	1b: one or both of FAULT1_COMP or FAULT2_COMP is set 0b: None of FAULT1_COMP or FAULT2_COMP is set	0b
[0]	DATA_ROLE	R	Current Port Data Role. This bit is changed depending on the connected results (as a Sink or Source) but may be changed dynamically by DR_Swap 1b: DFP 0b: UFP	0b

The TYPE register indicates the connection results.

Table 35. TYPE (Address: 0x65)

Bit	Field	Type	Description	Default
[7]	CC_RX_ACTIVE	R	The status of CC line. 0b: Connected CC line is in PD-idle 1b: Connected CC line is NOT in PD-idle	0b
[6]	Reserved	R		0b
[5]	DEBUGSNK	R	1b: In the states of DebugAccessory.SNK 0b: NOT in the states of DebugAccessory.SNK	0b
[4]	SINK	R	1b: In the states of Attached.SNK 0b: NOT in the states of Attached.SNK	0b

Bit	Field	Type	Description	Default
[3:0]	Reserved	R		0b

Table 36. DPDM_STATUS (Address: 0x66)

Bit	Field	Type	Description	Default
[7:3]	Reserved ~~DPDM_STATUS~~	R	~~The current legacy charger protocols supported~~ ~~0x00: Unattached.SNK~~ ~~0x01: Unattached.SNK~~ ~~0x02: Divider 3 Detection~~ ~~0x03: BC1.2 Detection~~ ~~0x04: Reserved~~ ~~0x05: QC2 Detection~~ ~~0x06: Hi-Z~~ ~~0x07…0x7F: Reserved~~	~~0x00~~000000b
[2]	CDP_FLAG	R	1b: CDP mode supported 0b: CDP mode not supported	0b
[1]	SDP_FLAG	R	1b: SDP mode supported 0b: SDP mode not supported	0b
[0]	DIVIDER3_FLAG	R	1b: DIVIDER3 mode supported 0b: DIVIDER3 mode not supported	0b

Table 37. CONTRACT_STATUS0 (Address: 0x67)

Bit	Field	Type	Description	Default
[7:4]	PD_CONTRACT	R	The current Contract established with a Source. For PD contract, it is established when a PD negotiation is done. 0000b: 5 V type-C Contract established 0001b: SRC_PDO_5V Contract established 0010b: SRC_PDO_9V Contract established 0011b: SRC_PDO_12V Contract established 0100b: SRC_PDO_15V Contract established 0101b: SRC_PDO_20V Contract established 0110b: SRC_PDO_PPS1 Contract established 0111b: SRC_PDO_PPS2 Contract established 1000b: SRC_PDO_PPS3 Contract established 1001b: SRC_PDO_AVS Contract established 1010b: SRC_PDO_28V Contract established (EPR PDO1) 1011b: SRC_PDO_36V Contract established (EPR PDO2) 1100b: SRC_PDO_48V Contract established (EPR PDO3) 1101b: SRC_EPR_AVS Contract established (EPR PDO4) 1110b…1111b: Reserved	0000b
[3:0]	DPM_CONTRACT	R	For DPDM contract, it is established when a DPDM request is sent and the VBUS voltage is measured without VBUS_OV and VBUS_UV flags. 0000b: 5 V Default Contract established 0001b: 5 V Divider 3 Contract established 0010b: 5 V SDP Contract established 0011b: 5 V CDP Contract established 0100b: 5 V DCP Contract established 0101b: 5 V HVDCP Contract established 0110b: QC2 9 V Contract established 0111b: QC2 12 V Contract established 1000b…1111b: Reserved	0000b

Table 38. CONTRACT_STATUS1 (Address: 0x68)

Bit	Field	Type	Description	Default
[7:0]	CONTRACT_CURRENT	R	The operating current information when an explicit contract (FPDO, checked by PD_CONTRACT) is established. Only for PD contract. 20 mA per LSB for 0x00 to 0x7D, the offset current is 0.5 A. 40 mA per LSB for 0x7E to 0xFF. The offset current is 0.5 A. 0x00: 0.5 A 0x01: 0.52 A … 0x7D: 3.00 A 0x7E: 3.04 A 0x7F: 3.08 A 0x80: 3.12 A … 0xFF: 8.17 A If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead. If the explicit contract is APDO (PPS, AVS, checked by PD_CONTRACT), 50 mA per LSB for 0x00 to 0xFF, The offset current is 0 A. 0x00: 0.00 A 0x01: 0.05 A … 0xFF: 12.75 A	0000b

The following tables shows the received PDO info from Source_Capabilities or EPR_Source_Capabilities messages.

Table 39. SourceCap_INFO (Address: 0x69)

Bit	Field	Type	Description	Default
[7]	Reserved	R		0b
[6]	VDM_MODE	R	After the Enter Mode ACK is sent or received successfully, the HUSB238A is activated in a VDM Mode. Exit activated mode could be A Exit Mode ACK sent or received successfully, HardReset sent or received, Entry to Unattached.SNK or Unattached.SRC 1b: An VDM Mode is activated 0b: An VDM Mode is NOT activated	0b
[5]	Power Limit	R	PPS PDO [27] of received Source_capabilities or EPR_Source_Capabilities messages 1b: DRP is supported 0b: DRP is not supported	0b
[4]	Dual-Role Power	R	PDO1 [29] of received Source_capabilities or EPR_Source_Capabilities messages 1b: DRP is supported 0b: DRP is not supported	0b
[3]	USB Suspend Supported	R	PDO1 [28] of received Source_capabilities or EPR_Source_Capabilities messages 1b: USB Suspend is supported 0b: USB Suspend is not supported	0b
[2]	USB Communications Capable	R	PDO1 [26] of received Source_capabilities or EPR_Source_Capabilities messages 1b: USB Communication is supported 0b: USB Communication is not supported	0b

Bit	Field	Type	Description	Default
[1]	Dual-Role Data	R	PDO1 [25] of received Source_capabilities or EPR_Source_Capabilities messages 1b: DRD is supported 0b: DRD is not supported	0b
[0]	EPR Mode Capable	R	PDO1 [23] of received Source_capabilities or EPR_Source_Capabilities messages 1b: EPR Mode is supported 0b: EPR Mode is not supported	0b

Table 40. SRC_PDO_5V (Address: 0x6A)

Bit	Field	Type	Description	Default
[7]	SRC_5V_DETECT	R	0b: Not detected 1b: Detect the PDO1	0b
[6:0]	SRC_5V_CURRENT	R	The max current information for PDO1 in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead.	000000b

Table 41. SRC_PDO_9V (Address: 0x6B)

Bit	Field	Type	Description	Default
[7]	SRC_9V_DETECT	R	0b: Not detected 1b: Detect a FPDO whose voltage is within 8 V – 10 V	0b
[6:0]	SRC_9V_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A …	000000b

Bit	Field	Type	Description	Default
			0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead.	

Table 42. SRC_PDO_12V (Address: 0x6C)

Bit	Field	Type	Description	Default
[7]	SRC_12V_DETECT	R	0b: Not detected 1b: Detect a FPDO whose voltage is within 11 V – 13 V	0b
[6:0]	SRC_12V_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A	000000b

Bit	Field	Type	Description	Default
			If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead.	

Table 43. SRC_PDO_15V (Address: 0x6D)

Bit	Field	Type	Description	Default
[7]	SRC_15V_DETECT	R	0b: Not detected 1b: Detect a FPDO whose voltage is within 14 V – 18 V	0b
[6:0]	SRC_15V_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead.	000000b

Table 44. SRC_PDO_20V (Address: 0x6E)

Bit	Field	Type	Description	Default
[7]	SRC_20V_DETECT	R	0b: Not detected 1b: Detect a FPDO whose voltage is within 19 V – 21 V	0b
[6:0]	SRC_20V_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A	000000b

Bit	Field	Type	Description	Default
			0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead.	

Table 45. SRC_PDO_28V (Address: 0x6F)

Bit	Field	Type	Description	Default
[7]	SRC_28V_DETECT	R	0b: Not detected 1b: Detect a EPR FPDO whose voltage is within 22 V – 28 V	0b
[6:0]	SRC_28V_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead.	000000b

Table 46. SRC_PDO_36V (Address: 0x70)

Bit	Field	Type	Description	Default
[7]	SRC_36V_DETECT	R	0b: Not detected	0b

Bit	Field	Type	Description	Default
			1b: Detect a EPR FPDO whose voltage is within 29 V – 36 V	
[6:0]	SRC_36V_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead.	000000b

Table 47. SRC_PDO_48V (Address: 0x71)

Bit	Field	Type	Description	Default
[7]	SRC_48V_DETECT	R	0b: Not detected 1b: Detect a FPDO whose voltage is within 37 V – 48 V	0b
[6:0]	SRC_48V_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A	000000b

Bit	Field	Type	Description	Default
			0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A If the source current capability is not the one listed above, use the one lower but the closest one. For example, if the source current capability is 4.33 A, use the 4.30 A instead.	

Table 48. SRC_PDO_PPS1 (Address: 0x72)

Bit	Field	Type	Description	Default
[7]	SRC_PPS1_DETECT	R	0b: Not detected 1b: Detect the 1st PPS PDO.	0b
[6:0]	SRC_PPS1_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A	000000b

Table 49. SRC_PDO_PPS2 (Address: 0x73)

Bit	Field	Type	Description	Default
[7]	SRC_PPS2_DETECT	R	0b: Not detected 1b: Detect the 2nd PPS PDO.	0b
[6:0]	SRC_PPS2_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A	000000b

Bit	Field	Type	Description	Default
			0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A	

Table 50. SRC_PDO_PPS3 (Address: 0x74)

Bit	Field	Type	Description	Default
[7]	SRC_PPS3_DETECT	R	0b: Not detected 1b: Detect the 3rd PPS PDO.	0b
[6:0]	SRC_PPS3_CURRENT	R	The max current information for the detected PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 100 mA per LSB. 0x00: 0.0 A 0x01: 0.1 A … 0x3F: 6.3 A 0x40: 6.4 A 0x41: 6.5 A 0x42: 6.6 A 0x43: 6.7 A 0x44: 6.8A 0x45: 6.9A 0x46: 7.0A 0x47: 7.1 A 0x48: 7.2 A 0x49: 7.3 A 0x4A: 7.4 A 0x4B: 7.5 A 0x4C: 7.6 A 0x4D: 7.7A 0x4E: 7.8A 0x4F: 7.9A 0x50: 8.0A	000000b

Table 51. SRC_PPS_VOLTAGE (Address: 0x75)

Bit	Field	Type	Description	Default
[7:6]	PPS1_MAX_VOLTAGE	R	The max voltage information for the detected PPS1 PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 00b: 5.9 V (0 V to 7 V) 01b: 11 V (7.02 V to 12 V)	00b

Bit	Field	Type	Description	Default
			10b: 16 V (12.02 V to 17 V) 11b: 21 V (Higher than 17.02 V)	
[5:4]	PPS2_MAX_VOLTAGE	R	The max voltage information for the detected PPS2 PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 00b: 5.9 V (0 V to 7 V) 01b: 11 V (7.02 V to 12 V) 10b: 16 V (12.02 V to 17 V) 11b: 21 V (Higher than 17.02 V)	00b
[3:2]	PPS3_MAX_VOLTAGE	R	The max voltage information for the detected PPS3 PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 00b: 5.9 V (0 V to 7 V) 01b: 11 V (7.02 V to 12 V) 10b: 16 V (12.02 V to 17 V) 11b: 21 V (Higher than 17.02 V)	00b
[1:0]	PPS_MIN_VOLTAGE	R	The max value of all of min voltage information for the detected PPS PDOs in received Source_Capabilities or EPR_Source_Capabilities messages. 00b: 3 V (0 V -3.14 V) 01b: 3.3 V (3.16 V – 3.46 V) 10b: 5 V (> 3.46 V) 11b: Reserved	00b

Table 52. SRC_PDO_AVS (Address: 0x76)

Bit	Field	Type	Description	Default
[7]	SRC_AVS_DETECT	R	0b: Not detected 1b: Detect the AVS PDO whose PDO [31…28]=1110b.	0b
[6:3]	AVS_MAX_VOLTAGE	R	The max voltage information for the detected AVS PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 1 V per LSB. 5 V offset. 0000b: 5 V (0 V to 5 V) 0001b: 6 V (5.1 V to 6 V) … 1111b: 20 V (higher than 19.1 V)	0000b
[2]	Reserved	R		0b
[1:0]	AVS_MIN_VOLTAGE	R	The min voltage information for the detected AVS PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 00b: 5 V (0 V to 6 V) 01b: 9 V (6.1 V – 9 V) 10b: 15 V (higher than 9.1 V) 11b: Reserved	00b

Table 53. SRC_AVS_PDP (Address: 0x77)

Bit	Field	Type	Description	Default
[7:0]	SRC_AVS_PDP	R	The PDP information for the detected AVS PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 1 W per LSB. 0x00: 0 W 0x01: 1 W … 0xFF: 255 W	0x00

Table 54. EPR_AVS_PDP (Address: 0x78)

Bit	Field	Type	Description	Default
[7:0]	EPR_AVS_PDP	R	The PDP information for the detected EPR AVS PDO in received Source_Capabilities or EPR_Source_Capabilities messages. 1 W per LSB. 0x00: 0 W 0x01: 1 W … 0xFF: 255 W	0x00

Table 55. SRC_EPR_AVS (Address: 0x79)

Bit	Field	Type	Description	Default
[7]	EPR_AVS_DETECT	R	0b: Not detected 1b: Detect the EPR AVS PDO whose PDO [31…28]=1101b	0b
[6:2]	EPR_AVS_MAX_VOLTAGE	R	The max voltage information for the detected EPR AVS PDO in received EPR_Source_Capabilities messages. 1 V per LSB. 20 V offset. 00000b: 20 V (0 V to 20 V) 00001b: 21 V (20.1 V to 21 V) … 11111b: 52 V (Higher than 51.1 V)	00000b
[1:0]	EPR_AVS_MIN_VOLTAGE	R	The min voltage information for the detected EPR AVS PDO in received EPR_Source_Capabilities messages. 00b: 5 V (0 V to 6 V) 01b: 9 V (6.1 V – 9 V) 10b: 15 V (higher than 9.1 V) 11b: Reserved	0000000b

Table 56. VDM_HEADER (Address: 0x7A)

Bit	Field	Type	Description	Default
[7:5]	Object Position	R	Structure VDM Header [10…8] of the received VDM message	000b
[4:3]	Command Type	R	Structure VDM Header [7…6] of the received VDM message 00b: REQ (Request from Initiator Port) 01b: ACK (Acknowledge Response from Responder Port) 10b: NAK (Negative Acknowledge Response from Responder Port) 11b: BUSY (Busy Response from Responder Port)	00b
[2:0]	VDM_TYPE	R	Structure VDM Header [4…0] of the received VDM message 000b: Discover Identity 001b: Discover SVIDs 010b: Discover Modes 011b: Enter Mode 100b: Exit Mode	000b

Table 57. VDM_VDO1_0 (Address: 0x7B)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO1_0	R	Structure VDM VDO1 [7…0] of the received VDM message	0x00

Table 58. VDM_VDO1_1 (Address: 0x7C)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO1_1	R	Structure VDM VDO1 [15…8] of the received VDM message	0x00

Table 59. VDM_VDO1_2 (Address: 0x7D)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO1_2	R	Structure VDM VDO1 [23…16] of the received VDM message	0x00

Table 60. VDM_VDO1_3 (Address: 0x7E)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO1_3	R	Structure VDM VDO1 [31…24] of the received VDM message	0x00

Table 61. VDM_VDO2_0 (Address: 0x7F)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO2_0	R	Structure VDM VDO2 [7…0] of the received VDM message	0x00

Table 62. VDM_VDO2_1 (Address: 0x80)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO2_1	R	Structure VDM VDO2 [15…8] of the received VDM message	0x00

Table 63. VDM_VDO2_2 (Address: 0x81)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO2_2	R	Structure VDM VDO2 [23…16] of the received VDM message	0x00

Table 64. VDM_VDO2_3 (Address: 0x82)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO2_3	R	Structure VDM VDO2 [31…24] of the received VDM message	0x00

Table 65. VDM_VDO3_0 (Address: 0x83)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO3_0	R	Structure VDM VDO3 [7…0] of the received VDM message	0x00

Table 66. VDM_VDO3_1 (Address: 0x84)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO3_1	R	Structure VDM VDO3 [15…8] of the received VDM message	0x00

Table 67. VDM_VDO2_2 (Address: 0x85)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO3_2	R	Structure VDM VDO3 [23…16] of the received VDM message	0x00

Table 68. VDM_VDO3_3 (Address: 0x86)

Bit	Field	Type	Description	Default
[7:0]	VDM_VDO3_3	R	Structure VDM VDO3 [31…24] of the received VDM message	0x00

Table 69. VBUS_MEASUREMENT (Address: 0x87)

Bit	Field	Type	Description	Default
[7:0]	VBUS_MEA	R	Sample VBUS voltage. 125 mV per LSB.	0x00

Table 70. SRC_ALERT (Address: 0x88)

Bit	Field	Type	Description	Default
[7]	EXTENDED	R	Alert Data Object [31] of received Alert message from connected source.	0b
[6]	OVP_EVENT	R	Alert Data Object [30] of received Alert message from connected source.	0b
[5]	SRC_INPUT	R	Alert Data Object [29] of received Alert message from connected source.	0b
[4]	OP_CHANGE	R	Alert Data Object [28] of received Alert message from connected source.	0b

Bit	Field	Type	Description	Default
[3]	OTP_EVENT	R	Alert Data Object [27] of received Alert message from connected source.	0b
[2]	OCP_EVENT	R	Alert Data Object [26] of received Alert message from connected source.	0b
[1]	BATTERY_STATUS	R	Alert Data Object [25] of received Alert message from connected source.	0b
[0]	Reserved	R	Alert Data Object [24] of received Alert message from connected source.	0b

Table 71. SRC_PPS_STATUS_VOLTAGE (Address: 0x89)

Bit	Field	Type	Description	Default
[7:0]	SRC_PPS_VOL_L	R	Combined with SRC_PPS_VOL_M as the highest 2 bits. The updated source output voltage. 20 mV per LSB. Offset is 3 V. 0x000: 3.00 V 0x001: 3.02 V … 0x3FF: 23.46 V	00000000b

Table 72. SRC_PPS_STATUS_CURRENT (Address: 0x8A)

Bit	Field	Type	Description	Default
[7]	Reserved	R	Reserved	0b
[6:0]	SRC_PPS_CURRENT	R	The updated source output current. 50 mA per LSB. 0x00: 0.0 A 0x01: 0.05 A … 0x7F: 6.35 A	0000000b

Table 73. SRC_PPS_STATUS_FLAG (Address: 0x8B)

Bit	Field	Type	Description	Default
[7:6]	SRC_PPS_VOL_M	R	Combined with SRC_PPS_VOL_L as the lowest 8 bits. The updated source output voltage.	00b
[5:4]	Reserved	R		00b
[3]	OMF	R	Real Time Flag field [3] of received PPS_STATUS data block.	0b
[2:1]	PTF	R	Real Time Flag field [2:1] of received PPS_STATUS data block.	00b
[0]	Reserved	R	Reserved	0b

Table 74. MNF_OFST0 (Address: 0x8C)

Bit	Field	Type	Description	Default
[7:0]	MNF_OFST_0	R	Manufacturer_Info offset 0: Vendor ID	0x00

Table 75. MNF_OFST1 (Address: 0x8D)

Bit	Field	Type	Description	Default
[7:0]	MNF_OFST_1	R	Manufacturer_Info offset 1: Vendor ID	0x00

Table 76. MNF_OFST2 (Address: 0x8E)

Bit	Field	Type	Description	Default
[7:0]	MNF_OFST_2	R	Manufacturer_Info offset 2: Product ID	0x00

Table 77. MNF_OFST3 (Address: 0x8F)

Bit	Field	Type	Description	Default
[7:0]	MNF_OFST_3	R	Manufacturer_Info offset 3: Product ID	0x00

Table 78. (Address: 0x90)

Bit	Field	Type	Description	Default
[7:6]	Reserved	R		0x00
[5:0]	Sink state	R	Current state of SINK FSM	

Table 79. (Address: 0x91)

[7:6]	Reserved	R		0x00
[5:0]	Source state	R	Current state of SOURCE FSM	

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