HBD HV Control and Monitoring System for the PHENIX Experiment at the Relativistic Heavy Ion Collider

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Abstract of the Thesis

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As an upgrade solution for measurements of the low-mass dielectron continuum in $\sqrt{s_{NN}} = 200$ GeV $Au+Au$ collisions at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory, a Hadron Blind Detector (HBD) has been installed in a field free region surrounding the collision vertex in PHENIX. The first operation of the detector in 2007 has shown critical performance deficits due to issues found with the Gas Electron Multiplier (GEM) HV powering scheme, which allowed severe discharges to occur within the GEM stack, most notably between the mesh and uppermost GEM that damaged a considerable fraction of the GEM foils. In response, the damaged GEM foils were replaced and the problem was carefully studied. Based upon these results, a new High Voltage Control and Monitoring System (HVC) was developed to specifically address possible sources of damage, while allowing optimal control over the detector for maximal performance.

The overall system comprises several novel hardware components including a new voltage divider board and trip detection/protection boards for each power supply module, while actual control of the HV is maintained by an intelligent software suite which incorporates Modern Optimal Control Theory. The software suite is made up of several concurrently operating subsystems, which process measurements fed back from the HV mainframe and modify the HV when deemed necessary. This software suite represents the first system based on true C/S architecture within the PHENIX HV Control environment and may be extended to other detector technologies requiring precision and stability.

The HVC system has been installed in PHENIX early 2009 and has proven its ability to regulate the HV of the HBD in an optimal way throughout the commissioning $p+p$ Run-9 and is expected to lead the detector through its final and most important operation in the $Au+Au$ Run-10 with the aim of enabling the HBD to acquire a substantial data set of the low-mass dileption spectrum. This data will present an opportunity to obtain significant insights into the characteristics of the Quark Gluon Plasma and to study chiral symmetry restoration and deconfinement.

To my parents.

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Chapter 1

Introduction

1.1 Quark Gluon Plasma and RHIC

Relativistic heavy ion collisions have proven to be an excellent method to explore nuclear matter under extreme conditions.

According to Quantum Chromodynamics (QCD), quarks are confined to hadrons in pairs of two/three and bound by gluons. At very small distances, their coupling constant α_s is small and quarks begin to act as quasi-free particles (asymptotic freedom, [8, 9]). At large distances, α_s increases and quarks are confined.

A phase transition from a color-neutral hadronic state to a state in which the degrees of freedom are the colored partons, meaning deconfined quarks and gluons, is predicted [10] to occur at energy densities of $\varepsilon \approx 1$ GeV/fm^3 and according to lattice QCD (see Fig. 1.1 for ε increase), can be achieved
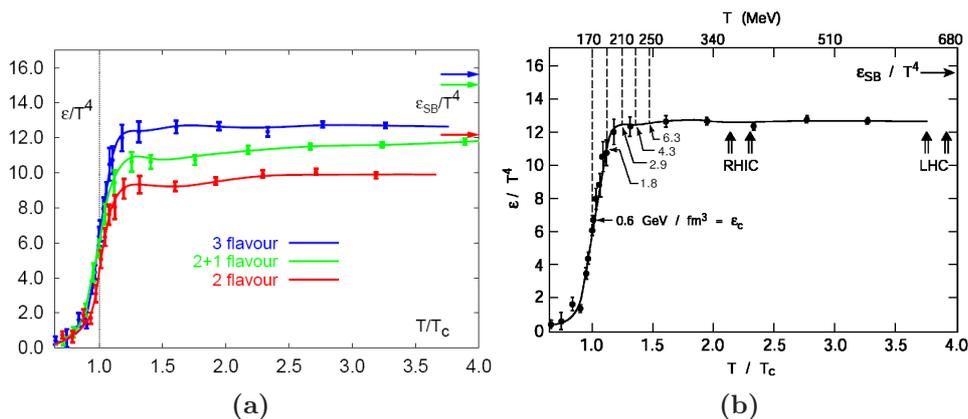
Figure 1.1: The energy density/T^4 as a function of T/T$_c$ in QCD [1].

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at a temperature of $T \approx 170 MeV \approx 10^{12} K$ [11] – the so-called Quark Gluon Plasma (QGP). It is assumed that such state may have existed microseconds after the big-bang and even still exists in neutron stars at densities of 0.6 fm^{-3}. Furthermore, calculations have shown that with disappearing baryon density and the transition to the QGP, chiral symmetry is restored after being spontaneously broken in vacuum due to non-vanishing effective quark masses [11]. In Fig. 1.2, a schematic version of the phase diagram is shown.
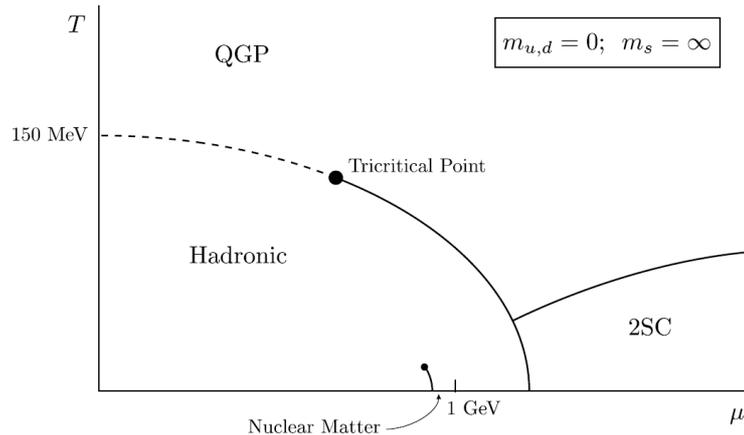
Figure 1.2: Schematic phase diagram of nuclear matter for 2 massless quarks and 1 heavy quark [2].

The Relativistic Heavy Ion Collider (RHIC), which started its operation in 2000, at Brookhaven National Laboratory is the world's first hadron collider consisting of two independent, intersecting rings that can accelerate heavy ions such as from gold to one hundred GeV/c order of the beam momentum with a designed luminosity of about 2×10^{26} cm^{-2}s^{-1}. The ions are accelerated in one ring clockwise, in the other counter-clockwise, and brought to collisions at six ring intersections, hosting the four experiments BRAHMS, PHOBOS, STAR and PHENIX, which have been specifically built to study a QGP with low baryon densities produced in $d + Au$, $Cu + Cu$ or $Au + Au$ collisions at center of mass energies of up to $\sqrt{s_{NN}} = 200$ GeV. As experimental results have shown, this new state of matter with high energy densities of $\langle \varepsilon \rangle \approx 15$ GeV/fm^3 has been achieved [12–15], as reported by each experiment in 2005.

Besides the study of the QGP, RHIC is also capable of colliding polarized $p + p$ at $\sqrt{s_{NN}} = 500$ GeV, which allow studies of the proton spin structure and the contribution of the gluon to the proton spin, and at these high energies allows to produce W bosons and therefore the opportunity to independently probe the $\bar{u}$ and $\bar{d}$ quarks. Nevertheless, throughout this paper we may only concentrate on collisions of gold ions, as these are of primary importance for

QGP studies at RHIC and our related discussions of the detector system we'll be introducing in chapter 2.

1.2   The PHENIX Experiment

As one of the four experiments at RHIC, PHENIX (Pioneering High Energy Nuclear Interaction eXperiment) allows high precision measurements of hadrons, leptons and photons with an excellent mass resolution and represents an advanced detector system, classifiable into three categories:

- **Global Detectors.** The Beam-Beam Counters (BBC), covering $3.1 < \|\eta\| < 3.9$, and Zero-Degree Calorimeters (ZDC) at $\eta \approx \pm 6.9$, provide global parameters as collision vertex position and time, a centrality measurement and serve as event triggers.

- **Central Arms.** The detector systems provide momentum, energy, and particle identification for charged tracks over a large p_T range from 0.2 GeV/c to 20 GeV/c, as well as an energy measurement of photons. The two arms are located at mid-rapidity covering each $\eta < 0.35$ in pseudo-rapidity and $\pi/2$ in azimuth. – Electron identification is realized by the Ring Imaging Čerenkov Counter (RICH) and the energy measured by the Electromagnetic Calorimeter (EMCal) in a match with the momentum determined by the Drift Chambers (DC). Hadrons are tagged via their time of flight and photons via their electromagnetic showers in the EMCal.

- **Muon Arms.**[1] Measurement of muons and decay hadrons. The two arms are at forward rapidity and cover both 2π in azimuth.

The PHENIX experimental setup is shown schematically in Fig. 1.3; the top shows the cross section of the central arms perpendicular to the beam pipe; the bottom also shows the two Muon Arms. A quick summary of rapidity and azimuthal coverage for each subsystem is summarized in Table 1.1.

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[1]Since our primary focus is on the HBD as part of the Central Arm detectors, the Muon Arms will not be explained in more detail; the reader is referred to additional literature [3].
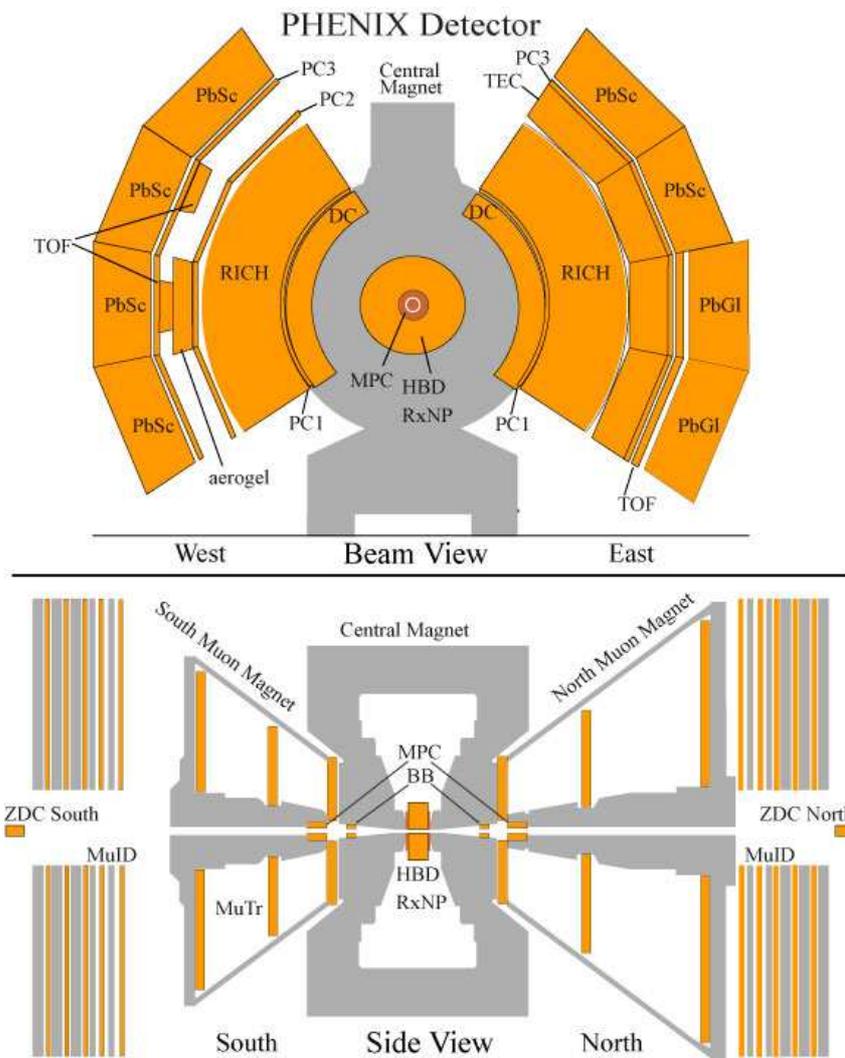
PHENIX Detector

Figure 1.3: Schematic of the PHENIX Detector configuration as of 2009. The cross section of the two central arms perpendicular to the beam pipe (top) and a view from the east with the beam axis along the horizontal direction.

Table 1.1: Summary of PHENIX detector subsystems [7].

Component	$\Delta\eta$	$\Delta\phi$	Purpose & Features
GLOBAL DETECTORS			
Beam-Beam Counters (BBC)	$\pm(3.1 - 3.9)$	2π	Start timing, fast vertex
Zero-deg. Cal. (ZDC)	± 2 mrad	2π	Minimum bias trigger
CENTRAL ARMS			
Central Magnet (CM)	± 0.35	2π	Up to 1.15 Tm
Muon Magnet South (MMS)	-1.1 to -2.2	2π	0.72 Tm for $\eta = 2$
Muon Magnet North (MMN)	1.1 to 2.4	2π	0.72 Tm for $\eta = 2$
Muon Magnet South (MMS)	-1.1 to -2.2	2π	0.72 Tm for $\eta = 2$
Drift Chambers (DC)	± 0.35	$2 \times \pi/2$	$\sigma_m/m = 1\%$ at $m = 1$GeV
Pad Chambers (PC)	± 0.35	$2 \times \pi/2$	Pattern recognition, tracking
Time Expansion Chambers (TEC)	± 0.35	$2\pi 2$	Pattern recognition, dE/dx
Ring Imaging Čerenkov Counter (RICH)	± 0.35	$2 \times \pi/2$	Electron ID
Time of Flight (ToF)	± 0.35	$\pi/4$	Hadron identification, $\sigma < 100$ ps
Lead-Scintillator (PbSc)	± 0.35	$\pi/2 + \pi/4$	Electron & photon ID, energy meas.
Lead-Glass (PbGl)	± 0.35	$\pi/4$	Good $e^\pm/\pi^\pm$ separation
MUON ARMS			
Muon Tracker South	-1.15 to -2.25	2π	Tracking for muons
Muon Tracker North	1.15 to 2.44	2π	–
Muon Identifier South	-1.15 to -2.25	2π	Steel absorber & Iarocci tubes
Muon Identifier North	1.15 to 2.44	2π	for μ/hadron separation

1.2.1 Global and Central Arm Detectors

Let us have a closer look on a few of the most fundamental detector subsystems presently in PHENIX installed.

Beam-Beam Counters. The Beam-Beam Counters (BBC) provide the crucial information of collision time and vertex position, a signal one can trigger data collection on and in collaboration with the ZDC allows to determine the centrality of the collision. There are two BBCs placed ± 144 cm North and South of the center of PHENIX, whereby each consists of 64 hexagonal shaped Quartz Čerenkov counters (see Fig. 1.4, measuring charged particles produced around the beam axis and based on the detection time differences of both, allow to determine collision time/vertex.

(a)   (b)

Figure 1.4: The basic components of the BBC. (a) 64 PMTs are mounted to one BBC unit; (b) each single photomultiplier tube (PMT) with a timing resolution of 50ps is of 25.4mm in diameter and has a 30mm thick Quartz radiator.

Zero Degree Calorimeter. Two Zero Degree Calorimeters[2] (ZDC) are installed 18 m from the center of PHENIX on either side in the direction of the beam pipe and have the purpose to measure spectator neutrons from nucleus-nucleus collisions, which is made possible by utilizing the DX magnet in front to deflect charged particles as spectator protons (see Fig. 1.5). Each ZDC contains tungsten alloy plates of three separate modules, which are read out via one PMT. One can then determine the centrality of the collision by the anti-correlation between energy deposited in the ZDC and total charge deposited in the BBC.

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[2]Each experiment at RHIC has a pair of ZDCs installed.
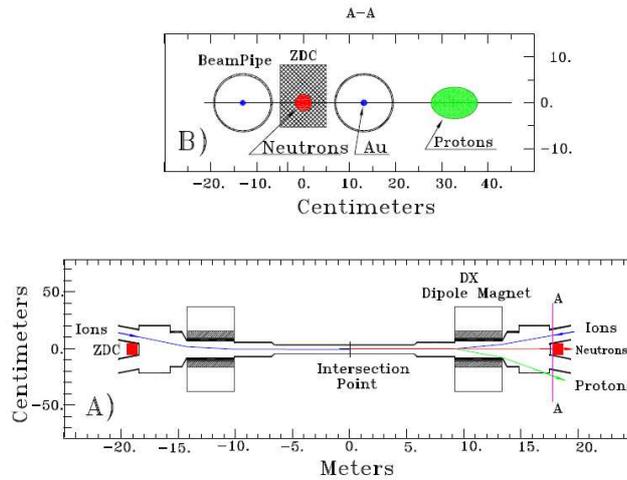
Figure 1.5: Schematic top view of the interaction region (bottom); Projection of proton/neutron deflection in ZDC plane [3].

Central Magnet Due to the bending of charged particles in the magnetic field provided by the Central Magnet (CM), their transverse momentum can be determined. The CM consists of inner and outer Helmholtz coils inside a steel yoke, generating an axially-symmetric magnetic field around the interaction. The two coils can be run either in the same polarity (++), resulting in a total field integral of $\int \boldsymbol{B} d\boldsymbol{l} = 1.5$ Tm in the first 2 m from the vertex, or can be run in opposite polarity (+-) and *achieve a field free region* in the first 50 cm from the vertex, which may allow a detector system in this region to assume straight tracks. The cross-section of the CM together with the Muon magnets and their fields lines in (++) configuration are shown in Fig. 1.6a.

Drift Chambers The main tracking detectors in PHENIX are the Drift Chambers (DC), which are multiwire gaseous chambers and based on the concept that electrons from primary ionization drift towards a wire after a time that is proportional to the distance of the track to the wire. This allows to measure trajectories of charged particles in the $r - \phi$ plane for determination of the particle's momentum and invariant mass of pairs. Each DC arm consists of a cylindrical titanium frame, which support a large net of wires with 42 cm in radial width and 180 cm in length. A basic illustration is shown in Fig. 1.6b.

Pad Chambers The Pad Chambers (PC) measure points in space along straight trajectories of particles, which have left the field-active region, and allow to reconstruct the $\breve{}z$-component of the momentum vector. The PC (see
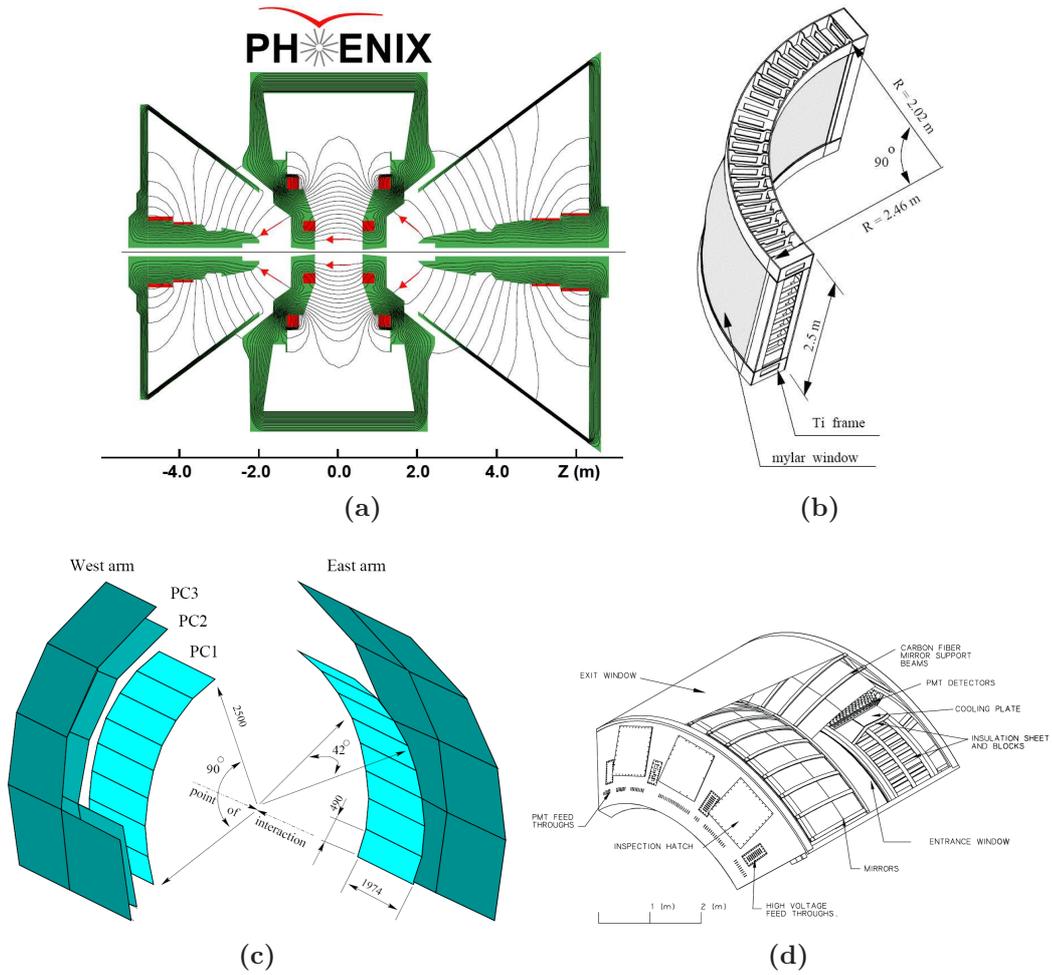
Figure 1.6: Important PHENIX Central Arm detectors. (a) The cross section of the PHENIX Central and Muon Magnets are shown with their field lines in (++) configuration; (b) A Drift Chamber Frame; (c) Illustration of the PHENIX Pad Chambers; (d) A cut-away view of the PHENIX RICH detector.

Fig. 1.6c) contains of three layers of multiwire proportional chambers and are positioned behind the DC (both arms), behind the RICH (west arm) and in front of the EMCal (both arms).

Ring Imaging Čerenkov Counter A Ring Imaging Čerenkov Counter (RICH) is installed in each Central Arm and has the purpose to separate electrons from the large background of charged pions. It contains 48 mirrors, which focus Čerenkov radiation onto two arrays of photomultiplier tubes and uses CO_2 as the radiator gas with an average of 12 photons per ring. A

schematic of the detector is shown in Fig. 1.6d.

Acceptance of Charged Particles Due to the CM field, charged particles are deflected in the azimuthal direction and so making their acceptance depended on the particle's transverse momentum p_T, charge q and effective azimuthal bent to DC, k_{DC} and RICH k_{RICH}, and can be described by:

$$\phi_{\min} \leq \phi_0 + q\frac{k_{\text{DC,RICH}}}{p_T} \leq \phi_{\max}, \tag{1.1}$$

where ϕ_0 represents the particle's emission angle, where $k_{\text{DC}} = 0.206$ rad GeV/c and $k_{\text{RICH}} = 0.309$ rad GeV/c [16].

1.2.2 Low-Mass Dileptons and S/B

Electron-positron pairs or dileptons, have proven to be valuable probes to discover the hot/dense matter formed in relativistic heavy ion collisions at ulta-high energies, and allow to study QGP characteristics as chiral symmetry restoration. As results from the ChErenkov Ring Electron Spectrometer (CERES) at the Super Proton Synchrotron (SPS) at CERN have shown, a large enhancement of the dilepton yield below the ϕ meson mass can be seen. This enhancement may be derived from in-medium modifications of the light vector mesons ρ, ω and ϕ. Since these vector mesons carry the very same quantum numbers as a photon, a coupling to an electron-positron pair can be seen:

$$\pi^+\pi^- \rightarrow \rho \rightarrow \gamma^* \rightarrow e^+e^-. \tag{1.2}$$

Even though collision energies at RHIC are sufficient to study the dielectron continuum, the multiplicity from collisions is so high, hence dN/dy ~ 650, that an enormous combinatorial background is produced and in a mass range of 0.3 - 0.5 GeV/c^2 a signal to backround ration $S/B \sim 1/300$ making it impossible for PHENIX to measure the low-mass pair continuum. This combinatorial background results primarily from uncorrelated pairs formed by tracks from π^0 Dalitz decays and γ conversions:

$$\pi^0 \rightarrow e^+e^-\gamma; \qquad \gamma \rightarrow e^+e^-. \tag{1.3}$$

In order to reduce this background, an upgrade solution had been developed for PHENIX and already installed in 2007 – the *Hadron Blind Detector*. In the following chapter, we shall discuss the principles this new detector system is based on.

Chapter 2

The HBD Detector

The PHENIX detector in its original design has only limited capabilities to measure e^+e^- pairs in the low-mass region due to the overwhelming yield of combinatorial background pairs, as we have already pointed out in Section 1.2.2. The recognition and rejection of these pairs is especially exacerbated by the incomplete azimuthal acceptance of PHENIX, which allows a low momentum electron from a dielectron pair and its spiraling track in the magnetic field to become unrecognized by the Central Arm detectors, while its counterpart contributes to the background through an erroneous or random combination of a detected positron from a separate pair.

A new detector system was developed to overcome this limitation of the PHENIX experiment and serve as an upgrade to the Central Arm detectors right about the collision vertex: the **Hadron Blind Detector** or hereafter referred as the **HBD**.

In this chapter, we introduce the fundamentals of the HBD and its first trial of operation in Run-7 at RHIC. The critical issues of the detector's high voltage (HV) supply as found during this run as well as their subsequential studies are presented. In summary of this initial HBD commissioning, the baseline problem preventing a successful operation is defined to motivate the development of a new *High Voltage Control and Monitoring System* for the HBD, which we outline in conclusion and preparation of its thorough discussion in this thesis.

2.1   Detector Concept

The fundamental idea of the HBD to address the combinatorial background issue in PHENIX is to take advantage of the fact that the opening angle of

pairs derived from γ conversions/π^0-Dalitz decays is considerably smaller than of pairs originating from light vector meson decays. Based upon this important fact, an HBD was designed and shall be discussed in the following.

2.1.1 Design and Implementation

By operating the PHENIX Central Magnets in $(+ -)$ configuration, an almost *field-free cylindrical volume*[1] is established, extending radially out to $\sim 50-60$ cm from the beam axis. This permits the preservation of straight particle trajectories and the corresponding opening angles of pairs within this region. Therefore, the HBD has been designed to fit into this beneficial environment surrounding the collision vertex. The detector consists of two identical semi-circular arms, referred to as *East* and *West* arm, with an active spacial coverage of radially $\sim$ 5cm (outside walls of beam pipe) to $\sim$ 55cm (before inner coil) with respect to the beam axis. The layout for the HBD installation in PHENIX with the location of the coils is illustrated in Fig. 2.1.
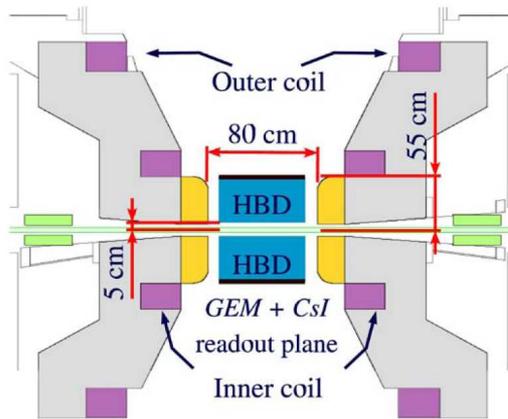
Figure 2.1: Location of the HBD and inner/outer coils in PHENIX.

Herewith, the baseline conditions are given to identify electrons from π^0-Dalitz decays and photon conversions by exploiting their small opening angle. The question of how to achieve this goal has been extensively studied in Monte Carlo simulations in [17] with different detector configurations and the aim of achieving a $S/B = 10/1$ or higher at the ϕ mass, which would represent a reduction of the combinatorial background of about two orders of magnitude. The results show an electron identification with an efficiency of $> 90\%$, a double hit recognition of background pairs on a single pad at a similar level

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[1]The compensation of the existent field allows only the integral of the magnetic field to be almost completely zero, but does not eliminate field components of non-zero value.

and a reasonable π rejection factor of ~ 100. Such a detector cannot be realized by only applying an opening angle cut to the collected data (e.g. 200 mrad), since many different particles are present. Therefore, the HBD needs to be capable of measuring Čerenkov photons produced in the gas volume of the detector.

Several potential key elements of this new detector system were considered and analyzed. The following final design has been adopted: a proximity-focused windowless Čerenkov detector with pure CF_4 as *radiator and detector gas*, utilizing triple-stacks of *Gas Electron Multiplier* (GEM) foils with a photocathode coated on the uppermost GEM as well as ~ 6.5 cm^2 hexagonal readout pads for charge collection.

As illustrated in Fig. 2.2, each arm consists of 2 large front and 8 small back panels made of layers of FR4/Honeycomb/FR4 (250μm/19mm/250μm), glued to a rigid FR4 frame, while the two side panels are mounted with plastic screws. The outer panels serve the detector with gas and high voltage (HV). There are two HV dividers mounted on either side with the capability of supplying voltage to 3 GEM detectors through corresponding HV terminals on the inside. The 5 inner panels are each equipped with 2 Triple-GEM detectors with an underlying readout plane consisting of 96 pads, which are connected to Front End Electronics (FEE) boards on the outer surface of the

(a) Exploded HBD Arm   **(b)** 3D layout of HBD
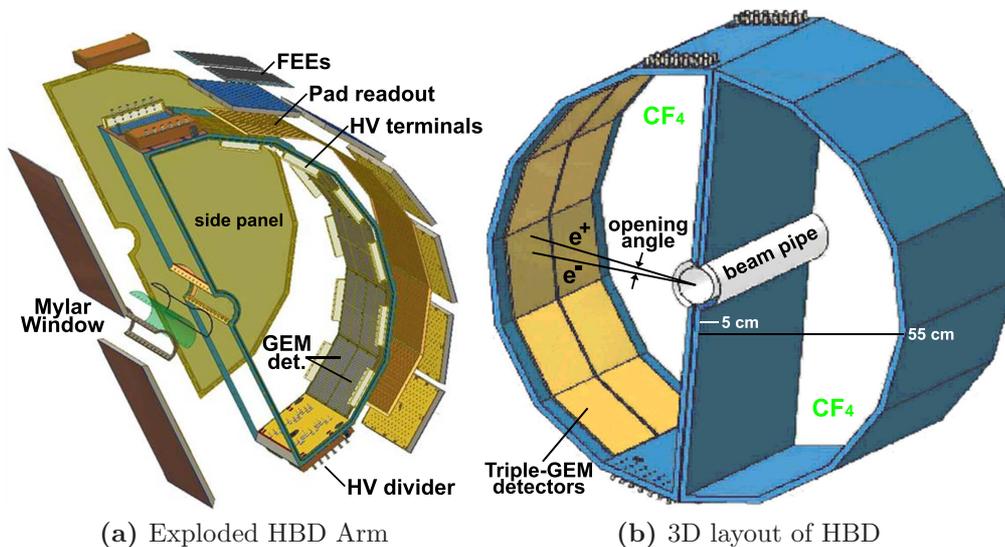
Figure 2.2: HBD Design Overview. In (a) an exploded view of one HBD arm with one side panel for clarity removed is shown with its installation around the beam pipe in (b).

detector. Each FEE consists of differential pre-amplifiers for each pad and Flash Analog-Digital Converters (ADC), which are accessed by the PHENIX Data Acquisition (DAQ) system during a so-called run of data taking[2].

For a more detailled understanding of the HBD principles, the key elements, such as the photocathode, radiator/detector gas, and GEM foils as well as the detailled method of identifying electrons with this detector scheme are discussed in the following sections.

2.1.2 Photocathode and Gas

Instead of focusing mirrors as in a RICH detector, which due to geometrical constraints in PHENIX would be impossible to implement within the field-free region, a UV light sensitive detector shall be placed in the path of particles produced in collisions. Therefore, the Čerenkov photons screening the detector form a circular blob image ($r_{\text{blob}} \sim 1.15$ cm) rather than a ring when using a mirror. Extensive studies in [4, 18] have shown, utilizing *CsI* as a film photocathode permits an absolute quantum efficiency of about 80% in the extreme ultra-violet (see Fig. 2.3a).

In order to allow the HBD a radiation budget $< 3\%$ of the radiation length, a separation of radiator and amplification media is unfavorable, since the window in between would serve as an auxiliary source of Čerenkov light and increase the radiation length. Therefore, in addition to the benefit of being sensitive to the full Čerenkov spectrum, a windowless configuration was adopted.

The choice of radiator and detector gas for the HBD has been one of the primary focuses of evaluation in the very early days of the HBD's conceptional design. Attention was focused on industrially produced *carbon tetrafluoride* (CF_4; see Fig. 2.3b). Due to fluorine ($1s^2$, $2s^2$, $1p^5$), having the smallest atomic radius of the period 2 elements and being the most electronegative element in the periodic table, its bound with carbon (C-F bond) is extremely strong, 105.4 kcal mol^{-1}, and highly polarized, with the electron density substantially on the fluorine atom. This statement arises from the significant electrostatic attraction between $F^{\delta-}$ and $C^{\delta+}$, instead of the classical covalent bond-sharing of electrons. Important for our study, however, is that the 2p electrons are held more closely by the nuclear charge (endothermic, -401.2 kcal mol^{-1}) than for example for oxygen (-312.9 kcal mol^{-1}), making it extremely difficult and

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[2]A "DAQ run" or the mode of "data taking" in this paper, shall be referred to the readout process of the HBD pads and storage of event data during ongoing collisions at RHIC.

(a) CsI Quantum Efficiency **(b)** CF$_4$ Molecule
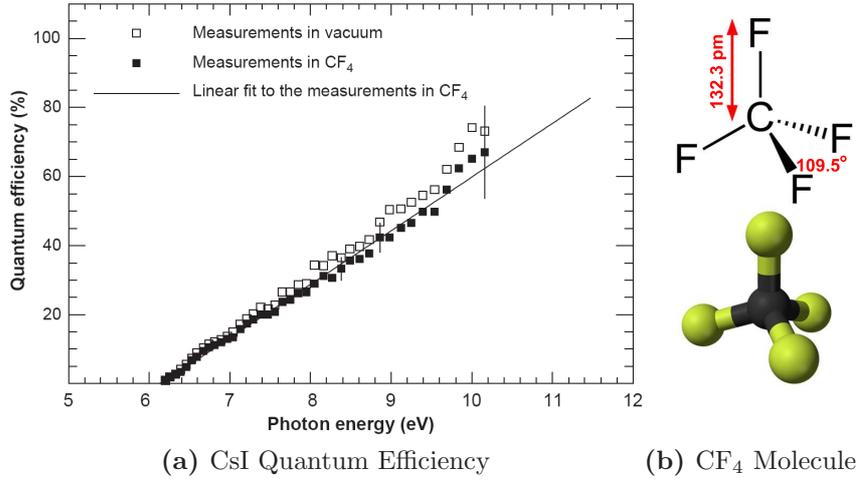
Figure 2.3: Absolute CsI Quantum Efficiency measurement in vacuum and CF$_4$ (a; [4]), and a model of the CF$_4$ molecule in (b).

very much E-field dependent to generate an electron-F$^+$ pair; [19]. Thus one can benefit from the unique opportunity with CF$_4$ as radiator and detector gas to take control over the detector's gain stability through the appropriate application of high voltage.

Another crucial factor is the transparency to Čerenkov photons of wavelengths < 108nm that allows the detector to exploit the high quantum efficiency of the CsI cathode in the deep VUV wavelength region. One can estimate the refractive index of CF$_4$ by either using each individual atomic index or measure the Gladstone-Dale constant with, for example, a Twyman-Green interferometer and He-Ne laser of known 633nm wavelength, and finds an excellent high refraction index[3] of $(n - 1) = 620 \times 10^{-6}$, making pure CF$_4$ suitable for a high level of Čerenkov light production and considerable for the HBD. As a consequence of the very large bandwith from $\sim$ 6eV (CsI threshold) to $\sim$ 11.5eV (CF$_4$ cut-off), single electrons transversing $\sim$ 50cm of the CF$_4$ in the HBD, radiate Čerenkov photons, which produce $\sim$ 35 primary photoelectrons through the Photo-electric Effect on the CsI, and therefore yield a large figure of merit $N_0 \approx 822$ cm^{-1}.

2.1.3 Gas Electron Multipliers

The fundamental challenge one faces is to design the HBD such that it can be sensitive to a very small amount of extracted photoelectrons from the CsI

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[3]The refraction index depends on the photon energy.

cathode, but be insensitive to electrons originating from ionization trails of charged hadron tracks. The difference between the two sources is that photoelectrons only appear close to the surface of the CsI film, while ionization electrons are spread throughout the gas medium. As originally proposed in [20], one can amplify localized primary charge from the photocathode by employing a parallel plate detector; Čerenkov light passes through a transparent Anode grid, creates photoelectrons on a photocathode beneath, which are then extracted, amplified and collected by the Anode. Such a detector has only one major issue: photons emitted during the amplification of photoelectrons shine back to the photocathode and therefore distort the measurement. This difficulty has been overcome by utilizing the *Gas Electron Multiplier*, hereafter referred as a **GEM** foil [21], since a strong suppression of photon-feedback is automatically given by its geometry, as discussed below.

A GEM consists of a thin, metal-clad polymer foil with a high density of chemically etched equidistant narrow holes. Commonly, Kapton and Cu are used as insulator and top/bottom metal layers, respectively. As manufactured at CERN, the hole pattern is first engraved on both sides applying photolithography, before the polymer is dissolved with a solvent equally. This procedure causes a slight double-conical shape of the holes as shown in a microscopic view of a GEM foil in Fig. 2.4a. Each foil has an equilateral triangular hole pattern at a pitch of 140μm (center-to-center) and an inner hole diameter of $\sim 50\mu$m in the Kapton and an outer hole diameter of $\sim 70\mu$m in the Cu.

The principle of a GEM is based on *electron avalanche multiplication* in strong electric fields produced by application of a potential difference between

(a) GEM foil   **(b)** *E*-field
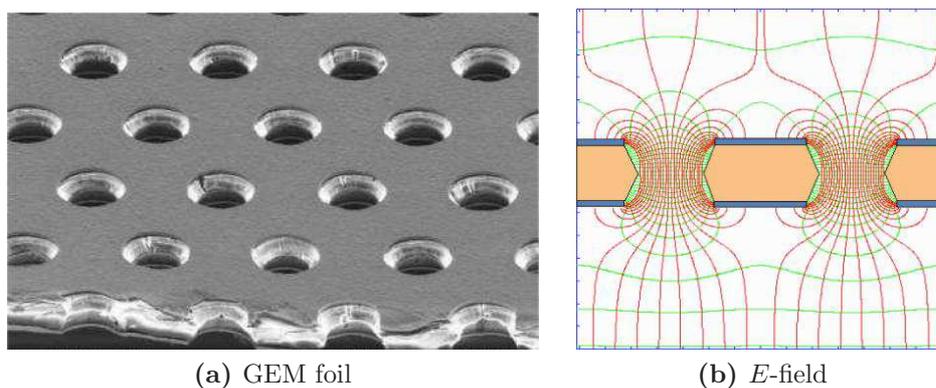
Figure 2.4: A Microscopic view of a GEM is shown in (a) and electric field lines of increased density within holes is illustrated in (b) when a voltage to the electrodes is applied.

the two conducting sides inside the holes. Each individual hole represents a proportional amplifier: electrons close to the GEM surface drift into the holes, multiply in avalanche and transfer into the next region. Since the electrodes are electrically separated from the charge collection pads, the pattern design for the readout unit can be chosen very flexible. One may also cascade several foils to achieve *higher gains* and a more *stable operation* as studied in [22, 23].

With the objectives of the HBD, the above principle has been customized and extended. All GEM foils cover an active area of $27 \times 23 \text{cm}^2$ and are segmented into so-called 28 **strips** with each 27cm in length, 8.1mm in width and separated by a 1 mm thin Kapton line from its neighboring strip. Every top electrode of a strip is soldered to a current-limiting **20MΩ segmentation resistor** to a **foil-wide top electrode** or **Top HV bus**. This segmentation reduces the stored energy during a discharge, meaning a spark from top to bottom electrode, and this way prevents severe damages to the GEM. The bottom electrode of each strip, on the other hand, is directly connected to a **foil-wide bottom electrode**. An image of an HBD GEM foil is shown in Fig. 2.5a.

Furthermore, one GEM foil is converted into a semi-reflective photocathode by evaporating a ~ 300 nm layer of CsI onto its top surface. In order to prevent a chemical reaction with the Cu, a thin layer of Au with another layer of Ni for a good gold-adhesion is coated on the surface. As demonstrated in [4], photoelectrons extracted from the CsI cathode are pulled into the nearest hole by a strong electric field (see Fig. 2.4b), which is to the order of 100kV/cm at the center of the hole, and responsible for the avalanche process. Two uncoated GEM foils are cascaded below to build a so-called **triple-GEM stack** with equidistant 1.5 mm gaps in-between, before the total charge is collected by hexagonal pads. In order to allow the construction of a stack with Mesh and prevent any warping of GEM surfaces, a FR4 frame stretches each GEM foil and with a 0.3 mm wide support across, maintains a constant gap between the GEMs. The primary elements of the stack shall be called **Top GEM** or *T-GEM*, **Middle GEM** or *M-GEM* and **Bottom GEM** or *B-GEM*. The entire GEM detector module is illustrated in Fig. 2.5b. The connection of every HV bus from GEMs in triple-stack configuration to a divider is discussed in Section 2.2.1.

Facing the detector's gas volume, meaning towards the collision vertex, a stainless steel **Mesh** of $\sim 90\%$ transparency is placed 1.5 mm above the photocathode and helps to establish a drift field, which drifts ionization electrons from hadrons or in general **minimum ionizing particles** (MIP) towards the Mesh, meaning away from the GEM holes, when biased by a slightly positive

(a) HBD GEM   **(b)** GEM Detector
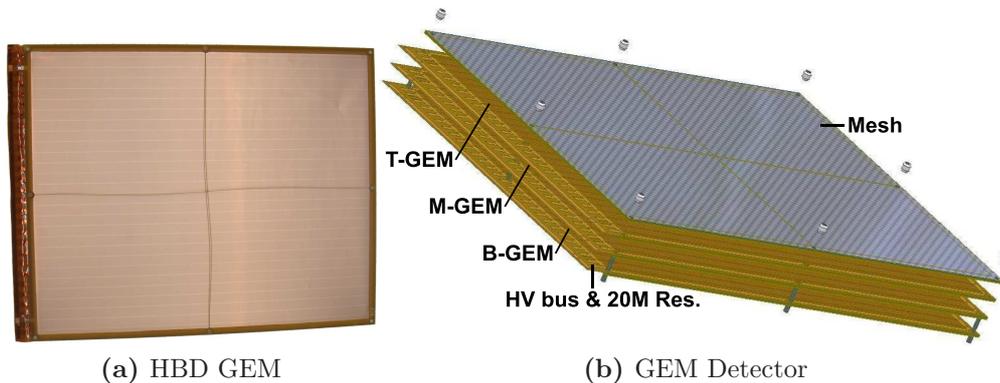
Figure 2.5: A photograph of an HBD-sized GEM foil is shown in (a) and in (b) a Triple-GEM stack with Mesh is illustrated.

voltage with respect to the top electrode of the GEM beneath. Such configuration finally empowers the HBD to be mostly insensitive to signals from charged hadrons / MIPs or to be *hadron-blind*!

2.1.4 Electron Identification Principle

In summary of the previous sections, we may now define the basics of HBD operation through high voltage (HV) application and introduce some of the conventional expressions we will be using throughout this thesis.

As originally proposed in [23], the gap between the Mesh and T-GEM is called "**drift**" with field E_{D}; the gap between GEMs are called "**transfer**" with fields E_{T}; and the gap between B-GEM and the pad readout (ground) is called "**induction**" with field E_{I}. The height of all gaps is fixed to 1.5 mm by the GEM foil's frame. The potential difference between the Mesh and the top electrode of the T-GEM (coated with CsI), is commonly referred to as the delta of their applied voltage and abbreviated with **dV**. In other words, one can express the dV by subtracting the magnitude of the Mesh potential with the magnitude of the T-GEM potential. A detailed calculation of fields and the dV is given in Section 3.2.1.

The HBD can be operated in two modes, which are defined by the configuration of E_{D}: the **Reverse Bias** (RB) or **Forward Bias** (FB) mode. In Fig. 2.6, the principle of each is illustrated. In Forward Bias mode, the Mesh electrode is biased with a *positive dV* such that charge produced by a traversing MIP within the drift gap is collected towards the GEM and amplified in
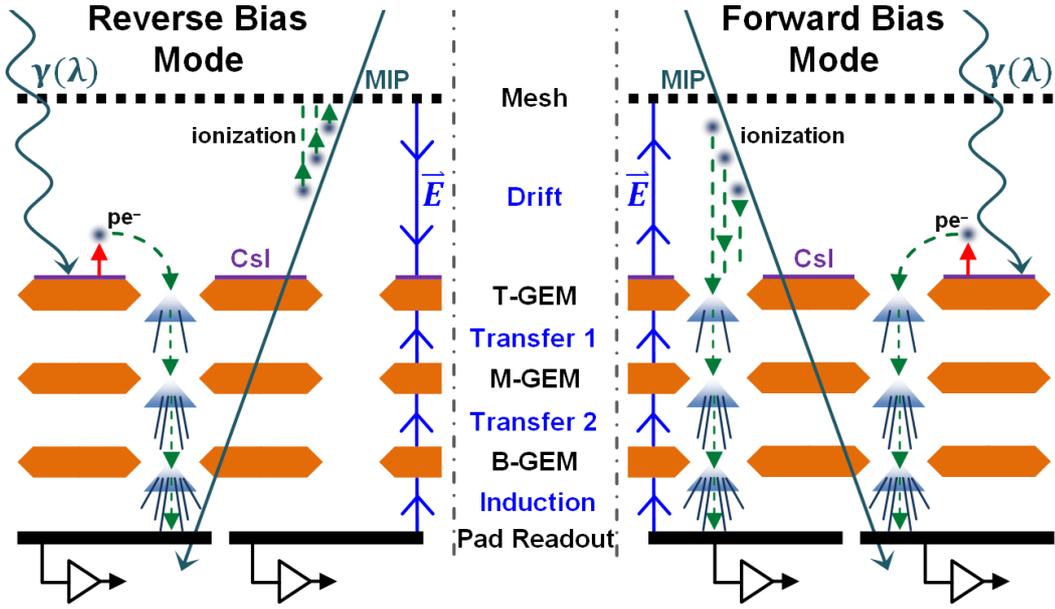
Figure 2.6: The basic principle of Reverse and Forward Bias operation of the HBD; the response to Čerenkov photons and MIPs to either mode is illustrated. The dashed arrows in red represent the photoelectron extraction from the CsI cathode, while arrows in green represent the transport of photoelectrons or/and ionization charge. The direction of the electric field lines within the gaps is displayed with blue arrows.

avalanche of the three gain stages of the triple-GEM stack. A Čerenkov photon produces a photoelectron (pe⁻) in the CsI surface of the T-GEM and is extracted and transferred into a nearby hole, where it undergoes the amplification process. The total charge is then collected on the readout plane. The overall signal one can plot in a pulse-height spectra thus represents a combination of amplified photoelectron and MIP charge, where the latter signal contribution is overwhelming and generates a background preventing the identification of Čerenkov blobs due to electrons. The novelty of the HBD is found by running it in its characteristic mode of reversed E_D, the Reverse Bias mode. It is defined by the Mesh electrode biased with a slight *negative dV* such that most of the MIP produced charge in the drift gap is collected by the Mesh, while the strong GEM field close to the CsI surface still allows photoelectrons to be collected and amplified.

As recent simulations in [5] have shown, electrons within a volume defined approx. 150μm above the T-GEM surface – meaning photoelectrons <u>and</u> ionization charge – are transferred into the GEM holes and therefore contribute to the final signal. This also means that about 90% of the ionization charge

(a) Charge Collection   **(b)** pe Efficiency
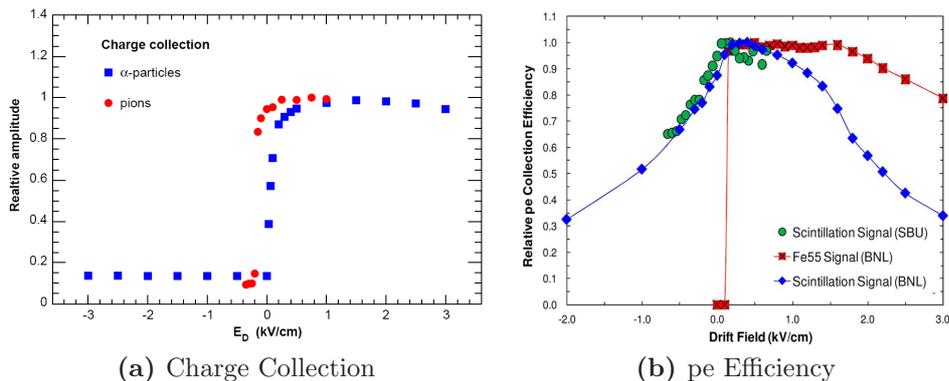
Figure 2.7: Collection of ionization charge (a; [4]) and relative photoelectron collection efficiency (b; [5]) vs. the drift field.

deposited by hadrons in the drift gap is swept away towards the Mesh.

Early experiments with α-particles and 1 GeV/c pions at KEK (High Energy Accelerator Research Organization, Japan) have proven a significant decrease of collected ionization charge when switching from FB to RB mode within an E_D of ~ 0.1 kV/cm (see Fig. 2.7a). One can find an optimal *photoelectron (pe) collection efficiency* as a function of the field in the drift gap, which is defined as the ratio of the number of photoelectrons collected and amplified by the GEM to the number of photoelectrons produced for a given quantum efficiency of the CsI photocathode. Experimental results of this characteristic property, as shown in Fig. 2.7b, shall emphasize the importance of setting the drift field with respect to its defining sensitivity to photons and insensitivity to MIPs. This however also means that the HV System powering this GEM detector needs to be capable of precisely generating such E_D-field in order to allow a maximal suppression of the MIP signals, or simply speaking, allowing the Hadron Blind Detector to be hadron blind.

In the analysis of data taken in RB mode, one can use the RICH and EM-Cal to identify electrons in an event, reconstruct their track with the Drift Chamber, and find pads of single and double hits by studying the measured amplitudes for each pad. Simulations have shown that a MIP of high momentum may produce ~ 1 Čerenkov photoelectron[4] and a single primary electron produces ~ 36 photoelectrons. Thus dilepton pairs from γ conversions and π^0 Dalitz decays can be distinguished due to their small opening angle from

---

[4]The threshold for photon production by hadrons $m/\sqrt{2(n-1)}$ depends on their mass m and refractive index n of CF_4. Due to a Čerenkov γ-threshold of ~ 28.3 in CF_4, pions with a momentum below 4 GeV will not contribute with photons illuminating the CsI cathode.

twice the number of photoelectrons produced by the single hits from light vector mesons.

2.1.5 Correlation of P/T and Module Gain

The quantities of pressure and temperature are known to have significant impact on the operational characteristics of any gaseous detector, especially for the HBD. Let us quickly review the governing fundamentals of this fact.

One can utilize the basic principles of classical kinetic theory of gases to estimate drift and diffusion properties of electrons in a gaseous medium at temperature T. Assuming the absence of any external force, electron motion can be expressed with a Maxwellian energy distribution, as shown by Boltzmann and Langevin, where an average thermal energy of $\varepsilon_{\mathrm{T}} = 3_2^/ kT \simeq 0.04$ eV at room temperature. Under the application of an electric field E, however, we know that, except for very low fields, the mobility of electrons is not constant and their energy can increase substantially between collisions with the gas molecules; due to Townsend, one can find the electron mobility μ to be

$$\mu = \underbrace{\frac{3\sqrt{3\pi}}{8\sqrt{2}}\sqrt{\frac{m+M}{M}}}_{X}\frac{e\lambda M^{1/2}}{m\sqrt{3kT}} = X\frac{e}{m}\left\langle\frac{\lambda}{c}\right\rangle \simeq \frac{e}{m}\tau, \qquad (2.1)$$

where e denotes the electron charge, m its mass, M the mass of a molecule, k the Boltzmann constant, λ and c are the electron's mean free path and RMS velocity, respectively, and τ the mean time between collisions. The factor X, as originally found by Langevin, can be approximated to its multiplying constant of 0.815, when one accounts for the fact that m is very small compared with M. As found by Boltzmann, $c = 1.086\ \bar{v}$, which by substitution of $\bar{v}$ for c changes X to 0.75 and $\mu \simeq e\lambda/m\bar{v}$. Since λ varies inversely as the gas pressure P and the electron energy, and therefore v, is a function of the reduced field E/P, the *electron mobility is thus a function of P* as 2.1 indicates.

Although all the above obtained relations hold, one needs to be careful when neglecting the factor X and building a theoretical model on a 'purely' Maxwellian distribution. When transforming Boltzmann's equation by a method of Hilbert, and deducing a series of coupled transport and energy conservation equations by expanding in Legendre polynomials,

$$f(\varepsilon,\phi) = \sum_{j=0}^{\infty} f_j(\varepsilon)P_j(\eta), \qquad (2.2)$$

with $\varepsilon = \|\boldsymbol{p}^2/2m\|$ and $\eta = \cos\phi$ representing the angle ϕ between v and $\boldsymbol{a} = e\boldsymbol{E}/m$, one can find for f_0, considering $m/M \ll 1$ for electrons:

$$(x + z)f_0'' + (2 + x + b/x)f_0' + 2f_0 = 0, \qquad (2.3)$$

where

$$x = \varepsilon/kT, \; z = \frac{1}{3}(eE\lambda)^2 (2m/M)(kT)^2. \qquad (2.4)$$

The solution for the first term $f_0 = (x + z)^z e^{-x}$, which has been solved by Pidduck (1916), shows that electrons do not acquire exactly a Maxwellian distribution of velocities, and in fact leads to a 11% increase of the numerical factor X in 2.1. Additionally, already at this stage, many assumptions were made: (i) the frequency ν of an electron-molecule collision depends linearly on the thermal velocity v_{T} of an electron; (ii) $\nu \approx \nu_e$, meaning the elastic collision frequency ν_e is expected to be much larger than the inelastic ν_{in}; (iii) the concentration of free electrons in the gas medium is assumed to be very small; (iv) only a constant and uniform electric field $\boldsymbol{E}$ is considered; the distribution function is neither (v) spatial nor (vi) time dependent; and since $m/M \ll 1$, (vii) only the first two terms are calculated. Unfortunately, Pidduck's solution remained unseen for a very long time, until independently rediscovered by Druyvesteyn, which then induced the development of electron transport theory by Compton, Davydov, Morse *el al.* (1935), Frost and Phelps (1962), and many others. However, even today, more than a century since Boltzmann's equilibrium, and various solutions for (i - vi), the limitation of (vii) remains only partially solved with a truncation after $j = 3$. Nevertheless, for our experimental study, the boundaries of measurable precision given by the current state of technological progress, and final understanding and reasoning for the related P/T subsystem of HVC, we may reduce our discussion to the combination of achievements by Pidduck ($T \neq 0$), Davydov and Morse ($\nu = \nu(v)$):

$$
\begin{aligned}
f_0(v) &= C \exp\left(-m \int_0^v \mathrm{d}v \frac{v}{kt + Ma^2/3\,(\nu_0 - \nu_1)^2}\right), \qquad (2.5) \\
f_1(v) &= -\frac{a}{\nu_0 - \nu_1} \frac{\mathrm{d}f_0}{\mathrm{d}v},
\end{aligned}
$$

where a normalizing constant $C \ll 1$ is introduced, and energy transfers in processes as rotational and vibrational excitations with molecules accommodated. What one shall for our purposes only deduce from 2.5 is that the number of free electrons capable of ionizing and exciting increases with the strength of the applied E-field, which one can for simplicity see when allowing

λ to be independent of v:

$$f \propto C \exp\left(-\frac{\varepsilon^2}{e^2 E^2 \lambda^2}\right), \tag{2.6}$$

where ε is the energy of the excitation/ionization. The mean free path λ can then be obtained from the first Townsend coefficient α, meaning the number of electron-ion pair created per unit length of drift:

$$\alpha = \lambda^{-1} = \frac{\sigma(\varepsilon)}{k}\frac{P}{T} \simeq 2.69 \times 10^{19} \frac{P}{760}\frac{273}{T}\sigma(\varepsilon) \text{ cm}^{-3}, \tag{2.7}$$

where the mobility of electrons standardized to 760 Torr and 0℃. The numerical term has been retrieved from a drift chamber performance study at CERN and is given to the reader for dimensional interest. Based on different molecular cross-sections at higher electron energies, in some gases, the collision cross-section $\sigma(\varepsilon)$ and so τ varies significantly along with E (Ramsauer). As a consequence, drift velocities and diffusion behavior can significantly differ for various gases at certain values of field and P/T. This means that depending on the chosen detector gas, for which one can use the corresponding Ramsauer curve to deduce $\sigma(\varepsilon)$, the detector performance may vary tremendously and affect the gain: The number of secondary electrons produced due to ionization by a primary electron transversing the gas over a total average distance of $s = \mu E/\alpha\bar{v}$, before neutralizing with a positive ion of the medium, is proportional to the gain G, and can be found as

$$G = A \exp\left(B \int \alpha(s)ds\right) \propto \exp\left(\frac{P}{T}\right), \tag{2.8}$$

where A and B are free variables. Since a change in P/T results in a corresponding exponential variation in gain, this has an even more significant impact for the HBD performance, as a triple-GEM configuration has to be taken into account:

$$G_{\text{HBD}} \propto \exp\left(\frac{P}{T}\right)^3. \tag{2.9}$$

This concludes a systematic introduction of the problem we are facing. A detailled approach to this issue is presented in Section 3.4.8.

2.2 Commissioning in Run-7

The HBD was installed in PHENIX for its first run in 2007. Due to severe issues of the detector's HV Control system and resulting damage making the detector difficult to operate, Run-7 served as an unexpected "engineering run." Only a few weeks after the beginning of the run, the West arm of the HBD had been dismounted for inspection and a study of possible problem sources.

In this section, we will have a look at how the detector was operated at this time and discuss the critical points, incl. the experience we've gathered, and deficits of the Run-7 HV system.

2.2.1 Detector Operation

The triple-GEM stacks were powered through a resistor chain consisting of three branches and one common HV supply. In case a discharge in one of the GEMs occurs, the voltage across the other GEMs is not affected, rather than in the case of a single-branch divider, where one can expect a significant voltage increase causing multiple discharges and severe damages to the GEMs.
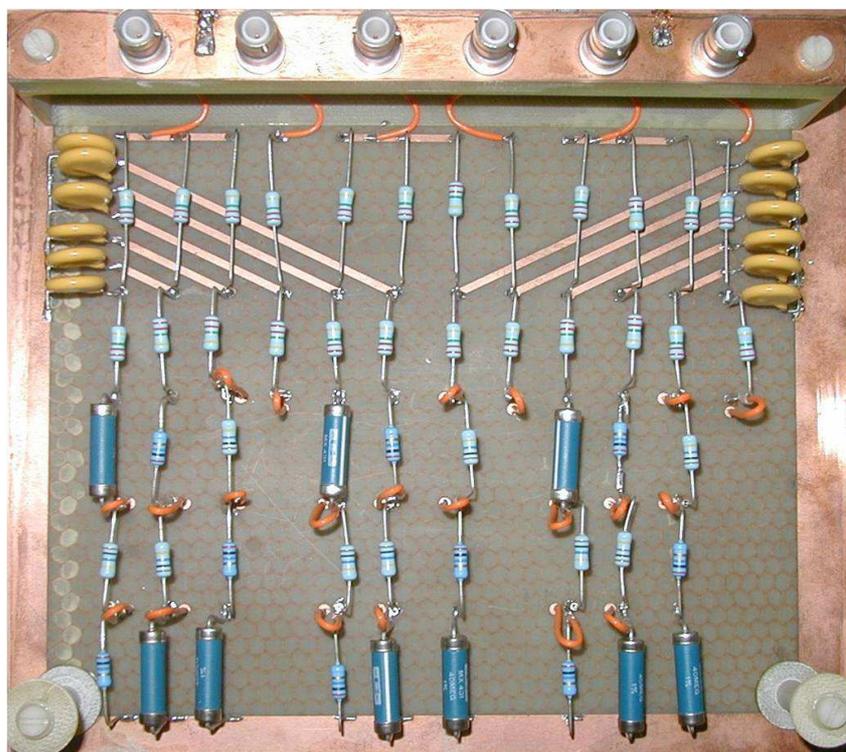
Figure 2.8: Run-7 HBD Resistor Chain

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A schematic of the Run-7 resistor chain is shown in Fig. 2.9. The top and bottom HV bus of each GEM foil is connected to one branch with a 10MΩ resistor across the foil. All branches have the same total resistance of 74.4MΩ and a filter capacitor on their HV input. The Mesh is powered by a separate HV supply and also has a bleeder resistor and filter capacitor to ground. Three resistor chains have been combined on one board and mounted on either side of both HBD arms. In Fig. 2.8, the actual board can be seen.
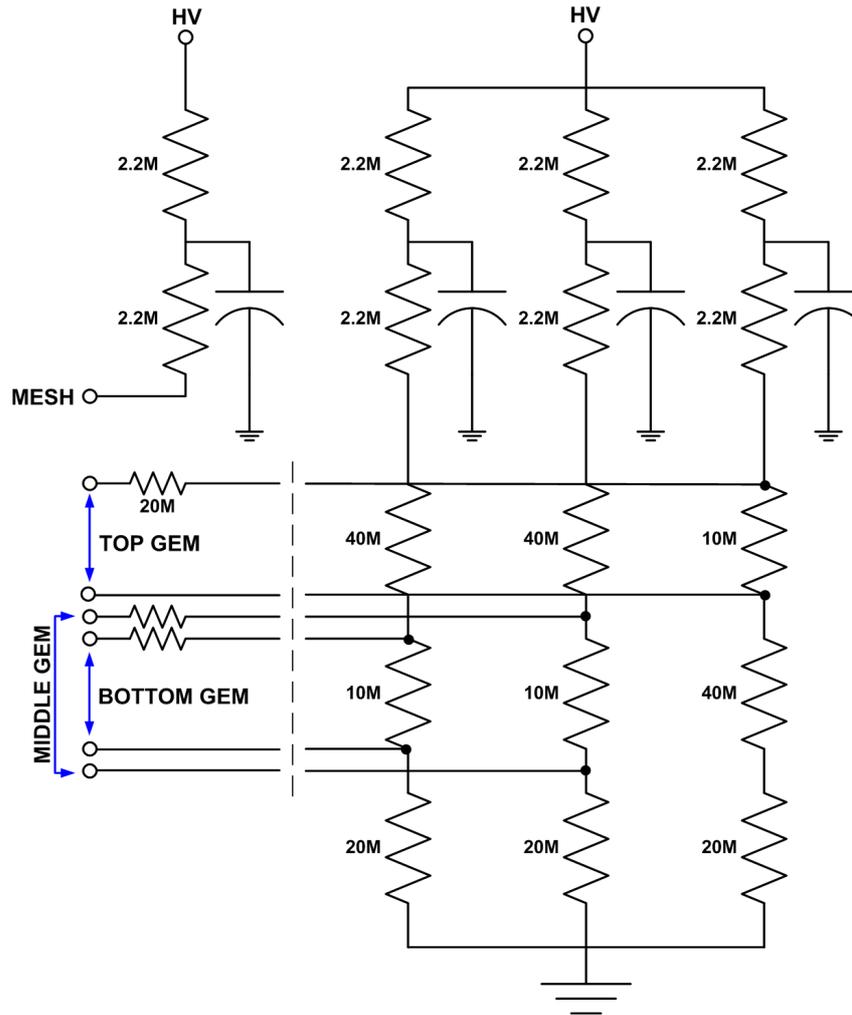
Figure 2.9: Schematic of Run-7 HBD Resistor Chain

The detector has been powered with LeCroy 1471N HV modules, serving four GEM detectors per HV board. The control software, written in Perl, established communication to the HV modules inside the Interaction Region

(IR) of PHENIX and sent demand voltages to these boards. The HV module would then bring up the HV on the GEMs and the corresponding Mesh through their resistor chain.

The overall powering scheme of the detector, summarized in functional blocks is given in Fig. 2.10.
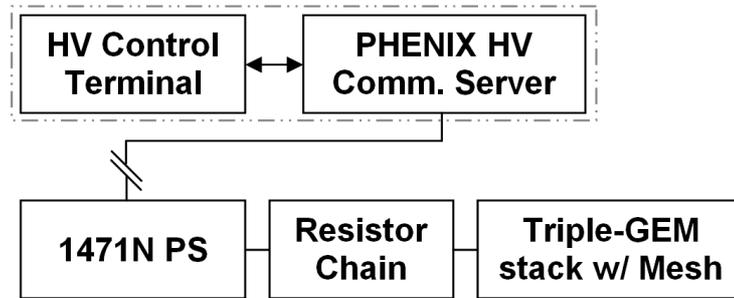
Figure 2.10: Run-7 HV Control and powering scheme

2.2.2 Performance Issues

The control system configured the 1471N such that when a small current draw in the GEM-stack is detected, e.g. through micro-sparks, it would initiate a so-called hardware-based *trip*, which instantly deactivates HV generation of the GEM channel, while the Mesh channel is still at full operational voltage (e.g. 4000V). As a result, the dV between Mesh and Top GEM increased

(a) GEM zoom 1   (b) GEM zoom 2
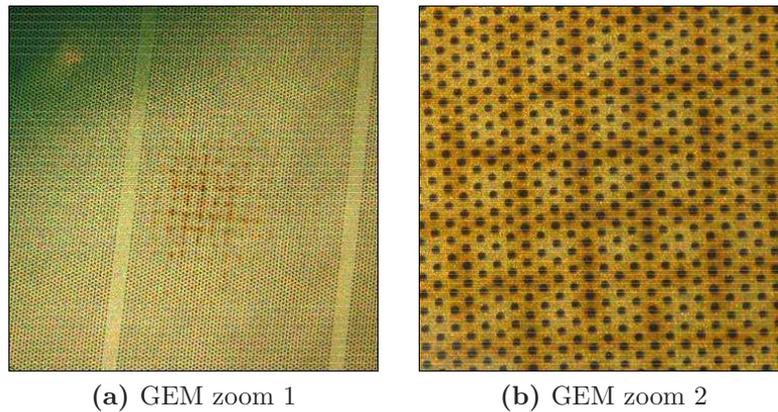
Figure 2.11: Damaged Top GEM foil from Run-7. The burned grid pattern is clearly visible.

rapidly up to the Mesh voltage, caused a large spark and damaged the GEM, before the LeCroy finally tripped the Mesh channel. Due to optical coupling, it is thought that this spark also initiated trips in other stacks simultaneously, which then also suffered from the same dV problem.

Another issue was the installation of filter capacitors in the resistor chain, especially with the bleeder resistor on the Mesh. Every time the 1471N tripped a channel, the stored energy dissipated and contributed to the discharges in the stack. Additionally, a firmware problem of the LeCroy caused stored energy in its filter capacitors on the HV output to also dissipate through the detector milliseconds after a trip was initiated.

Overall, a considerable fraction of the GEM foils were severely damaged and prevented to bring the HBD up to operational voltages in order to allow the detector to take data. The damaged Top GEM foil of Fig. 2.11 clearly indicates a burned grid pattern from the Mesh.

The HV Control software caused further instabilities, e.g. through dead loops in the code following a system crash or one-by-one transmissions to the PHENIX HV communication server resulting in an enormous load on the server and inappropriate traffic conditions. Furthermore, the reconstruction of trips has been extremely difficult as only a data logging system of HV parameters with a low sampling rate existed.

2.3 Upgrade Strategy for Run-9

The motivation for a new HV Control system for the HBD was well demonstrated by the experience outlined above. The previous system did not allow the HBD to perform the measurements it was built to take, but instead may have contributed to the detector's severe damage.

2.3.1 HV Upgrade Requirements

The new HV system needs to address the following key issues of the Run-7 system:

- dV between Mesh and Top GEM exceeds acceptable value during a trip condition;

- Stored Energy in filter capacitors of resistor chain contributes to energy in discharges in stack;

- Trip conditions of the 1471N lead to stored energy in the HV output filter capacitors that can only dissipate through the detector;

- Lack of calibration functions for true output voltage of the 1471N;

- Instabilities in module gain due to P/T fluctuations;

- The software control causes instabilities on hardware and software level due to the lack of control structures in the code and its conceptional design;

- Inadequate logging system of HV (control) parameters.

Besides solving these basic key concerns from Run-7, the new system shall further allow optimal control over the detector for maximal performance.

2.3.2   System Design Overview

The HBD *HV Control and Monitoring System* (HVC) introduces three fundamental components to the control scheme of Run-7:

- New Resistor Chain, with the goal to minimize the amount of stored energy, synchronize the decay time of GEM and Mesh channel at the event of a hardware-based trip and optimize the achievable gain without the need to increase the chain's input voltage.

- 1471N Phase Detector and Relay Board, with the goal to monitor the voltage generation directly on the power supply board and ground the GEM-stack and Mesh channel simultaneously, if either one appears to have a trip issued by the LeCroy.

- HV HBD Control Server and Client, with the goal to allow intelligent, stable, high-efficient, precision control of the detector and the dynamic self-improvement of control functions, if deemed necessary.

A general schematic of the powering scheme of HVC is presented in Fig. 2.12. – This thesis will focus on the design and development of the HVC.
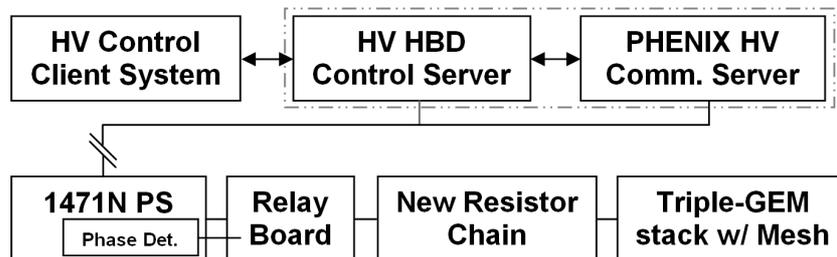
Figure 2.12: Run-9 HV Control and powering scheme

Chapter 3

HV Control and Monitoring

The fundamental concept with its underlying theory and design as well as experimental testing and installation of all hardware and software components of the new *High Voltage Control and Monitoring System*[1] for the HBD in PHENIX is being presented in this chapter.

First we are introducing an intelligent approach to address previous HV issues of the HBD, which shall built the foundation of understanding the overall development strategy of the system. A more quantitative discussion of the three established hardware-based solutions follows. In command of these hardware assemblies and in charge of neutralizing their limitations, a software-based solution defines the global core of the Control System and is studied systematically from its theoretical design to programmable realization, testing and final installation in the PHENIX experiment.

3.1 The Control Philosophy

The HVC system shall be built on the founding walls of mathematical system theory, incorporate the present state of Optimal Control Theory and enhance its capabilities by utilizing state-of-the-art high performance computing (HPC) technologies. One may wonder about the origin of such anomalous approach – in favor of creating a system with the mission to govern an entity such as high voltage (HV). The reasoning lies in the subjects of the applied control, the Gas Electron Multipliers (GEMs). The development, application and research of GEM foils and their operation and behavior under certain circumstances is still a new one. The struggle of the HBD in Run-7 with an infelicitous powering scheme has clearly shown that not all GEM processes under HV are

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[1]The name of this control system, "<u>H</u>igh <u>V</u>oltage <u>C</u>ontrol and Monitoring System," comprising hardware and software components, is hereafter referred as the *HVC* system.

quantitatively well understood. An ensuing visual inspection of damaged foils provided valuable insight into the reconstruction and coupling of possible consecutive incidents during the run, and served as a baseline study for the HVC system. However, a comprehensive knowledge of *all* parameters affecting the GEM performance, e.g. the occurrence of shorted strips, cannot be presently justified. But that is exactly what true *control* from its subject requires!

The word "control" is very often misunderstood and misused. It can be seen as an abstract concept in which policies define actions at *expected* parameter values, as provided by the subject of control or the executing control unit itself. Since we do not know *all* variables and their expected value for our subjects, the triple-GEM stacks, we shall extend this classic definition of control and treat GEMs as *dynamical subjects*, for which unknown parameters are uncovered by reproducing patterns of known parameters over time. In other words, a control system always needs to have an expected value it can compare a measured or monitored value with, in order to respond with a certain control action, if deemed necessary. In case there is no expected value for a certain behavior of the monitored subject, the control system first needs to learn from the subject, before an expected value can be computed and finally used to respond with an appropriate control action, if such behavior is found again thereafter. That is why modern techniques of Optimal Control Theory and HPC shall be utilized for the development of the HVC system.

Before we proceed, the reader shall note the following fundamental definitions used throughout the paper. The subject of control, meaning the monitored GEM-stack, may be called the **control target**. A device executing the control commands to the control target is known as a **controller**. An **event** is understood as any change of the control target, e.g. a spark or resulting short of a GEM. The **resolution** of events is referred to as the ability to detect an event. Any other conventions are introduced in the text.

Perfect Control. The *Perfect Control* may be assigned to a system with the technology to not only detect but act in *single event resolution*. Such a system provides unquantized information of every single event process within the structure it is supposed to monitor and control, as well as endued with the knowledge of how to add meaning to each event and its inner correlation to neighboring events. Furthermore, it has the ability to learn from every possible event pattern with simultaneous enrichment of its knowledge as well as adjustment of its final control performance accordingly. At our present time, the required technology to achieve this ultimate goal does not exist. One may easily identify the key obstacle: the event resolution.

Regardless of control target and parameters to observe, high event resolution provides valuable information about the target and the opportunity to discover a previously unknown behavior. In case of a particle detector, most of the time the highest achievable resolution of HV control events is not necessary, since one really cares about is the sufficient readout capability to do Physics. Nevertheless, for an extremely voltage sensitive GEM detector as the HBD, the sampling rate of control parameters and their measurable precision is crucial in order to better understand the detector's performance, and operate more efficiently, while possessing an improved power to protect GEM foils from severe HV damages.

With the general objective and elimination of previous high voltage issues of Run-7 in mind, we may now define the philosophy we are following throughout the design process of the HVC system.

Control Objective. A control system shall fulfill the requirements of *Perfect Control* with high event resolution as close as technologically achievable, in order to embrace stability, safety and precision in voltage application to the triple-GEM stacks of the HBD, while allowing the detector to be selectively sensitive or mostly rejective to minimum ionizing particles (MIPs). The design should furthermore provide the opportunity for multi-level upgrades as technological progress permits.

The fulfillment of this Control Objective has been made possible through the implementation of the *Theory of Dynamic Control*, hereafter referred to as *TDC*. Due to the fact that one is not expected to be familiar with Modern Optimal Control Theory, the interested reader is referred to the Appendix A for a detailled introduction to HVC's TDC.

Control Diagram. The TDC principles are illustrated in simplified terms in Fig. 3.1, the control diagram. Here, HVC with power supply (PS) represent the controller (C) and the HBD the control target or also known as the control plant (P). With every control command $u(t)$ being sent to the detector, its PS-measured output $y^*(t)$ (S) is combined with possible disturbances of the plant, e.g. P/T, and of the controller itself in evaluating correlation with a dynamic reference $r_{y,k,z}(t)$ in order to determine the success $\epsilon(t)$ of the previous control action. Since we allow a human being to initiate the generation of control parameters, all user requests $x(t)$ must first pass a policy $p(t)$, which is pre-defined and additionally modified by the system-internal result of ϵ. If we would assume linearity and time-invariance of C, P and S, one may use Laplace transformation to obtain the relation between their transfer functions

without disturbance:

$$\begin{aligned}
Y(t) &= P(t)U(t) \\
U(t) &= C(t)\Xi(t) \\
\Xi(t) &= R_y(t) - S(t)Y(t).
\end{aligned}$$

We can now simply solve for the output Y in terms of its reference R_y:

$$\begin{aligned}
Y(t) &= P(t)C(t)[R(t) - S(t)Y(t)] \\
&= \left(\frac{P(t)C(t)}{1 + P(t)C(t)S(t)} \right) R(s) = Z(t)R(t),
\end{aligned}$$

with $Z(t)$ as the well-known closed-loop transfer function; defined in other words, the forward open-loop gain over the closed-loop gain plus one. It especially emphasizes the original idea of the desired behavior of Σ, as defined in the reference, governing the final output to the detector. This would be truly the case if $|P(t)C(t)| \to \infty$ and $S(t) = 1$, which is from a technical point of view presently not achievable. It is rather a matter of how well the control system is able to *optimize its output* and so minimize the difference $|R(t) - Y(t)| \approx 0$.
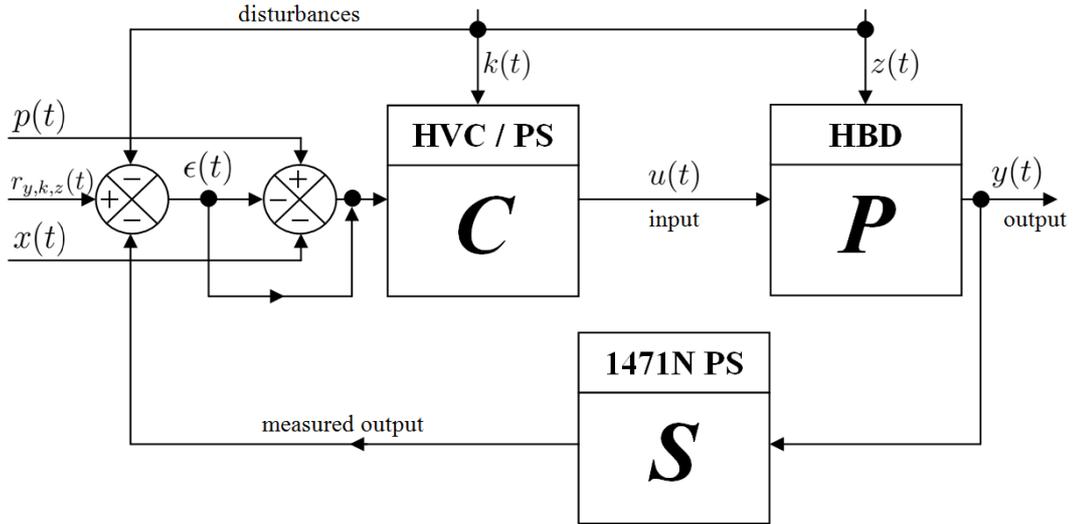
Figure 3.1: HBD HVC Control Diagram.

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3.1.1 Global Response Time Constant

The Theory of Dynamic Control displays an universal control system in meeting all the requirements set by the CO. However, it may be mathematically possible, but not directly applicable in terms of technological limitations and restrictions within the PHENIX control environment. The main issue lies in the previously appointed call of high event resolution or definition of the time set T.

There are generally speaking two control devices causing a limitation of resolution: the voltage/current measurement by the power supply (LeCroy) and registration with a digital computer (HVC). The mathematical operation of quantitation takes place in various of their components as e.g. the analog-to-digital converter (ADC), digital-to-analog converters (DAC) or the finite word length in registers. This process of rounding arithmetical numbers is irreversible and information will always be lost. A quantizer, a zero-memory in/output device, simply designates the interval(s) in which its input lies, which means that the **measured quantity reclines in a known region**.

Obviously, this leads us to the question of how to deal with quantized measurements in respect to control. We need to accept that there exists a mutual relationship between control and estimation through their direct connection with the system as a whole, and so the measuring device will have influence of the choice of control laws that shall give optimized satisfactory results.
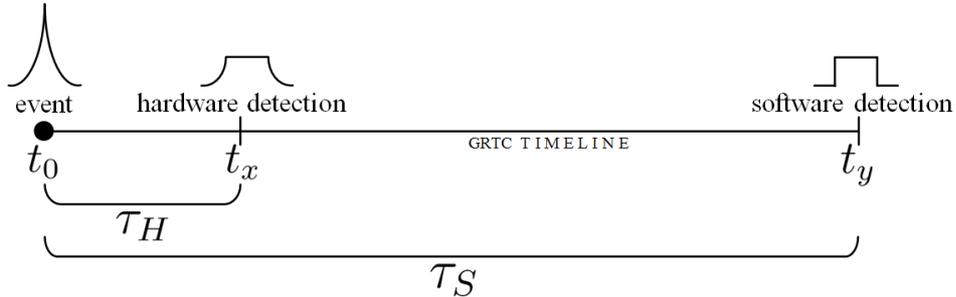
Figure 3.2: Observer-based event detection principle in respect to hardware and software limitations.

From the theoretical point of view, an elegant solution can be found by accepting approximation in dual space, which only needs a small enhancement of the TDC model. Therefore, we are introducing two distinct local observers of the control medium with each having different time dependencies and a unique policy. As illustrated in Fig. 3.2, an event, a discharge between top and bottom electrode of a GEM or generally an infinitesimal change of state, takes place at t_0. Its detection if measurable by hardware, e.g. LeCroy's ADC,

may be possible at t_x. Its detection after additional quantization by software, e.g. HVC on a digital computer, at some later point may occur at t_y. The information of the measured event, represented by ξ, shall be observed by $\mathcal{O}_X$ at t_x and $\mathcal{O}_Y$ at t_y. In the most general case of event information transport from x to y we find:

$$\xi|_{\mathcal{O}_X(t)} \neq \xi|_{\mathcal{O}_Y(t)}, \quad \text{for almost}\forall t \geq 0. \tag{3.1}$$

This is true due to quantized measurements with a 8-bit resolution at 100kHz of LeCroy's ADC and "delivery time" of measured samples from the PS memory via mainframe to software control. In Fig. 3.3 we demonstrate the overall sequence and symmetry of *successive transports*[2] of sampled events. Each tick on the timeline stands for a measurement by the ADC, while each filled circle on the timeline indicates the HVC detection of a previously measured event by the ADC. The distances between each detection event, labeled with boxes, circles and triangle, on either side (PS or HVC), can vary, but are in a known region.
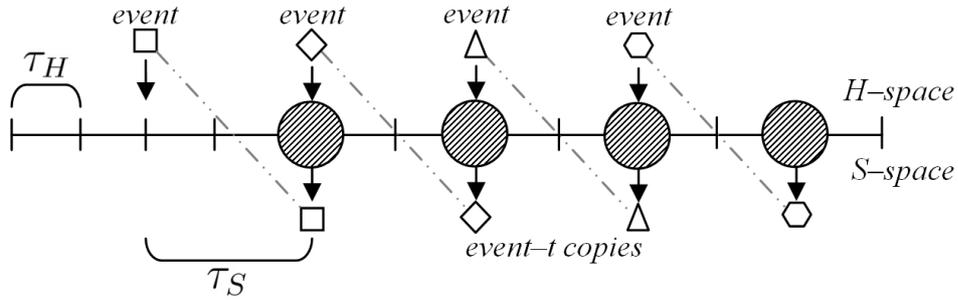
Figure 3.3: HVC-governed event sampling and successive transport.

May i, j be counters of successive detected events by hardware and software respectively and t the continuous space time, then we can find

$$\xi(t_j)|_{\mathcal{O}_Y} = \xi(t_i)|_{\mathcal{O}_X}, \quad t_j > t_i \forall j, i \in \mathbb{N}_0, \ \forall t \in \mathbb{R}^+, \tag{3.2}$$

which simply means that the information of the sampled measurement by the LeCroy is invariant under transport to HVC.

At this point, we introduce a new variable to allow improved coordination.

---

[2]A successive transport is defined as the invariance of data delivered to HVC. In case bits got lost, the transport is declared unsuccessful and not used for analysis; an additional delay of τ_S is induced.

Definition 1 *A response time constant τ shall represent the time it takes from a measurable event at t_0 to be detected by a device and so its first ability to respond in appropriate control action if necessary.*

In reference to Fig. 3.2, we find the response time constants for hardware (H; PS) and software (S; HVC) with their respective event counters i, j:

$$
\begin{aligned}
\tau_i^H &\approx t_i^x - t_i^0 \\
\tau_j^S &\approx t_j^y - t_j^0 = \tau_i^H + \left(t_j^y - t_i^x \right), \quad \forall i \geq j,
\end{aligned}
$$

where one may easily find by expressing (3.2) in terms of ξ, that undetected event information at τ_j^S is inherited from states at τ_i^H. Therefore, τ_j^S shall be called a *global response time constant* (GRTC) for j. With this quantized measurement, we may now approximate the detection times to be globally the same for all i, j:

$$
\begin{aligned}
\| \tau_{i+1}^H - \tau_i^H \| &\stackrel{!}{=} 0 \quad \Rightarrow \quad \tau_i^H = \text{const} \xrightarrow{fixed} \tau_H \\
\omega_a \leq \| \tau_{j+1}^S - \tau_j^S \| \leq \omega_b \quad &\Rightarrow \quad \omega_{a,b} = \text{const} \xrightarrow{fixed} \tau_S.
\end{aligned}
$$

This allows us to conclude the *GRTC Principle*:

$$
\xi(t)|_{\mathcal{O}_Y} = \xi(t)|_{\mathcal{O}_X}, \quad \forall t \in [0, \tau_S] = \Lambda_i, \forall i \; \mathcal{O}_X\text{-detected events.} \tag{3.3}
$$

Since $\exists \tau_H \in \Lambda_i \; \forall i \in \mathbb{N}_0$, its entire event information $\xi(t)|_{\mathcal{O}_X}$ and control behavior and failure can be approximately revealed $\forall t \in [t_j, t_{j+1}]$ through the analysis of its near past and presence in comparison of proven event patterns from previous experimental study, in order to determine appropriate control functions to optimize its future.

3.1.2 System Development Approach

In the previous section, we have learned the fundamental theoretical background for the development of a HV Control System that fulfills together with the TDC all and beyond the requirements for the HBD operation. The question, however, that has not been answered yet is: How do we realize a practical development of such a system and especially, how do we approach such big challenge?

The idea is to follow the GRTC Principle closely and eliminate HV problems as seen in Run-7, that can occur on the so-called *fast-response level* (τ_H), while providing stable backup solutions on the *slow-response level* (τ_S).

First, all possibilities for energy storage in the resistor chain needs to be removed and further modified to ensure dV^3 boundaries between Mesh and Top-GEM in forward and reverse bias configuration. Since LeCroy 1471N high voltage modules are used to power the detector, one needs to be aware of two drawback features. The first concerns about precision – the difference between demand voltage and actual applied voltage, which is rather a general issue in HV application independently from module manufacturer. Therefore, a high precision calibration of the output should be used by the commanding mainframe control (HVC) as one of the references for its control function. The second concerns about the momentary dissipation of stored energy in its output filter capacitors through the detector, every time a channel would trip. Therefore, an additional protecting device needs to be placed in between power supply and resistor chain, which shall discharge stored energy of both power supply and detector via a resistor to ground and additionally trip the corresponding second channel of GEM/Mesh.

The Software-based control is far more complex and requires superior knowledge of GEM behavior and control patterns of all *hardware components, that each represents a control system itself*. Fundamentally, its data communication internally and externally as well as robustness are primary requirements. The approach here is a Client/Server architecture and segmentation of control and feedback monitoring duties. For further stability purposes, all major actions and calculations need to be performed on the client. All internal action routines have to follow a unique philosophy:

- Question all control references before their usage;

- Self-monitor and apply watchdogs to control functions;

- Trust command execution, but question always its application!

In the following section, we are going to discuss each hardware component in detail, before HVC, the main unit of control will be introduced, starting with a design overview and finally its subsystems.

---

^{3}The dV represents the delta of two potential differences.

3.2 Fast-Response GEM Protection

In this section we are concerned about control actions within the τ_H regime. Every hardware component we implement for this HV System needs to support the CO and as a whole makes the ultimate goal of efficient and safe operation of the HBD possible. The "efficiency" on the hardware level is primarily covered by the usage of a resistor chain powering the GEM foils through a single supply line from the power supply, which narrows our attention to their design since they must provide a safe GEM operating environment. As we have seen in Run-7, one of the key issues was the stored energy in the floating grid's filter capacitor to discharge through a large spark onto the top of the Top-GEM every time the LeCroy would trip. Besides the moving dust that needs to be addressed during the detector's assembly, another problematic issue coming from the 1471N module itself has been found. Whenever a channel trip occurs, the stored energy in LeCroy's filter capacitor on its HV output would dissipate through the GEM foils. This unfortunate feature has been addressed by the introduction of a trip detector, sensing the disappearance of phase on the LeCroy board and initiating HV relays of Mesh and GEM channel to connect to ground simultaneously, resulting in a global discharge of the system.

It is crucial to understand that all of these components, resistor chain, 1471N module, trip detector and relay board, represent their own control system with certain open-loop based non-dynamic control functions. As we have learned through our previous theoretical discussion, the knowledge of control patterns on this hardware level needs to be fed to the software-based control references of HVC for optimization of its control. Therefore, we introduce and study each component separately, which is done in systematic order.

3.2.1 Advanced Resistor Chain

In the design concept of a new resistor chain for safe operation of triple-GEM stacks with drift Mesh, a primary aspect is to minimize the stored energy in the system and limit the dV between Mesh and Top-GEM, while the choice of resistors in each *string*[4] need to be invariant under HV application of up to 1kV and shall allow transfer and induction fields for optimized module gain.

Stored Energy. When connecting each string with HBD-sized, 27cm × 23cm, GEM foils, an effective capacitance of $C_{\mathrm{GEM}} \sim 4.23\mathrm{nF}$ is added to every string of the divider. For a typical operational voltage of the GEM channel

---

[4]Hereafter, a *string* is referred to as one of the three parallel branches of a resistor chain.

V_{chain} of 4kV and a nominal resistance of 84MΩ for each chain string, a total stored energy of $W_{\text{GEM}} \approx 1.44 \times 10^{-3}$ J within the entire chain can be expected. Any additional stored energy should be prevented and therefore all filter capacitors are removed, which have been used in the chain of Run-7. Only a harmless 3nF capacitor from the bottom electrode of the Bottom-GEM to PCB ground is kept for low-pass filtering.

Trip Synchronization. Suppose the HV channel of the GEM stack trips at 4kV, while its Mesh stays up at about 3.9kV. Obviously this could involve sparking to the top of the Top-GEM and may result in unnecessary shorts. The idea to prevent such a scenario and to ensure simultaneous tripping of both GEM and corresponding Mesh channel is to introduce a *controlling device* with the goal to synchronize their decay time in order to keep the dV at the moment of the trip as low as possible. Therefore, two 250V *zeners* are installed between the Mesh and the top of the Top-GEM in back-to-back configuration. In case the GEM channel trips and so the dV exceeds 250V in either configuration, Forward or Reverse Bias, one zener will open and suddenly make the floating Mesh channel draw current. If one has set the programmable trip current of the corresponding LeCroy channel low enough, the Mesh channel will trip almost instantly. Since this trip current can be pre-set, the question would be how low can one define such a setting in order to achieve optimized GEM/Mesh trip synchronization? Based on measurements in the laboratory, a trip current lower than $\sim 1.5\mu$A is not recommended, as spontaneous tripping due to a sensitivity problem of the LeCroy PS is possible in this region. A stable setting of 5μA has proven success.

Resistors. The selection of resistor values is of fundamental concern for the performance of the detector, since we are defining the ratio of transfer and induction fields. Let us quickly verify this by a simple calculation. The voltage drop dV_{GEM} across the GEM is simply the current of the particular string times the parallel resistance across the GEM:

$$dV_{\text{GEM}} = \frac{V_{\text{chain}} R_{\text{GEM}}}{\sum R_{\text{string}}^i} = I_{\text{string}} R_{\text{GEM}}, \qquad (3.4)$$

where we define

$$R_{\text{string}} = \sum R_{\text{string}}^i = R_a + R_{\text{GEM}} + R_b,$$

with R_a and R_b the resistance *a*bove and *b*elow R_{GEM} of the particular string respectively. The latter definition may seem redundant on first sight, instead

already accounts for the possibility of varying R_{GEM} and therefore required adjustments to a string, in case of shorted GEM strips in particular more than two and so allows to equalize the dV, which essentially affects the entire module gain. The reader is referred to sections 3.4.10 and 4.3 for a more detailed discussion and practical application of corresponding control principles.

The field of transfer E_T between the Top–Middle (T-M) and Middle–Bottom (M-B) GEM foils results then simply by the voltage difference of their bottom and top electrodes respectively over the gap height d_{gap} between them:

$$E_T^{T\text{-}M/M\text{-}B} = \left[\underbrace{I_{\text{string}}^{M/B} R_a^{M/B}}_{V_{M/B}} - \underbrace{I_{\text{string}}^{T/M}\left(R_a^{T/M} + R_{\text{GEM}}^{T/M}\right)}_{V_{T/M}}\right] \times d_{\text{gap}}^{-1}, \tag{3.5}$$

where $V_{M/B}$ represents the potential difference between the top of the particular string and the top electrode of the $\underline{M}$iddle/$\underline{B}$ottom-GEM of the stack, while $V_{T/M}$ stands for the potential difference between the top of the neighboring string and the bottom electrode of the $\underline{T}$op/$\underline{M}$iddle-GEM. For the drift and induction fields we find

$$E_D = \frac{V_{\text{bias}}}{d_{\text{gap}}} \tag{3.6}$$

$$E_I = \frac{I_{\text{string}} R_b^T}{d_{\text{gap}}}, \tag{3.7}$$

where V_{bias} is the relative voltage to the Mesh. One may note that all drift, transfer and induction gaps are $d_{\text{gap}} = 1.5 cm$ and each field is a function of resistors installed, which proves our initial statement.

Another question one should ask concerns the precision of the resistors and their linearity under high voltage. Even though manufacturers label them with a certain percentage offset to their color code indication, one may sometimes even find much better precision. Nevertheless, for our application we require a precise measurement of all resistors we install on the divider. In terms of linearity, we need to prove their reliability under conditions the resistors will experience with the installation in the chain. A simple method is to apply a precisely known voltage to the resistor and simply measure the current of same or even higher precision, which can be done with a picoampmeter. A more detailed discussion of results for resistors installed in the HBD for Run-9, one may find in section 3.5.2.

Voltage Asymmetry. In a multi-stage gain system, individual elements can hold a particular voltage (gain), that however, the system as a whole is not necessarily able to operate with in the same way. Thus the idea of Voltage

Asymmetry is that if one can identify, isolate the weak point of the system and relieve it from its gain burden, one can increase it at some other point.

As we have already discussed in Section 2.1.4, the photoelectron collection efficiency is strongly affected by the drift field. One can further study the affect on the collection efficiency by modifying the field within the GEM hole and the transfer gaps. The results of this study, presented in Fig. 3.4a, show that the number of collected photoelectrons Npe is independent of the voltage applied directly across the GEM over a large range of gain. The same effect can be seen by varying the potential across the transfer gap (see Fig. 3.4b). However, one can increase the dV across the transfer gaps and keep the dV across the GEM constantly low, while still achieving higher effective gains through the resulting improvement of transfer and collection efficiencies. Therefore, the resistance across the transfer gaps needs to be significantly increased with respect to the resistance across the GEM. This essentially means that the detector can then be operated at much lower supply voltages to achieve still a high gain or additional "free gain," while the discharge probability is automatically lowered.
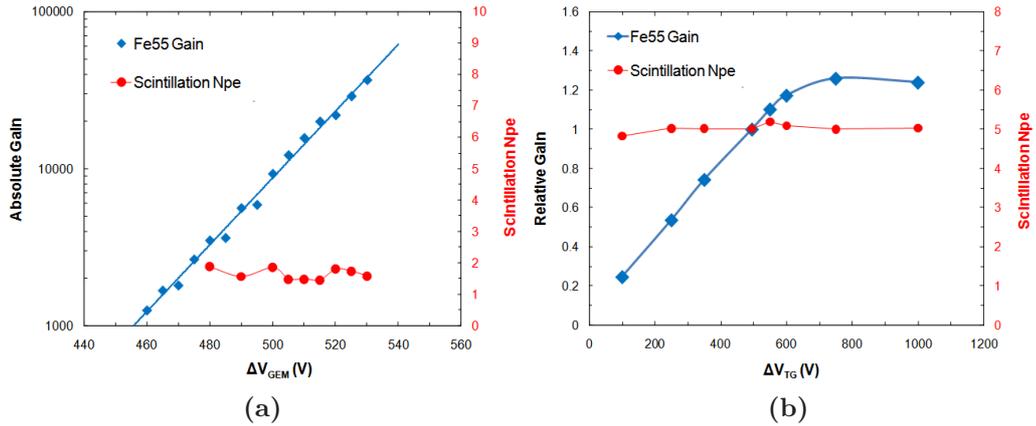
Figure 3.4: GEM gain and scintillation signal as a function of the voltage across the GEM is shown in (a), and in (b) the GEM voltage is kept constant while the voltage across the transfer gap is raised [5].

Final Design.   The image in Fig. 3.5 and schematic shown in Fig. 3.6 present the new voltage divider for the HBD. The indices used are ordered by increasing resistance. For simplified on-board measurements during the conditioning process, jumper cables are provided on top of every chain for its isolation. HV wires going to the individual GEM-stack are fed from below the board through

appropriate holes next to the GEM resistors. Except the permanently installed resistors R_0 and zener diodes, all resistors are mounted on miniature boards for convenient replacement, if deemed necessary (see Section 4.3).

Resistor values in Table 3.1 have been used for Run-9. As one can easily prove by calculating the respective nominal fields for a given V_{chain} and voltage bias, the transfer fields are always identical, while the induction field is much higher with the purpose to support improved charge transfer efficiencies.
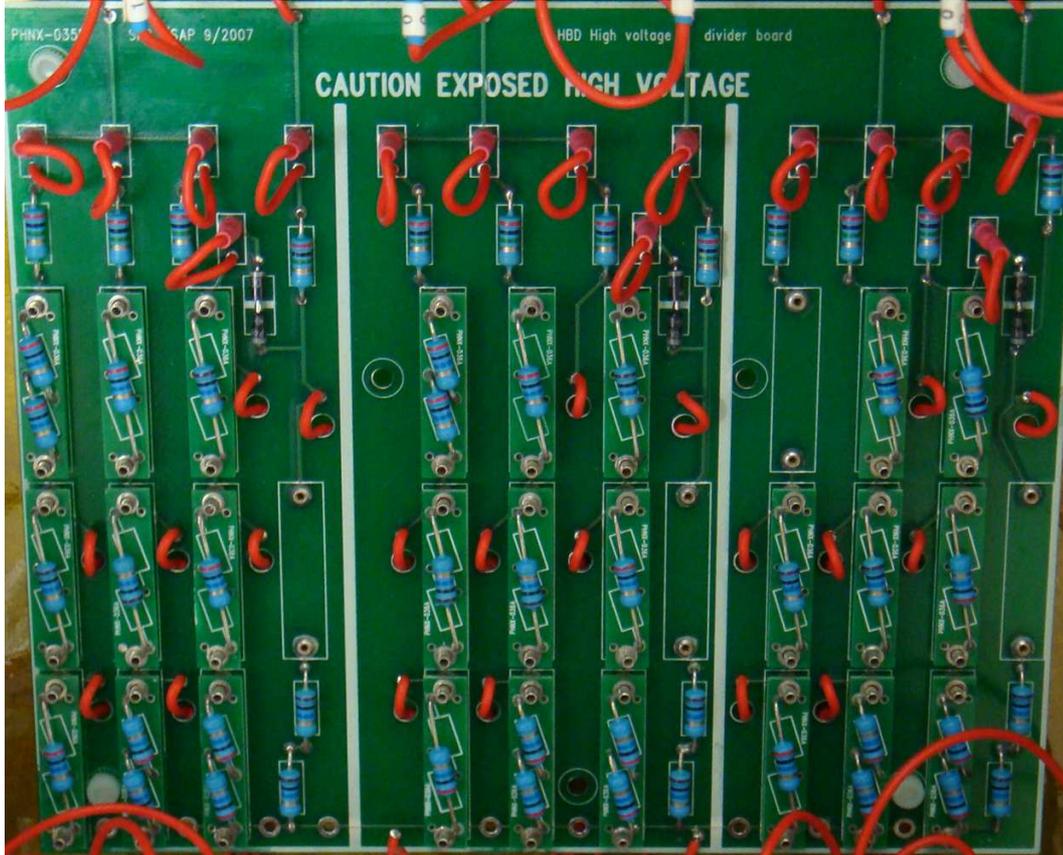
Figure 3.5: PCB board with all resistors and zeners installed for Run-9. One board hosts three resistor chains, each powering one GEM detector module.
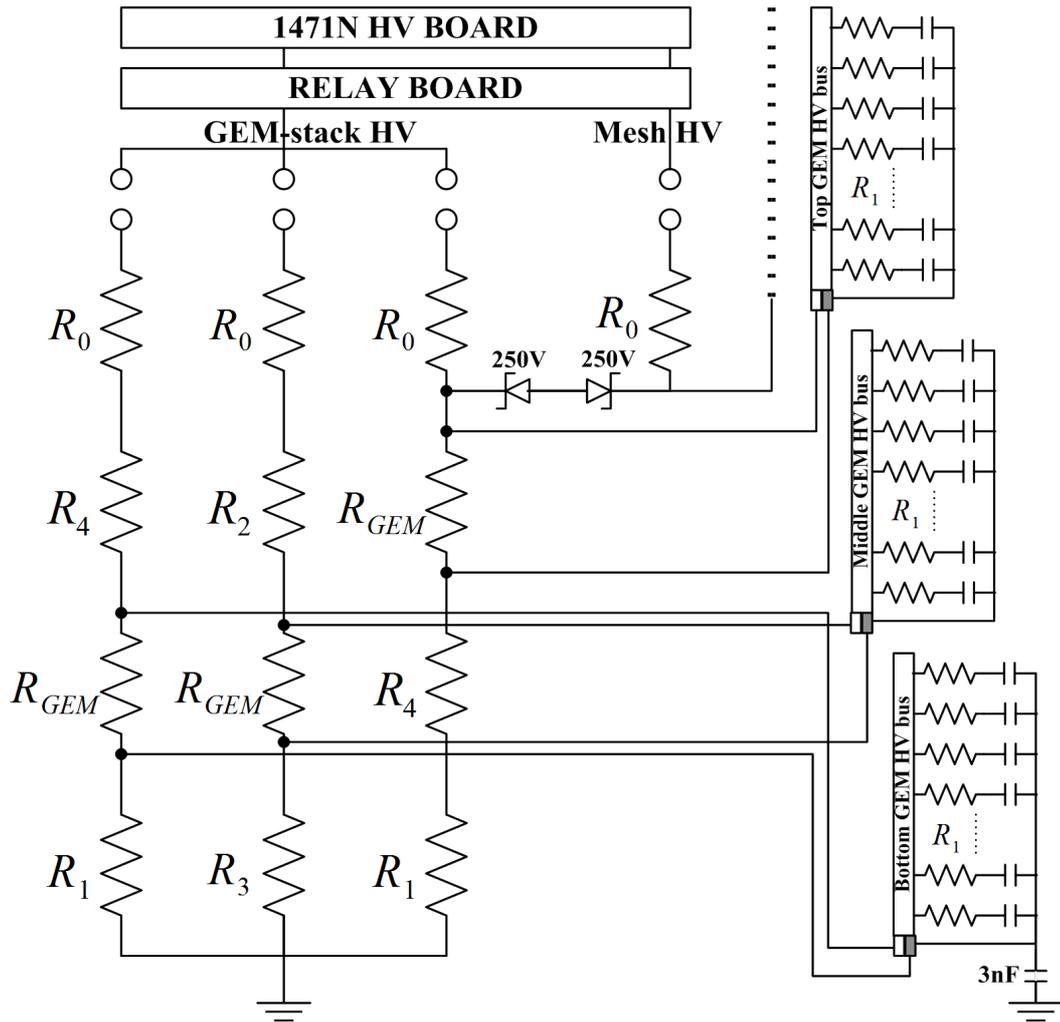
Figure 3.6: Schematic of resistor chain for Run-9. The resistor values are as follows: $R_0 = 2\text{M}\Omega$, $R_1 = 20\text{M}\Omega$, $R_2 = 26\text{M}\Omega$, $R_3 = 46\text{M}\Omega$ and $R_4 = 52\text{M}\Omega$. A clear overview is shown in Tab. 3.1.

Table 3.1: Divider Resistors (nominal; in MΩ) used in Run-9.

Bottom GEM	Middle GEM	Top GEM
2	2	2
52	26	**10**
10	**10**	52
20	46	20

3.2.2 LeCroy 1471N Power Supply

Understanding the internal principles of high voltage generation we are attempting to control proficiently from the external, is not just beneficial but essential for optimized control. Blind control means having no control at all! A study of the fundamental control actions taking place on the board will then allow us to indicate and possibly solve issues the 1471N PS might have.

The 1471N high voltage generation module is an 8-channel HV supply of fixed negative output polarity and has been designed to meet the 1450 mainframe crate system. Its output is fully programmable up to 6kV for $200\mu A$ with a nominal set resolution of 500mV and *proposed* precision of $\pm$ (3V + 0.1% of setting) at 25°C with a minimum load below 300V required for best accuracy and stability below 100 ppm/°C. The AC contamination riding on the DC output (ripple) is lower than 50mV peak-to-peak. The channel trip current or trip threshold can be set with a resolution of <15nA, which is compared to a current measurement of the same, although at a proposed resolution with trip condition detection of <10ms. This feature has been disabled during voltage ramps with a charging current of $\sim$ 2mA due to charge-up effects during this process. This HV board requires a 24V power supply with $56mA + 330\mu A/\mu A$. A standard mainframe can supply $\sim$ 3.75A per slot.

The divider for Run-9 presents to the LeCroy a resistive load of 28MΩ, which would allow us to reach a maximum voltage of 5.6kV. Since for the HBD a supply of $\sim$ 4kV is sufficient, the HV hardware limit of the module has been lowered to 5kV and so additionally satisfies standard SHV cable ratings and BNL safety policies. This hardware limit can be set directly through a
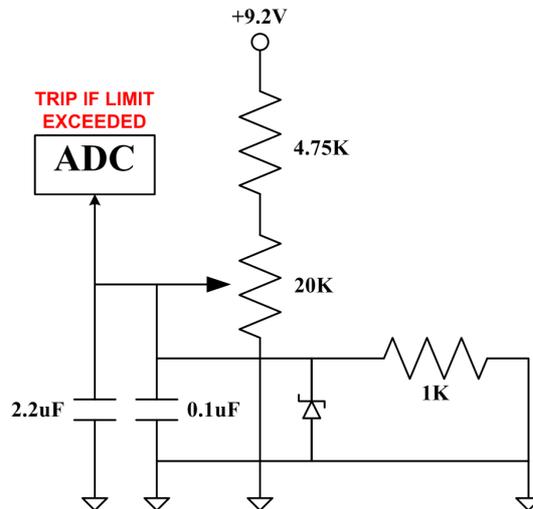
Figure 3.7: Schematic of HV hardware limit.

potentiometer and 1000:1V test point on the front panel of the 1471N module. The low voltage of this test point is measured by the on-board ADC and enforced by the firmware, if the output voltage exceeds this limit, which is illustrated schematically in Fig. 3.7.

In the following we shall discuss the basic units every 1471N board comprises:

1. Mainframe-Module Communication

2. Baseline Control

3. Operational Control

4. LV Generation

5. HV Generation

6. Measurement

The chosen order represents a complete circle of actions, while of course many other processes are taking place in parallel, which we are not able to talk about in this scope. It is important to keep their inner relation and so coordination in mind. Fig. 3.8 shows an extremely simplified picture the reader may use along our discussion of each unit.
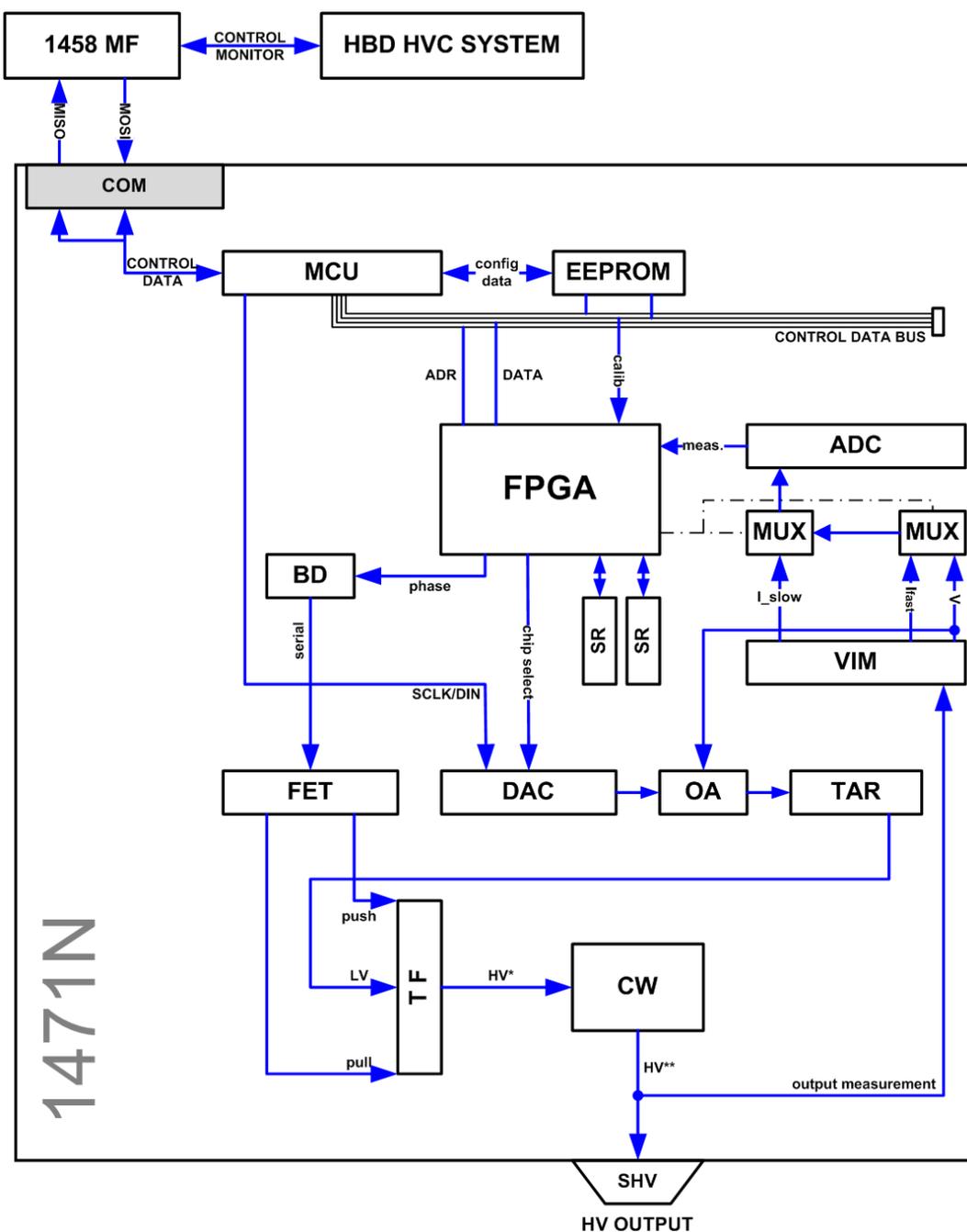
Figure 3.8: Functional Diagram of the 1471N HV module.

The following acronyms have been used in Fig. 3.8 and are assumed to be known hereafter. – **MF**: Mainframe 1458; **MC**: Microcontroller; **EEPROM**: Electrically Erasable Programmable Read-Only Memory; **FPGA**: Field-Programmable

Gate Array; **SR**: Shiftregister; **BD**: Octal Buffer/Line Driver; **FET**: Field-Effect Transistor; **DAC**: Digital-Analog Converter; **OA**: Operational Amplifier; **TAR**: 3-Terminal Adjustable Regulator; **TF**: Transformer; **CW**: CockcroftWalton Multiplier; **VIM**: Voltage/Current Monitor; **MUX**: Multiplexer; and **ADC**: Analog-Digital Converter.

Mainframe-Module Communication. The 1458HP mainframe (master), containing 90A, 24V power supplies per slot, sends the following control commands per channel through the MasterOut-SlaveIn (MOSI) line, a serial connection to the 1471N COM pin 14:

- Demand Voltage (V)

- Ramp Up Rate (V/s)

- Ramp Down Rate (V/s)

- Trip Current (μA)

- Trip Peak Current (μA)

- Channel Enable (0,1)

- Ramp Trip Enable (0,1)

- Measured Voltage Deadzone (V)

- Measured Current Deadzone (μA).

The *Trip Current* and *Trip Peak Current* are compared to the slow and fast-measured current respectively. The two deadzones are part of the mainframe's control update system and indicate, if the measured voltage/current has changed by a pre-set value. If these would be set to zero, effectively every measurement would be seen as a positive variation, since a change of the least significant bit from update to update is very likely. The *Ramp Trip Enable* determines, if trip currents are enforced during ramping or not. This feature has been disabled for the HBD due to common charge-up effects of GEM foils. All other control properties are self-explanatory.

The measurements of each channel by the 1471N (slave) are sent through a second serial connection from COM pin 12, the MasterIn-SlaveOut (MISO) line, which are:

- Measured Voltage (V)

- Measured Current (μA)

- Measured Peak Current (μA)

- Channel Status (ID)

- High Voltage Limit (V).

When the master transmits control commands to a particular slave on MOSI, it sends it to all slaves. If the included slave address matches with one of the slaves, the module will respond on MISO and return the received token to acknowledge and execute the command. In case one message has not been received by the master, in the next transaction, the slave will find a negative receive status of the master in the message and re-submits the information. A unique ticket number in the message allows tracking of all submissions.

The structure of the message by the master to transmit control commands is of the form:

{*slave address*} {*master-receive-status*} {*channel-address*} {*space*} {*ticket number*} {*space*} {*control command*} {*terminator*};

and reads in an actual transaction

1000 (0000 + geographic address) (00000110/00010101) (ASCII-digit) (00100000) (ASCII-digit) (00100000) (cmd) (00001101).

The slave message instead is build as follows:

{*slave-receive-status*} {*ticket number*} {*space*} {*response*} {*terminator*}.

Baseline Control. In the power-up sequence of the 1471N module, the mainframe will set the system reset bit of the *Microcontroller* (MC) HC11 and activate the bootstrap. If the control byte of this sequence is set high, a standard boot is being initiated, where the *EEPROM* AT28C010 becomes static/read-only, the baud rate / serial connection speed is set (e.g. 19.2k), voltage output calibration coefficients are loaded into the FPGA, and all channels are disabled from voltage generation until commanded otherwise via MOSI. If the first bit is driven low, inner circuit programming is possible as the MC executes the ROM code within itself. In order to modify calibration constants one would need to ensure that the second bit is set to zero, which will allow to write to the EEPROM. During these special maintenance modes the module is not able to operate.

One may immediately recognize the need of *calibration coefficients*. The 1471N is not able to make hardware-based adjustments to calibrate its output

voltage, measured current or measured voltage. Instead an external measurement with a resistor chain of well known value and high-precision voltmeter is performed and final results are loaded into the EEPROM: 3 constants for a quadratic polynomial in case of measured voltage and demand voltage, and 2 constants for a linear function in case of measured current. These corrections are then used by the HCMOS 8-bit MCU, applied to the requested output voltages from the mainframe message by sending it via its Serial Peripheral Interface (SPI) with a nominal bus speed of 2 MHz to a Digital-Analog Converter (DAC) and its following components for *HV generation* (see below *LV/HV Generation*). The MCU and its components are shown in Fig. 3.9.
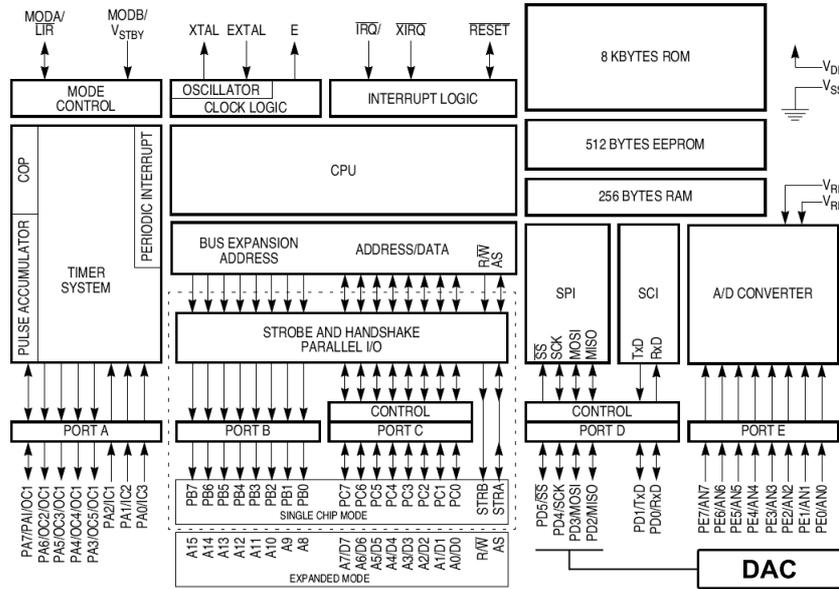
Figure 3.9: Illustration of MCU Internal [6] and Serial Bus to DAC units.

Operational Control. The actual heart of the entire system is the high performance and capacity *Field-Programmable Gate Array* (FPGA) XC4000E, which includes very flexible, programmable architecture of Configurable Logic Blocks (CLBs) and surrounding Input/Output Blocks (IOBs), providing respectively, functional elements for logic construction and the interface between package pins and internal signal lines.

The DC output of the 1471N is based on a *switching regulator technique* with the ability of pulse-width modulation, one of the key differences to linear regulators. Control over the output voltage is realized by using a current switch with a constant frequency and variable pulse duration τ over period T, the *duty cycle*. Therefore, a **push-pull topology** is chosen, where a DC-DC

convertion is accomplished with a high-frequency transformer of fixed ratio and two switching Field-Effect Transistors (FET), one pushing current in one way, the other pulling it the other way. This method allows minimal power dissipated in the FETs and so keeps the operational temperatures low due to higher efficiency. However, a low-pass filter needs to be implemented near the output in order to prevent radio frequency interference and to keep the ripple voltage as low as possible.

One of the key responsibilities of the FPGA is to generate these push-pull signals or so-called **phases** to the FETs. The detailled method to generate these phases is as follows. A shift register (SR) is made into a counter, which shall provide a specific logic square wave to control the two FETs for each output channel. Therefore, two clocks are used to trigger the change of the SR state: a 100kHz clock synchronized to a 800kHz clock. If the FETs would be fired for every channel at the same time, severe instabilities of the overall system could arise. Thus a symmetric activity wave for the transistors shall be generated across one complete cycle, identified by the leading edge of the 100kHz wave. Let us have a look at a Verilog (HDL) algorithm to generate such an event pattern.

Program 1 1471N: FPGA Phase Generation Algorithm

```
1     always   @(posedge x800k or posedge Reset)
2        if (Reset)     SR    <= 0;
3        else           SR    <= {SR, (SR[5:3] == 3'b000) & x100k};
4     always   @(posedge x800k or posedge Reset)
5        if (Reset) begin
6           phase    <=   8'hff;
7           phase_   <=   8'hff;
8        end
9        else if (EnableAll) begin
10          phase    <=   ~(SR & Enable);
11          phase_   <=   ~({SR[4:1], SR[8:5]} & Enable);
12       end
13       else begin
14          phase    <=   8'hff;
15          phase_   <=   8'hff;
16       end
```

As one can see in line 3 of the HDL script, the states of the SR in one complete loop are set to:

c1 83 07 0e 1c 38 70 e0.

The code and its final push-pull signal is illustrated in Fig. 3.11.

Each bit horizontally corresponds to one output channel of the 1471N and vertically its state at a given time. Initially all states are active low and no voltage is being generated. The HVC system notifies the MCU via the 1458HP mainframe (see Section 3.3), which then allows the start up process to begin at the leading edge of the 800kHz wave and so drives the first bit high. A global rule is defined for bits 3 to 5; if no bits are high within this band, a "1" otherwise "0" is added to the SR. After $\tau = 1\mu$s another "1" bit is added and the same after $2T$, which pushes the first high bit into the control band. At this point the start up is complete and an endless loop at the 100kHz clock rate has been started. Since at state 5 the band is low again, a "1" will be added and so on. These states are then exported into the 8-bit *phase* register (HDL line 10), which corresponds to one of the two FETs. As shown in line 11, there is a separate register, called *phase_* for the other FET. The easiest way to find *phase_* would be to simply invert its partner and so switch the transistor pair simultaneously. However, in reality a small deadtime is needed to prevent shorting out the power supply. This extra time is given by adding a one clock delay on either side of the 3 high bits. Therefore, we create the concatenation of bits 1-4 and 5-8, swap the nibbles and take the bitwise complement. The pair, phase and *phase_*, is then sent to two high-speed Si-gate CMOS *Octal Buffer/Line Drivers* HCT540 with 3-state inverting outputs, each splitting the control byte and serving the FETs for all 8 channels. Fig. 3.10 shows the logic diagram of one of the eight drivers. The tri-state feature, however, has not been used for the application of driving the phases to the FETs. Instead, its

Figure 3.10: Logic diagram of one of the eight Buffer/Line Drivers.

FET 1 (PUSH)   **FET 2 (PULL)**

0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	init. reset (all low)
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	init. / prepare routine
0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	

HV states:

0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0	0
1	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0	0
2	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	1
3	0	0	1	1	1	0	0	0	1	0	0	0	0	0	1	1
4	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
5	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0
6	1	1	0	0	0	0	0	1	0	0	0	1	1	1	0	0
7	1	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0

control band   800 kHz   100 MHz   phase generation   trip condition positive

(a) Control bits for both FETs.

1471N channel activity

0 — bit high "1"
1
2 — bit low "0"
3
4
5
6
7

100 kHz

3.69 ms
phase
phase_
1.23 ms   1.23 ms

(b) Illustration of phases per channel.

Figure 3.11: Push-Pull Signals for HV Generation of the 1471N. (a) Control bits for FETs of *phase* and *phase_*, (b) Phases for one FET for each of the 8 output channels (left) and the difference between *phase* and *phase_* signals (right).

primary purpose is to decouple and protect the FPGA from possible transients

dissipating back from the FET and furthermore to invert the signal. During the configuration process at the start-up of the FPGA, the output ports are driven high, which would accidentally drive the FETs. The phase invertion of the BD prevents such uncontrolled states.

When the mainframe sends the control commands incl. demand voltages and trip currents, through the MOSI line, the MCU utilizes the control bus to forward this data to the address of the EEPROM for storage as well as to the FPGA, which writes current and peak current thresholds to its own RAM.

As we have discussed earlier, the MCU is responsible to send via its SPI output the digital signal of demand voltage to every channel's DAC simultaneously. Since the FPGA is the only unit that has the power to compare measured currents from the ADC against limit violations, it needs a fast method to shut off voltage generation. First, all outputs are driven high to eliminate the phases. At this point, the MCU still allows the production of HV. Thus the FPGA uses the chip select (CS) control line (SPI bus) to enable or disable each DAC's input used by the MCU and throws an interrupt signal to the MCU. This gives the FPGA master control of the two fundamental key components needed for HV generation: the FET and DAC.

LV Generation. The first step of generating the final HV output is to convert the serial signal from the MCU to a voltage, which is accomplished by using a 14-bit *Digital-to-Analog Converter* (DAC) MAX544 that operates on a single +5V supply, with <0.5LSB[5] integral linearity error and <0.9LSB differential linearity error. This device has 3 digital inputs: the chip select (CS) for the FPGA, the data input (DIN) and serial clock input (SCLK) for the MCU. The high bits of the inverted CS signal provides a frame for the serial data loading at DIN. Following the bit high-to-low transition, the DIN data is shifted in one single bunch into a serial input register on the rising edge of the SCLK. At the next CS low-to-high transition, the 14 data bits with 2 low sub-bits are transferred into the data latch. If the FPGA would set the CS
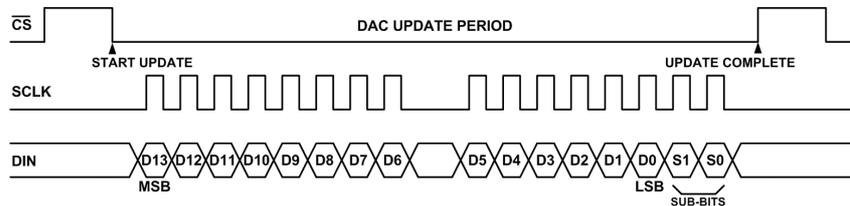
Figure 3.12: DAC timing diagram; update execution in-between CS low bits.

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[5]LSB stands for Least Significant Bit.

high too early, the DAC data will be corrupted and a reload is required. The timing procedure is illustrated in Fig. 3.12.

The DAC itself is based on an inverted R-2R resistor ladder network forming 2 LSBs and 4 MSBs[6], derived from 15 identical high-precision resistors, allowing the lowest (output-transferred) glitch energy possible as well as a low output impedance. A low-impedance reference voltage V_{ref} of +3V is used with a $0.1\mu F$ ceramic capacitor for high-frequency and a $6.8\mu F$ polarized capacitor for low-frequency bypassing. Each 2R resistor in parallel is driven by logic gates. These allow for each high bit a contribution of V_{ref} to the final output voltage, which is then weightend from MSB to LSB through dividing resistors R. One can easily calculate the achievable low voltage (LV) outputs:

$$ V_{\text{out}}^{\text{DAC}} = \frac{V_{\text{ref}} D_{\text{latch}}}{2^n} = V_{\text{ref}} - \frac{V_{\text{ref}} \times 16383}{16384} = V_{\text{res}} \left(2^n - 1 \right), \qquad (3.8) $$

where D_{latch} represents the decimal value of the $n = 14$ DAC bits sent by the MCU. This means that the output voltage range is from 0mV to $\sim 3\text{mV} - V_{\text{res}}$ with a resolution V_{res} of $\sim 0.183\text{mV}$. The entire process is schematically summarized in Fig. 3.13.
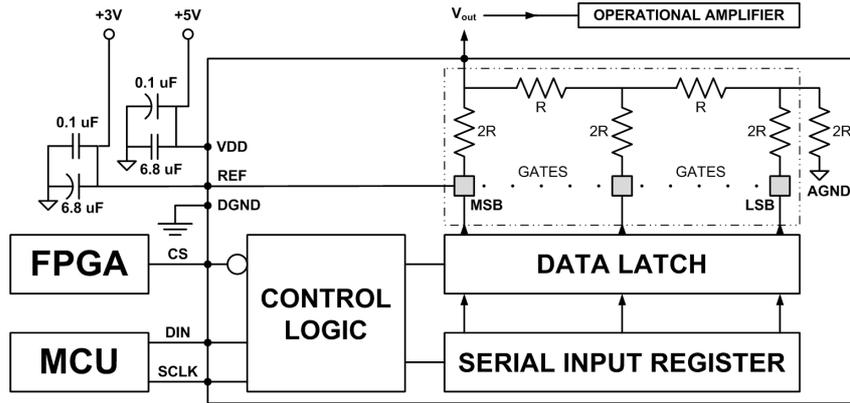
Figure 3.13: DAC functional diagram with internal schematics.

In unipolar mode, the DAC output is driven with a high-speed, dual JFET input operational amplifier (OA) TL082 for which certain requirements have to be met. As we know, the output resistance $R_{\text{out}}^{\text{DAC}}$ of the DAC is constant ($6.25\text{k}\Omega$), however builds a resistive divider with the OA's input resistance $R_{\text{in}}^{\text{OA}}$ and results in a gain error. In order to keep this error below 0.5LSB, one should ensure a $R_{\text{in}}^{\text{OA}} > [R_{\text{out}}^{\text{DAC}} \times (2^{-1} 2^{-14})] = 205\text{M}\Omega$. In the 1471N, $R_{\text{in}}^{\text{OA}} = 10^{12}\Omega$.

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[6]MSB stands for Most Significant Bit.
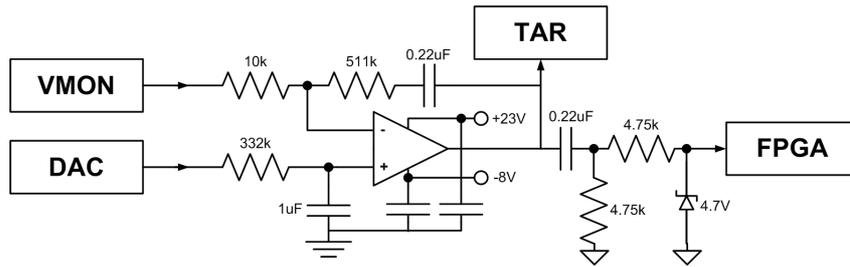
Figure 3.14: Operational Amplifier with voltage monitor (from VIM) and DAC inputs. The OP output represents the TAR input and is checked against AC contamination riding on the pure LV DC signal with the FPGA.

The OA is implemented based on the concept of a *voltage follower* to study the generated DAC output and final applied HV. In any regulated power supply of push-pull topology, one needs to ensure not to induce any AC effects of significant amplitude. Therefore, we are measuring, as shown in the VIM unit, the HV voltage output after final multiplication by the Cockcroft-Walton and feed the result on a scale of 0-3V as the comparing component to the DAC output into the OA with a RC to the OP output (high-pass filter). Furthermore, a low-pass filter line of 152Hz is added for analysis in series with a voltage limiting 4.7V zener to the FPGA (Fig. 3.14). In case AC is detected, the FPGA will initiate an *AC trip* and reset the phases of the corresponding channel to zero with an interrupt signal to the MCU.

Let us assume the current HV output voltage is zero and we begin LV generation. At this point, the VMON OA input will not contribute at all. A 3-Terminal Adjustable Regulator (TAR) is then used to maintain a *desired*
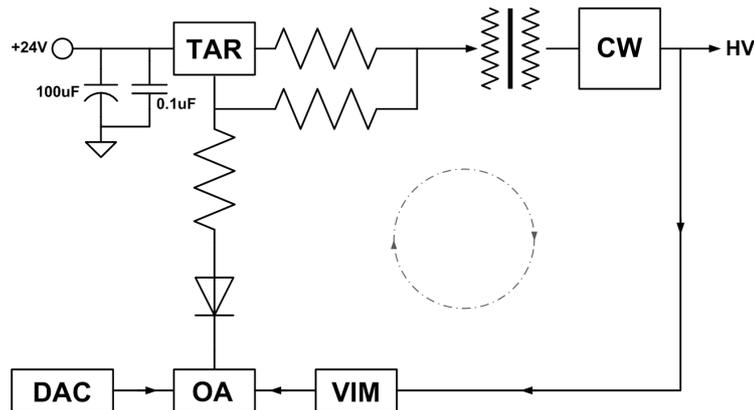
Figure 3.15: Closed-loop Control Supply using an Adjustable Regulator (TAR)

constant voltage delivered to the center pin of the transformer. Its reference voltage between output and adjustment pin is then dynamically modified based on the measured return from the VMON, and so regulating the power necessary to achieve the desired HV output. This completes a closed-loop control system, as shown in Fig. 3.15.

HV Generation. In a final step, the TAR voltage and push/pull transistors to ground are connected to a *transformer* (TF) with two secondaries, one primary and a 20:400 turn ratio. The FPGA-generated phases for FET-pair operation allows a small time gap t_g of 1.23 ms between switching times. In theory, one could change the direction of the field instantaneously and so connect one transistor to ground while at the time same its pair disconnects. However, in pratice, there will be a moment in time when both FETs are connected to ground, which results in peaking high voltage. In order to prevent such a case, an approximation of the sinusoidal wave must be accepted. Fig. 3.17 illustrates what one would see at the transformer's output in comparison with the two FET's turn-on activity. Although the ratio $3t_g{:}t_g$ is quite significant, meaning the FET-on over FET-off periods, the slowing effect of the magnetic field to follow the FET switching decreases the actual timeout response t_r. Therefore, one can find $t_r \ll t_g$ to be always true.
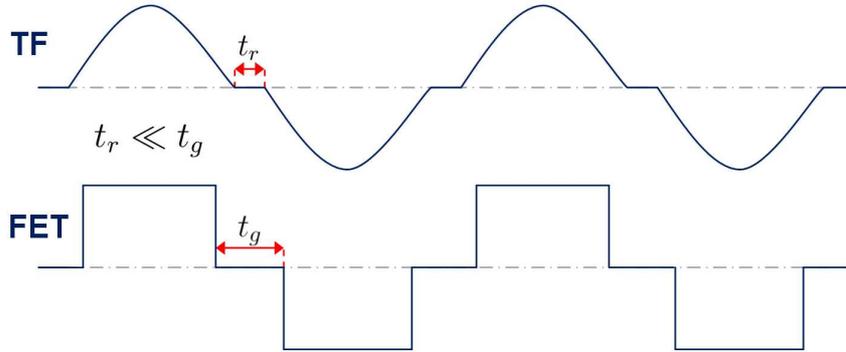
Figure 3.16: Illustrative comparison of FET signal with final output by the transformer

The transformer's output voltage is then brought to its final high DC level by the multiplying stages of a *Cockcroft Walton* (CW) design. Each diode has a peak reverse voltage of 2kV and forward current of 20mA, and capacitors a value of 4700pF. The final CW high voltage is available through a SHV connector and from there via HV cables fed to the resistor chain to power the HBD. The CW output also hosts 3.3nF filter capacitors and a 200MΩ bleeder resistor to ground. As experimental results have shown, the LeCroy
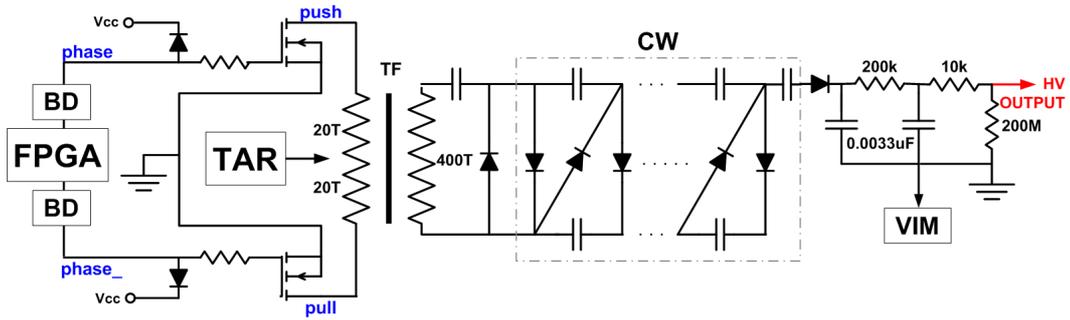
Figure 3.17: Overview of HV Generation with the FPGA, TAR, TF and CW as the main components

firmware does not ground these capacitors whenever a trip condition is met, which causes their stored energy to dissipate through the power supply's load. Fig. 3.17 presents a summary of the HV generation.

Measurement. The fundamental piece of information for HV Control, internal trip handling and TAR adjustment is provided through a Voltage, Slow- and Fast-Current measurement/monitor (VIM) on the output of the CockcroftWalton. It consists of inverting amplifies with low- and high-pass filters. There is one line for the voltage measurement and a dual for the peak- and slow current. The difference between fast and slow lies in their detection. Slow current has a much higher threshold and so changes over time less frequent as compared to the sensitive fast current measurement. This provides the end user the opportunity to perform trip control through both measurements.

The three measurements per channel are performed with a 14-bit Analog-to-Digital Converter (ADC) AD7872. In order to accumulate these 24 data set more efficiently, a concatenation of two CMOS analog Multiplexers (MUX) MAX396 with one COM output to the ADC's differential amplifier input is controlled timely by the FPGA, before then every measurement is sent to the FPGA for storage and analysis. Important here is the system synchronization to the ADC data. Therefore, we detect the leading edge of the serial clock from the ADC synchronously and use a counter marking the time interval between ADC conversions. At the start of this counter, a conversion pulse is generated to then receive and correct the ADC data with previously loaded calibration coefficients from the EEPROM into internal memory cells. After each conversion pulse, the MUX channel is switched to the following channel and so the settling time for the next ADC measurement can begin. The results are first moved to a shift register to accumulate a whole data word before writing to the RAM takes place. At this point, both current thresholds

and their measurement are available in the Data RAM, which allows their comparison. If the slow current or peak current exceed their thresholds or AC current has been detected, the FPGA will shut off the phase generation for this particular channel and send an interlock signal to the MCU, which will then stop transmissions to the DAC.

The final results of measurements, momentary channel settings and their status are then sent through the MISO to the mainframe when an update is requested.

3.2.3 Trip Detection for LeCroy Systems

The 1471N HV module initiates a trip every time a channel's measured current is in excess of a pre-set trip threshold. Other trip states are the violation of the hardware HV limit or the detection of AC contamination riding on the pure DC signal. The internal procedure of actions by the FPGA at positive trip conditions has been already discussed in the previous section. One may have noticed that one fundamental step in this procedure is missing: the grounding of the channel's RC filter on the HV output (see Fig. 3.17). As a consequence, the decay of the HV signal contains significant voltage spikes, which correspond to the stored energy the LeCroy dissipates through the GEM or Mesh channel.

Another issue we have learned from Run-7 is the possibility of a large dV between Mesh and Top GEM, especially when one of the two HV channels trips. Therefore, we have already implemented a Zener on the resistor chain with the purpose to prevent a dV > 250V. However, what if its service would fail or be not as sufficient as it should operate from a theoretical point of view? These questions are not only required according to HVC's Control Objective, but justified and strongly supported by experimental studies presented in Section 3.5.1.

The idea to solve both issues – the spontaneous discharge of the RC filters affecting the GEMs and the unsynchronized decay of the GEM/Mesh channels causing a large dV after the FPGA has issued a trip – is to monitor the FET phases from the FPGA, detect their disappearance and instruct an external device to safely discharge the entire system, 1471N GEM/Mesh channels and divider board / GEMs. Therefore, we introduce two new hardware components: the *Trip (Phase) Detector Board* and *HV Relay Board*[7]. The latter one is discussed in the following section. At this point, we present the method of phase monitoring utilized for the trip detection.

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[7]The Trip Detector and Relay PCB have been designed by S. Boose and S. Polizzo from Brookhaven National Laboratory.

FET Phase Monitoring. The first action by the FPGA in a trip condition is to drive the phase high for both FETs of the particular channel. Since both Buffer/Line Drivers (BD) invert the phase, the serial signal sent to the FETs disappears, which will initiate the deactivation of HV generation. One BD serves the 8 push-FETs, while the other serves the 8 pull-FETs of the corresponding channels. As illustrated in Fig. 3.18, a trip detector board probes the phases from one BD without their distortion as ensured by on-board mounted diodes. The actual signal represents a square wave with an amplitude of 5V; its structure has been already discussed and shown in Fig. 3.11. One can measure either 5V, when the FET is providing a path to ground for the transformer (TF) or 0V when the FET is deactivate, meaning its partnering FET may draw the primary TF current in the opposite direction within a period of ~ 6.15 ms. If after this period one does not measure 5V again, the FPGA has issued a trip. The phase detector simply looks for such *discontinuities of the phase*. Therefore, a Flash Microcontroller (PIC 18F4620-I/ML) with a 10MHz clock allows 220pF capacitors to be charged by the phase signal, which is directly measured with its internal 10-bit ADC. Approximately every $10\mu s$ a measurement is made and an *interrupt counter* increased, if the measured value represents a 0V state of the phase. A new loop begins then with driving
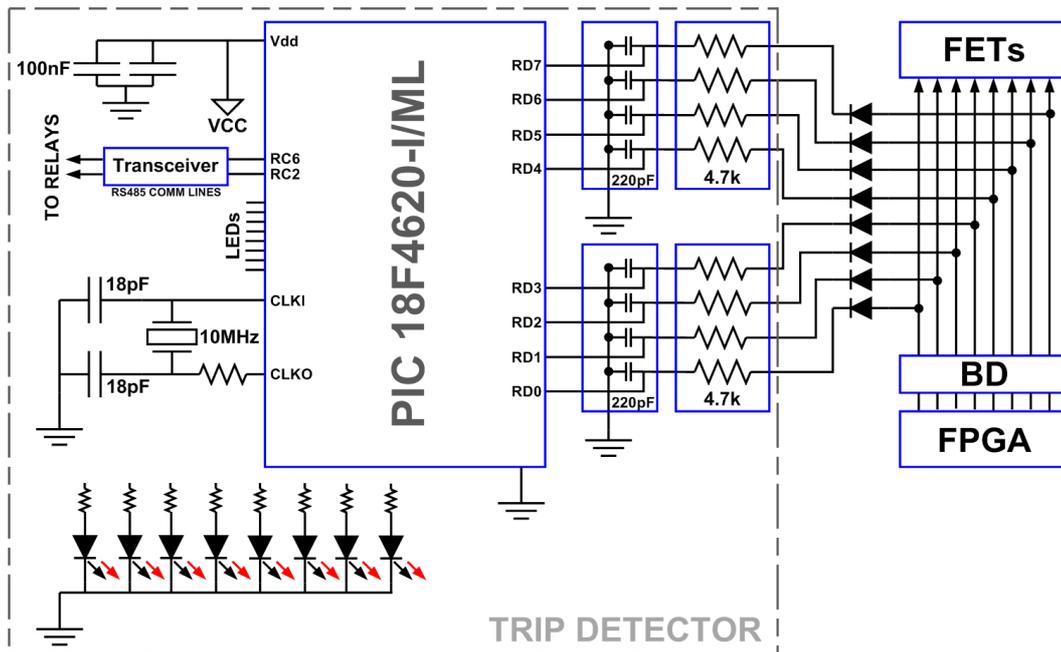
Figure 3.18: Illustration of the Trip Detector Board implemented in the 1471N. The phase for each channel is probed between the Buffer/Line Driver (BD) and FET.

the RD ports (see schematic) to discharge the capacitors and their charge-up is allowed again for a new measurement. A globally defined array captures the 2 different *states* a channel can be represented with:

- **State 0**: No Phase or Phase Interrupted – no voltage is being generated;

- **State 1**: Active Phase – voltage is being generated.

The array is used to drive on-board mounted LEDs, which red light indicates State 0. Furthermore, the state information is sent via a RS-485 Transceiver to the Relay Board's state machine every $\sim 60\mu$s, where HV relays are operated accordingly (see next section).

An internal control loop sets a trip flag for a particular channel, if its interrupt counter continues to increase after ~ 6.15 ms. This flag immediately sets the channel's index of the array to State 0 and informs the Relay Board the trip at the next RS-485 transmission.

3.2.4 Relay HV Protection

The Trip Detector Board, which is mounted directly onto the 1471N board, utilizes HV relays to provide a path to ground and discharge the stored energy in both the 1471N power supply and the triple-GEM stacks simultaneously. A Relay Board, containing HV Relays and $10k\Omega$ bleeder resistors, is placed in-between the 8 HV supply lines from the 1471N and the resistor chains for 4 HBD modules (GEM-stack and Mesh). The front panel hosts 16 SHV connections with 1471N inputs and neighboring identical outputs; a plain HV gateway is realized. A schematic overview of the implementation of this new hardware component in the HV System is given in Fig. 3.19. The Relay Board's microcontroller (MC) receives the channel states via RS-485 from the Trip Detector
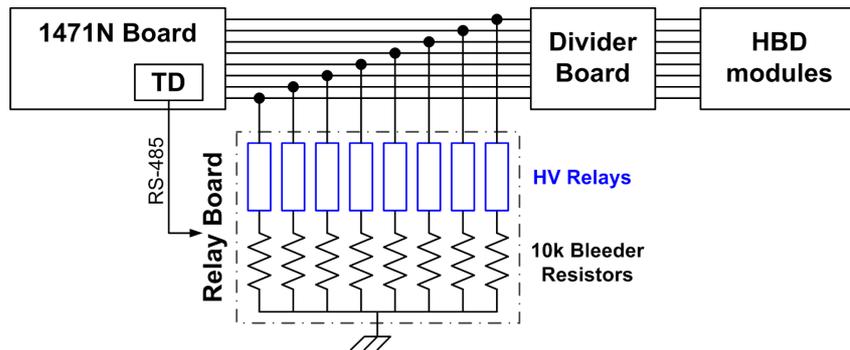
Figure 3.19: Overview of Trip Detector and Relay Board implementation in the HV System

and either opens or closes a channel's corresponding relay depending on its active or inactive FET phase, respectively.

Due to the obvious fact, that one always has to protect the control circuit (LV) from the HV portion of the board, an HV Relay consists of two basic components: a gate and a magnetic coil. When the Trip Detector reports the disappearance of phase for a particular channel, a magnetic coil inside the relay is energized by the MC in providing a digital ground to a +24V source. The produced field pushes a movable bottom electrode of the gate towards its top electrode, which is in direct contact with the HV line between 1471N and the HBD divider. The closed gate creates then a path to the chassis ground of the Relay Board. This gate is kept closed for a period of 10s, ensuring a complete discharge of the entire system with additional safety time. Furthermore, the state of the relay is conveniently displayed by a Dual Color LED on the front panel of the board (green if no phase; red if active phase). Fig. 3.20 summarizes the operation of the HV Relay for one channel.
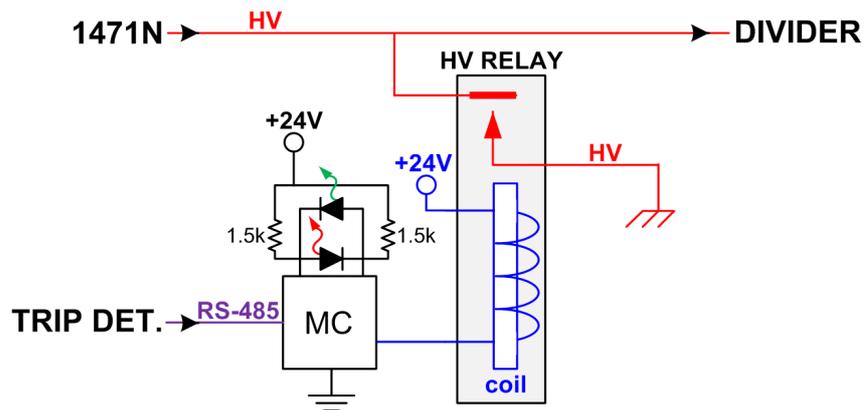
Figure 3.20: HV Relay operation for one 1471N channel with an interior view of the relay. A Dual Color LED indicates the status of the relay.

3.3   Software System Design

The fundamental steps of systematic software design have been already accomplished. The elimination and understanding of previous HV problems of the HBD in Run-7 has led us to the design of a new theoretical model of dynamic control (TDC) that not just addresses each of these issues, but rather proposes a new standard of state-of-the-art software control systems for HV-sensitive particle detectors. The other key requirement before one shall begin designing functional structures of the actual program has also been met by the precise study of elements of the medium to be control. One may realize, the only commonality between the HV Control software of Run-7 and the new HVC of Run-9 is the one of HBD-controllability, although with bidirectional results. HVC represents a control system written from scratch based on TDC and modern high-performance computing techniques.

At this stage, questions of implementation into PHENIX Control, data and object modeling as well as communication and selection of the primary programming language have to be answered.

3.3.1   PHENIX Control Infrastructure

In the early days of PHENIX, an *Experimental Physics and Industrial Control System* (EPICS) implementation had been used for high voltage control purposes, which unfortunately caused a lot of trouble: broadcast floods affecting the data acquisition (DAQ) or even complete HV system crashes requiring Input Output Control (IOC) reboots on a regular basis. EPICS has been designed by Alamos National Laboratory and Argonne National Laboratory with the focus on providing a set of software tools to control large experiments as e.g. particle accelerators with many successful results worldwide, however, it seemed for PHENIX at the end too complex for the little it actually had to do for stable HV control. The consequence was its complete replacement with a conventional *HV Server* that loops over channels on mainframe(s) for status updates and responds/executes control commands of its clients.

A serial communication using the RS-232 interface of the LeCroy 1458HP mainframes is established via an Equinox ELS-16 II Terminal Server (TS) supporting TCP/IP (Transmission Control Protocol/Internet Protocol) and 16 possible thin clients within the Interaction Region (IR), providing location-independence of the server and so guaranteeing improved robustness of the system.

Although, the ARCNET interface would allow character transmissions of

¡ 4μs rather than $\sim$ 0.5ms for serial with a 19.2k boud rate, it is sufficient for the control of high voltage. However, if one would like to achieve a higher resolution of voltage/current measurements, ARCNET would be the better choice.

Presently, every detector subsystem has their own **HV server/client** pair with an assigned physical host server, called the **VA**. The PHENIX shift crew, in particular the Shift Assistant (SA1), or detector experts can login to the corresponding VA machine, start the HV server by loading a detector specific configuration file and *use the client* to control their mainframe(s). Understanding the fundamental control infrastructure in PHENIX is for sure a necessity in order to attach a new control system properly to the present configuration, but one should not make the control design dependend on this *underlying* structure! If at any time in the future, technological progress and financial support allow significant improvements to data readout and communication, the control system does not have to be re-designed from scratch, rather simple modifications to control policies, data references and time constants need to be modified.

3.3.2 Modern C/S Architecture

The \use of client" has been commonly understood by detector experts to login to the assigned VA machine where their HV server is residing and write TCL-TK or Perl TK scripts that simply call the HV client to either change HV properties or return them periodically, tokenize the response and display the results in a Graphical User Interface (GUI) to the user. This procedure, which seems so natural to us, is based on the idea of Centralized Computing – an already predominant popular mode in the 1970s, where client computers where not powerful and a central large-scale server could so handle all the primary processing. The connecting machines requesting the information for display are then not more than thin clients or terminals, mirrors of server process results. This configuration is widely known as a *Terminal/Server (T/S) Architecture*. But suppose a complex control system needs to run heavy-duty processes that need to be handled by the server, while at the same time many other clients want to run requests for updating data analysis reports from the same server. An enormous burden on the server would result, which may not necessarily lead to a system crash, but depending on the CPU, may cause a significant slow-down of the entire system.

T/S probably works well for many detector subsystems that do not require data analysis, feedback responses and modern graphical display. However, based on experiences of a T/S-based system in Run-7 and new computing re-

quirements for TDC, the HBD requires the upgrade to distributed processing through the implementation of rich clients, based on a true *Client/Server Architecture.* Unlike in the 1970s, today's PCs or even Laptops with multi-core CPUs deliver by far enough CPU power to perform high-speed feedback control and HV monitoring simultaneously. Since implementation guidelines to PHENIX shall be met, a new server additionally to the HV Server is needed: the **HBD Server**, which we will discuss in detail in the latter part of this section. Here the control system running on some client sends an update request and control command to the listening HBD Server on the VA, which uses the RPC-based HV Server/Client pair as a gateway to send the control command to the mainframe and calls the HV Client for the latest channel status, before
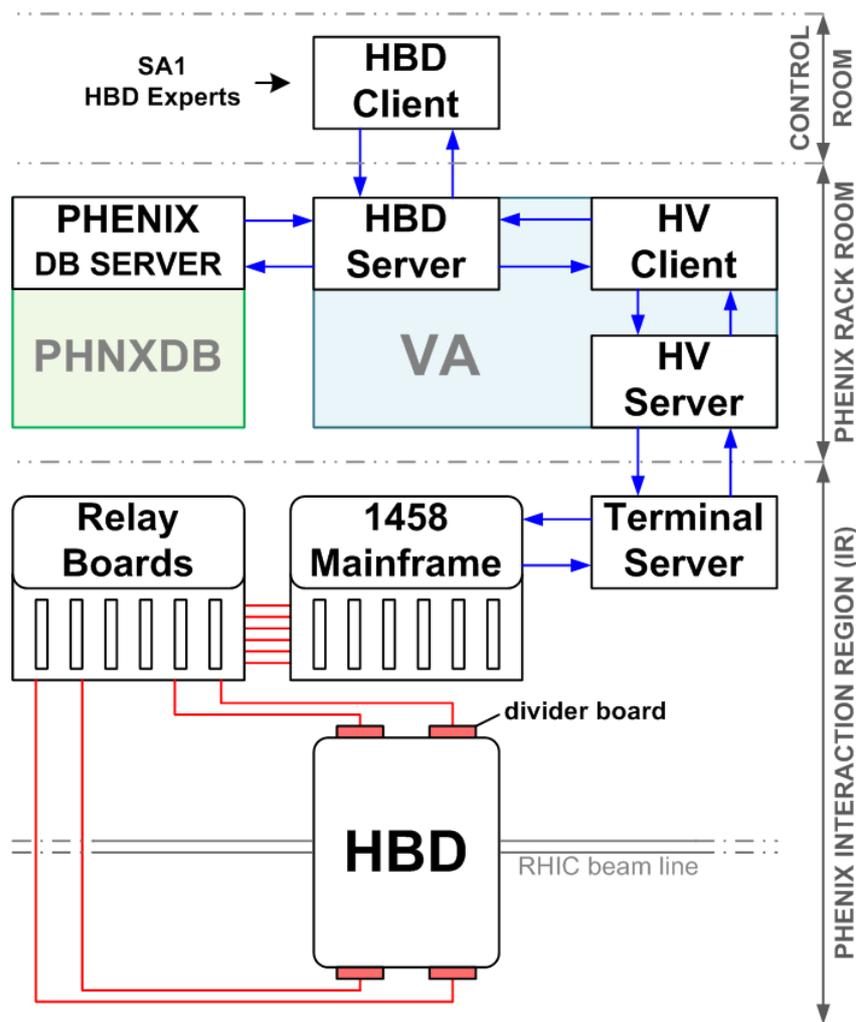
Figure 3.21: Control Overview with the HVC Client/Server model

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in a compact one-time transmission, keeping the network traffic low, the requested data is supplied to the client and independently from this call stores the measurements to the *PHENIX database server*. At this point, the **HBD client** *analyzes* the data in comparison with references and previous event data, and based on loaded control policies performs further control actions. A simplified diagram of the process is shown in Fig. 3.21.

The PHENIX HV client/server is implemented with system-defined Remote Procedure Calls (RPC), which are simple, robust and efficient. For the more complex network-distributed HVC client/server the communication concept of a Message Passing Interface (MPI) has been chosen with a custom written protocol for high voltage control. The idea is based on concurrent programming theory where processes execute in parallel and communicate with each other either through shared memory or by passing messages through network(s). One may find other applications of such systems in computer clusters or supercomputers. Another requirement we ask the final HVC system to comply with is platform independence and superior stability, which brings us to the final question of the choice of programming language.

Most PHENIX control systems have been written in Perl TK or other C-related languages. However, with the above described control outline in mind as well as the time constraints for a proven final crash-tested system to be used in Run-9, one of the fastest growing languages has been considered: Java. Its object-oriented structure merges code and data into indivisible objects with the power and flexibility through the paradigms of class, instance, inheritance and polymorphism. In contrast, Perl being of procedural nature, code and data are kept separately and functions sequentially with no protection for dead loops / memory leaks. Important for a C/S-based HVC is of course the quality of SSH networking, which initially led to the creation of Java by introducing a virtual machine (JVM), making it secure and platform independent, while C or Perl expose their low-level system units and require 3rd party products. In terms of performance, Java has significantly improved since the JavaGrande Conference of High Performance Computing (HPC) in 2000, causing its originating bad reputation in HPC.

As recent studies in [24] have shown, critical tasks as Just-In-Time compilation and Garbage Collection are mastered of significantly approaching level to the highly ranked Fortran MPI, which shows a promising development of new JVMs taking advantage of multi-core chips. Introduced by the NASA Ames Research Center, NAS Parallel Benchmarks can be used to test the performance of systems needed for scientific purposes as they have been derived from computational fluid dynamics. One can for instance run a Fast Fourier

| (a) IS kernel | (b) EP kernel |
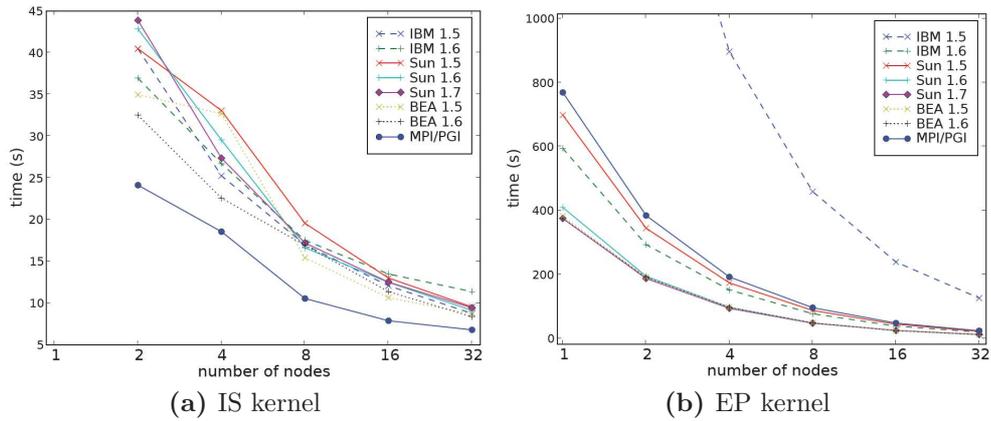
Figure 3.22: Computational performance of Java vs. Fortran

Transformation to solve differential equations, Integer Shifts to move large amounts of data (IS) or an Embarrassing Parallel (EP) to generate pseudo-random floating points according to a Gaussian. A Java vs. Fortran MPI/PGI problem class C comparison of the IS and EP kernels on a Gigabit Ethernet cluster[8] is shown in Fig. 3.22.

As one can clearly see, the execution time depends on the JVM vendor, but overall Java performs close to Fortran, indicating similar computational qualities. In respect to C/S communicational performance, a Conjugate Gradient (CG), sending 429248 50B and 86044 300kB messages over the Gigabit net-

| (a) Execution time | (b) Message density distribution |
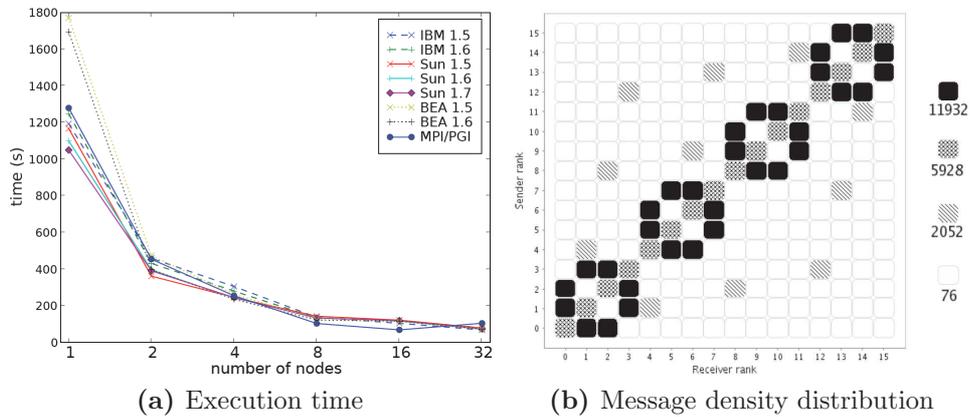
Figure 3.23: C/S communicational performance of Java vs. Fortran for CG kernels

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[8]50 nodes (Quad Core AMD Opteron 2218, 2.6GHz), 4 GB memory, running Red Hat Enterprise Linux 5 with Linux 2.6.18 kernel connected to 4 Cisco-3750 switches.

work, Fig. 3.23 shows that messages are sent in a uniform manner over time, and for all Sun JVMs, Java performs even better than Fortran – a leading MPI.

The previous discussion meets the development requirement to provide our TDC-based system a language to expand with technological progress in future applications. This concludes our decision process of which language to choose for the development of the HBD HVC. The following 4 layer design shall be used for production:

- HBD Server and HVC Client (HVC): Java with latest JVM

- Backup HV Client Call: Perl TK

- Offline Run Data Analysis: C++ with Root

- Offline Run Data Plotting: JpGraph (PHP) for Web.

3.3.3 Dynamic Negative Feedback

With the fundamental conditions for a multi-threaded HVC application being met, we may now present the solution of how high voltage control in conjunction with the TDC model is realized for the HBD software control system. The idea is based on **global and local process control** monitoring/management.

Hence, common control systems use a source of reference to compare their fed-back output with, in order to optimize their control, known as *Negative Feedback*. The popularly understanding to have created a controller responding completely dynamically to its control medium by applying references based resulting controlled variables is a misconceiving assumption, which needs to be redefined. Even if one would use a matrix with each element corresponding to a reference with the control output choosing the element it has to be compared with for further control action, the feedback is still of *static* nature. The rather perspicuous reason can be found in deviations of the control medium by external disturbances not necessarily measurable at the systems output due to its absorbed structure resulting from summarizing each internal process' output with inherited outputs of previous processes. *Dynamic Negative Feedback* requires the measurable evaluation of system controlled variables and their known static reference in conjunction with subsystem references generated by internal processes themselves.

HVC uses an even extended version of this definition (see implemented in Fig. 3.24). A static reference of L1471N module specific voltage and expected

current calibration coefficients, a run-based reference containing demand voltages, trip and trip peak currents as well as desired module activity, and a set of policies representing control demands for various event scenarios are loaded initially to a control monitor (CM), also called watchdog or Eagle Eye. A global control command is sent to the system. The work load is then divided into different processes with each internal function sharing its results to functions following in time through a defined memory. Each functional output is monitored by the CM. With the completion of the process, a corresponding local reference receives the inherited result of the last function and makes an entry into a global *online reference*, which will be used during the next cycle of the process. At the same time, the aggregation and executing command module receives the set of results. If any issues have been observed during the command handling by the processes, the CM can deny to acknowledge the command's execution and initiate reprocessing according to management described in the policy. Otherwise, the HBD or mainframe will be treated with the command. The measured result from the mainframe is then read back into the online reference. At this point, online references are additionally cross-analyzed with static references and policies, before new control actions are issued or previous results optimized.

3.3.4   PHENIX HV Client/Server

Based on principles found in the WA98 HV System of the Large Acceptance Photon and Hadron Spectrometer at CERN, the PHENIX HV system has been redeveloped in 2002 after the failure of an EPICS implementation. The RPC-based replacement, the HV Server and HV Client, hereafter referred to as `hvserver` and `hvclient` respectively, shall be presented based on implementation by HVC.

When starting the `hvserver` it expects the detector specific configuration file *config_hbd.dat*, which contains definitions for the mainframe name (e.g. MF17), the location of the terminal server (e.g. *ts5.phenix.bnl.gov*), the TS port for the mainframe as well as HV channel IDs, their position within the 1458HP rack and 1471N module. GEM and corresponding Mesh channel are always assigned as a pair of neighboring channels and contained within one LeCroy module. This makes it easy when the connection to the Relay boards is made and possible issue tracking gets involved; all channels of one HV module refer to one Relay board. Furthermore, an hierarchical grouping allows to tie the 10 channels of the HBD East and the other 10 channels of the HBD West together, while additionally either a single channel can be addressed via its ID or all channels of HBD East and West together. The structure is as follows:

```
                    idstring "HBD"
                    Mainframe MF17 ts5.phenix.bnl.gov
                    3002
                    Subsystem HBD
                    ChannelGroup HBD
                    ChannelGroup HBDE HBD
                    ChannelGroup HBDW HBD

                    1471 WN1 MF17 0 0 HBDW
                    1471 WN1M MF17 0 1 HBDW
                    ...
                    1471 WN4 MF17 0 6 HBDW
                    1471 WN4M MF17 0 7 HBDW
```

These strings are then simply tokenized and saved to the session-driven configuration of the server. A TCP/IP socket communication to open a Telnet session to the mainframe is established based on the TS location/port. From then on, the server loops over all HV channels periodically by requesting a status update of measured values and settings from the mainframe. Therefore, the 1458's *RC command* is sent, which by specifying the requested property, e.g measured voltage (MV) or measured current (MC), returns a string of latest measurements for all channels. This string is then also tokenized by the server and kept in memory until new updated values overwrite the previous status. The looping frequency is $\sim$ 3-5 chn/s. On the same VA machine, the `hvclient` is then used to either select individual channels based on their defined ID, HBD East or West channels, or all channels of the detector. One can then display momentary settings and measured values of the selection or take immediate action on them. For a client requesting a status update, currently stored data is accessed from the memory and provided to the client in tabular format:

```
Chn    Age   MID     DV        MV        MC       MPC      RUP   RDN    TC       TPC    ···
WN1    0     1471   -2500    -2500.2   -89.636   -89.661   25    25   -109.296   -200   ···
WN1M   0     1471   -2431.0  -2431.8   -0.011    -0.031    25    25     -5       -200   ···
 :     :      :       :         :         :         :       :     :      :         :    ···
WN4    3     1471   -2500    -2500.4   -89.324   -89.390   25    25   -109.180   -200   ···
WN4M   3     1471   -2500    -2500.3   -0.019    -0.025    25    25     -5       -200   ···
```

The server also introduces the concept of "mainframe delay," which is a variable to set of how often `hvserver` reaches out to the mainframe for data updates. The *Age* identifier simply displays then the time of how many seconds ago the present data has been updated. For the HBD this value is set to zero and so allows HVC to process new measurements as soon as data streams in from the Interaction Region (IR). As one can easily see in the return example

above, WN4 and WN4M are going to be updated at the next loop. A summary of all return properties per channel is provided in Tab. 3.2.

Table 3.2: High Voltage Control Parameters returned from the `hvserver`.

Channel Property		
ID	Type	Description
Chn	CONFIG	Channel name define in *config_hbd.dat*
Age	CLOCK	Time after last data update (s)
MID	RETURN	High voltage module ID
DV	CONTROL	Demand Voltage (V)
MV	RETURN	Measured Voltage (V)
MC	RETURN	Measured (Slow-)Current (μA)
MPC	RETURN	Measured Peak Current (μA)
RUP	CONTROL	Ramp Up Rate (V/s)
RDN	CONTROL	Ramp Down Rate (V/s)
TC	CONTROL	Trip (Slow-)Current (μA)
TPC	CONTROL	Trip Peak Current (μA)
MVDZ	CONTROL	Measured Voltage Deadzone (V)
MCDZ	CONTROL	Measured Current Deadzone (μA)
HVL	CONFIG	Hardware High Voltage Limit (V)
CE	CONTROL	Channel Enable/Disable (0,1)
ST	RETURN	Channel Status (ID)

If control commands for demand voltage, trip/peak current, HV generation enabled or disabled, or mainframe on/off, the individual command format for ID-based selection is translated by the server into the mainframe *command LD* and executes the request. In case the PHENIX DAQ is running, an ODPC interface is used to keep a log of mainframe values, which are stored in a PHENIX database.

3.3.5   HBD HV Client/Server

The demand of high-efficient and stable conditions in a multi-threaded dynamic feedback control system induces unexceptionally the ability to provide a solid foundation for simultaneous monitoring without initiating additional pressure on the unit executing final control actions to the detector. Such an installation is not given to us with the standard `hvserver`. The strategy to

solve this problem resides in a *computational one-to-one conversion of TDC*. Let us quickly recall the model and define the idea of this conversion.

Design Principle. Every process represents its own globally static control system (master). At least another sub-process (slave) is needed to allow its transformation to a closed-looped and globally dynamic control system. Both master and slave are hosted on two separate layers, where we mean with a layer, a period of time when several processes or their internal functions are running in parallel. **Imagine a network of communicating processes. A function of one process shall be capable of affecting a function of another process on the same layer by modification of the particular process' control references (global parameters used by functions). This modification is made dynamic by introducing a *control monitor* of the function's performance for each layer and process. A control monitor can be understood as an independent process, which reads local and global parameters of functions during their execution. The monitor writes the collected data to a so-called online reference for this function. The online reference is then utilized to compare present parameters with those found during previous runtimes of this function, which allows the optimization of parameters governing the function in future runtimes. Since the online reference may vary from layer to layer, communicating processes are then capable to impact each others performance dynamically. If these requirements are met, one has found an intelligent control system with the ability to control itself. Such a system demands the fundamental need of the segmentation of control responsibilities, which can be provided by technologies as multi-core and grid computing with a C/S architecture.** This design concept is illustrated in Fig. 3.24.

This simply implies that whenever control to the HBD shall be performed, the collaboration of *the pair*, HBD Server and Client, is needed, making it an indistinguishable entity. Additionally to our previous discussion of C/S architecture, we do not understand the server as being the clients' servant, but rather as being served by client calls. Thus, the HBD server is the master process on the highest level of control hierarchy and may reject immediate execution of the clients' control commands, if either its own stability is in jeopardy or external delivery and other control components are non-responsive. These decisions are made the different policies of operational layers.

(a) Runtime Global   **(b)** Process Internal
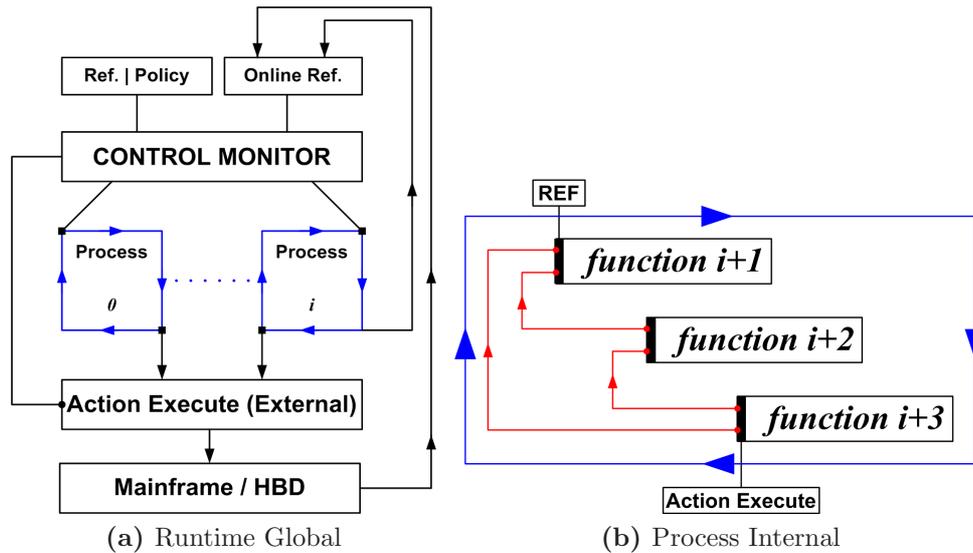
Figure 3.24: Concept of communicating processes – a computational conversion of TDC

Normal Operation. Expecting the mainframe through terminal server or `hvserver` available, the 5 main active layers of the HBD Server during normal operation can be summarized as follows:

1. **Communication Layer**: (1) The `hvclient` is used as a slave to provide a gateway to HBD, whereas the ***hvserver** is completely invisible* to the layer until a broken communication to the mainframe is detected. This structure complies with the PHENIX infrastructure, but does make control actions dependent on this intermediate step; a direct connection to the mainframe would be more efficient and safer, allowing to develop powerful exception treatments. That is why this layer is precisely aware of the `hvserver`'s functionalities and prepared in case of its crash to still maintain stability until a successive reconnection can be established. All clients are suspended during this time. Since there would be no information about the HBD status during this period, the communication layer will be initiating a rush-status analysis as soon as the `hvserver` has been recovered. Based on the emergency settings of the layer's control policy, an optional socket to the mainframe via TS can be opened to either continue control during the unavailability of the HV server or bring the detector to a lower voltage for safety purposes, if for instance the DAQ is not running PHYSICS.

   (2) The client ↔ server communication is realized through the message passing technique. Before any command can be sent to the server's port,

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an initial authentication login procedure (see below) has to be successful, involving a secured connection using the SSH protocol. Once the communication to the server has been established, strings with presenting ID can be passed through the socket.

(3) The Java Database Connectivity (JDBC) API is implemented to read/write from/to PostgreSQL databases on the two PHENIX database servers `phnxdb1` and `phnxdb2`. Each data object receiving data from the client or database uses a convenient database naming scheme by opening the connection to a DB ID, which refers to specifications as corresponding server location, port and DB access conditions that are loaded from an external XML file. Detector experts can so easily change this file in case a swap or reorganization of the databases is required; there is no need to make modifications to HVC.

2. **Data Backup**: Extremely crucial for the reconstruction of a resulting GEM status and response to external disturbances as well as final evaluation of detector performance during an entire run at RHIC, is the ability to look back and analyze the HV data at every instant of running time. There are in general two different kind of backups: a direct 1:1 mainframe response capture and a controlling client analysis capture. The first one is a high-performance thread running on the HBD server, since it is part of the global control enforcement. Activated when starting the server, this process runs independently from any client and is synchronized to backup request by the controlling client through an unique logging ID.

3. **Data Analysis**: The server does only perform low-level data analysis to provide global parameters, such as P/T conversions and binning, to *all* clients. But even these basic computations have to be triggered by connecting clients and are part of the particular data object class called. In our architecture, using rich clients, heavy analytic processing is prohibited on the server side during normal operation!

4. **Control Actions**: Clients have the optional feature to execute child scripts of HVC locally on the VA machine, e.g. to run ROOT macros and plot large amount of data. Another service the server provides is hosting an executable process for external communication as part of a detector emergency alert system. Depending on its configuration, it is able to notify a pre-selected group of HBD experts about the event of a severe detector problem requiring immediate attention. This message can be either delivered via a satellite transmission of either a simple

text message to any mobile device or a phone call with a digital voice. However, these are all partial control actions as they have been initiated by a controlling client. What if no clients are connected? In this case, the server becomes a monitoring client with the power to disable channels, if an expected current draw is exceeded (see TripProtect System), and transforms back into normal mode as soon as a controlling client logs in.

5. **Client Control**: The client sends an ID for a control function specified in the command handler of the server together with the actual data the command shall be executed with. In case data to the mainframe needs to be sent, a new buffered output stream object of an instance of the running `hvclient` process is generated and executed. If the ID corresponds to a database interaction function, the command handler passes the data to the server data class, which depending on the command calls the save- or loadToDB function of the corresponding data object for data parsing and handling.

The high performance conditions for every layer impose certain basic functionalities. First off, the protocol, authentication and server logic have be separated and the ability to transfer/reception of Strings, Bytes, Binary and serialized Java objects over standard TCP connection through a secured SSL/TLS port from identifyable clients a necessity. Since the number of clients cannot be infinite, a threshold of served clients has to be set. Furthermore, in case the server is restarted to load a new XML configuration file or suspended
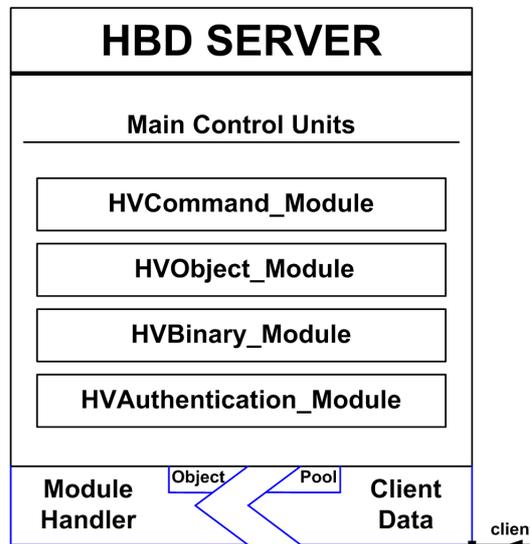
Figure 3.25: HBD Server Design Structure

for any other reason, its connected clients should not be killed. With these fundamental implementations being met, the server's excellent robustness is supported by its exception handling and structure with divisions as illustrated in Fig. 3.25.

Every client connected has its own `ModuleHandler`, which is associated with either receiving or sending `ClientData`. Threads are then taken from the object repository and executed to perform any control action. At start-up of the server, the configuration file *HVCServer.xml* is read and references to all module objects are created. As soon as the boot process has been successfully completed, the Backup Thread is started, and clients are able to login.

Multi-HVC Clients. It is well understood from our previous discussions, 'control' can only exist if a 'monitoring' of its medium exists. As HPC applications of the MPI have shown, one can distribute the 'monitoring' to a multitude of processes or physical machines, but finally the actual control is executed by one single process. If this action is triggered within a defined cluster, the controlling process does not have to be the same for every consecutive loop. However, in the case of HVC, we do allow a human being to execute control actions to the detector as well as multiple clients connecting to the server. This of course raises the question of how safe control can be guaranteed? The following fundamental hard-coded policy has been implemented to address this issue and cannot be changed:

Definition 2 *(Single Control)* *Only one single client can perform control on the HBD, while others own monitoring privileges. An evaluation of user access level is required to enter either one of the two modes.*

Overall, there are three user level: SA1, HBD Experts and Administrators/Superusers. The server does only accept one instance of a SA1 client, while allowing multiple instances of expert and administrator clients. HVC combines all three user levels and only changes the login procedure and access privileges. Let us demonstrate the principle with a first-time login after `hvserver` and HBD server have been started.

The system is primarily installed on the SA1 computer in the Control Room at PHENIX, which is surrounded by the PHENIX firewall and RHIC/ATLAS Computing Facility (RACF) firewall. Running the system with a SA1 access request, a direct connection to the HBD server on the VA machine is established and the main control panel will appear. At this point, full control over the detector is granted.

However, let's assume experts or assigned superusers install the platform-independent HVC client on their Home-PC, the user at start-up will first see a

splash window indicating the software version, before a first-time access frame appears. Here the path to the user's RSSH public-key and a 16-digit authorization key are requested. Since the HV server is running on a VA machine belonging to the Federal Computer System at BNL, high security guidelines are introduced not just to follow U.S. Government policies but prevent any vulnerability of the HBD. Therefore RACF uses MIT's authentication system Kerberos, where a Ticket-Granting Ticket (TGT) is generated for approved scientists, in order to control access to the computing grid. The HV Control System additionally introduces an authorization key that can be only provided from system administrators, or designated HBD experts. Together with the TGT or public key, the system connects to the RHIC SSH gateway *rssh.rhic.bnl.gov* with provided BNL ID, continues to SSH into *va022.phenix.bnl.gov*, the HBD assigned VA machine, and finally is able to communicate with the HBD server. The main control panel appears in Expert Mode, but all control functionalities are disabled, since the SA1 currently online; only monitoring is possible at this point. The difference between Expert and SA1 mode is based on the possibility to modify control policies of the detector; one of the primary access units is the *ParaConfig Exchange Module*, which we will discuss under Control Subsystems. In case the Expert decides to take over control, he can perform such a request under User Management. The SA1 is notified and asked to acknowledge. If the request is denied, the Expert will have to contact the PHENIX counting house directly to continue. If no response (causing timeout after 10s) or permission is granted, the Expert will receive full control, while the SA1 allows only monitoring functionalities. The same procedure applies to two Experts exchanging control privileges.

At this point, both HBD Server and HVC Client are running with various sub-processes already actively monitoring in use of the server's Communication Layer. Any control action, either by user or system, is based on a suite of control divisions, which we shall study in the following section.

3.4   Control Subsystems

The HBD HV Control and Monitoring System (HVC) represents an entire suite of inner-dependent subsystems with each contributing to the successful operation of the HBD. The clear division of control functionalities follows the concept of segmentation in support of performance and self-stabilization. Although, HVC enfolds about 130K lines of program code with a client contribution of $\sim 70\%$, we will attempt to dissuss the main division of each subsystem sequentially, but only in respect to their functionality affecting the overall control of the HBD.

3.4.1 Mainframe Backup Thread

The momentary status of all GEM-stacks in the detector is measured by the 1471N, stored locally on the 1458HP mainframe and kept in memory for a certain rate by the `hvserver`. There are 5 crucial reasons why each of these channel updates have to be permanently logged for multiples of the global response time constant τ_S:

- Offline Reconstruction of GEM behavior to external disturbances (e.g. $\Delta P/T$, magnetic fields);

- Performance Studies of HBD during an entire Run at RHIC;

- Performance Monitoring of HVC control actions by detector experts.

All of these investigations can be done with offline analysis tools. The latter is needed for HVC calibrations, usually done at the beginning of a Run at RHIC or if any hardware changes to the HV System during a Run. One may also consider the state reconstruction of channels or stability and trend analysis for GEM-stacks by the Control Monitor of HVC clients, which are optional and can be defined in their corresponding policies. This option is very useful to allow HVC to do online reconstruction. The control system would become sensitive to long-term GEM status changes and could recommend control policy changes to detector experts through a comparison of detected event patterns in correlation with simultaneously recorded data of other sources, e.g. module gain, P/T, HV changes or the magnetic field in the central region.

Data Management. Therefore, *hvdb*, a new PostgreSQL database of high efficient complex structure has been developed for HVC and is hosted on the PHENIX server *phnxdb2*. The entire mainframe capture for all channels is stored in the so-called *¡mod¿log* tables, which are using the Lehman-Yao high-concurrency B-trees as their indexing method. Each table entry contains GEM-stack and Mesh data without any modifications directly from the 1471N modules. Additionally, six identifiers (GID) have been introduced to associate entries with those from other module tables as well as control actions and their results initiated by the HVC client (Tab. 3.3).

Data Backup Sequence. The general principle of how HVC's Central Mainframe Backup System is operating shall be discussed in the following. As soon as `hvserver` is running, the HBD server can be started by executing the `startHBD` on the same VA machine. In the *main()* the *HVCServer.xml* is

Table 3.3: Global Identifiers in `hvdb` for measured 1471N HV data.

GID	Source	Binding
id	HVC Server	Measurements throughout all modules
logid	HVC Client	Control Actions and Measurements
run	DAQ Run Control	Segments of measured PHENIX data
runid	HVC Server	PHYSICS or JUNK/CALIB data
logtime	VA Server	Measurements taken at unique time
bias	HVC Server	Bias voltages applied

loaded to configure the server, before the *HVThread()* is called. This will then first load HV calibration data from the hvdb using the ParaChainDataObj and writes each element to the vcalib vector object. The main data backup loop runs then with a frequency of $\tau_S^{-1} - const_{db}$ Hz in order to ensure new measurements for every update. The setting for the global response time constant and a constant depend strongly on the channel update rate of the `hvserver` and the network traffic restrictions to the database server respectively. For Run-9, the following optimized settings have been used:

$$\textbf{Run-9 Timing:} \qquad \tau_S = 5\text{s}, \, const = 0.057. \qquad (3.9)$$

This means it takes about 7s to complete one backup loop. Its sequence begins with a check of the mainframe power, which if OFF will timeout with a standby flag for 3s and check again. Otherwise, HV data is imported using a self-terminating hvclient runtime process with a buffered-stream readout of the data and finally stored into a vector. If the data is corrupted or the vector empty, a timeout of 7s and data exception flag is set, which will return us back to the beginning of the loop. A successful data check will initiate the preparation of global settings for the backup execution sector. First the system data and time of the VA machine are saved in `SDAT` and `SCLK`. Then an unique global ID issued by a controlling client is saved as `logid`. Since the clock on the VA machine and the clients host can be very different, e.g. an expert runs the controlling client from California or in other timezone of the world, `SCLK` and client clock `CSLK` are not synchronized by time, but correlated by the `logid`, which indicates the latest control command executed to the HBD. For slow P/T monitoring, every 10min pressure and temperature data is loaded from the *hbd* database, converted from inH20/K to Torr/K and transferred to the calibrations database *calib*. With these three global parameters set, the backup execution sector is entered. Here a connection to hvdb and daq is established. Since every measurement throughout all channels shall be not only identifyable through a date and time, but also an universal ID, the clock

sequence on hvdb is raised by one. The DAQ runnumber is the primary identification of datasets in PHENIX and very important for the analysis of Physics HBD data. Therefore, we extract the runnumber and runstate from the daq and define a runid to indicate PHYSICS and JUNK/CALIB runs. We also calculate the applied bias using vcalib. Finally, the entire set of data collected is then transferred to the ¡mod¿log tables of hvdb using prepared statements.

This backup system represents the only continuous thread on the server side. As mentioned multiple times, the main control logic is handled by the server's counterpart. The remaining subsystems of HVC we are going to discuss in this section belong to the client.

3.4.2 Global Detector Status Module

At the very moment, the authorization procedure succeeds during the HVC client login and access has been granted to enter the system, the most extensive control-required division becomes active, the GDSM (Global Detector Status Module). It is responsible to feed all other components of HVC with new measured data, organizes exception handling and shared internal/external memory, while these processes are controlled and monitored in respect to τ_S. In other words, one can understand GDSM as a watchdog of floating data through the internal network of processes and allows them to communicate with each other. The boundaries of the GDSM are protected against access requests from any non-GDSM process; interruptions within these walls are strongly prohibited and secured this way to prevent any stability issues on the data update level. However, it provides the so-called Data Exchange Module for local and global channel updates to hvdb, which is accessable by every process throughout the system, allowing to update these parameters based on detected or initiated status changes.

GDSM Startup. The first action in HVC's *main()* function is to generate a logfile locally in the user's file system to which exceptions are written to by GDSM's *ErrorLog* class. New files are automatically generated if the file size exceeds 100×10^3 bytes. Every single function throughout every single class of the entire HVC client catches any possible exception during its operation, prevents the avalanche to other processes and reports the cause and treatment of the exception to the *ErrorLog*. Following, the *Main Control Panel* is initialized, displayed and detected by an event listener, triggering the reset of `hvserver`'s *mainframe delay to 0s* and secondly the execution of the **HV Data Update** thread as well as synchronized *System Clock* thread in parallel.

There is only one class containing all control functions, the **ActionBean**, which is heavily under supervision of GDSM's *Control Monitor* or so-called *Eagle Eye*. If any process would like to execute functions in *ActionBean*, the passing of requested functions' command IDs to the class' only visible *synchronized object* is enforced, which may deny (based on configuration policy) or permit the execution of desired control functions in the order they are received. One can so implement internally the C/S philosophy and guarantee a safe control handling environment.

The update thread operates then a status bar on the *Main Control Panel* and sets its progress to zero, before requesting the execution of a system-wide *data update function* in *ActionBean*. If the execution is successful, a timeout according to the global response time constant τ_S is initiated and visually indicated by the progress bar in small iterations preparing the user to expect new data streaming in as soon as the update loop is complete. The GRTC is used by all processes according its extention of the TDC model. For Run-9, the following setting has been chosen:

$$\tau_S = 5s, \tag{3.10}$$

which as one may find is matched for the same reason with the server's configuration 3.9.

Data Update. Let us now have a closer look at the update function. It contains a series of dependent actions, that order has been carefully timely balanced in respect to their execution, analysis and handling times, their influence on the overall system stability and inner-dependencies on preceding actions of the series:

1. **Controlling Client.** The Single Control rule for clients as defined in 2 can only be enforced, if clients can communicate their access level with each other. This is realized indirectly through the HBD server. Due to the hierarchy of user levels, a distinction of two cases is made already at the level of the data update: (1) If the current user of this client is not the SA1, a request to the server is sent to update the local system of an existing SA1 client. The information is stored in shared memory of the *User Management System.* (2) In case the current user is identified to be the SA1, the server is questioned if any 'control shift' has been requested by an Expert. If this proves to be true, the SA1 is notified and looses

control privileges.

2. **MF Channel Data.** A complete caption of parameters listed in Tab. 3.2 for all channels from the 1471N HV boards is stored in a data vector and checked for corruptness. If this initial test fails, may the vector be null, the update is ignored and a clone of the previous data is used downstream this series until the function is executed again with the following update cycle. Otherwise, the mainframe data object receives the vector to tokenize and store the components to the data memory.

3. **Local/Global Status Parameters.** The current control status of the detector is represented by *hvdb*'s *globalpara* and *controlpara* data sets and modified by GDSM every time at least one of their parameters is proven to have changed. The first contains information as for example mainframe power, bias or trip protection on/off, while the latter identifies individually each channel's trip or ramp status etc. (see below). At this point of the sequence, these parameters are requested from *hvdb* and kept in the GlobalPara data object (see below).

4. **Channel Configuration Data.** Every single channel is treated differently, may it be from operational voltages to trip currents and bias voltages (see ParaConfig Exchange Module). These configurations or rather control parameters are loaded from *hvdb*'s *configdata* set and used to calibrate monitoring processes and to perform finally control on the detector.

5. **Fast Status Modification.** In rare cases, the MF channel data sets do not include general mainframe parameters, but do have significant impact on control and primarily display – specified requests are sent to the mainframe to compare the current state with the previously reported status captured in hvdb. Typically the power status of the mainframe needs to be verified. If data from step 2 does not match with the MF return of the actual power status, *hvdb* is updated accordingly and the previous memory entry replaced (fast).

6. **Data Display Distribution.** Frame labels indicating the global detector status on the Main Control Panel, or the channel activity status in the Module Control Panel or channel configuration settings in ParaConfig Exchange Module's Options Panel are updated throughout the entire system under access of the corresponding data objects received in step 3 and 4.

7. **Slow Status Modification.** Global or local status parameters stored in the database as *channel trip states* have to be always synchronized with the actual status on the mainframe to allow universal monitoring. Therefore, data received in step 3 and 4 is put into correlation with possible scenarios that may have changed their previous state: e.g. tripped channels have been disabled/enabled to recover or modifications that have not been initiated by HVC, e.g. a power loss of the mainframe rack. Possible corrections are made to hvdb and displayed during the next update cycle (slow).

As one can see, we are using hvdb as partial external storage or rather 'infinite' memory extention to the controlling client's local, allowing monitoring clients to essentially be synchronized with each other without any direct communication necessary. Therefore, the HBD server accesses in multiples of τ_S the database server once and keeps the current set of data updates ready for connecting clients. In that sense, the C/S architecture shows its real power.

The display of GSDM results is already initiated in step 6 of the update sequence, but can be extended simply by accessing the corresponding data objects.

Trip Detector Algorithm. A basic rule for transmissions to *hvdb* says that no entries of channel states can be made without verifying the status on the mainframe. Hence, if a channel has been enabled through the Module Control panel, the system is not allowed to make an entry to the database; it must first verify if the transmission has been successful. The very same applies to trip status changes. In the last step of the update sequence, a small trip detector algorithm synchronizes *hvdb* with mainframe and uses the knowledge from Section 3.2.2. The principle works as follows.

Let c_{mf}, c_{db} and c_v be counters of tripped modules out of n HV channels reported by the mainframe, hvdb for hardware and hvdb for virtual trips respectively, where $n = 40$ for currently 20 modules installed in the HBD. The trip vectors for mainframe v_j^{mf}, hvdb v_j^{db} and its update v_j^{dbu} (trip: 1; no trip: -1, default), as well as 2×2 data matrices $\mathcal{A}_{x|y}^i$ (GEM-stack), $\mathcal{A}_{x|y}^{i+1}$ (Mesh) and data vector a_z^j for trip results loaded from memory (step 2 and 3 of update sequence) for respectively GEM-stack, Mesh channels and hvdb of the entire module. While i, j indicate channel/module indexes, x, y, z are state IDs of

following meaning:

$$
x = \begin{cases} 0 & \text{if chn enabled;} \\ 1 & \text{if chn disabled.} \end{cases} \quad y = \begin{cases} 0 & \text{if chn operating;} \\ 1 & \text{if chn tripped.} \end{cases}
$$

$$
z = \begin{cases} 1 & \text{if mod hardware tripped;} \\ 2 & \text{if mod virtual tripped.} \end{cases}
$$

First let us find the trip vectors for various scenarios with $0 \geq (i+2, j+1) < n$, where we define trip $= 1$, no trip $= -1$ (default):

$$
\mathcal{A}^i_{1|1} \wedge \mathcal{A}^{i+1}_{1|1} \longrightarrow v^{mf}_j = 1 \tag{3.11}
$$

$$
\mathcal{A}^i_{1|(0,1)} \wedge \mathcal{A}^{i+1}_{1|(0,1)} \wedge a^j_1 \longrightarrow v^{db}_j = 1 \tag{3.12}
$$

$$
\mathcal{A}^i_{0|0} \wedge \mathcal{A}^{i+1}_{0|0} \longrightarrow v^{mf}_j = -1 \tag{3.13}
$$

$$
\mathcal{A}^i_{0|0} \vee \mathcal{A}^{i+1}_{0|0} \wedge a^j_1 \longrightarrow v^{db}_j = 1 \tag{3.14}
$$

$$
a^j_2 \longrightarrow c_v + 1. \tag{3.15}
$$

Since we are only interested in mismatched mainframe and database vector elements, we are detecting 3 possible state variations:

- Both GEM and Mesh channel enabled & tripped within $t - \tau_S$, but *hvdb* represents module as not tripped;

- Both GEM and Mesh channel enabled & recovered and operating, but *hvdb* represents module as tripped;

- Both GEM or Mesh channel disabled & not tripped, but *hvdb* represents module as tripped.

In the latter state, we already eliminate its counterpart, since we know from the LeCroy's FPGA that there is no possibility to ever have a channel disabled and shown as tripped at the same time. If we then ask for this comparison with the requirement $v^{mf}_j \neq v^{db}_j$ and $0 \geq j < n/2$, we find

$$
v^{mf}_j = 1 \wedge v^{db}_j = -1 \longrightarrow v^{dbu}_j = 1, \ c_{mf} + 1
$$

$$
v^{mf}_j = -1 \wedge v^{db}_j = 1 \longrightarrow v^{dbu}_j = 0, \ c_{db} + 1,
$$

where inconsistencies are counted and stored in the v^{dbu}_j, indicating what *hvdb* should actually look like. The final stage is then to transfer this information to hvdb. Here we also consider the previously global trip status of the detector, which was set with the philosophy: If at least one channel has tripped, the global trip status – c^{global}_h for hardware, c^{global}_v for virtual trips – must follow and

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indicate a trip. Based on the results gathered, an update to hvdb is necessary if at least one of the following statements are met:

$$c_v = 0 \wedge c_v^{global} = 1 \implies \text{ to hvdb: } c_v^{global} = 0;$$

$$c_{mf} > 0 \vee c_{db} > 0 \implies \begin{cases} \text{to hvdb:} v_j^{dbu}; \\ c_{mf} > 0 \wedge c_h^{global} = 0 \implies \text{to hvdb: } c_h^{global} = 1; \\ c_{mf} = 0 \wedge c_h^{global} = 1 \implies \text{to hvdb: } c_h^{global} = 0. \end{cases}$$

This brings us of course to the question: How can these updates sent to hvdb as efficient and safe as possible, without any interruptions of the main update loop – key word 'data exchange.'

Data Exchange Module. The enormous set of processes working with the local and global status data, requires a procedure to modify single parameters of the overall status without conflicting with other processes, while ensuring identical transfer string generation. The idea is to leave the organization of correct structure to a data exchange object (DEO) and the secondary readout and transaction to the execution module in ActionBean. The particular process then just needs to write individual updates to global and/or local status parameters of DEO and request from ActionBean to execute the hvdb status update function. Once this is done, the exchange module generates two new objects, *global* and *local vector* para, and loads the entire data from DEO into these plain parameters. For those entries that have not been changed by the initial process are still on their default value. In case a new value is detected, the global or local para data is entered into a newly generated global and local data object. Otherwise, the shared memory is accessed and the latest hvdb data is used to fill unchanged status entries. Finally, both objects are combined into one single transmission message and sent to hvdb. Before the Data Exchange Module declares its success, all DEO modifications are reset to their default.

3.4.3 ParaConfig Exchange Module

The most important information for any control system is the availability of control parameters and resources to compare the controlled output with. In section 3.1 we have discussed the need to allow a human being to modify these crucial settings, instead of using a fixed resource with dynamic modifications by HVC alone. Independently from the aspect that one should *never leave control to a machine* without scientific expertise and insight of a human, one needs to face the fact that this may introduce a lack of safety or performance when erroneous parameters are provided. This introduces the idea of

the ParaConfig Exchange (PCE) Module, which has the purpose to minimize the propability of resulting damage to the detector by defining operational boundaries for HVC users. Furthermore, security issues by using an accessable database are addressed.

There is only one access point in HVC to modify or add control parameters: the *Options* panel, which is available only to clients logged in as Experts and allows to observe and change the following main configurations:

- **Detector Gain.** The gain or amplification factor of collected charge on the readout pads over the initial entered primary electrons entering the Top-GEM is directly related to the field strength within the GEM holes and corresponding transfer and induction fields. A selection on what gain the detector should be run on can be made, starting from 2000 to 10000 in 2K steps. PCE will then already on the HBD server side choose from individual pre-defined settings per module and return to the client operational voltages to achieve the desired gain.

- **Plateau Voltages.** The Standby and Operating voltage plateaus can be defined for each individual GEM channel, where a default HV limit of 4.5kV is set. For individual stack tests, one can select modules that should not be included for ramps to each of these plateaus.

- **Forward/Reverse Bias.** The Mesh voltages are defined by the dV across the Top-GEM and Mesh. The polarities for Forward and Reverse Bias can be ignored, but their limit of default $30\mu A$ should not be exceed.

- **Ramp Behavior.** There are four HV ramp-up modes that allow to configure the voltage application incrementally to their Standby or Operational plateau. One can either set channels to follow a linear continuous ramp (V/s), a step function of equal steps (integers) and timeout length (s), an automatically calculated raise in exponential form with a slow asymptotic approach to the final target voltage or an individual ramp procedure with custom timeouts can be defined. The ramp down behavior is set for all channels to be linear with a constant ramp velocity.

- **Trip Currents.** The trip thresholds (μA) for each GEM stack can be defined based on the difference above the standing current measured by the LeCroy. The limits for GEM Peak and Mesh Slow/Peak currents for every channel are set absolute, since these values are not required to scale with the applied voltage.

- **TripProtect.** In addition to hardware trip currents, one can define more sensitive trip thresholds for each channel in terms of the percentage of the expected current (EC). The TripProtect System, as discussed later on, will use these percentages to set the software threshold to EC + (%/100 × EC). If the measured current exceeds this limit, the system will issue a so-called *virtual trip* and ramp the channel down.

The GDSM activates in section 6 of the update function in ActionBean the data transfer of control parameters currently on-file in *hvdb* to the PCE module, which are then displayed in the Options panel. At the entry point of control data to PCE, each settings is analyzed in terms of format, boundary conditions and unauthorized modification. In the latter case, a possible thread by an intruder or data corruption on *hvdb* is expected. Therefore, the current state of HV applied to the detector is reconstructed with GDSM data IDs. First, measurements reported by the mainframe are compared with the control data. Let's assume a complete match is found, then the user may modify the present settings and request the update of control parameters. At this point, PCE will load the entire data set from all input fields to the Customs' Data Verification Procedure, which ensures that boundaries for all settings are met. In case the verification fails, the user is informed and pointed to the incorrect setting. Otherwise, a transaction data message with an unique client-specific encrypted *hbdstatus* ID is generated and entered into the control data and status data sets of *hvdb*, indicating that the HBD may expect a change of control parameters soon. This unique hbdstatus ID contains property changes of associated channels as well as information about the requesting client. One can also optionally update the mainframe directly with configurations except demand voltages for GEM and Mesh channels. This option is favorable for situations when a planned ramp-up of all channels needs to be executed with a minimal completion time.

Suppose with the beginning of a new update cycle of GDSM, the initial mapping of the current mainframe state $\mathcal{S}$ with the proposed new mainframe state $\mathcal{S}'$ represented by the received control data does not succeed. The latest non-executed *hbdstatus* ID is being identified in the status and control data sets, which corresponds to one global *logid* that is being used by the backup thread of the HBD server to allow data tracking. With the channel information of property updates contained in the hbdstatus, corresponding data sets are accessed where a compact timeframe is defined by the same *logid*. In order to verify that the control parameter update request has been issued by an authorized client, the following conditions have to be met:

$$id_{chn(i)} = id_{chn(j)} \wedge t_s - \frac{\tau_S + const}{2} \leqslant t_i = t_j, \forall i, j \in \mathcal{S}'_{chn(id)},$$

where id stands for the unique sequence number every channel entry by the Backup thread receives, t_s the Unix time referring to the entry of the hbdstatus ID in the status and control data sets, $const$ the processing time defined by the HBD server and $t_{i,j}$ represent the Backup thread entry times for channels i, j determined by the hbdstatus ID. Furthermore, the user identification portion of the hbdstatus ID is verified with registered Expert users of HVC. If this verification procedure succeeds, PCE will allow the user to either further modify present control parameters or grant their direct transfer to the mainframe.

3.4.4 Detector Power and Bias Master

The control of the mainframe power and module bias setting illustrates very well that every process throughout the HVC client, requires the collaboration with the GDSM.

Assume for a moment such collaboration would not be available. In this case, one would simply issue the MFOFF command to the mainframe, which disconnects every channel from HV generation; the MCU on all 1471Ns in the mainframe crate will ramp every non-disabled channel with the chosen RDN speed to zero volts, eliminate the serial stream to the DAC, while the FPGA blocks its input via chip select and stops the phase production to the FETs. However, all channels do still have the status 'enabled' in the EEPROM, which will result in a *loose-of-control* scenario when the mainframe is being turned on again: all channels will ramp at the very same time to their previous demand voltage setting, may it been on Standby or Operational, and if there would be no TripProtect System (see below) the entire detector would not thankfully virtual-trip. If conditions have changed at the time of reactivation, for example, relatively high backgrounds are measured in PHENIX or the central magnet coils are operated or lower operational voltages are required due to a significant change of P/T in the IR – this uncontrolled ramp would maybe have caused a possible damage to the detector.

In respect to data taking, an immediate change from reverse to forward bias during a PHYSICS run, would cause unusable data segments hereafter, since due to inversing dV between Mesh and Top-GEM, ionizing particles would not be rejected anymore.

With the introduction of the Detector Power Master (DPM), status data can be directly requested and immediately analyzed for selective actions, since in section 5 of GDSM's update function, the MF power status as reported directly by the mainframe and its *hvdb* representation have been synchronized. The DPM then disables every enabled GEM-Mesh pair and sets both chan-

nels to a demand voltage of zero, which is stored in each EEPROM of the 1471Ns. If the action is confirmed by GDSM after successful ramp down, the Data Exchange Module is used to reset all global status entries in *hvdb*, before the mainframe is completely turned off. In case of sudden power loss of the mainframe rack due to a defect of the cooling system and following interlock of exceeded rack temperature, the 1471N will not issue immediate HV generation as soon as power supply from the 1458HP resumes, but also does not reset demand voltages and 'enable' flags for each channel. This is why DPM verifies each channels' DV and CE state, and if necessary resets these parameters, before the mainframe is turned on.

During a zero-field run at PHENIX, meaning the central magnets are off, while beams are still in the RHIC rings and collisions taking place, one may like to take calibration data and wish to change from reverse to forward bias mode. This change follows a two-step preparation process: First, the current DAQ status is requested from GDSM. As soon as it is shown that no PHYSICS data running is active, a flag with the request to change the module bias is set in *hvdb* and in local memory in correlation with a bias set verification by the PCE. Since this change involves the modification of voltage to the Mesh channels, only the Ramp Control System (see below) is authorized to perform this change, which however relies on the correct bias inspection by the Bias Master.

3.4.5 Module Control Master

The control over HV channels is always only permitted in the form of GEM-Mesh pairs or modules. The LeCroy obviously does not know the difference between these two channels and their meaning; thus, their synchronized operation must be guaranteed. Therefore, the *Module Control Master* ensures the strict compliance of this fundamental rule and allows the user to change states of either individually selected or entire HBD East/West modules. There are 4 states every module or pair member may experience:

- **Disabled.** There is no phase generation by the FPGA and the DAC input is blocked. The HV output to module is not possible!

- **Enabled.** The phase generation by the FPGA is active and the MCU supplies a serial signal to the DAC in order to achieve the requested demand voltage (DV) based on the calibration coefficients stored in the EEPROM. The HV output to module is possbible!

- **Hardware Trip.** Due to either exceeding slow, peak or AC current thresholds, the FPGA discontinues phase generation as well as the MCU does not supply any serial signals. The HV output to module is not possible!

- **Virtual Trip.** The TripProtect System may disable and set a module's demand voltage to 0V, in case a lower or higher current threshold for the particular channel is exceeded. The HV output to module is not possible!

The Module Control is a live monitor of these four states as it is incorporated in GDSM's data distribution section of its update function in ActionBean. In order to change a channel's state from disabled to enabled, one needs to first use the Detector Power Master to turn the mainframe power ON and then select the desired modules in Module Control to request a change of their state. At this point, each selected GEM-Mesh pair's demand voltage is set to 0V. If the measured voltage indicates an ongoing ramp down, the system monitors the module until both pair members have reached 0V, before the corresponding channels are enabled and ready for HV application.

If a LeCroy-issued hardware or TripProtect-issued virtual trip occurs, one can use Module Control to recover these trips. The 1471N firmware requires a state transfer from its tripped status to disabled and then enabled, in order to allow HV generation to this module. Since for virtual trips, the corresponding channels are already disabled, one only needs to enable the channel to recover. Module Control will then finally reset via GDSM the status IDs for these modules.

The internal structure of Module Control is based on a high-efficient, high-performance pointer technology as introduced in the C-programming language. While Java is naturally not designed to draw direct links to references, a pointer structure has been recreated by pointing each module to a pre-specified position in the code; no memory intensive loops are necessary anymore. Due to this design, Module Control owns the fastest control command execution throughout HVC.

3.4.6   Ramp Control Algorithm

The core of every HV System belongs to that algorithm that is responsible to apply high voltage to its modules in a safe and effective manner. Due to the requirements of the PHENIX control infrastructure, HVC is demanded to use the `hvclient` as a commanding tool for all parameter submissions and so relies

on the stability of this underlying transfer object. Unfortunately, it has been found that the current version of this client/server may reach a buffer limit of acceptable commands within a certain timeframe. In respect to the additional HBD-specific request of synchronized GEM-Mesh channel operation, one can easily assume that if such buffer limit is reached, only GEM or Mesh channel could receive HV without the other pair member and so cause a hardware trip of the Mesh channel due to momentary current draw (trip current set low) as result of a Zener opening the path to the Top-GEM resistor chain to ground when a dV of 250V is exceeded. Considering such a scenario as a rather violent process, HVC's *Ramp Control System* has been designed to eliminate any possible communication issue to the 1458HP mainframe, while allowing synchronized ramping of individual modules as well as bringing up the entire detector to its operational level almost completely synchronized with a maximum delay time from channel 0 to 19 of $< 2s$. The system is based on a complex control algorithm, which we shall discuss in the following.

Overview. The idea is to divide control responsibilities into two threads synchronized to each other. One, the Ramp Control (RC) System shall be handling the entire logic and observation of the data transfer, while the other, the Mainframe Control (MC) System shall be executing the transfer to the mainframe in collaboration with RC. After a primary initialization procedure, where the TripProtect System is terminated and all process data is gathered, a simulation of the proposed ramp provides, if successful, a single data matrix Λ_{ij}, which is transferred to MC for upcoming upload requests to the mainframe. There are overall two transfer requests operated and monitored by RC. In case the simulation reported a ramp to a *higher voltage* (e.g. Standby to Operational) based on the currently measured, the *transfer request 1* is sent to MC, including trip currents, trip peak currents and ramp up/down velocities for GEM-Mesh pairs. MC verifies this request and executes the transfer of parameters from Λ_{ij}, which were verified by the ramp simulation and therefore require modification on the mainframe. In the meantime, RC awaits a successful report of the transfer by MC, before GDSM provides constant new data packages to RC for the monitoring of the transfer. As soon as it has been proven that all transfer parameters are in place on the mainframe, *transfer request 2* is issued. This request includes the demand voltages for GEM and Mesh channels. The procedure as for transfer request 1 is repeated. However, not only the successful transfer of demand voltages, but the resulting measured voltages on each channel are carefully monitored. If for any reason, the ramp does not follow precisely as pre-calculated during the simulation, RC will force

a correction and activates the resend option of MC. As soon as the measured voltages have reached their demand voltages, a status update to hvdb is sent, the TripProtect System reactivated and RC put into Standby mode. In case a ramp to a *lower voltage* (e.g. Operational to Standby) is scheduled, trip currents or trip peak currents would not be uploaded to the mainframe during transfer request 1, since the entire detector would trip off, if the calculated trip setting for the target voltage is lower than the currently measured current at higher voltage. This scenario is very likely if one ramps from Operational $\sim$ 4kV to Standby $\sim$ 2.5kV. Therefore, all trip settings are transferred after successful completion of transfer request 2.

Initialization Procedure. The RC System can be activated by either a system call, e.g. if an automatic trip recovery is enabled, or a controlling client through the Main Control panel with the selection of Standby or Operational. In both cases, an activation function in ActionBean is called, which will either start the RC and MC thread if the function is being executed for the first time or release the RC System from its Standby mode – a 1s timeout loop. First on RC's duty list is the identification of the originating Ramp Call, may it be for Standby, Operational or Trip Recovery ramps. Before the actual initialization continues, the Channel Enabled (CE) status from GDSM is requested. If at least one GEM-Mesh pair is enabled, all monitoring clients are notified about the ramp status via the Data Exchange Module, otherwise the process is aborted and returned to Standby mode. Due to the charge up effect and additional current draw during ramping, the TripProtect (TP) System is terminated during this time in order to allow RC to operate the HV without virtual trips. For stability reasons, TP does not allow immediate interruption of its process. Therefore, RC waits for the successful termination report from TP, which resides in the meantime of HV operation in its own Standby mode.

In order to achieve an optimized output for demand/bias voltages in respect to the actual applied voltage, HV calibration coefficients are loaded from the HBD server (hvdb) directly into shared memory. This data is not required constantly and so is not part of GDSM's update function. Finally, the entire mainframe, status and calibration data sets are imported and stored in their own data objects, which shall be used for the ramp simulation. The operation of the main process can be precisely configured through various RC parameters, e.g. timeouts, iterations to target voltages (ramp mode) or boundaries, as well as state vectors and matrices, e.g. Λ_{ij}. The initialization of these global run variables is based on an internal policy reference and can only be changed by Administrators or Superusers. Before the main RC process is activated, all data objects are analyzed for secondary corruption, meaning except of being

null, the order and boundary limits of each value have to be approved. In case the verification fails, the Abort function is called, which updates *hvdb* and monitoring clients of this action, reactivates TP and brings RC back into Standby mode.

Simulation of Ramp.   The entire logic of RC is contained in the simulation of the requested ramp for each module. The state of each channel at their final target voltage needs to be pre-calculated, e.g. the trip current above an expected standing current or bias voltage. Furthermore, during the monitoring of the ramp, one would like to estimate how the LeCroy should perform optimally during its voltage iterations to finally reach the desired state. The transfer results are stored in the data matrix Λ_{ij}, where i indicates each of the 20 GEM/Mesh pairs and j the desired change of properties. Starting with the first module, by default EN1, corresponding MF, status and calibration data is written to local variables, whereby a mapping of their channel IDs is required. When this check is passed, the desired demand voltage DV' for the GEM is set to either Standby, Operational or a custom (e.g. for calibrations; see Section 4.4) value, which is based on the original system call. In comparison, demand voltages for GEM (DV) and Mesh (DVM) presently on the mainframe are written to local variables. This allows us to determine the new trip current TC' for the GEM's desired DV':

$$EC' = \frac{DV'}{\sum \left(\sum_{\chi=B,M,T} R_\chi \right)^{-1}}, \qquad (3.16)$$

$$TC' = EC' + TC^+, \qquad (3.17)$$

where EC' represents the expected current at DV' over the parallel resistance of the corresponding divider and its installed resistors of precisely measured value for Bottom (B), Middle (M) and Top (T) GEM. The additional current above standing, TC^+, is defined within the PCE module using the Options panel by HBD Experts.

Before the new trip settings can be written to the data matrix, a Low-Level-Exception check is performed:

$$DV' < DV \xrightarrow{TC'} I'_{ij} = TC', I'_{i(j+1)} = 1, \qquad (3.18)$$

where I'_{ij} is the data matrix for trip currents to be transferred to the mainframe after the final target voltage has been reached. At this point, we are able define

transfer set 1 (t-set 1) for the GEM/Mesh pair:

$$TC \neq TC' \in \mathcal{B}_{ij} \wedge I'_{i(j+1)} \neq 1 \quad \xrightarrow{TC'} \quad \Lambda_{ij}, \qquad (3.19)$$

$$TPC \neq TPC' \in \mathcal{B}_{ij} \quad \xrightarrow{TPC'} \quad \Lambda_{ij}, \qquad (3.20)$$

$$TCM \neq TPCM' \in \mathcal{B}_{ij} \quad \xrightarrow{TPCM'} \quad \Lambda_{ij}, \qquad (3.21)$$

$$TPCM \neq TPCM' \in \mathcal{B}_{ij} \quad \xrightarrow{TPCM'} \quad \Lambda_{ij}, \qquad (3.22)$$

$$RUP \neq RUP' = RUPM' \in \mathcal{B}_{ij} \quad \xrightarrow{RUP'} \quad \Lambda_{ij}, \qquad (3.23)$$

$$RDN \neq RDN' = RDNM' \in \mathcal{B}_{ij} \quad \xrightarrow{RDN'} \quad \Lambda_{ij}, \qquad (3.24)$$

where we ask each property to be within the bounds defined in $\mathcal{B}_{ij}$. Ramp up velocities RUP' for GEM and $RUPM'$ for Mesh are supposed to be always identical in order to keep the dV during the ramping as small as possible, otherwise the Zener may get activated and trip the Mesh channel, before the Relay Board would trip its corresponding GEM channel.

With the first set definition complete, we may now prepare the second transmission by determining the new bias voltage:

$$I_T = \frac{DV'}{\sum R_T}, dV = R_T^{2M} \times I_T, \qquad (3.25)$$

$$DVM' = DV' - dV + bias_{+FB,-RB}, \qquad (3.26)$$

where we first calculate the current passing through the top chain of the divider and the voltage drop across the 2MΩ resistor, which is where the back-to-back 250V Zener to the Mesh is installed. The difference between applied voltage on GEM channel and dV would determine a Mesh voltage with effectively zero bias. Any variation, which we indicate with $bias_{+FB,-RB}$, may either providing forward bias, if positive, or reverse bias, if negative. The polarity of this variable can be controlled with the Bias Master (default: RB).

In case, the demand voltages DV' or DVM' are not below the maximal HV limit (default: 4.5kV), RC will be aborted. Otherwise, we are able to define *transfer set 2* (t-set 2) for the GEM/Mesh pair:

$$DV \neq DV' \in \mathcal{B}_{ij} \quad \xrightarrow{DV'} \quad \Lambda_{ij}, \qquad (3.27)$$

$$DVM \neq DVM' \in \mathcal{B}_{ij} \quad \xrightarrow{DVM'} \quad \Lambda_{ij}. \qquad (3.28)$$

In a final step, expected voltage readings returned from the LeCroy are simulated with the knowledge of DV', DVM', RUP/RDN and τ_S, and stored in $\mathcal{Q}_{ij}$ for comparisons during the monitoring sequences.

Data Transfer to Mainframe. Precisely timed coordination is provided by synchronizing the RC and Mainframe Control (MFC) clocks. Therefore, RC notifies MFC to start its clock at the rising edge of a defined reading of the system clock (SCLK), which is set by default to +100ms to the present SCLK status. Furthermore, each thread has ordered progress IDs throughout the program code, which allows to observe each others process status. The entire simulation data is then transferred to MFC: Λ_{ij} as well as counts c_1, c_2 of expected parameter transfers of t-set 1 and 2 respectively.

After this initial preparation of MFC, a request of the t-set 1 submission to the mainframe is sent to MFC, including the current progress ID from where the request in RC is issued. This will cause MFC to be released from its Standby mode and initiate the verification of the RC system progress with an independent identification of the requested t-set transmission. Since the actual communication between the two threads is much more complex as illustrated here, the exchange of progress ID ensures proper operation and safe exception handling. The MFC will then transfer the t-set 1 portion of Λ_{ij} in GEM/Mesh pairs to the mainframe and confirm the synchronously awaiting transfer verification by RC. This will activate the mainframe monitor in interaction with GDSM, which verifies the reception of the t-set 1. The same procedure is repeated for the submission of t-set 2, however, besides the correct loading of demand voltages, the resulting measured voltage is closely monitored in respect to $\mathcal{Q}_{ij}$ as additional reference.

Suppose the monitor finds a successful DV' submission only for the GEM, but not its corresponding Mesh channel. Based on the configuration of the RC system, two possible actions are possible. RC will force an immediate communication link to the mainframe, either via hvclient or directly through the terminal server, and may disable the GEM/Mesh pair together or stop the GEM channel from further ramping, resend the DVM' and resumes the GEM ramp as soon as the measured voltage of the Mesh indicates a pass of the GEM's intermediate voltage level. Finally, in case the target is at a lower voltage, the new trip currents can now be safely transferred. If the overall transactions to the mainframe have been successful, *hvdb* is updated, TripProtect reactivated and RC returned to Standby mode.

3.4.7 GEM Module Surveillance

The main user-based monitoring capability of HVC is provided for all clients with the introduction of the HBD Module Surveillance Panel. All fundamentally important parameters received from the mainframe are refreshed with an update rate of $\tau_S + 1s$, including demand voltage, measured voltage, measured current, measured peak current, ramp up/down velocities, trip (peak) currents

for the GEM channels and demand voltage and measured voltage/current for the Mesh channels. A status indicator informs about the module activity (enabled/disabled) and a trip flag about hardware or virtual trips. Additionally, detector performance and configuration parameters are displayed:

- **Applied dV.** When one chooses a certain desired module gain through PCE in the Options panel, Ramp Control will set the Mesh voltage accordingly. In order to verify the actual applied dV on the mainframe, the Surveillance panel reconstructs the dV based on measured GEM and Mesh voltage.

- **TripProtect.** As discussed in detail in Section 3.4.10, the TripProtect System allows to monitor its dynamic control parameters *deadzone low* (DZ_l) and *deadzone high* (DZ_h), indicating lower and upper current thresholds. The measured current (MC) of the GEMs may vary within the created band, however, as soon as the threshold in either direction is passed, a virtual trip is initiated and the entire module disabled. Optimally the MC should be centered for healthy or recently calibrated[9] GEMs. Therefore, the MC:EC indicator is provided, which simply calculates $^MC/_EC \times 100$ to easily identify how well a GEM is centered and in which direction it tends to move. The current TP percentage for each module is shown as well, providing a complete picture of GEM performance.

3.4.8 P/T Monitor and Control Unit

The enormous impact of gas pressure and temperature variations on the gain of the detector modules has been already extensively studied in Section 2.1.5. In the following, we will present the HVC approach to this issue.

As conceptionally expected by the exponential relationship between module gain and P/T in Eq. 2.9, it is proven that 1% change in P/T results in a gain variation of $\sim 26\%$ in CF$_4$. This is shown in Fig. 3.26, where the P/T range between 2.52 - 2.55 Torr/K is specifically marked, since it represents a typical range one may expect during operation at PHENIX.

The question one may ask now is how one can correct for these variations in order to still keep an overall stable gain during operation. The idea comes

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[9]If during an IR access changes to the resistor chains are made, e.g. resistor replacements after a short has been detected, or high voltage modules are swapped within the 1458HP crate or even replaced, the HVC calibration will update TripProtect coefficients for optimal performance and center the MC:EC to 100% (see 4.4).
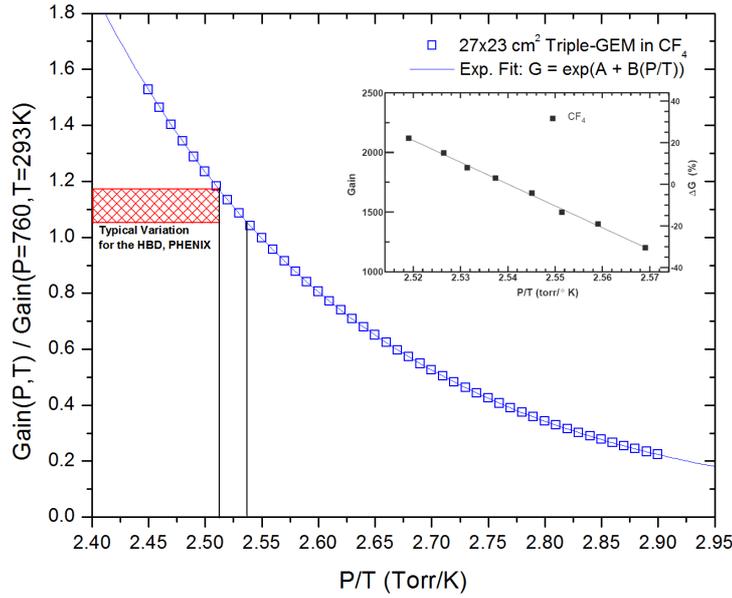
Figure 3.26: Gain in respect to a standard pressure P = 760Torr and temperature T=293K as a function of measured P/T. The shown data is taken with a triple-stack 27×23 cm^2 GEM and fitted with an exponential.

directly from 2.8 and the effect of the strength of the E-field on the ionization, 2.6, and so avalanche process in the GEM-stack, which we control through the applied high voltage. One can summarize this scheme as follows:

$$[P/T] \uparrow\downarrow \Longrightarrow [G] \downarrow\uparrow \xrightarrow{\text{correction}} [HV] \uparrow\downarrow \Longrightarrow [G] \uparrow\downarrow, \qquad (3.29)$$

meaning, if the P/T increases, the gain decreases exponentially, which needs be corrected by a change in raising the applied HV, and vise versa. However, in order to know precisely to which extent the HV needs to be corrected, an expected known gain behavior for each GEM-stack is required for a particular measured P/T in the detector.

Therefore, one can use the following 2-step procedure to achieve a P/T - gain calibration for each module. The idea is to obtain the relative gain for each module by expressing it with respect to one pad of a chosen module for which the absolute gain has been measured. In a first step, *cosmic rays* can be used as a baseline measurement of collected charge. It has been found that a MIP transversing a gas medium of CF$_4$ molecules deposits 7keV/cm, from which 54eV are required to produce one electron-ion pair. Since the height h_d of the drift gap is 1.5mm, one can expect for one cosmic ray entering the HBD

at an angle ϕ between $\angle$(*Top-GEM surface,particle track*) of 90:

$$N_e = \frac{7\text{keV/cm} \times 0.15\text{cm/sin}\phi}{54\text{eV}} \simeq 19e^- \text{primary electrons.} \qquad (3.30)$$

However, one does not really need to know the exact number of electrons produced due to the impact of a single MIP, since at this step only a relative relationship between pads/modules is needed and a distribution of incoming tracks depositing charge in the drift gap can be assumed to be equal. For
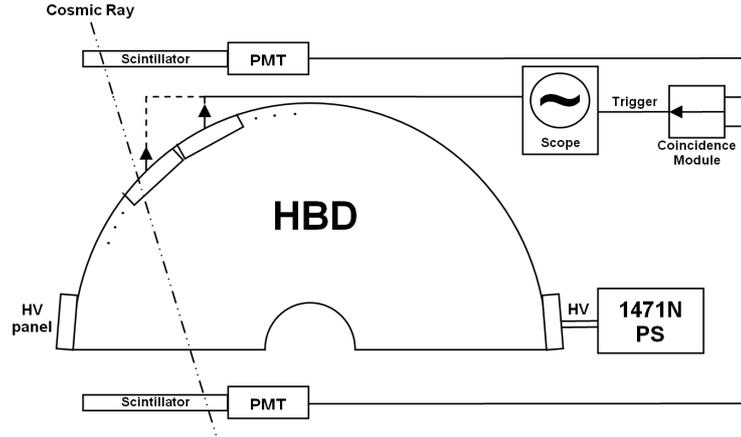
Figure 3.27: Cosmic Ray measurement in laboratory to obtain a relative gain for each module.

this experiment, as illustrated in Fig. 3.27, one places a scintillator with a Photomultiplier Tube (PMT) above and below the HBD, and use a coincidence module as a trigger. The particular GEM module is powered through the actual Run-9 resistor chain as discussed in Section 3.2.1 and the applied HV is kept constant throughout the experiment. The collected charge by the pre-amplifier of one particular pad is then readout via an oscilloscope, making an entry to the pulse height spectra at every triggered event. After some defined time, one can take the mean of the peak, and apply a calibration coefficient retrieved previously to convert measured voltage (mV) to the actual collected charge $\langle \mathcal{Q} \rangle$. This procedure shall be repeated for all the pads of each module, which then provides information about the gain uniformity across the GEM-stack. When the measurements for all desired pads are complete, the *relative gain* from *one pad of a chosen module*, e.g. the one that has shown the highest gain, can be used as a baseline for all other pads. Therefore, a multiplication factor α_j^i is introduced for every i-th module and its j-th pad to express the individual measured charge $\langle \mathcal{Q}_j^i \rangle$ with respect to the preference pad's charge

$\langle \mathcal{Q}_x^0 \rangle$, which can be written as

$$\langle \mathcal{Q}_j^i \rangle = \alpha_j^i \langle \mathcal{Q}_x^0 \rangle, \ \forall i \in \{1, 19\}. \tag{3.31}$$

Furthermore, throughout the entire series of measurements, the P/T is measured precisely within the detector.

In the next step, a Fe^{55} source, placed over the reference pad, emits 5.9keV X-rays, which create $109 e^-$ in the module's drift gap. After a sufficient spectra is accumulated and a value of collected charge $\langle \mathcal{Q}_x^0 \rangle$ obtained, one can calculate the *absolute value of gain*, which then can be used to determine every other pad's absolute gain by expressing it through the multiplication factors α_j^i received by the cosmic ray measurement. Note that this procedure is repeated for a number of applied HV settings up to a safe non-sparking state of the stack.

As soon as the detector is installed in PHENIX, the DAQ in Standalone mode can be used to readout the pre-amplifier of all 96 pads per module. One can then use actual collisions at RHIC to measure the module gain from the produced scintillation background.

The described procedure has been used before the detector was installed in PHENIX for Run-9. The results for each detector arm are shown in Fig. 3.28.

Together with the measured P/T during the cosmic measurements and so direct relationship with the multiplication factors as well as the variational behavior as shown in 3.26, one can divide the P/T deviation into 5 segments, each representing the center of a so-called HV *trigger bin*. Each center shall vary to its boundary and so transition to the neighboring bin by $\frac{1}{2}\%$, which corresponds to an expected change of gain of $\sim 13\%$ in either direction. These P/T segmentations are then implemented as part of an HVC subsystem, called **P/T Control—Monitor**, with the purpose to monitor the P/T measured inside the HBD, while keeping accordingly the gain variations under control, and optimally within a small band or completely suppressed.

Since all clients have monitoring rights and at least one controlling client is always required, the P/T system has been split into an active part, residing on the HBD server, and a secondary part on the requesting control client, initiating the update generation of P/T monitoring on the server. This request has been implemented as part of GDSM's update routine and incorporated within the PCE module on the server side, where Operational voltages are prepared for submission to the child PCE module of the controlling client. As soon as the τ_S-dependent update is requested by the client, the HBD server analyzes if a change of currently applied HV is necessary in order to keep the gain

(a) HBD Sector WN

(b) HBD Sector WS

(c) HBD Sector EN

(d) HBD Sector ES
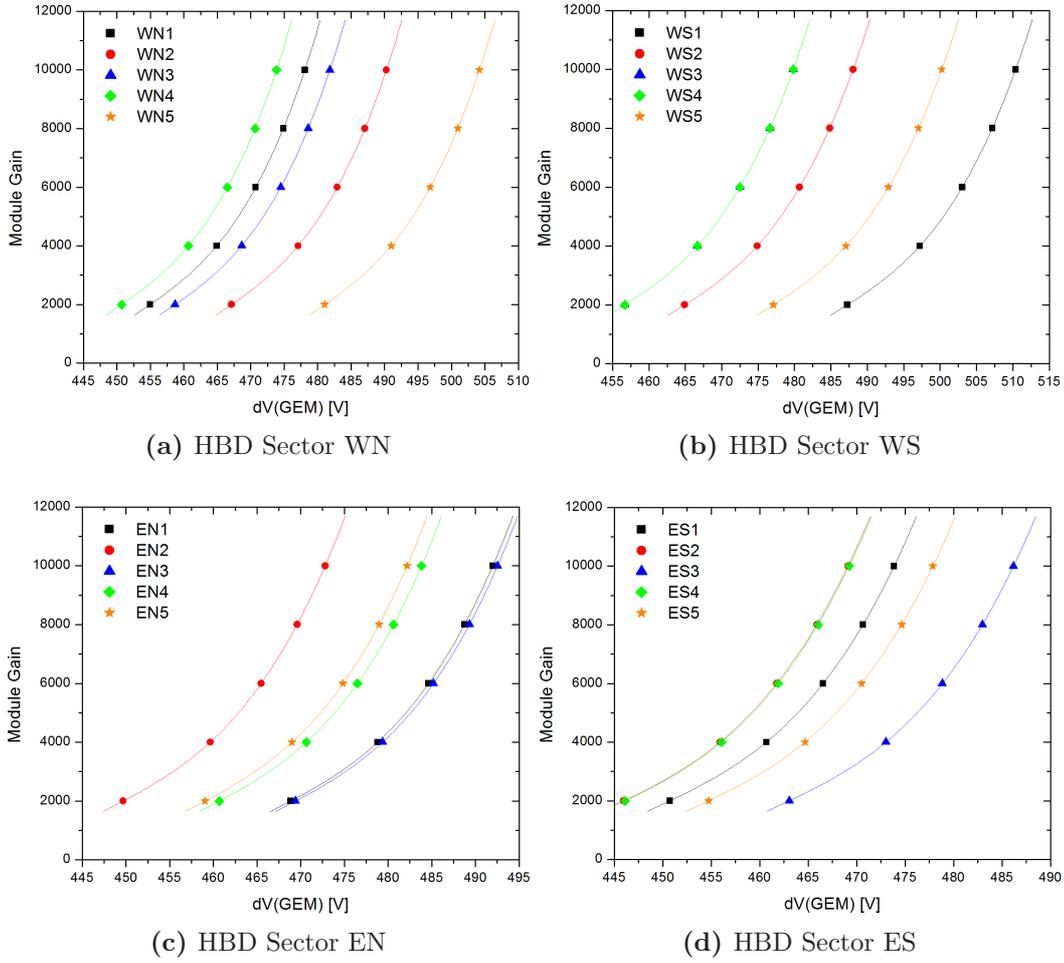
Figure 3.28: Gain Calibration Curves for P/T Control & Monitor.

stable. Therefore, the `hvdb` database is accessed to retrieve the latest center-of-bin P/T trigger settings, and generates the bin boundaries. Measurements of pressure and temperature inside the HBD East and West, and the absolute pressure in the IR are transferred periodically to the `hbd` database in the units of inches of water and Kelvin. The latest data is then loaded from this database and pressures are converted into Torr by using the constant convertion factor of 1.868, before the resulting P/T value is verified with the currently loaded P/T bin, which corresponds to a specific voltage table that has been created based on the gain calibration curves. In case the newly measured P/T has passed its previous bin and remained in this state of voltage violation for 2 successive `hbd` updates, a so-called *ptid* is set to inform the client of this event and to request an approval of the set *ptid*. As soon as the controlling client

97
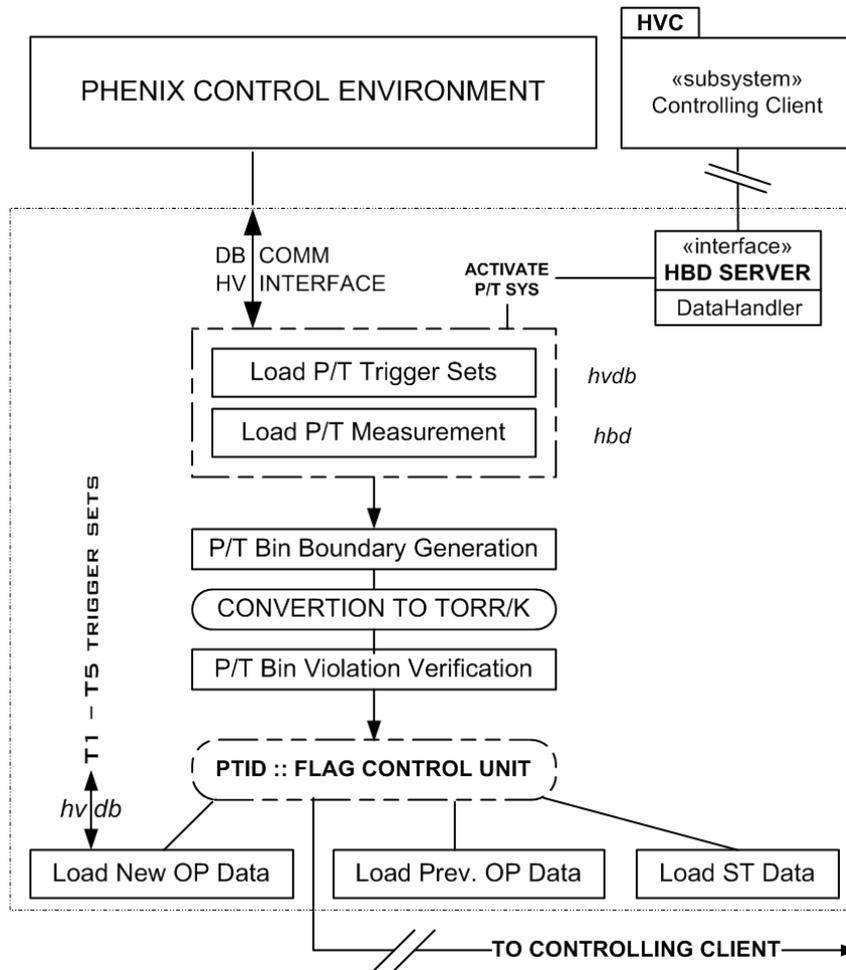
Figure 3.29: Simplified Illustration of HVC's P/T Control and Monitor Unit.

returns an approved *ptid*, new Operational voltages for each module are loaded and transferred to the child PCE module on all connected clients. If the SA1 in the PHENIX control room is permitted by HVC to change the actual applied HV, and permission from the Shiftleader is granted, the execution of RC initiates the upload of the voltages from the new P/T HV set, which will cause the gain to either drop or raise, depending on the change to a lower or higher *ptset* and therefore correct for gain fluctuations induced by P/T.

3.4.9 Local and Satellite Alert Communication

The availability of visual *action reports* from internal processes is not just fundamentally important for developers to verify the correct operation of a system, but also for the interaction with the actual end user. The final imple-

mentation of the HV System in the PHENIX Control environment, where shift crews operate the HV of detectors, who are not necessarily familiar with the HBD and its operation, induces that smooth and safe running conditions can only be guaranteed, if the communication between shifter and control system is perspicuous. There are overall two sources to initiate a message to the user: either in direct response to a user request or by the system itself.

User-driven Communication.   Some control systems do not report about the execution of a requested function until the execution is already completed and the resulting state reached; may this be due to a freezing GUI during the process or a lack of sufficient consideration of notifications during the program design. This has caused common confusion between SA1 shifters in the past and has been addressed in the development of HVC. Whenever the user requests the execution of any process, the Logging System will make a note of this request to the local logfile and issue the display of an "Action Approval" message, explaining the action itself and its consequent result, which must be acknowledged by the user before the action and related sub-processes can be executed.

In case certain restrictions for the execution of processes apply, e.g. if the measured P/T has passed its bin boundary, requiring bin adjustment with associated new operating voltages and the corresponding HV change is requested during an ongoing PHYSICS run, HVC may deny the execution of the process and inform the user of preliminary duties in order to proceed with a new request. This way, some guidance and correct handling of HVC can be ensured.

System-driven Communication.   The *Control Monitor* or *Eagle Eye* serves as the global watchdog of all processes. It is based on 3 observe-and-control methods used for every single process:

1. *Known Exceptions.* – Boundary functions are introduced to set certain expectations on I/O objects. For example, if a just received data stream is loaded into a new vector object, but the vector, which shall be used throughout the rest of the process, is incomplete/corrupted or even null, a known exception message is sent to the Control Monitor.

2. *Try/Catch.* – The entire or essential code of a process is riddled with *try* statements. If an exception occurs that has not been addressed through the boundary functions, meaning an unforeseen scenario, the system will catch this severe exception and send it to the Control Monitor.

3. *Control Variables.* – Internal functions of processes are always set private with the exception that at several so-called control point within the code, the status of a function as well as system clock count are written to public control vectors, which are observed constantly by the Control Monitor. When error messages are sent by the previous two methods, their cause can be reconstructed and used to determine how the operation of the process shall continue. During regular runtime, the observation allows to verify boundaries of variables and minor exceptions.

A typical response by the Control Monitor using method (1) would be an incomplete data stream from the mainframe and visible in the Surveillance Panel, where "—" are printed for the missing vector element. Otherwise, if one would not catch this although rare problem, the entire system can crash. An example for method (2) would be if the hvserver has crashed and the communication to the mainframe is interrupted. The user would see an error message, while the HBD server is brought into Standby mode. For method (3), one could for example expect a message when the measured P/T is out of its bin.

However, in order that the user can be informed about any of these reports, the Control Monitor has to make a case to the Logging System, which then makes an entry to the local logfile as well as produces the display message for the user. Based on its configuration in terms of severity of the system error, e.g. severe massive tripping, the Logging System may transfer the message to the Satellite Communication Module, where we mean with "satellite", outputs of this module will leave the local machine where the controlling HVC client is running. The idea is to minimize the downtime of the HBD during datataking of such severe scenarios and therefore contact an HBD Expert directly by HVC before the SA1 in the PHENIX Control Room is able to figure out that the found problem requires Expert knowledge. The delivery method of the alert can be customized: either a text message or actual phone call with a digital voice message can be sent to the Expert On Call, its Assistant and/or the Expert In Charge. This allows the immediate attention of severe HV issues.

Independently from anything that has been discussed previously, the just described principle of the Control Monitor *is* the reason why HVC is able to fulfill the TDS requirement of overall optimal **System Stability**.

3.4.10 Slow-Response GEM Protection

The introduction and acceptance of the global response time constant τ_S allows us to include control policies in the HVC software that are based on underlying control systems of much smaller response time τ_H, as the LeCroy power supplies, Trip Detector with Relay boards and the resistor chains containing the control subjects, the cascaded GEM foils. All control components have not only been combined with the purpose of establishing an efficient powering scheme for the detector, but rather preventing severe damages to the GEMs through HV application. The approach hereby is to detect harmful discharges through the associated current draw and throw at some defined threshold an immediate interrupt to this process by deactivating the energy source of the sparking, the HV generation, and discharge the stored energy in the particular GEM-stack and HV output capacitors of the channel. This is a very common procedure in many detector experiments requiring high voltage and is seen as a *protection method*, preventing *further damage* to the detector. Thus, it is fundamentally important to understand what protection really means and how it can be realized most effectively.

Based on our discussions in Section 3.2, there are currently 3 trip-initiating sources: the Zener, causing the Mesh channel to suddenly draw current, if a dV of 250V is exceeded, while a low trip threshold for the corresponding LeCroy channel is set; the HV Relay, grounding the output of the HV channel as a loss of its phase is detected; and the FPGA itself, which issues a trip in excess of pre-defined thresholds of ADC-measured slow/peak currents, AC component and hardware-dialed HV limit, besides the forced contribution of special cases when Zener or Relay are active. We conceive each source's functionality, but do we grasp their role in "maintaining" healthy GEM foils? Therefore, let us first clarify to what extend *GEM protection* is actually possible in respect to technological limitations we are facing.

There have been many speculations for what can cause damage to the detector during operation. Certainly, after Run-7 and the detailed inspection of problematic GEM foils, but also the Run-9 performance, as discussed in chapter 5, show strong indications, that the amount of dust particles in the detector remaining after production and installation in PHENIX are the primary source of shorting GEM strips. A hypothetical idea would be the following: Although, the molecular composition is unknown, let us assume the dust particle may have ferromagnetic constituents. Through electrical or magnetic forces, resulting from applied fields in the GEM-stack or ramping of the Central Magnets in PHENIX, dust particles residing on the GEM surface may be moved and fall into the holes. Corona discharges at sharp edges of the CsI

or Cu layers may even support this process. The shortening of the field lines by these moving point charges can initiate a spark to the bottom electrode – a small plasma, ionizing CF_4 and dust molecules, and essentially burning a conducting film into the hole wall, which then represents a shorting path of some resistance R_{short} between the two electrodes. For further discussions, let us classify these shorts:

Definition 3 *The effect of a GEM, consisting of n segmenting strips, in an electrical circuit can be divided into 3 different states based on experimental experience:*

1. **No Short: $R_{short}^n \to \infty, \forall n$.** *The GEM appears to be an almost perfect inductor and considered to be operational <u>stable</u> and <u>healthy</u>, if its measurable impedance is $> 50\,G\Omega$.*

2. **Partial Short(s): $0 < R_{short}^n < \infty$.** *The GEM appears to have one or more conducting path(s) of measurable impedance between $10\,M\Omega - 50\,G\Omega$ and is considered to be operational <u>unstable</u> and <u>damaged</u> of n-dependent varying degree.*

3. **Dead Short(s): $R_{short}^n \approx 0$.** *The GEM appears to have one or more conducting path(s) of measurable impedance $< 10\,M\Omega$ and is considered to be operational <u>stable</u>, although <u>severely damaged</u> of n-dependent varying degree.*

The transfers from state (1) $\to$ (2) or (2) $\to$ (3) are bi-directional, but form an open-loop system; transitions between (1) and (3) are not possible.

As one may notice, state transitions from dead/partial shorts to a healthy GEM are possible. This can be explained with the transpassing current flowing through the shorting film and breaking the bounding structure an instance or a certain period after its creation. One can use this principle to *condition the GEM* by applying high voltage directly across the GEM, using a power supply with current-adjustable output, e.g from Bertan (see Section 4.3).

In our hypothesis, we have accused dust particle to be responsible for temporary or permanent sources of damaging GEM foils under HV application. Even though this may be a erroneous assumption, the fact is that a shorting path from the top to bottom electrode has been created and results in lowering the parallel resistance R_{para} of the entire divider chain, which, if measurable by the 1471N, forces a supply of more current in order to maintain the desired output voltage.

Let us illustrate the scenario with some numbers from the new resistor chain for Run-9 (see 3.2.1). We may refer, hereafter to its strips of resistors in parallel configuration as *strings*. Each of the 3 strings has a total nominal resistance of 84MΩ with a $R_{\mathrm{GEM}} = 10$MΩ resistor installed across every GEM, where in parallel to R_{GEM} each strip of the GEM has a permanent current-limiting $R_{\mathrm{limit}} = 20$MΩ resistor connected in series with the top-electrode. For a perfectly healthy GEM, $R_{\mathrm{short}} \approx 0$, the current only flows across R_{GEM} and results in a total parallel resistance of the entire chain of 28MΩ. If now suddenly one of the 28 strips of one of the 3 connected GEM foils in one string has become a dead short, R_{limit} and R_{short} now contribute in parallel to R_{GEM} (10M$\Omega \rightarrow 6.67$MΩ), reducing the string's total resistance to ~ 80.67MΩ and essentially the total parallel resistance of the chain to ~ 27.62MΩ. If one would assume an applied voltage of 4kV, a current increase of $\sim 1.97\mu$A can be expected with one shorted out of 84 strips. This change in current can then be measured by the LeCroy's ADC.

The reader may realize, that we are only able to sense a certain current increase *in response* to the actual short $\geq \tau_H$, meaning *after* the damage to the GEM already occurred. The idea of GEM protection can then be understood as a **Secondary Protection Method** to prevent further sparking and expansion of partial to dead shorts by issuing a *protecting trip*. As visual inspections of GEM foils reaching a sparking state have shown, discharges are usually not limited to only one strip, but rather occur on multiple repetitively. The interruption of this process then effectively changes the state of the local environment and may minimize the propability to fall into the same state after re-energizing the GEM, depending on how low R_{short}^{i} remained for i previously sparking strips. In case shorts of only very high impedance remained and essentially can still be considered as healthy GEM foils, one of the goals of secondary protection is reached. However, if the lasting damage falls already into the category of a partial short, meaning the time and energy of previously created plasmas have been sufficiently large, one may find the entire GEM-stack to be very unstable as R_{short}^{i} is still changing and therefore causing random variations of gain that induces large difficulties for the analysis of collected pad readout data, if these occur during a Run of the PHENIX DAQ. Therefore, a dead short is generally preferred to achieve more stable module operation. Another goal of secondary protection is then to indicate the grade of partial shorts, which may detector experts allow to force a dead short by conditioning the particular GEM directly; the downtime of a module delivering optimized results can be minimized. When asking for the reduction of such downtime, a fundamental requirement for protecting trips automatically

arises: a justified trip execution through filtering, meaning the dynamic distinction between harmful developing partial shorts and instantaneous current draws or self-healing partial shorts of small timely window. At this point, the question may be raised of where and how such intelligence of GEM protection can be implemented? Let us address this problem from a hardware standpoint we are presently facing.

Most HV power supplies do not allow to take custom control over their trip behavior; neither widely used modules by CAEN nor LeCroy. In the case of the L1471N, ADC slow current measurements are calibrated with coefficients of a 3rd-order polynomial for "true" HV output voltages and used to determine positive trip conditions by the FPGA. Unfortunately, it has been found that smallest current variations within $1\mu A$ cannot be sensitively analyzed for "true" triggering of an over-current trip event. This is also related to the fact that HV generation is deactivated at the first positive over-current reading and may induce random tripping. Furthermore, these trip settings cannot be adjusted automatically by the FPGA, instead the controlling HVC client has to pre-calculate and submit these configurations to the mainframe after a certain target voltage has been reached and its settling time passed.

The HBD requires to be sensitive to small variations of $< 2\mu A$ in current change to allow recognition of dead shorts for a broad range of high voltages. If one would compare a typical Operational voltage of 4kV to a typical Standby voltage of 2.5kV, a minimal short detection of $1.97\mu A$ and $1.2\mu A$ is required respectively, where one requires even lower thresholds in order to allow secondary protection overall.

One could still try to change of the FPGA code and improve calibration coefficients in the EEPROM, which would be certainly a solution for HBD demands with the lowest response time, but still not sufficient for dynamic control, as the status of GEM foils and installed divider resistors for shorted strip compensations may change. In addition, the mainframe communication protocols do not support the transmission of additional configuration, which may be used to update control parameters in the EEPROM and so adjust the FPGA's trip sensing. Even though, one could imagine such a customized FPGA code, at the end a backup system, as the Relay board, is still required to prevent dissipation of stored energy from the output capacitors. Nevertheless, ADC current measurements reported to the mainframe have a sufficient precision to confidently determine variations of $\approx 0.5\mu A$, allowing an external monitor to make trip decisions, rather than the FPGA itself. Therefore, we shall deactivate the FPGA-controlled trip execution by increasing slow current thresholds far above standing currents (e.g. $20\mu A$) and leaving fast current

settings at unreachable $200\mu A$. The control of over-current trip executions may then be provided by introducing an intelligent current monitor on HVC clients, the TripProtect System.

The TripProtect System. The system is based on the precise knowledge of an *expected current* draw EC at any applied voltage as well as the current draw EC' one can expect due to a single new dead short. GEM foils of one or more shorts require additional knowledge of the expected current when dead/partial short(s) may transform back into very high impedance shorts. This defines the operational frame (OF) of the TripProtect System (TPS). The idea is then to create an internal symmetric window of dynamic boundaries, which define in respect to the surrounding OF, upper and lower *deadzones* $DZ_{h,l}$.

TPS monitors continuously in collaboration with the GDSM, measured currents MC of GEM and Mesh channels at Standby voltages and beyond, and may trip the GEM/Mesh pair, if at least one of the following conditions is met:

1. MC of the GEM channel has entered or passed DZ_h or DZ_l, indicating a new or recovering partial short respectively.

2. MC of the Mesh channel has passed a user-defined low static threshold (default: $1\mu A$; must be $< TCM$), indicating that the Mesh may physically touch the Top-GEM or the Zener has been activated.

3. The dV between GEM and Mesh channel has exceeded their desired FB/RB setting or a user-defined static threshold (default: 200V; must be $< 250V$ Zener breakdown), indicating e.g. a failure of the Relay board after a Mesh hardware trip, a failure of the Zener after a GEM hardware trip or improper external DV modification via the terminal.

Since TPS does not rely on the Zener, 1471N trip circuit or Relay board, a trip is understood as ramping both GEM/Mesh channels synchronized with a constant ramp down rate to 0V, while keeping the dV between GEM and Mesh constant. Depending if the pair has been operated in RB or FB mode, the Mesh then GEM channel or vise versa will reach 0V – defining the moment when their dV is being equalized and the trip procedure complete. Such a trip issued by TPS is called a *virtual trip*.

Both trip conditions, (2) and (3) are based on fixed settings through the PCE module, which are simply compared with measurements of slow current and voltage, and are considered trivial. Thus, we would like to now focus on the systematic determination and final enforcement of $DZ_{h,l}$.

The ADC measured current MC reported by GDSM must be precisely calibrated to approximate an expected current EC as a function of any given measured voltage MV. Therefore, all installed resistors in every string of all 8 dividers used to power the HBD have to be measured of very high precision and written to the `hvdb` database. Furthermore, TPS expects that all used resistors do maintain a constant resistance throughout the entire range of operation; a verification up to 500V using a Picoampmeter and High-Precision voltage source is recommended. Using the total parallel resistance of the divider chain R_{chain}, one can define the expected current as

$$EC = \frac{MV}{R_{\mathrm{chain,h}}} \approx MC, \tag{3.32}$$

which then can be used to calibrate the measured voltage according to two different methods. The first uses all measured resistors in the chain to retrieve $R_{\mathrm{chain,h}}$ (no participating shorts) and applies correction factors to MV and MC, which have been previously measured in the laboratory and stored in `hvdb` (only necessary if significantly off). This may be done, by using a divider of precisely known resistance and measure an HV output series for all 8 channels of the 6 1471N boards used to power the HBD. The second method is based on a HVC-controlled sequence of MV and MC measurements up to 4kV with the actual detector connected (can be done during IR access), which determining values of total chain resistance are fitted to a function, which then represents our $R_{\mathrm{chain}}(MV)$. As for the first method, correcting factors to MV and MC can be applied. Even though the user may choose, which method shall be used, the second method does still always do cross-checking with results expected by the first method.

These initial preparations to determine EC form the baseline to calculate the current EC' one can expect when a dead short in one of the GEM strips would occur (+) or recover (-):

$$EC' = EC \pm dI, \tag{3.33}$$

where dI represents the change of current due to the short:

$$dI = \left| \frac{MV}{R_{\mathrm{chain,s}}} - \frac{MV}{R_{\mathrm{chain,h}}} \right| = EC \left| R_{\mathrm{chain,h}} R_{\mathrm{chain,s}}^{-1} - 1 \right|, \tag{3.34}$$

whereby $R_{\mathrm{chain,s}}$ stands for the parallel resistance of the chain with one dead short. If corrections to MV are applied for EC determination, one has to apply these as well for dI. Also in this case, the user has the choice to select from 3 different methods. They all again differ from the procedure to find a

suitable representation of resistances in the chain. Let us have a look at each method.

1. *Method: dI-Nom|1.* The total *nominal resistance* of a string containing one dead short is given by

$$R_{\text{tot,s}} = \frac{1}{R_L^{-1} + R_{\text{GEM}}} + (R_{\text{tot,h}} - R_{\text{GEM}}) \simeq 80.67\text{M}\Omega, \qquad (3.35)$$

where R_L^{-1} is the 20MΩ current-limiting resistor mounted in series with the top electrode of the strips inside the HBD and $R_{\text{tot,h}} = 84\text{M}\Omega$ the total nominal resistance of one healthy string. The respective parallel resistance for a chain with one short and its healthy counterpart,

$$R_{\text{chain,s}} = \frac{1}{R_{\text{tot,s}}^{-1} + 2R_{\text{tot,h}}^{-1}}, \ \ R_{\text{chain,h}} = \frac{1}{3R_{\text{tot,h}}^{-1}}, \qquad (3.36)$$

which allows us then to find the simplest version of a current increase due to one dead short:

$$dI_{\text{nom}|1} = \frac{(R_{\text{GEM}} + R_{\text{L}}) DV^-}{R_{\text{GEM}}^2 - R_{\text{GEM}} R_{\text{tot,h}} - R_{\text{L}} R_{\text{tot,h}}} + \frac{DV^-}{R_{\text{tot,h}}} \qquad (3.37)$$

$$\approx 4.92 \times 10^{-4} DV^-, \qquad (3.38)$$

where one should note that a negative polarity of demand voltage DV^- is expected, which is the raw value reported by the 1471N. All resistor values in this method are entirely based on nominal expectation; the demand voltage represents then just a linear scaling factor.

2. *Method: dI-Nom|2.* The same procedure as in method 1 is used, however, the EC component, as shown in (3.34), shall not be dependent on nominal resistor values, but rather correspond to measured resistor values MR_{chain} and a measured reference voltage MV_{ref} (e.g. 4kV). As part of HVC, one can execute an *EC calibration run*, which will provide all required *EC* values for every GEM-stack and is used to determine dI. The difference to (3.37) is then rather small:

$$dI_{\text{nom}|2} \simeq \underbrace{MV_{\text{ref}} MR_{\text{chain}}^{-1}}_{\text{meas. } EC} \times \underbrace{\left\lfloor R_{\text{chain,h}} R_{\text{chain,s}}^{-1} - 1 \right\rfloor}_{\text{mult. factor: } \Gamma} \qquad (3.39)$$

$$= \frac{EC^-}{3} \left| \frac{(R_{\text{GEM}} + R_{\text{L}}) DV^-}{R_{\text{GEM}}^2 - R_{\text{GEM}} R_{\text{tot,h}} - R_{\text{L}} R_{\text{tot,h}}} + 1 \right| \qquad (3.40)$$

$$\approx 1.38 \times 10^{-2} EC = const, \qquad (3.41)$$

except that at the time when a calibration is completed, EC represents a precise approximation of MC, and is used as a reference to multiply with a constant nominal value Γ, providing finally a fixed dI for all operating voltages. Note that TPS uses again the negative polarity for expected current EC^- in Eq. (3.40).

3. *Method: dI-Meas.* The ideas of a scaled dI for any given voltage from method 1 and a dynamic baseline from method 2 are combined to create a dynamic *dI* determination principle. Therefore, we express the measured parallel divider resistance by the LeCroy for all operational voltages in terms of a polynomial function $R(MV)$. In case all GEM-stacks in the particular chain do not have any previous shorts at the point of calibrating $R(MV)$, a linear approximation is sufficient. It is recommended to run the automated calibration of its coefficients Λ_i on a regular basis (see 4.4), especially after resistors in the chain have been modified or additional shorts have occurred since the last calibration.

We may find dI with such a function as follows:

$$dI_{\text{meas}} \simeq \frac{MV}{R(MV)} \left| \frac{R(MV)}{R_{\text{chain,s}}(MV)} - 1 \right| \tag{3.42}$$

$$= EC^- \left| \frac{(R_{\text{GEM}} + R_{\text{L}})}{R_{\text{GEM}}^2 R(MV)^{-1} - 3R_{\text{GEM}} - 3R_{\text{L}}} + \frac{1}{3} \right|, \tag{3.43}$$

which furthermore can be expressed in terms of $n+1$ coefficients Λ_i of $R(MV)$,

$$dI_{\text{meas}} \simeq R_{\text{GEM}}^2 MV \left\{ 3 \sum_{i=0}^{n} \Lambda_i MV^i \times \right. \tag{3.44}$$

$$\left. \left[3 \left(R_{\text{GEM}} + R_{\text{L}} \right) \sum_{i=1}^{n} (\Lambda_i MV^i) - R_{\text{GEM}}^2 + 3R_{\text{GEM}}\Lambda_0 + 3R_{\text{L}}\Lambda_0 \right]^{-1} \right\}.$$

In most cases $n = 4$ is sufficient, but left to the user within the TPS configuration. For any given voltage, dI scales onto a dynamic baseline of EC.

If one has chosen the method TPS shall be using for the determination of dI and herewith the one could expect for one new dead short, the next task is define an internal window of allow current draws. This final step is under full control by the user through the particular choice of a so-called *Trip Sensitivity Level* S_L, which can either be set as a percentage globally or for each GEM channel individually. The S_L value then confines the percentage offset between

EC' and EC, which we call the *TripProtect* $TP_\%$ and define as:

$$TP_\% = \left(\frac{EC'}{EC} - 1 \right) - S_L. \qquad (3.45)$$

These settings are conveniently available to modify with the Options panel and are furthermore displayed in the Surveillance panel as well as the actual deadzones used by TPS to enforce intelligent trip protection:

$$DZ^{+,-} = EC \pm \left(\frac{TP_\%}{100} \times EC \right). \qquad (3.46)$$

Therefore the system monitors the mainframe data whenever the controlling HVC client is online. The HBD server may use its own TPS, if no clients are connected. Let us have a quick look at the runtime procedure within the TPS thread. When started after the login procedure into HVC is completed, the Control Monitor or Eagle Eye activates the TripProtect System. During its initialization, control variables (e.g. state vectors) are defined, resistor chain data is imported from `hvdb` and checked for consistencies (e.g. matching parallel resistance) as well as they system's synchronization with the HVC system clock. The MON-CONTROL of the TPS starts then the monitoring loop. First, the entire MF, Status, Calibration (e.g. $TP_\%$) is loaded through GDSM and verified for possible corruption. If a reset due to positive results is not required, $DZ^{+,-}$ boundaries of channels at or above Standby status and negative hardware or virtual trip flag are written to the global DZ-state vector. As soon as all channel data has been processed, an entry to the state vector of a counting trip clock is made if a channel has violated one of its deadzones. After the analysis of new incoming data is completed and the particular channel's DZ violation count has exceed a limit, which is set by the user through the Options panel, a virtual trip is executed and the HV generation of the channel deactivated.

Since the current draw during ramping can be slightly higher than the expected current at the momentary monitoring of the measurement, which is especially supported by the τ_S related delay of current/voltage updates, the TPS must be deactivated during this process. Therefore, MON-CONTROL allows the interrupt from authorized threads as the Ramp Control system; after successful completion of a currently running monitoring cycle, TPS will be brought back to its Standby mode, until being reactivated after ramping is completed.

3.5 Development and Testing

The systematically developed theoretical model for the HBD HV Control and Monitoring System, the extensive study of each hardware component and finally the careful design of controlling subsystems, which has defined our preceding discussions, have significantly relieved the approach to take the challenge of actually developing such an HV system. Certainly, the final version as presented previously has been significantly influenced by discoveries made during the development and testing period, and so do not have to be discussed at this point again, however, one should note that without a precise baseline, as generally introduced in section 3.1, the HVC system would have never been able to practically realize in such a short time frame until its actual online performance during Run-9. The project that has drawn significant impact on the development as well as preparations for the Run, as a HV calibration method, shall be discussed in this section.

3.5.1 HBD Simulation Project

With the ongoing rebuild after Run-7 due to severe HV damages to the GEM foils, the design development of a new HV System, now known as HVC, has been proceeding much faster than the production progress of the actual detector. The PCB boards for the Trip Detector and Relay Board (see Fig. 3.30) have been etched and populated according to their design concept, LeCroy 1471N modules calibrated by Universal Voltronics (UVC; company who ob-

(a) Trip Detector Board   **(b)** HV Relay Board
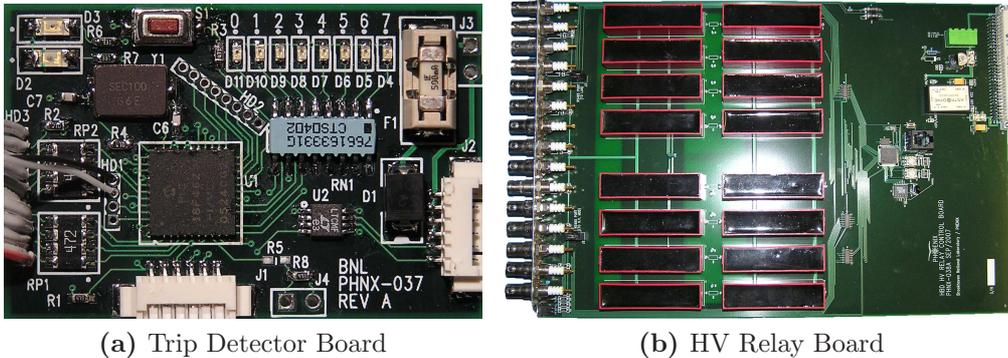
Figure 3.30: Trip Protection boards, where (a) senses the disappearance of phase on the 1471N, notifies (b), which then takes the corresponding GEM/Mesh pair channel with a $10\text{k}\Omega$ resistor to ground. The boards are part of HVC's Fast-Response GEM Protection system.
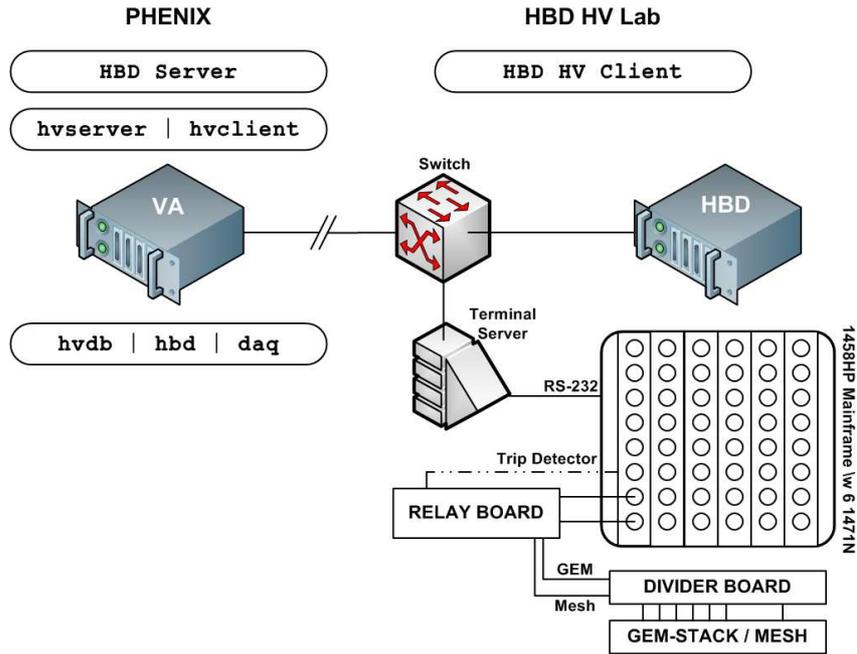
Figure 3.31: Network Diagram of the HBD Simulation Project.

tained the rights to modify the EEPROM calibration values) and modified with the Trip Detector mounted on top of the FPGA with readout cables to the 8 phases distributed by the Buffer Line driver.

However, there has been *no HBD in the IR* to test all software components of the pre-stages existing at this time, and even though the detector was expected to be installed back in PHENIX on time, it was clear that extremely little time was given to verify the correct functionalities of the new system within the PHENIX control environment together with all hardware components in place. For any other HV system in PHENIX this situation may have been sufficient, but certainly not for a system that was designed from scratch and based on control principles that have never been experienced before, not just in PHENIX, but any other nuclear detector facility in the world. This has lead to a project called, the *HBD Simulation Project*, which was called into service on December 12, 2007 and had the purpose to study, further develop and test the new HVC system for the HBD without sacrificing crucial time during the commissioning time after the detector's arrival in the IR for Run-9. (see Appendix C.1 for images)

The groundbreaking concept has been to recreate PHENIX within the IR and an HBD in terms of HV at the HBD HV laboratory (Physics Bld., BNL), while still using the actual PHENIX control infrastructure outside of the IR. The idea is illustrated in Fig. 3.31. An IBM eServer, equivalent to the VA

rack server in PHENIX, is officially registered with a static IP address and connected to the internal BNL network via a switch. From this machine a SSH connection to the VA machine in PHENIX is established, which contains the `hvserver` and `hvclient`. As one may recall from section 3.3.4, the configuration script of the `hvserver` contains in its header the address of the terminal server inside of the IR that connects to the HBD mainframe. This address is changed to *localhost*. Since another port of the switch in the HV laboratory hosts an Equinox ELS-16 Terminal Server (same as in the IR) with publically secret IP and a serial connection to a 1458HP mainframe with 6 HBD-modified 1471N modules, one can open a SSH tunnel from PHENIX to the TS port of the mainframe in the laboratory, e.g.

```
ssh -l hbd -L 7023:{TS-IP}:23 -L 3001:{TS-IP}:3001 {HBD Server address}
```

which when executing the `hvserver` with the modified configuration script, allows direct control over the HV modules in the mainframe at the laboratory through PHENIX. For this particular purpose, 2 HV-secured test boxes have been built, containing, the new Run-9 HV divider and a HBD-sized 27cm × 23cm triple GEM-stack with Mesh in air, which then has been connected to a denoted GEM and Mesh channel on the 1471N modules. This procedure permits to perform various studies and test the actual HVC under operational conditions as well as its behavior under extreme circumstances, while using for the system's standpoint an existing HBD that virtually resides inside of the IR.
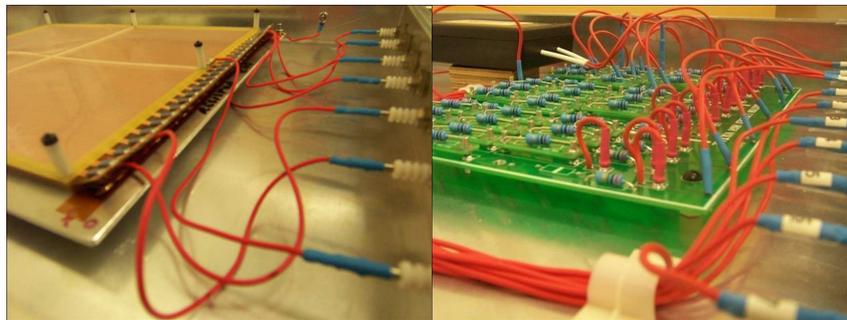
(a) Triple GEM-stack   (b) Resistor Chain

**Figure 3.32:** Main Test Components to Simulate the HBD.

The setup described above has then be used to test every single component of the system from normal expected operation to extreme conditions. We shall quickly discuss here the most important.

- Since the closest "operating" control mechanism is represented by the resistor chain, an obvious check has been to verify the feasibility of the thin-film resistors used for HV application. Therefore, a Picoampmeter has been used to apply voltage of 0.01% precision up 500V across the resistor, while measuring its resistance with the same device. One should note that no resistor in the circuit will "see" a potential difference higher than 1kV, but rather in some cases much lower. The resulting resistance was as expected perfectly linear up to 500V and can be fairly expected to be likewise beyond, which also has been verified by the manufactorer. Even in case there would be a small deviation at higher voltages, the dI determination method of TPS would detect such and automatically compensate for it due to its baseline. Also, the Zener breakdown voltages on all 8 divider boards have been verified to be $\sim 250V$ and checked to activate in back-to-back configuration if the dV between Mesh and Top-GEM is exceeded.

- The performance of the Trip Detector / Relay Board has been tested extensively. First the phase signal, which is generated by the 1471N's FPGA and sent to the FET has been measured with an oscilloscope and verified to be a 100kHz square wave with a constant 5V pulse height. Since the output of the two Buffer Line drivers are inversingly the same, the signal responsible for the negative phase, meaning pulling the current on the transformer downwards, has been chosen without further reasoning for the readout with the Trip Detector. The board was carefully mounted above the FPGA chip and grounded through the 1471N as well as powered with a 24V DC supply through PIN A9/11 of LeCroy's power supply bus to the mainframe. Since a stable supply is required for the Trip Detector's PIC, the supply line has been measured via an high-precision voltmeter over a long period of time while various other scenarios were tested, e.g. ramp up/down and trip behaviors. With the positive result of this baseline test, one were then able to visually verify the correct states of the LED on the Trip Detector board, indicating *phase* or *phase* for HV generation or executed trip condition, respectively, which were in expected synchronicity with LED states on the Relay board, and so proving the fundamental communication between PICs on the Trip Detector and Relay board via their RS-485 ports.

  Originally the relay board has been designed to fit next to its serving 1471N board into the 1458HP crate, which would power its digital control circuit and so additionally safe space for the final installation in the IR. However, as multiple tests have shown, during an initiated trip condition of one LeCroy channel, the closure of the corresponding discharge

relay initiates multiple trips on other channels of the same board. This unfortunate phenomenon can be explained due to a very small spark when the relay closes, which induces a coupling through air to the trip circuit on the open backplane of the LeCroy board. If one provides sufficient shielding in between the two boards, the effect disappears. In practical terms, such shielding is not effectively possible within the spatially restricted mainframe crate. Therefore, a much safer solution has been utilized by building special aluminum boxes to hold and power each Relay board individually. These shall then be placed later, as discussed in section 3.6.1, in a physically separated rack in the IR. Further experiments using these boxes have shown to have eliminate the trip coupling issue.

The divider test box as shown in Fig. 3.31, allows via its BNC outputs to either connect a floating scope for measurements directly across a 10MΩ GEM resistor or a regular digital scope measuring with an additional divider in parallel. The latter experiment shall be discussed in the following. In order to probe the HV output signal during a trip from voltages up to 4kV, one needs to ensure that the scope is mostly decoupled from the divider and not distort the signal through its imple-
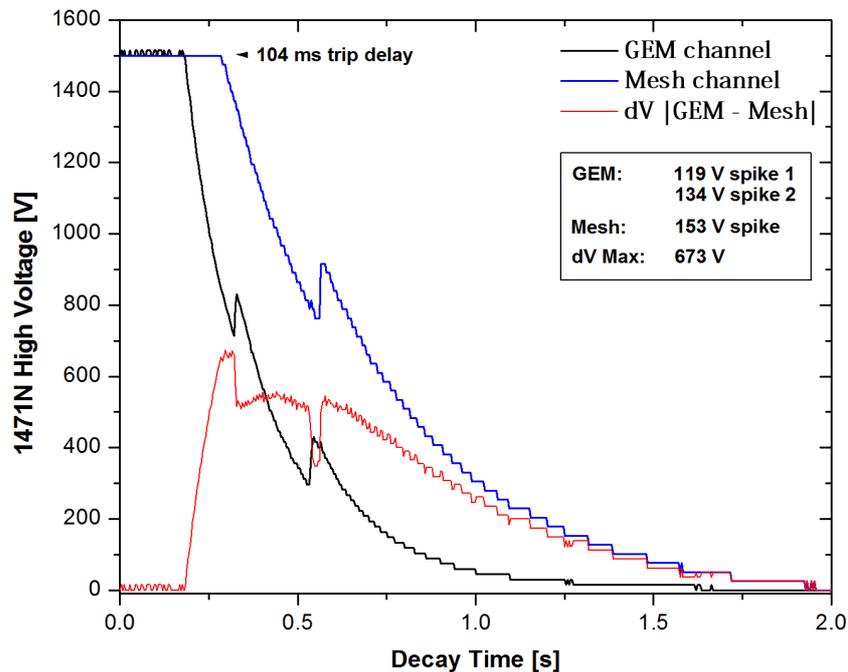
Figure 3.33: Measurement of a 1471N trip at 1500V without a Relay Board implemented
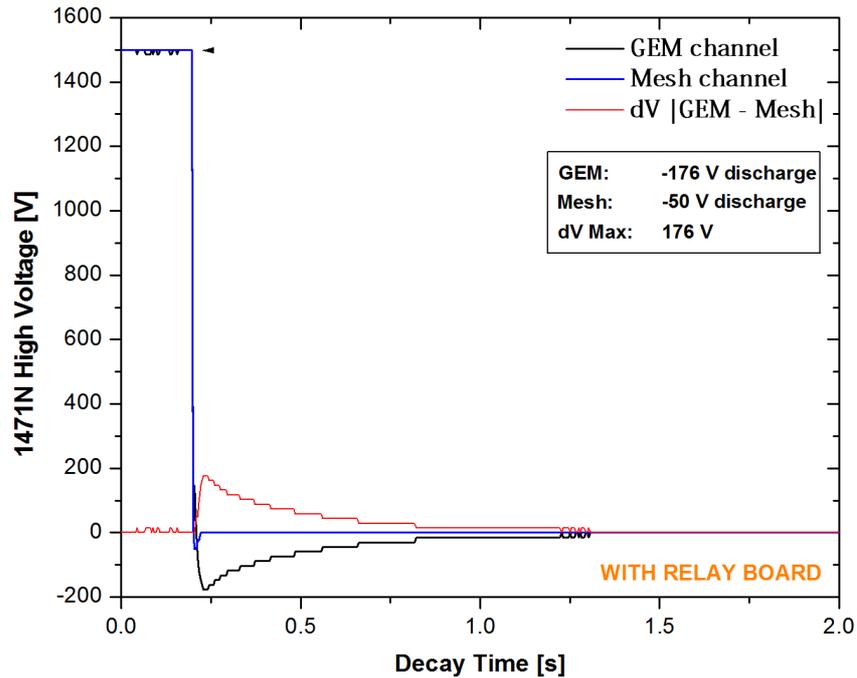
Figure 3.34: Measurement of a 1471N trip at 1500V with a Relay Board implemented. The discharge corresponds to the 10k bleeder resistor to ground.

mentation in the circuit. Therefore, a $1G\Omega$ resistor was utilized, which realized a 1000:1 voltage divider.

A trip was initiated by ramping the GEM/Mesh channels up to the particular voltage with each a trip threshold of $200\mu A$. Then only the GEM channel has been tripped by lowering its threshold below the present current draw. This activated the Zener, which finally also tripped the Mesh channel. The results of this test are rather suprising. If no Relay Board is implemented, the Zener is not capable of keeping the dV below its breakdown voltage (e.g. 250V). Furthermore, as presented in Fig. 3.33, spikes during the discharge can be seen, which correspond to the stored energy in the 1471N's RC filter on the HV output. In comparison with the Relay board in place, shown in Fig. 3.34, both issues are solved: the synchronized decay of GEM/Mesh and the voltage spikes during the discharge.

- While all the above tests were operated by the HVC client, an intense crash testing program involving each subsystem has been performed additionally. The purpose was measure the time constants of every algorithm and optimize each accordingly, then to find possible instabilities

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if certain internal time constants between various processes were conflicting with each other as well as using system print out methods to monitor and so improve every single function's actions throughout HVC in response to external changes to the measured subject.

All subsystems discussed in section 3.4 are running in parallel and coordinate with each other. The Control Monitor or Eagle Eye represents then the monitoring eye over every single function, process and thread with the authority to take over control of certain actions by either modifying the related local flag(s) (used to control case statements) or stopping, restarting or activating other processes or threads to resolve a found performance issue by the system itself or the detector. Since every subsystem as well as Eagle Eye has many optional processes and threads, which can be used to run additional analysis algorithms and may be requested by the user to be active, the idea is then to find an optimal start-up sequence of each process to still allow running all threads in parallel and finally to try to crash the entire system, providing information which process initiated the crash and essential find the maximal load the system can hold, which is certainly dependent how many CPU cores are available. First results of these tests were unsatisfying with continuously reaching the maximal capabilities of memory and CPU power, and so were causing severe system crashes. However, the internal process logs that are written to local files were extremely helpful and allowed to improve the control algorithms in such way that not just all threads and processes were able to run simultaneously in a smooth manner while keeping the memory low through triggered flushing, but even permitted to add many other functionalities, which were suggested later on by other HBD group members.

As one will see in chapter 5, studies of the simulation project and their changes and enhancements of HVC significantly contributed to the success of the HBD in Run-9. In a next step on the road to the final installation in PHENIX, we shall discuss an HV calibration method, which proves to be critical for the TripProtect System.

3.5.2   LeCroy 1471N Calibration

Significantly important for the Ramp Control and associated correct bias voltage, as well as the proper functionality of the Trip Protect System require the knowledge of *actual output voltage* by the 1471N modules.

As being partially still part of the HBD Simulation Project, the setup shown in 3.31 has been used to calibrate and essentially check all 6 modified

LeCroy modules' reliability before installing them in the HV rack in PHENIX. Therefore, the following procedure has been used: the HVC client is used to define a custom ramp up procedure. When executing RC, the system ramps with a rate of 10V/s, channel 0 on a given 1471N module from 0 - 3kV in 50V increments with a timeout of 10.5s for each, and from 3 - 4kV in 10V increments with a timeout of 10.5s for each, while an high-precision voltmeter is used to measure the applied voltage using the resistor chain of section 3.2.1. The measured voltage and measured current together with the demand voltage provided by the 1471N and measured voltage by the voltmeter are written every second to a local database. All resistors in the chain are measured very precisely in nS. The mean of voltage and current measurements at every voltage plateau is calculated and together with the information of divider resistance and therefore the load visible to the 1471N, the offsets between applied and desired output voltage are then fitted with a polynomial as a function of demand voltage. The coefficients are then written to `hvdb` and used, if chosen in the Options panel, by RC to apply corrections to achieve desired output voltages to the detector.

As one can see in Fig. 3.35, the actual applied voltage, as measured through the voltmeter, raises linearly and deviates in comparison to the desired voltage or demand voltage (DV) requested from the LeCroy; the zoom-out plot high-
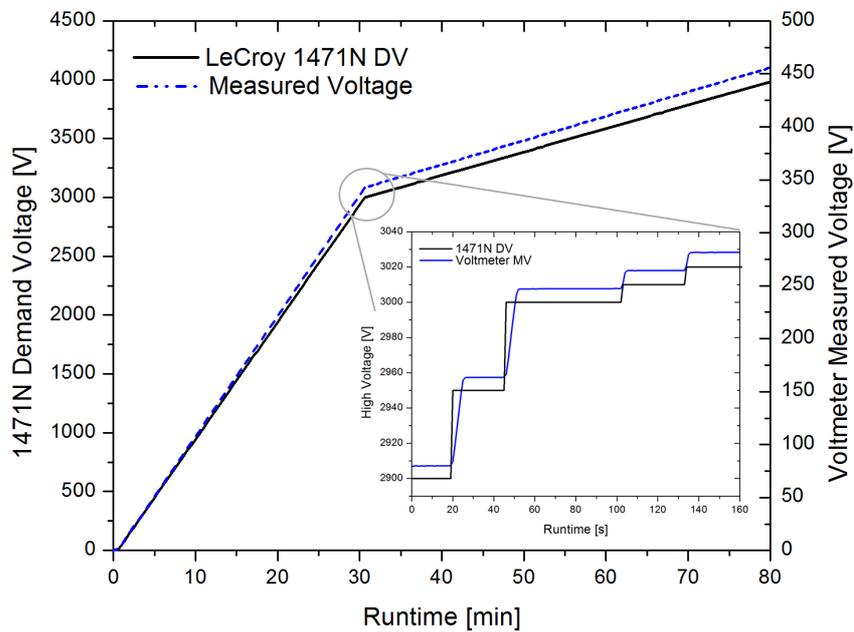
Figure 3.35: Demand Voltage in comparison with actual Measured Voltage over the runtime of the calibration routine.

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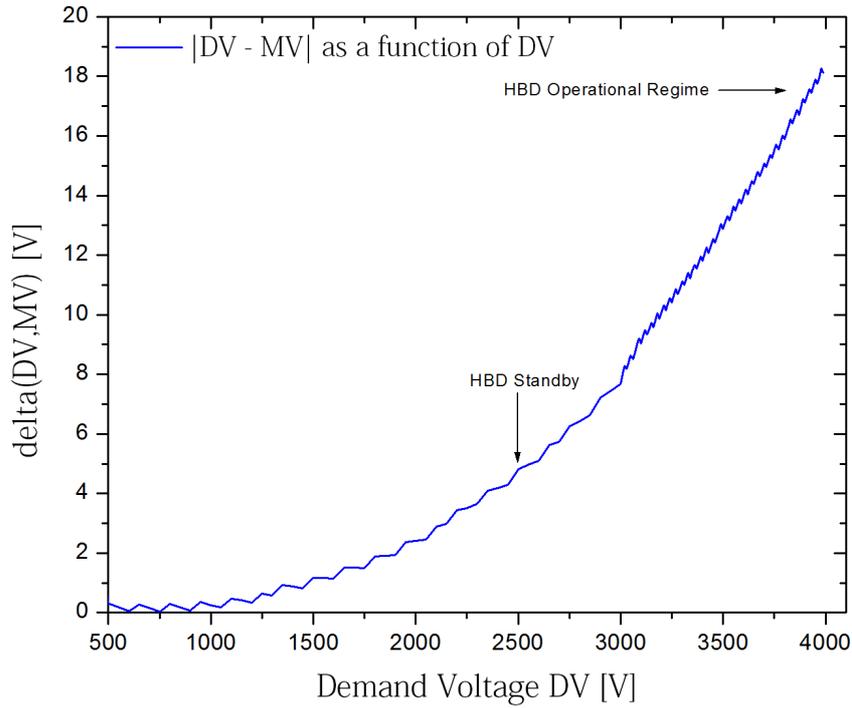
Figure 3.36: The Delta of Demand and Measured Voltage as a function of Demand Voltage.

lights this fact even more. A study of this deviation has shown that at lower voltages the delta between desired output voltage and actual applied voltage by the LeCroy is non-linear, while at higher voltages the offset seems to be linear, which is the operational regime where the HBD is taking data and the bias voltage is of significant importance (see Fig. 3.36).

The HBD Simulation Project had found its end with the installation of the HBD in the IR early December 2008. In a final step of preparing Run-9 calibrations, all resistors installed on every divider board on the detector have been precisely measured in nS, recorded in a certain sequence and transferred to `hvdb` for later use of the TripProtect System. Additionally, each resistor has been labeled according to a specifically designed codex to track any changes (e.g. dead shorts etc.) during Run-9 or Run-10 (see Fig. 3.37).

(a) R-Measurement Sequence

(b) Resistor Codex

(c) Resistor Identification on the HBD via Codex
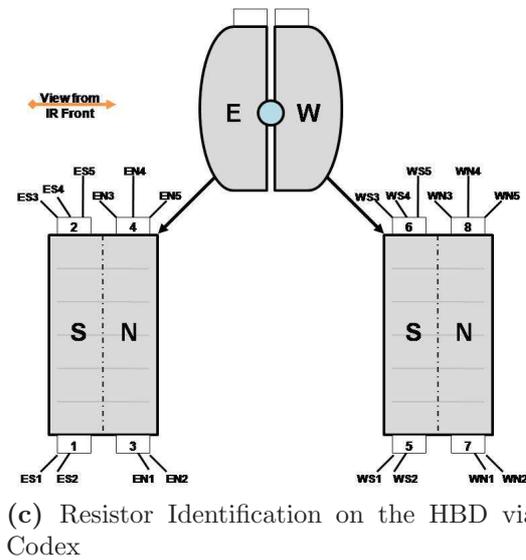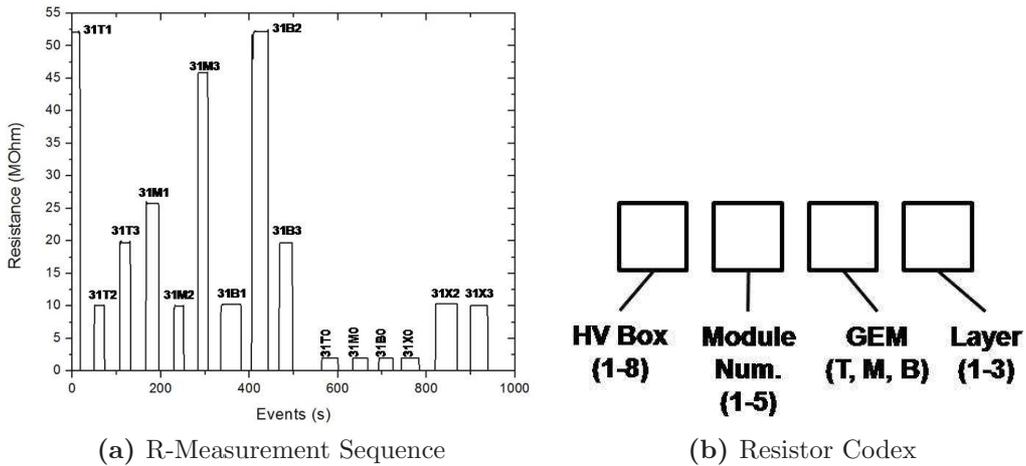
Figure 3.37: Measurement of all divider resistors installed in the HBD.

3.6 Installation in PHENIX

After the successful completion of the design, development and testing of the HBD HV Control and Monitoring System, all of its hardware and software components have been installed in PHENIX in January 2009 after more than 2 years of intense High Voltage research. The transition from the laboratory to the actual control environment in PHENIX went extremely smoothly, which can be understood as the achieved goal of the HBD Simulation Project.

Generally speaking, the entire installation has been completed in two rela-

tively easy steps: first all hardware components, as 1471N modules and Relay boards, are installed on the bridge above the detector, and then all software components installed on the SA1 terminal in the control room.

3.6.1 IR On-Bridge Channel Testing

The entire HV supply for the HBD is located on a bridge built across PHENIX with the detector installed below around the beam pipe. There are two racks; one specifically for the LeCroy PS and the other only for the Relay boxes. The first contains the 1458HP mainframe, which is shared with another mainframe by the Reaction Plane detector group. The rack needs to be water cooled due to the fact that these are high powered mainframes. In case the cooling is defect or supplies are turned off, temperature sensors will cause the power to this rack to be shut off.

With the calibration of each modified 1471N module complete, each board has been installed. In order to communicate with the mainframe, a few steps were required. The BB2 rack containing the terminal server (located North to the HBD on the ground level), identified as TS5, had to be powered up and the RS-232 cable from the mainframe on the bridge connected. Following the line out of the IR, the Ethernet cable from the terminal server was connected to the internal network switch in the Rack Room and configured. All VA machine are communicating with each other through their own switch, which then had to be connected with the other one and so allowing to access the mainframe via TS5.

Back on the bridge, a laptop has been used to run HVC. As part of its tool, the *IR:MF Channel Check* has been used to identify the correct addressing of each channel for GEM and Mesh. The program ramps channel by channel to 50V, first HBD sectors East North → East South, then West North → West South, while one can use a voltmeter to measure and so verify the correct channel assignment. After each channel, the system disables the previous. This test was completed without any problems.

In a next step all Relay board, contained in aluminum boxes, were installed horizontally in their own rack, directly next to the mainframe rack. Between each box, a small gap for air flow as been given. The required 24V and 5V are supplied externally and fed from the mainframe rack. Then the SHV cables (jumpers) between 1471N and Relay boards have been been brought from below to each rack. All cables have been connected in such way that the strength on the outlets is minimized and additionally prevent any possible erroneous connection, which was achieved by shortening the length of each cable to reach only one possible outlet optimally.

The same test as for the 1471N has been repeated, however, this time with the Relay boards connected and a measurement on the HV output channels, neighboring to the corresponding channel input connector from the 1471N. Additionally one were able verify the correct display status of the Relay board LEDs, which proves also the correctness to the Trip Detector on the LeCroy and the correct communication cable used between the two boards.

Finally, the outputs for GEM and Mesh channels were connected to the actual SHV cables reaching down to the detector and supplying HV to all resistor chains, which are mounted in boxes on top and bottom of the HBD.

3.6.2 Implementation to PHENIX Control

Since all of the crucial communication issues were addressed during the hardware installation, the last and not really surprisingly easiest step had to be completed: the installation of the HVC server and client in the control room of PHENIX.

The HBD Simulation Project had used a tunnel from the VA machine to operate HV on the mainframe in the HV laboratory. All that had to be done, was removing the tunnel from the procedure to establish communication to the mainframe, and change the configuration file of the `hvserver` to the address of the terminal server and related port from where the HBD mainframe is accessable. The HBD server was always running on the VA machine during the simulation project, meaning all that was missing for controlling the HBD from the SA1 terminal is a local HVC client. As part of the distribution package of HVC, all one actually needs to do is either run the installer or execute the JAR-file directly by referencing the required Java libraries.

The installation of the HVC Control System was successful and completed within minutes without complications.

Chapter 4

Run-9 Commissioning

Even though the HBD Simulation Project, as discussed in Section 3.5.1, allowed to debug and crash-test the system intensively, the HVC system had never controlled an actual HBD before the RHIC $p+p$ Run-9. Several dynamically changing elements became necessary to determine the optimal control functions: 20 triple-GEM stack channels and 20 corresponding Mesh channels to be operated simultaneously as GEM-Mesh pairs (rather than just one during simulations); the GEM foils' hardware/virtual trip and partial/dead short history; the change of divider resistors during IR access; unexpected crashes of the `hvserver` and the VA machine itself; varying P/T measurements and instant discontinuity of their *hbd* database updates; possible human error of the shift crew and SA1/Expert users; the enforcement of none-HV changes during ongoing DAQ runs; and scenarios that are unknown before they actually occur.

Many of the control systems in PHENIX have years of Run experience incorporated, but still require special attention due to unforeseen circumstances during the Run as well as undiscovered bugs in the code. Therefore, the commissioning of a system during a Run is of fundamental importance in order to minimize the probability of momentary control failures.

The responsibility of the HVC system during Run-9, its commissioning progress and operation of the HBD, has been enormously high. After the HV-related failure of the HBD in Run-7 and its following complete rebuilt, the detector and its first successful commissioning has been entrusted to a completely new HV control system, the HVC. Furthermore, the introduction of its novel computing techniques to the PHENIX infrastructure has been under special supervision.

In this chapter, we will summarize the main activities during the Run-9 commissioning of the HVC system.

4.1 Noise Reduction in Pad Readout

As a fundamental first step, even before any collisions take place, one needs to ensure that all systems of the entire detector can be powered up and operated without affecting each other. The HV system itself has passed this baseline test already in the laboratory and had shown the same level of performance after the installation in PHENIX. However, other instruments of the HBD, e.g. the Resistance Temperature Detectors (RTD) for temperature measurements, Differential Pre-Amplifier and Flash ADCs for the pad readout, become subject of this check.

Pre-commissioning tests of Run-9 in early February 2009 have shown that the HV System, in particular the power supply of the Relay Boards, as well as the supply of the RTD elements (located inside the detector), have been inducing significant noise on the readout of the pads. This coupling effect can be understood as a result of an insufficiently stabilized voltage supply and the *common ground* with the Pre-Amplifiers. Especially for the HBD, a minimal pedestal threshold is required to observe the relatively small primary signal from electrons.

In the laboratory, a 24V and 5V DC stabilized power supply was used to operate the Relay Boards. This option, however, was not available for the rack in which the Relay boards have been installed in the IR. Fire safety regulations require additional cooling, which only for the HV mainframe rack has been provided. Originally, the actual rack supply of the mainframe had been used and trimmed to the appropriate voltages. Due to additional noise

(a) Noisy Relay Supply   (b) Stabilized Relay Supply
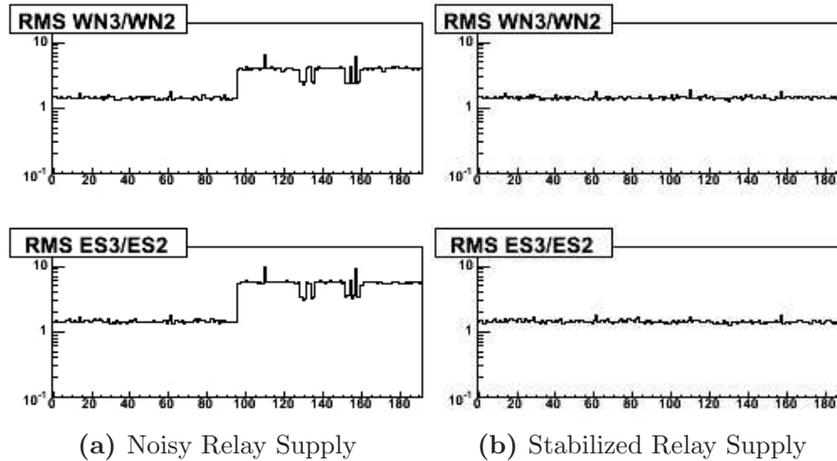
Figure 4.1: HBD Pad Readout. In (a), a noisy power supply for the Relay Board has been used and replaced in (b) with a stabilized supply.

in the pad readout and spacial limitations in the mainframe rack, a custom stabilized voltage supply has been built and placed inside the rack with supply lines to the neighboring Relay rack. In Fig. 4.1, the RMS values for the 92 pads of module WN3, ES3 (channels 1 - 92) and WN2, ES2 (channels 93 - 185) are plotted. The RMS in (a) for WN2 and ES2 are 3.7 and 5.3 respectively. As one can see in (b), the induced noise on modules WN2 (RMS 1.4) and ES2 (RMS 1.4) has been completely removed by changing the Relay power supply. The same idea was followed by powering the RTD elements with a clean power supply, which finally showed similar successful results.

4.2 dV Scans and Module Bias

In chapter 2, we have already discussed the method of rejecting Minimum Ionizing Particles (MIP) and the primary importance for the HBD. One of the goals of the HVC system is to optimally allow this rejection through generating the appropriate drift fields, which is done by adjusting the dV between Mesh and Top GEM, known as the *bias voltage*. The reader is referred to Section 3.2.1 for detailled calculations.

In order to find the optimal reverse bias (RB) voltage for each module, meaning a maximal suppression of the MIP signals, a so-called *dV Scan* is performed. The procedure is as follows:

1. Logged into the HVC client as an Expert user, one may check the *Bias Master* panel to ensure that the detector is in Reverse Bias mode (Fig. 4.2). Then the *Options* tool (see Fig. 4.3) can be loaded and *Bias > Reverse Bias* selected. At this point, the bias voltage for each module shall be set to the same value and then saved to `hvdb`.

Figure 4.2: HBD Bias Master Switch panel of HVC.

2. The *Ramp Control* (RC) of HVC is used to ramp the detector to each module's operational voltage, whereby the previously saved bias settings
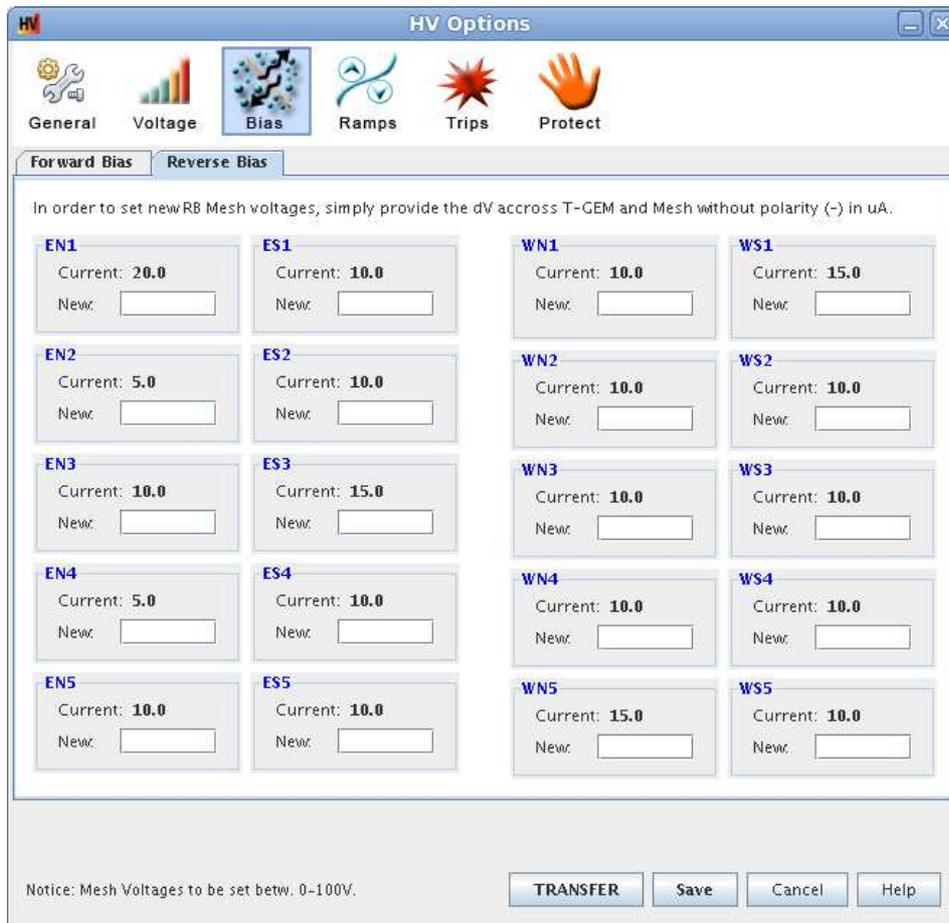
Figure 4.3: Options Tool and Bias Configuration of the HBD.

are loaded for the determination of the final Mesh HV. One may verify the desired applied bias voltage by looking at the reconstruction column in the *Surveillance Panel*.

3. As RHIC collisions are taking place, with reasonable backgrounds, the PHENIX DAQ system is activated to read out the HBD pad signals for about 5 million events. A unique run number is associated with the collected data and written together to its PRDF file and independently by HVC to `hvdb`.

4. After repeating steps 1-3 for multiple bias voltages, typically from 0V to 25V RB in 5V steps, one can plot the resulting *pulse height spectra* for all modules. Each histogram represents a combination of signals resulting from scintillation light and MIPs, following an exponential and Landau

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distribution, respectively. In Fig. 4.4, the results of the first dV Scan of Run-9 for four modules is presented. Each line corresponds to one DAQ run at a certain bias voltage: +30V forward bias (red; 2.9M events), 0V or zero bias (black; 2.1M events), -5V RB (green; 2.5M events), -10V RB (blue; 2.5M events), -15V RB (yellow; 2.7M events) and -20V RB (magenta; 2.1M events). One can clearly see the separation and suppression of the MIP signals and this way find the optimal bias voltage for every module individually. The final dV values can be entered with the *Options* tool to `hvdb`, which are then permanently enforced by RC at any particular voltage.

A legitimate concern one may have is the linear supply of the actual output voltage. The dV Scan is done at the currently used P/T trigger set, meaning a specified operational voltage at some presently measured P/T. If a few hours after the scan, the P/T significantly varies and finally falls into a new trigger bin, the operational voltage for each module will change. Even though the

(a) Sector Scan EN2

(b) Sector Scan ES3

(c) Sector Scan WN2

(d) Sector Scan WS1
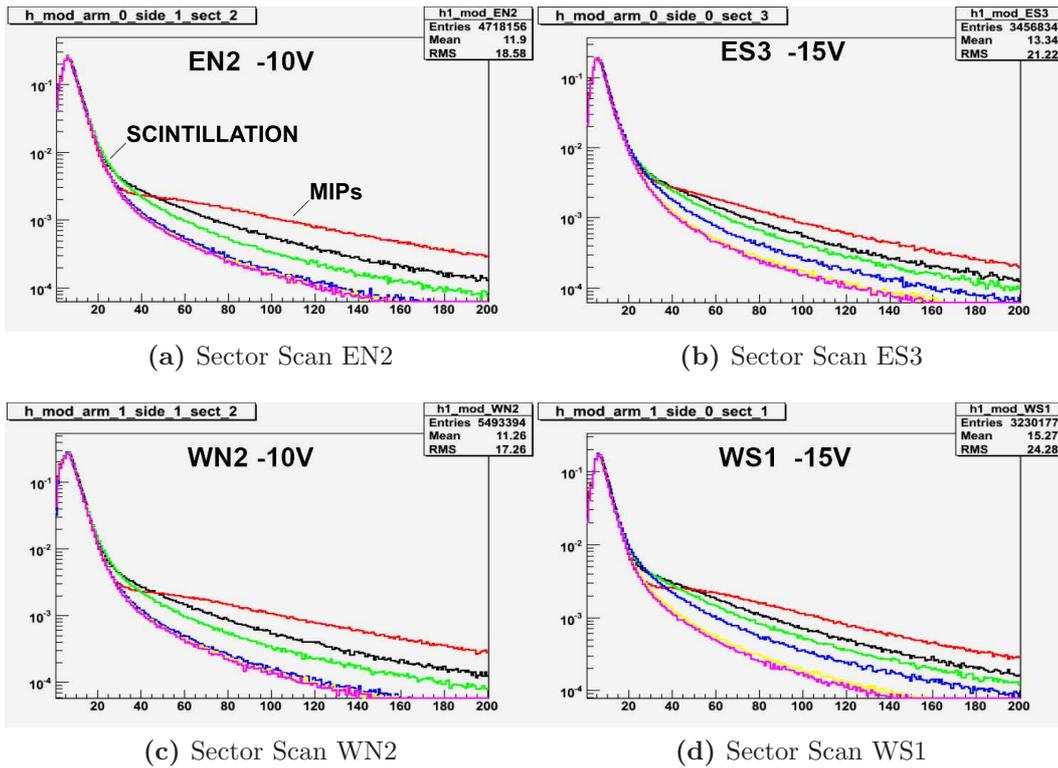
Figure 4.4: HBD Run-9 dV Scan Results (DAQ run numbers: 2740[58]-[63]). (see text for color scheme)

bias voltages are fixed, a deviation from the optimal rejection is possible, if the output voltage would follow a non-linear behavior. Exactly this issue has been already addressed during the HBD Simulation Project. As we have seen in Section 3.5.2, the 1471N modules do provide a non-linear output, especially at high voltages. Therefore, HVC utilizes calibration functions to accommodate for these variations and so allows the same MIP rejection factors as achieved during the dV Scan for all P/T trigger bins.

The dV Scan has been repeated several times during Run-9 in order to attune for changes of the GEM foils and replacements of 1471N boards. Only a few modules required a 5V change of their bias voltage, while all others remained unchanged throughout the entire run.

4.3   Resistor Modifications and Bertan Tests

The TripProtect System (TPS) notifies the shift crew and HBD experts through a virtual trip alert, if any of the modules appear to have a new partial or dead short. In such a case, as extensively discussed in Section 3.4.10, the overall current draw of a triple-GEM stack has exceeded a certain deadzone or threshold as determined by TPS. The critical consequence is a significant gain drop of the particular module. If a partial short is present, the gain may even vary during a run of the DAQ and therefore make the analysis of the data from this sector extremely difficult.

On a bi-monthly basis, access to the IR is granted and therefore allows to compensate for shorts by replacing resistors on the particular divider board. Each GEM foil has a $R_{\text{GEM}} = 10\text{M}\Omega$ resistor across, while the remaining resistors have been chosen to increase the dV across the transfer gaps in order to achieve higher effective gains, which then allows to operate the detector at lower voltages (see Section 3.2.1; *voltage asymmetry*). The additional current draw through the GEM changes this ratio and requires a modification of the chain. The idea is to measure the current across the GEM, identify the resistance of the short and replace either the resistor across the GEM or modify the corresponding string. The goal of this modification is to essentially still keep the same current ratio to the other strings as there would be no short at all. In terms of the Run-9 divider board, this means that one would like to keep a total resistance of 84MΩ per string. A complete dead short in one of the strips would lower this resistance by $\sim 3.3\text{M}\Omega$. In this case, the compensation is trivial, since the R_{GEM} can be simply replaced with a 20MΩ resistor, which results again in a parallel resistance of the original 10MΩ. However,

aside from this "perfect" infinite impedance status, typically partial and/or multiple shorts are present, which may exacerbate this procedure.

The LeCroy measures the current of the entire chain, meaning the sum of all three parallel strings, and therefore does not provide any information of which GEM of the triple-stack is suffering from a new short. Furthermore, the 1471N is only capable of measuring current in the μA regime from 1 - 200μA and therefore wouldn't be sensitive to partial shorts at lower voltages, e.g. $R_{\mathrm{GEM}} > 50\mathrm{M}\Omega$ at a dV of 50V. Therefore, the so-called *Bertan* HV supply is used for measurements in the nA regime. The procedure of these tests in the IR is as follows:

- HVC is brought into IR Access mode, which shuts down the 1458HP mainframe;

- The three jumpers on the divider board are lifted, the R_{GEM} resistor removed and the Bertan PS connected;

- The voltage is brought up in small steps to 500V or until GEM sparking prevents a further increase;

- At each step, a current reading is taken and the corresponding resistance of the short R_{short} plotted live versus the applied voltage in order to observe the overall trend the GEM is following; if measurements at previous IR access days were taken, a comparison can provide insight to the short development over time;

- Based on these measurements, one can then calculate the optimal replacement resistor for R_{GEM},

$$R_{\mathrm{replace}} = \frac{10\mathrm{M}\Omega \times (R_{\mathrm{short}} + 20\mathrm{M}\Omega)}{R_{\mathrm{short}} + 10\mathrm{M}\Omega},$$

and in case a non-linear current increase is found, the resistor replacement with R_{replace} at an operational dV is recommended.

Nevertheless, if a partial short is present and its trend indicates a development to a dead short at higher voltages, the selection of the replacement resistor may be sometimes made with the assumption of a continuing progression towards a complete dead short. As an example of such a scenario in Run-9, test results of the Top GEM of module EN4 for two consecutive IR access days are presented in Fig. 4.5. After HVC reported a virtual trip of this module, Bertan measurements on 05/13/09 have shown that the Top
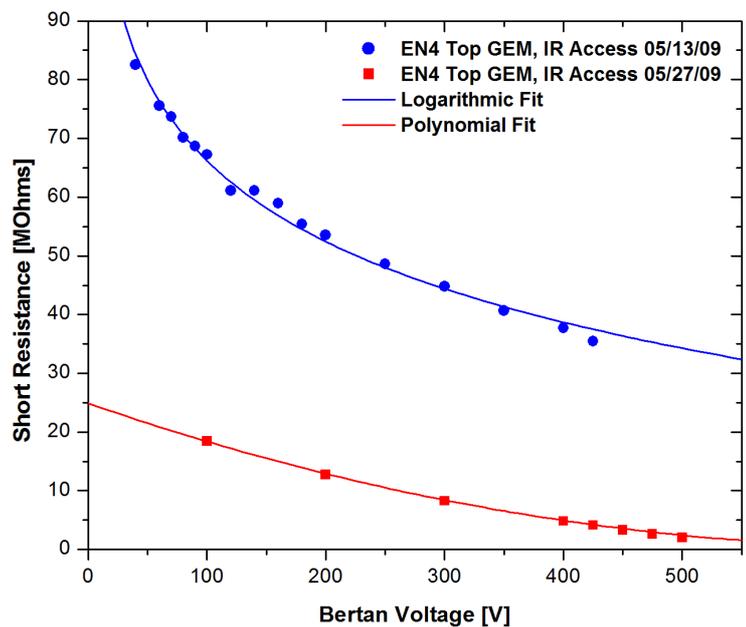
(a) Measurement of the short's resistance
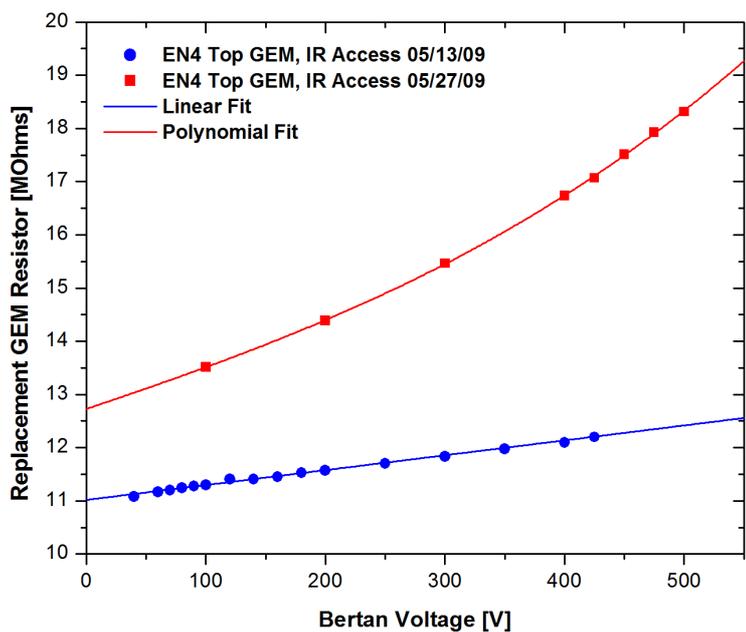
(b) Optimal 10MΩ GEM Resistor Replacement

Figure 4.5: Bertan Test Results of module EN4. The comparison of two IR access days shows the development of a partial (blue line) towards a dead short (red line).

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GEM had a partial short of logarithmically varying resistance over the entire dV range. According to (a), a plateau at approx. 50MΩ is reached on an operational voltage level, and based on (b), a replacement of the 10MΩ GEM resistor with a 12.2MΩ resistor is suggested. Even though the resistor modification seems to be appropriate at the time of this measurement, the state of EN4 is extremely unstable and may either heal itself or develop furthermore towards a dead short. This means that during such a process the gain will significantly fluctuate and may become for certain DAQ runs and their analysis not useful. Nonetheless, the new resistor has been put into place and EN4 has been ramped up to operational voltage with HVC, meaning with the LeCroy, in order to verify the expected current draw of the entire chain. During the next two weeks of regular data taking, the partial short became worse and another Bertan test on 05/27/09 was required. As seen in (a), the variation of the short resistance over the entire voltage range is now much smaller and closer to a complete dead short. Although (b) recommends a replacement resistor of about 18.5MΩ, a 20MΩ resistor has been chosen instead, as one can assume a continuation of this trend towards a dead short.

4.4 HV Module Calibrations

The HVC Ramp Control (RC) and TripProtect System (TPS) have been calibrated initially at the beginning of Run-9. All resistors installed in any divider board were precisely measured and results written to `hvdb` in order to allow the application of correction factors when new demand voltages are sent to the 1471N modules (see Section 3.5.2). As already discussed in Section 3.4.10, the deadzones of TPS also require to be dynamically adjusted for each module. The expected current (EC) and so initially the measured current (MC) of a module shall be centered between the upper and lower virtual trip thresholds for all possible applied voltages. This has to be true at the time the voltage-dependend calibration function for EC is generated. However, when during an IR access resistors in the chains are modified in order to compensate for previously detected shorts, such an initial calibration of EC has to be repeated in order to be sensitive to new partial/dead shorts.

The HVC suite comprises a completely automated TPS calibration system, which one can activate in Expert Mode under *Tools > Eagle Eye > HV Calibration*. The panel of Fig. 4.6 opens and by clicking the "Calibration" button, the user permits HVC to take full control over the HBD; all other functionalities on the main control panel are deactivated during this time. It is recommended to run this calibration right after the resistor modifications were made on the IR access day and preferable before any new stores begin

Figure 4.6: HV Calibration Control Panel for TPS.

and the regular data taking continues.

The control routine HVC will use for this calibration is as follows:

- Depending on its previous configuration by a superuser, the RC ramps the entire detector along a globally defined step function. Each step represents a certain voltage, which we may refer to hereafter as a *key voltage.* Once such a key voltage has been reached, the HBD is kept on this plateau for a fixed timeout period, before all modules are ramped to the next higher key voltage. The default configuration would ramp the detector from 500V to 4kV in 100V steps with a timeout period of 60 seconds. During the entire ramp, the Backup System on the HBD Server tags all measurements with a unique `runid`. As soon as the ramp is complete, all channels are disabled and demand voltages are reset to 0V.

- After the successful completion of the ramp, the tagged collected data in `hvdb` is being analyzed. First each key voltage is identified by comparing demand and measured voltages. The settling time of the current after

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reaching the particular plateau is taken into consideration and removed from further analysis. It can be usually found 1 or 2 $\times \tau_S$ after the measured voltage has approached its demand. The remaining voltage and current measurements on each plateau are then used to compute their mean values respectively. This information is already sufficient to characterize each module with only 5 values: the mean ratio of all voltages and currents, meaning the parallel resistance of the entire chain; the total variation of resistance dR from minimal to maximal key voltage; and 3 coefficients of a 3rd order polynomial fit, describing the behavior of the resistance at all key voltages.

- All 5 characterizing values are written to the control configuration policy of HVC for each module and centrally stored on the HBD Server. The polynomial coefficients are then used by TPS to dynamically vary the EC for all applied voltages. One may then already recognized constantly 100% in the MC:EC column of the Surveillance Panel, which means that the measured current represents the center of the threshold bin for any particular voltage. At this point, TPS is now sensitive to new partial or dead shorts.

All the analysis results are provided even online on the HBD Expert website right after the calibration run has been completed. The voltage vs. current and parallel resistance vs. voltage is plotted immediately and allows to track the health of each GEM-stack throughout the entire Run-9. As an example, problem module EN4 is shown in Fig. 4.7 for three separate calibrations after an IR access. The significant change of the dR value as well as the non-linear behavior over all key voltages from 04/02/09 to 05/27/09 already indicates the presence of shorts. A healthy GEM-stack would have a typical dR of about 0.2μA.
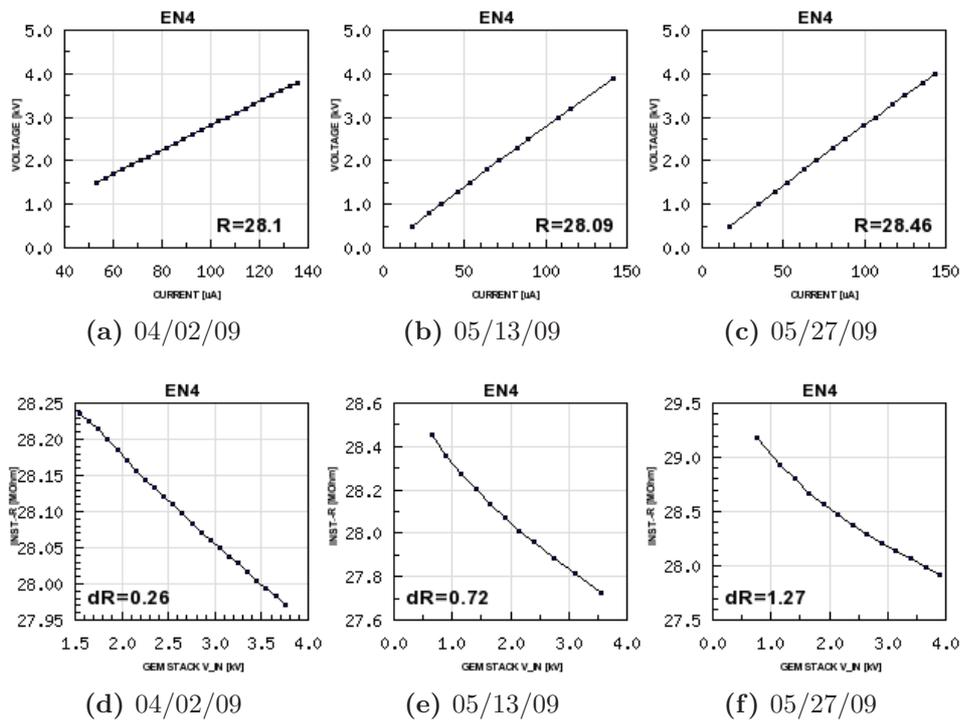
Figure 4.7: Run-9 TPS Calibration Runs for module EN4. The voltage vs. current relation in (a-c) remains linear, while the progression of parallel resistance vs. voltage in (d-f) proofs the short development.

Chapter 5

Results and Discussion

One of the remarkable possibilities the HBD HV Control and Monitoring System has introduced, is the ability to gain insight into not just internal processes of the system itself but also the state of every single GEM-stack, which, as discussed in chapter 3, is realized through the continuous data logging into `hvdb` by the Global Detector Status Module (GDSM) and Mainframe Backup Thread, respectively. This logging feature has been one of the most useful tools throughout the commissioning process of Run-9 and allowed the reconstruction of events that may have led to new or a change of partial shorts of any particular module over any given period of time, which is vital in diagnosing possible improvements with the HBD HV scheme.

Since the Control Monitor of HVC has access to external resources, e.g. the PHENIX DAQ, HBD signal data (module gain), P/T measurements inside the detector, the applied field of the Central Magnets as well as its own storage of previous data in the database, which are used by the system to determine new control functions or verify itself of the TDS-required optimal control state and are after the completed internal analysis written to `hvdb`, one has been able during Run-9, to essentially monitor the internal performance of the system and therefore determine if a modification of the system's control policies would be necessary to improve its overall performance as well as that of the HBD.

Due to the imprint of control actions and states of each GEM-stack over time recorded in `hvdb`, making this database the most trusted source of HV information, one can study the performance of HVC in direct relation to the overall HBD performance. In this section we may present a summary of the results obtained from Run-9.

5.1   Online Performance and Stability

After its installation in PHENIX, the HVC system went officially online on January 30, 2009 and has been used during the commissioning of the HBD, before on March 1, the Shift Crew at the PHENIX Control Room began to actively running the controlling HVC client for first RHIC collisions. The system has been in control of the HBD for more than 4 months, before on July 7, the Run-9 ended and the system brought to offline status.

The system has been running for ~ 3790 hours and collected a total of 12 GB of HV data in `hvdb`; the contribution of raw module data (GEM and Mesh channel) from the mainframe is ~ 362 MB/module. The amount of data produced is reasonable as one needs to account for the fact that the TripProtect System requires an update rate of 5s in order to efficiently detect variations of current; hence, the MF Backup System needs to catch and record the same package of data in order to allow the Control Monitor later on the determination of optimally applied control (see 3.1).

As requested by TDS and predicted by the concurrent programming methods used to obtain system stability (see 3.4.11), Run-9 has proven that HVC is capable of running stably independent of requested control actions by users as the SA1 or HBD experts. Over the entire operational time of Run-9, neither the HBD Server nor the HVC client did crash once of a self-induced cause. However, one was able to see the *hvserver* crashing multiple times, which even then did not induce a crash of the HBD Server. Since all detector subsystems in PHENIX are required to use the *hvserver* as a tool to send commands to the mainframe, the crashing of this server is a general concern and causes every HV system to crash – except HVC.

5.2   Module Trip – Magnetic Field Correlation

Early studies in Run-7 have strongly indicated a relation between the appearance of partial/dead shorts in GEM foils and the ramping of the Central Magnets (CM). The theory at the time, which remains unchanged until today, assumes dust particles, which have remained after the production process inside of the detector, move and fall into the GEM holes, causing a spark of enough energy to create a film inside the hole of some resistance. This indicates that the cleanliness during production is fundamentally crucial in minimizing such effects.

During Run-9, the Central Magnets have been ramped up/down many times, usually at the end of a fill or IR access days to provide detector subsys-

tems the opportunity to obtain calibration data (Zero-Field Runs). Before the Shiftleader executes the ramp from the control terminal, the SA1 is asked to bring the HBD to 2500V, which we call Standby voltage. Nevertheless, unlike to the "phenomenon" found in Run-7, a clearly proven correlation pattern between CM and new GEM shorts as a function of time was not possible to find. Although, there have been extremely few indications over the entire period of Run-9, that such correlation might exist. However, in comparison with the detector production techniques used for Run-7 and Run-9, which have been for the latter different for each arm, one can find a clear correlation between (cleanliness–amount of dust particles) and the appearance of shorts. As an overall review of Run-9 shows, primarily only modules in the East Arm have suffered new shorts during the Run, while the West Arm, for which a different production method with a much higher degree of cleanliness was utilized, performed close to perfect.

5.3   Gain Stability

As we have discussed in detail in Section 3.4.8, the HBD requires a stable gain, especially during a single Run of the PHENIX DAQ, in order to allow data analysis. There are overall 2 possible sources to affect the gain: either by changing the HV or variations of P/T. Since we have control over the HV, the P/T remains a variable that must be accounted for. The P/T Monitor and Control Unit have specifically been designed to use the information of measured P/T to determine how HVC would need to adjust the applied voltage in order to achieve an overall stable gain. In the following, we will present the results from Run-9 and discuss if the applied corrections were successful.

5.3.1   HV and Module Gain Behavior over Runtime

The data collected in Run-9 has shown that for modules with partial or dead shorts, a variation in gain is not completely controlable as random fluctuations can occur during a Run (state when HV modification is prohibited), which can be understood as a change of R_{short}; this behavior is highly enhanced for modules with partial shorts. Therefore, we shall compare a problematic East Arm module with partial shorts, EN3, with a module from the West Arm with no shorts, WN3.

Gain Variation – HV const.   In Fig. 5.1, the measured (mean) voltage from `hvdb` and measured gain from the pulse height spectra (stored in the

OnCal database) for a series of runs over global runtime is plotted. As one can see, in this case for EN3, the HV has not been changed by HVC, but the gain did increase by $\sim 50\%$. Between the two significant data points, a zoom-out box for applied voltage indicates that the detector has been at Standby before a new run started at operational voltage, but with a dramatic change in gain. A charge-up effect within the GEMs after such long downtime may have affected the E-field within the GEMs, which in turn affects the gain. As the measured P/T during this timeframe indicates, as shown in Fig. 5.2, P/T varied only by $\sim 0.25\%$ and therefore stayed within its bin of [2.529 - 2.556] Torr/K. The goal, as discussed in section 3.4.10, is to create a permitted gain window of about $\pm 10\%$. HVC recorded this scenario and reported the problem.
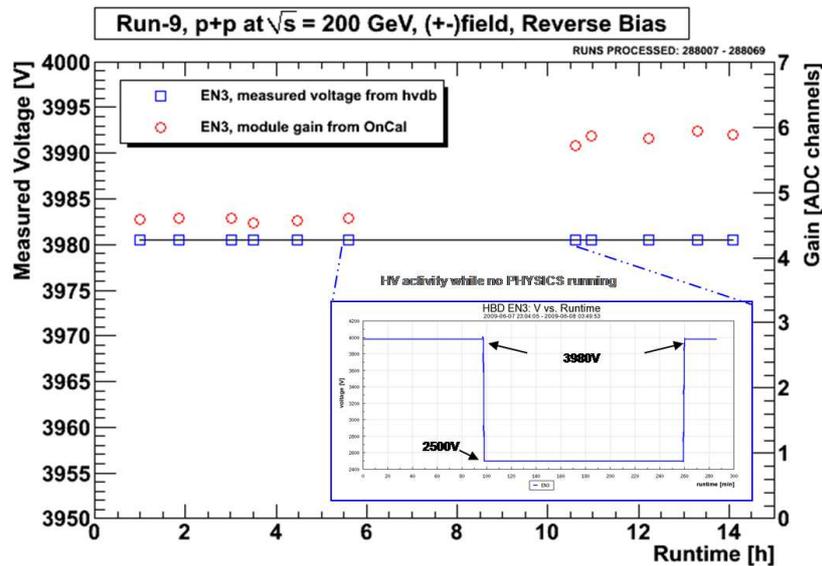
Figure 5.1: Measured voltage and Module Gain vs. Runtime for sector EN3

Gain Variation – HV Adjustment. In another example, shown in Fig. 5.3, the gain of EN3 increased dramatically by $\sim 96\%$, while the module tripped earlier and the HV had to be adjusted due to a significant change of P/T (see Fig. 5.5), passing the P/T boundary to the next higher bin. If one compares this with WN3 in Fig. 5.4, a much smaller change of 22% in gain was found for the same time period. This relatively large variation for a healthy module as WN3 is rather unusual, however, does not matter if the overall gain stays within the allowed band and does not randomly fluctuate.
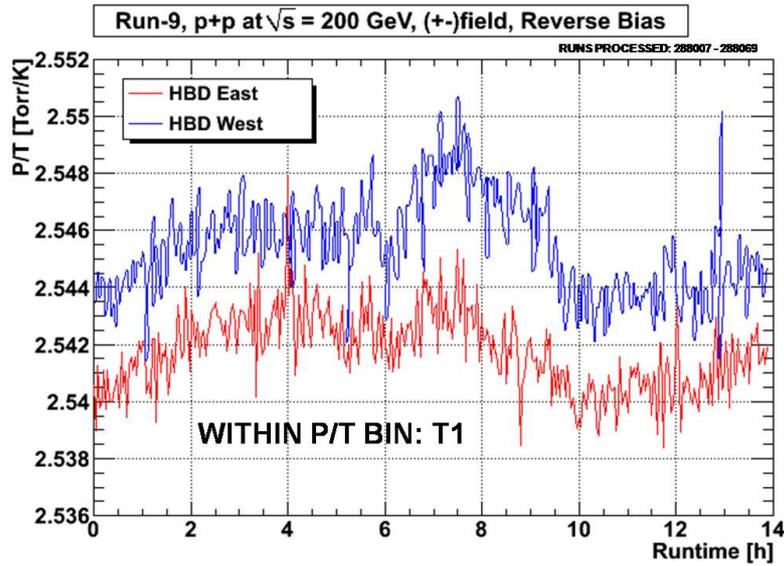
Figure 5.2: Measured P/T vs. runtime of 5.1.
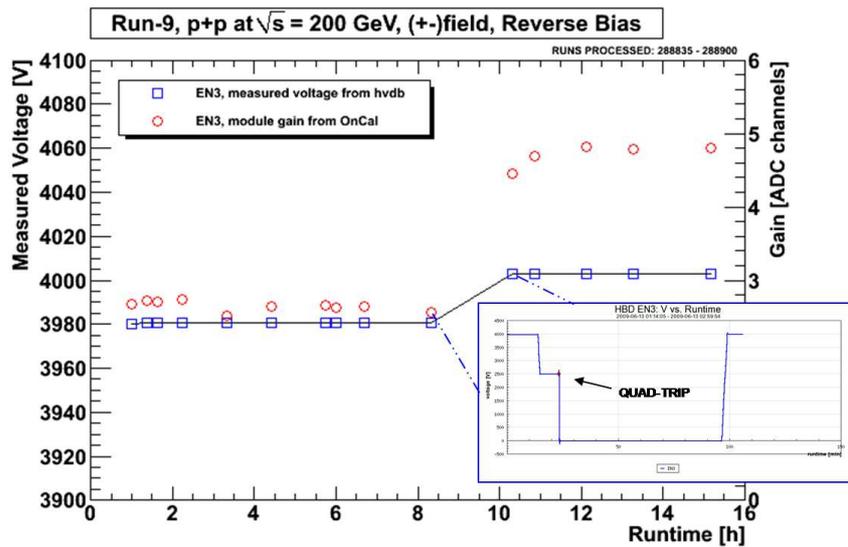
Figure 5.3: Measured voltage and Module Gain vs. Runtime for sector EN3.

Gain Stable – HV Adjustment. The previous case for WN3 is addressed with the fact that HVC does perform long-term analysis to determine a modules characteristics. Therefore, we zoom out from Fig. 5.4 and see a change of correcting voltage and a remaining overall stable gain. The change to a different T-bin has been justified by the variation from T1 to T2 bin (Fig. 5.7). An IR access and even higher P/T in between the downtime, did not

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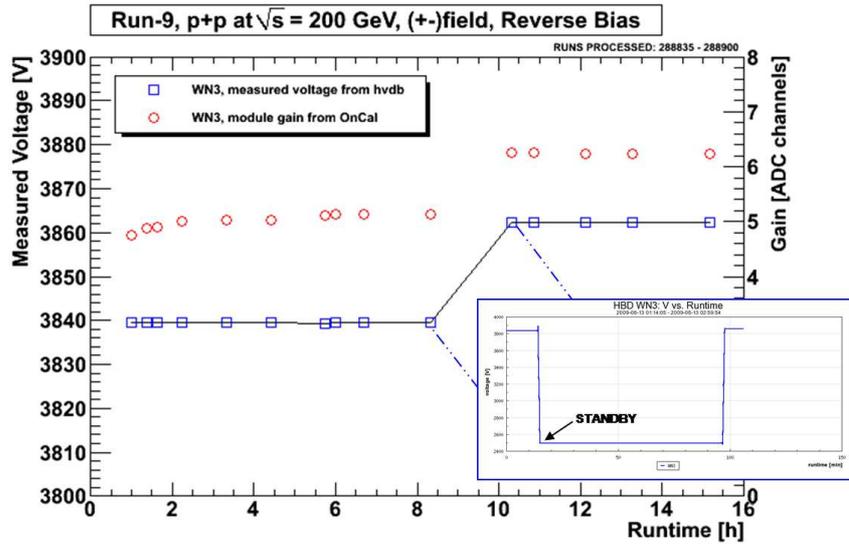
Figure 5.4: Measured voltage and Module Gain vs. Runtime (as 5.3) for sector WN3.
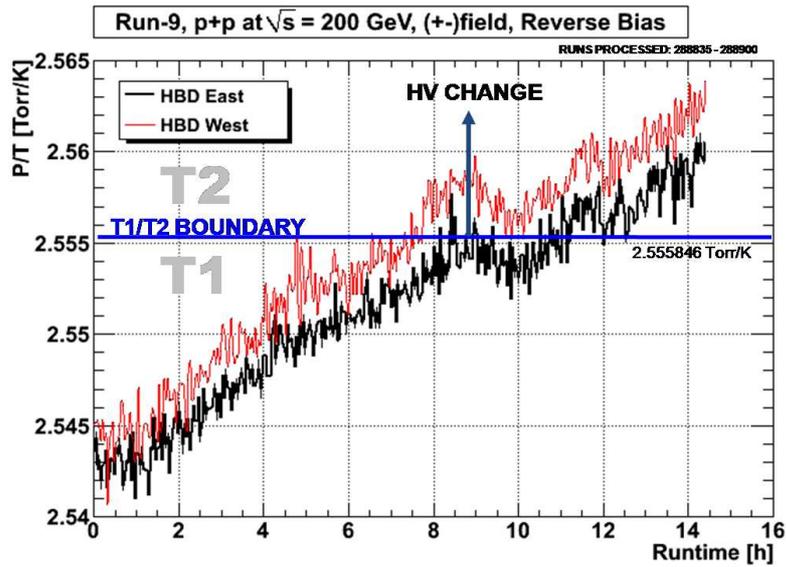
Figure 5.5: Measured P/T vs. runtime of 5.3 and 5.4.

make any difference.

Gain Stability for Run-9 200 GeV runs. In summary for corrections applied during Run-9, it has been found that P/T variations, which are weather-dependend (Fig. 5.8) in terms of changes in pressure, most of the times stay

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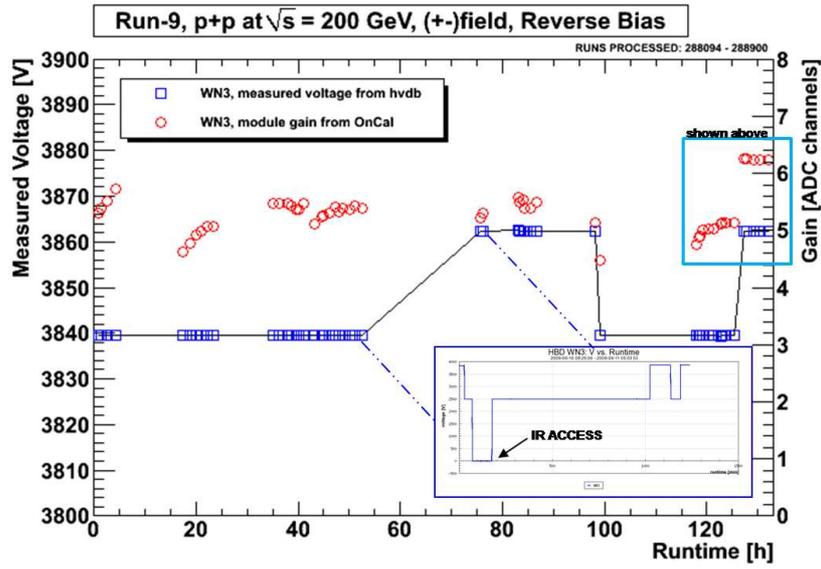
Figure 5.6: Measured voltage and Module Gain vs. Runtime for sector WN3.
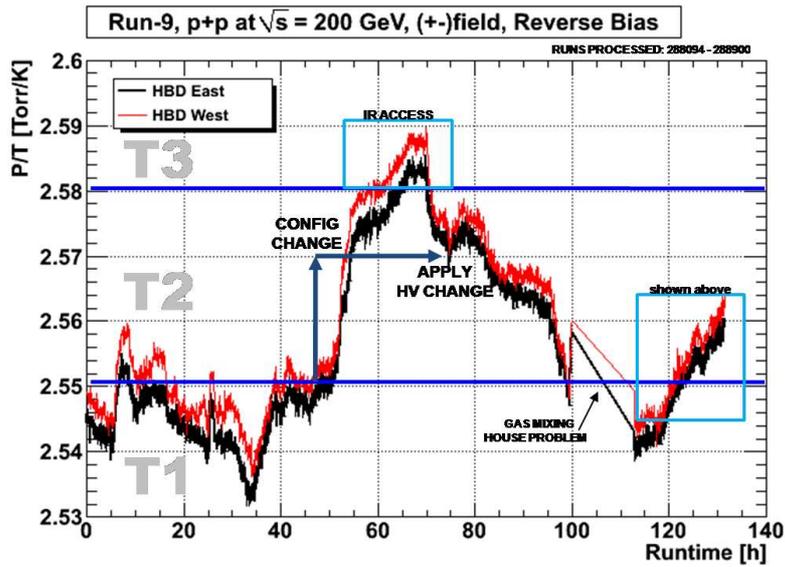
Figure 5.7: Measured P/T vs. runtime of 5.6.

within the bins T2 and T3, which refer to [2.556 - 2.583] and [2.583 - 2.61], respectively. Fig. 5.9, where gain for one module from the East and the other from the West is plotted for all 200 GeV runs in T2 and T3 bins, and proves that the overall HV corrections do keep the overall gain stable.
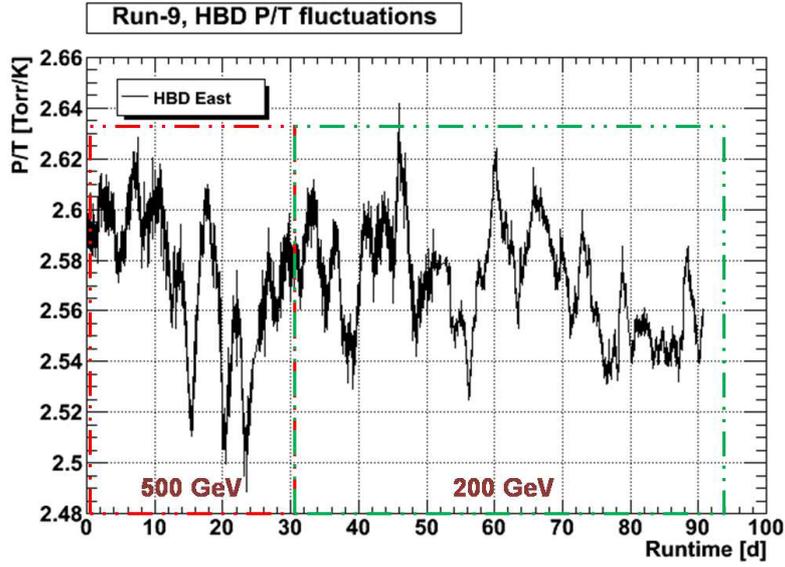
Figure 5.8: Measured P/T vs. runtime of all runs in Run-9.
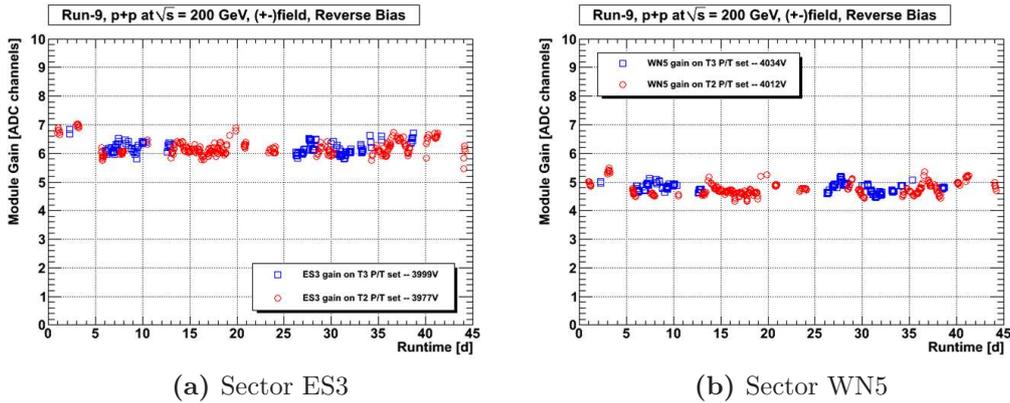
(a) Sector ES3   (b) Sector WN5

Figure 5.9: Module Gain for P/T sets T2 and T3.

5.3.2 Gain Fluctuations in Respect to P/T Variations

The purpose of the previous section has been to illustrate that the gain of modules with partial shorts is extremely difficult to control. However, if a module is completely healthy (no shorts) or does only have dead shorts, HVC's P/T Control Monitor allows the compensation of gain fluctuations due to P/T variations very effectively. Fig. 5.10 shows a comparison of P/T fluctuations and the measured module gain of WN5 for the entire Run-9 period. As one can see, the gain is overall stable, while tremendous P/T fluctuations occur.
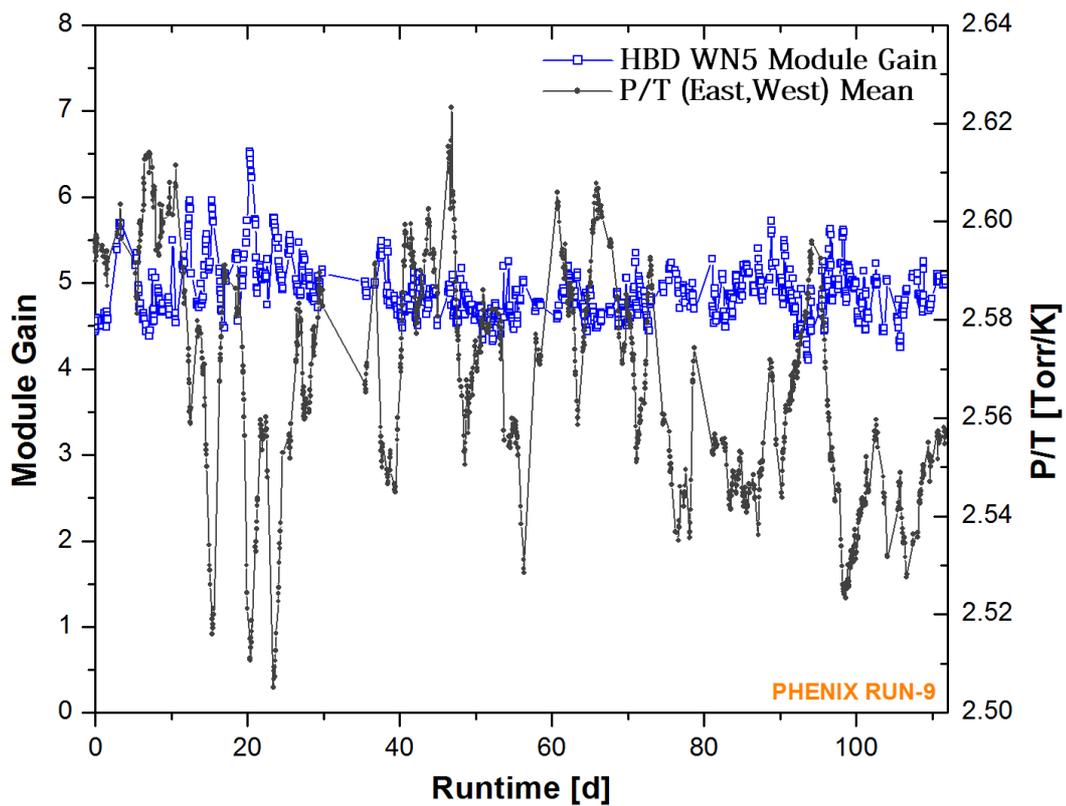
Figure 5.10: Measured P/T and Module Gain of WN5 vs. runtime of all runs in Run-9.

Chapter 6

Summary and Outlook

A new High Voltage Control and Monitoring System (HVC) for the Hadron Blind Detector (HBD) was developed and shown to optimize the detector's performance through intelligent HV application.

Based on the damaging sources for GEM foils, as found in the HBD in Run-7, a fast-response GEM protection system implemented to eliminate any stored energy that may dissipate through the GEM stack. It comprises a 1471N LeCroy module for which the phase sent to the FET is measured. At its disappearance an external HV relay is activated to prevent any severe discharge to the GEM stacks. Since the Mesh channel is not drawing any current, a back-to-back zener diode is used to control the dV between Top GEM and Mesh to prevent discharges of the Mesh to the top electrode of the Top GEM.

The overall control system is following fundamental concepts of Optimal Control Theory and the introduction of a global response time constant. The transformation to its pratical realization has been achieved by utilizing a modern C/S architecture and concurrent programming with multicore processors. Each subsystem has been designed to fully use these baseline resources.

The entire system has been extensively tested as part of the HBD Simulation Project, which allowed to simulate the HBD in a laboratory environment while using the control infrastructure of PHENIX remotely. It is due to this project that the following installation in PHENIX and final operation has been a great success.

The HVC system has been controlling the HBD throughout the p+p Run-9 at RHIC and has met all expectations and beyond. The system is expected to lead the HBD through its most important operation in the Au+Au Run-10.

There are many opportunities for other applications of HVCs underlying control principles and possible extensions. One can extend HVC to other detector technologies by modifying 3 fundamental objects:

- Control Parameters,

- Sampling Rate,

- Analysis of Parameters.

HVC moves with the technological progress in computing (multi-core, grid, etc.) and is already capable of controlling high performance applications, where hundreds of parameters change dynamically and a pattern recognition is needed within milliseconds.

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Appendix A

HVC Theory of Dynamic Control

The foundation we are building on the model of a high voltage control system in fulfillment of the Control Objective (CO) is based on novel ideas and concepts of *Modern Optimal Control Theory*. Since we do not expect the reader to be familiar with corresponding mathematical structures, we are first providing a few basic notes, before exploring and defining the core of the system, which is finally used for practical development of the HBD HV System.

General Notes. Assume a system, which future is entirely determined by its initial affecting conditions, while the near future varies smoothly with the initial data. If we now allow certain parameters of such a system to change at every instant of time, we find ourselves a control system of smooth dynamical relationships. Having the scope of the final control purpose in mind, we shall restrict our discussion to a smooth dynamical system, which is governed by a family of ordinary differential equations (ODE) on a finite dimensional smooth manifold. The family is parametrized by *control parameters* $u(t)$ and defined on a Riemannian manifold M, which is also known as the *state space* of the control system. As discussed in more detail later on, parameters include e.g. module activity, demand voltages, ramp up/down speeds or hardware/virtual trip currents. Their admissible values are free to set at any time through a *control* or a *control function*. Once the control has been fixed by this selection, the control system transforms into a nonautonomous ODE, which solution represents an admissible trajectory of the control system – a curve in the state space, and is so uniquely determined by its initial condition or state. Simply speaking, different controls "generate" different admissible trajectories, filling the attainable set of an initial fixed state or starting point.

A first problem the final HV Control System (HVC) needs to be capable of

to solve is the one of *Controllability*, the systematic characterization of states reachable from the initial one. Once the potentiality to reach a certain state has been established, the system may then solve the *Optimal Control* problem by determining the shortest admissible trajectory connecting initial and final state and the minimization of other possible cost.

State Space Model. The desired behavior of a dynamical system Σ can be achieved through careful determination of controlling parameters $u(t)$, the input, via analyzing conjunction with its measurable controlled parameters $y(t)$, the output, as well as disturbances $z(t)$ of Σ, the reference vector r_u and external requests $x(t)$ by HVC users. The process is realized by introducing an intelligent controller, which finally executes the control function. Crucial for the practical implementation is to understand that the concept of Σ contains an inseparably associated time set T, demanding the timely execution and evaluation of admissible actions at each moment of time $t \in T$. A technique to handle the HBD-specific requirements and definition of T are discussed in terms of a global response time constant in the following section. Here we only need to be aware of the fact that $T \subset \mathbb{R}$ is ordered and so continuous in time with naively speaking variable gaps from t_i to t_{i+1}, $\forall\, i \in \mathbb{Z}$. Both, the input and output may retrieve their values from a fixed set U and Y respectively. However, it is important to notice that the input segments of a system should never allowed to be arbitrary functions $\omega : (t_i, t_{i+1}] \rightharpoonup U$, but rather be belong to a restricted policy class Ω. The very same we apply for the output, although with much milder restricted segments $\gamma : (t_{i+1}, t_{i+2}] \to Y$.

Let us now summarize our discussion formally:

Definition 4 *A smooth dynamical system Σ, in respect to its feasibility of high voltage control, shall be defined by the following axioms:*

(a) *There exists a given ordered time set $T \subset \mathbb{R}$, a state set X, a set of controlling parameters U, a set of admissible controlling functions $\Omega = \{\omega : T \to U\}$, a set of controlled output parameters Y, and a set of controlled output functions $\Gamma = \{\gamma : T \to Y\}$.*

(b) *X and Ω are topological spaces.*

(c) *The control space $\Omega = \varnothing$ (nontrivial) has a control segment $\omega_{(t_i, t_{i+1}]} \in \Omega$, which is restricted to $(t_i, t_{i+1}] \cap T, \forall i \in \mathbb{Z}$.*

(d) *There exists a transfer function $\Phi : T \times T \times X \times \Omega \to X$, also referred to as a trajectory, which value represents the state $x(t) = \Phi(t; \tau, x, \omega) \in X$ resulting at time $t \in T$ from the initial state $x(\tau) \in X$ at initial time $\tau \in$*

T through the execution of the control $\omega \in \Omega$. Due to the smoothness of Σ, the state-transition map Φ has the property of $(\tau, x, \omega) \mapsto \Phi(\cdot; \tau, x, \omega)$ defining a continuous map $T \times X \times \Omega \to C^1(T \to X)$.

At this point, we'd like to notice that whenever we talk about a (control) *event* or phase, we do refer to the pair (τ, x), with $\tau \in T$ and $x \in X$. The event space or phase space of Σ is also known as the set $T \times X$.

As one may recall, a dynamical system governed by an ODE is a *flow*, a one-parametric group of transformations, generated by a vector field. Hence a control system represents a family of vector fields, which parameters are invariant under transformations induced by smooth transformations of the state space. This almost self-introduces the idea to extend our previously defined classical model to the much more powerful era of Modern Geometry. Here we gain a wide class of re-parametrizations of vector field families, which are recognized as **feedback transformations** in Control Theory or gauge transformations in Geometry and Mathematical Physics. Furthermore, the structure of attainable sets and admissible trajectories is closely related to the dynamical system generated group of transformations, which symbolize the heart of Geometry. By following this abstract path, the overall control system we are designing may seem more complex on first sight, however, instead it rather simplifies the entire practical design process as seen later on through its beautifully symmetric structure. For the discussion of this extended state space model, the reader may also note that by following the notational convention, hereafter, a state is referred to as q, rather than x in the classical theory.

Let us introduce a smooth k-dimensional manifold M, a Hausdorff paracompact topological space endowed with a smooth structure. Recalling its fundamental property, it is covered by coordinate neighborhoods, a system of open subsets, $M = \cup_\alpha \mathcal{O}_\alpha$. The local coordinate system defined by a homeomorphism $\Phi_\alpha : \mathcal{O}_\alpha \to \mathbb{R}^k$ for all subsets, such that all compositions $\Phi_\beta \circ \Phi_\alpha^{-1} : \Phi_\alpha(\mathcal{O}_\alpha \cap \mathcal{O}_\beta) \subset \mathbb{R}^k \to \Phi_\beta(\mathcal{O}_\alpha \cap \mathcal{O}_\beta) \subset \mathbb{R}^k$ are diffeomorphisms. A reminding illustration of this coordinate system we'll be using to define our control system on, is shown in Fig. .

Using this formalism, the future state $q(t, q_0)$ with $t > 0$ of a dynamical system is again completely determined by the present state $q_0 = q(0, q_0)$. The flow P^t is $q_0 \mapsto q(t, q_0)$ and the *dynamics* of the system $\dot{q} = V(q)$ with $q \in M$ and can so be identified by one vector field $V(q)$. Since we would like to control this system by affecting its dynamics, we introduce a family of vector fields V_u, which we parametrize through the previously discussed control parameters
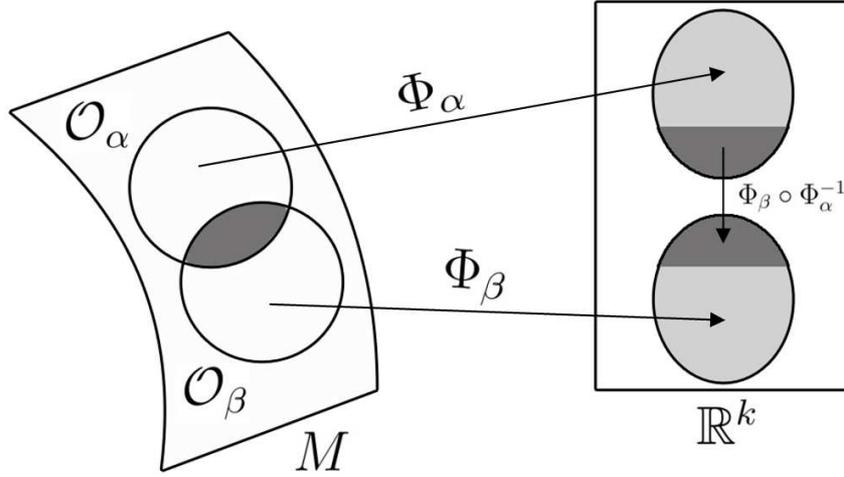
Figure A.1: Coordinate System for HBD HVC system, defined on a smooth manifold M.

$u \in U$, whereby the control-para space U is a subset of a smooth manifold to restrict allowed control actions to the detector. What we find is the most *general version of a control system*:

$$\dot{q} = V_u(q), \qquad q \in M, \;\; u \in U, \tag{A.1}$$

where $\forall u \in U$ the corresponding vector field $V_u \in \mathrm{Vec}M$ generates the flow P_u^t. In this respect, consider the following basic scenario: suppose one would like to raise a currently applied voltage by 1kV. Since there are multiple ways to reach this plateau, the system will choose from a pre-selected ramp pattern; we may assume asymptotic. The current state with all its parameters, incl. measured voltage, current, etc., is represented by the point $q_0 \in M$. First off, the system will calculate the entire set of n control parameters $u_i \in U, i \in \{1, n\} \subset \mathbb{N}$ that are necessary to achieve the target voltage. During a ramp, the overall system may leave its equilibrium and cause instabilities the control needs to adjust for. Therefore, the proposed control strategy u_i needs to be evaluated ahead of the execution in terms of achievable points, which shall be for our example consist of 5 control functions:

$$\{P_{u_5}^{t_5} \circ \cdots \circ P_{u_2}^{t_2} \circ P_{u_1}^{t_1}(q_0) | t_1, \ldots, t_5 \geq 0, n \in \mathbb{N}\}$$

The 2-D surface of this operation is shown in Fig. A.2 (left). In reality however, the system needs to evaluate all reachable points, which are given by the attainable set $\mathcal{A}_{q_0}$, as illustrated in Fig. A.2 (right), for (A.1) with piecewise-constant control from an initial state $q_0 \in M$ for a specific time

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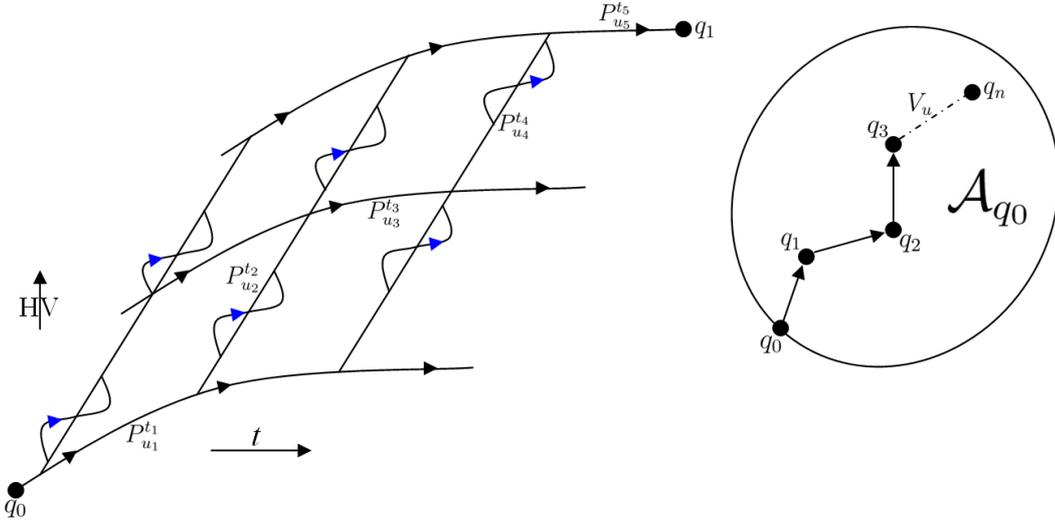
Figure A.2: 2D surface of control trajectories (left) and the attainable set (right) for voltage modifications by HVC.

$t \geq 0$:

$$\mathcal{A}_{q_0} = \{P^{\tau_k}_{u_k} \circ \cdots \circ P^{\tau_1}_{u_1}(q_0) | \tau_i \geq 0, \sum_{i=1}^{k} \tau_i = t, u_i \in U, k \in \mathbb{N}\}. \qquad (A.2)$$

As previously discussed, we need to restrict possible control actions in order to realize practical operation and so need to allow only positive ordered $t \in T \neq \emptyset$. The attainable set may now be defined as:

$$\mathcal{A}_{q_0} = \bigcup_{t \in T} \mathcal{A}_{q_0}(t). \qquad (A.3)$$

At this point we are able to define the final dynamic control system we shall use for its technological development for the HBD:

Definition 5 *(TDC) A smooth HV control system operating on the state space M is a smooth mapping $f : V \to TM$, where $V = M \times U$ is a locally trivial bundle over M, $TM = \bigcup_{q \in M} T_q M$ a tangent bundle, and $f(V_q) \subset T_q M$ for any $V_q = \{q\} \times U$, $q \in M$. An admissible pair for control action is a bounded (compact closure of image) measurable mapping $v(\cdot) : [t_i, t_{i+1}] \to V, \forall i \in \mathbb{N}$ such that $t \mapsto \pi(v(t)) = q(t)$ with submersion π is a Lipschitzian trajectory in M with restricted attainable set $\mathcal{A}_{q_0}$ and $\dot{q} = f(v(t))$ for almost all $t \in [t_i, t_{i+1}] \subset T$, where the T represents the set of (resolution) τ_S-dependend, ordered times $t \geq 0$ and its integral cost is a functional $J_{t_i}^{t_{i+1}}(v(\cdot)) = \int_{t_i}^{t_{i+1}} \Phi(v(t))dt$ with Φ being a smooth scalar function on V.*

The task to realize such a control system in practical terms is not an easy one. TDC is fundamentally helpful to understand and visualize the underlying concepts compactified in mathematical patterns, but overall it tells us more than we actually may want to know, even far more than we can presently absorb or profitably analyze. Especially in science it seems to be ironical that we first have to throw away information in order to understand. At least from today's state of technological progress and the level of our current intellectual development, we cannot wrestle with a high order of complexity, instead we must consequently simplify.

Appendix B

P/T Control Tables of Run-9

In this chapter, we present the configuration tables for each of the five P/T bins and all possible adjustments to achieve a gain of 2000 (g2k), 4000 (g4k), 6000 (g6k), 8000 (g8k) and 10000 (g10k). The HBD was primarily operated on the *g2k* settings during Run-9.

Table B.1: P/T trigger bin thresholds in Torr/K for Run-9. [center of bins (ID = CB), lower bin threshold (ID = LT), upper bin threshold (ID = UT)]

ID	T1	T2	T3	T4	T5
CB	2.542383	2.569309	2.596235	2.623162	2.650088
LT	2.52892	2.555846	2.582772	2.6096985	2.636625
UP	2.555846	2.582772	2.6096985	2.636625	2.663551

Table B.2: HV Settings for Trigger Bin T1.

Chn	g2k-HV	g2k-dV	g4k-HV	g4k-dV	g6k-HV	g6k-dV	g8k-HV	g8k-dV	g10k-HV	g10k-dV
EN1	3917	466.310	4000	476.190	4049	482.024	4084	486.190	4111	489.405
EN2	3784	450.476	3867	460.357	3916	466.190	3951	470.357	3978	473.571
EN3	3896	463.810	3980	473.810	4029	479.643	4064	483.810	4091	487.024
EN4	3755	447.024	3838	456.905	3887	462.738	3922	466.905	3949	470.119
EN5	3829	455.833	3913	465.833	3962	471.667	3996	475.714	4023	478.929
ES1	3788	450.952	3872	460.952	3921	466.786	3955	470.833	3982	474.048
ES2	3796	451.905	3880	461.905	3928	467.619	3963	471.786	3990	475
ES3	3871	460.833	3954	470.714	4003	476.548	4038	480.714	4065	483.929
ES4	3720	442.857	3804	452.857	3853	458.690	3888	462.857	3915	466.071
ES5	3792	451.429	3876	461.429	3925	467.262	3960	471.429	3987	474.643
WN1	3892	463.333	3941	469.167	4025	479.167	4060	483.333	4087	486.548
WN2	3881	462.024	3930	467.857	4014	477.857	4048	481.905	4075	485.119
WN3	3790	451.190	3839	457.024	3923	467.024	3958	471.190	3985	474.405
WN4	3809	453.452	3858	459.286	3941	469.167	3976	473.333	4003	476.548
WN5	3941	469.167	3990	475	4073	484.881	4108	489.048	4135	492.262
WS1	3988	474.762	4037	480.595	4121	490.595	4155	494.643	4182	497.857
WS2	3892	463.333	3941	469.167	4024	479.048	4059	483.214	4086	486.429
WS3	3794	451.667	3843	457.500	3927	467.500	3962	471.667	3989	474.881
WS4	3806	453.095	3855	458.929	3939	468.929	3974	473.095	4001	476.310
WS5	3867	460.357	3916	466.190	4000	476.190	4035	480.357	4062	483.571

Table B.3: HV Settings for Trigger Bin T2.

Chn	g2k-HV	g2k-dV	g4k-HV	g4k-dV	g6k-HV	g6k-dV	g8k-HV	g8k-dV	g10k-HV	g10k-dV
EN1	3939	468.929	4023	478.929	4072	484.762	4106	488.810	4133	492.024
EN2	3806	453.095	3890	463.095	3938	468.810	3973	472.976	4000	476.190
EN3	3919	466.548	4002	476.429	4051	482.262	4086	486.429	4113	489.643
EN4	3777	449.643	3861	459.643	3909	465.357	3944	469.524	3971	472.738
EN5	3851	458.452	3935	468.452	3984	474.286	4019	478.452	4046	481.667
ES1	3810	453.571	3894	463.571	3943	469.405	3978	473.571	4005	476.786
ES2	3818	454.524	3902	464.524	3951	470.357	3986	474.524	4012	477.619
ES3	3893	463.452	3977	473.452	4026	479.286	4060	483.333	4087	486.548
ES4	3743	445.595	3826	455.476	3875	461.310	3910	465.476	3937	468.690
ES5	3815	454.167	3898	464.048	3947	469.881	3982	474.048	4009	477.262
WN1	3914	465.952	3963	471.786	4047	481.786	4082	485.952	4109	489.167
WN2	3903	464.643	3952	470.476	4036	480.476	4071	484.643	4098	487.857
WN3	3813	453.929	3862	459.762	3945	469.643	3980	473.810	4007	477.024
WN4	3831	456.071	3880	461.905	3964	471.905	3998	475.952	4025	479.167
WN5	3963	471.786	4012	477.619	4096	487.619	4130	491.667	4157	494.881
WS1	4010	477.381	4059	483.214	4143	493.214	4178	497.381	4205	500.595
WS2	3914	465.952	3963	471.786	4047	481.786	4082	485.952	4108	489.048
WS3	3816	454.286	3865	460.119	3949	470.119	3984	474.286	4011	477.500
WS4	3829	455.833	3878	461.667	3961	471.548	3996	475.714	4023	478.929
WS5	3890	463.095	3939	468.929	4022	478.810	4057	482.976	4084	486.190

Table B.4: HV Settings for Trigger Bin T3.

Chn	g2k-HV	g2k-dV	g4k-HV	g4k-dV	g6k-HV	g6k-dV	g8k-HV	g8k-dV	g10k-HV	g10k-dV
EN1	3961	471.548	4045	481.548	4094	487.381	4129	491.548	4156	494.762
EN2	3828	455.714	3912	465.714	3961	471.548	3996	475.714	4022	478.810
EN3	3941	469.167	4025	479.167	4074	485	4108	489.048	4135	492.262
EN4	3799	452.262	3883	462.262	3932	468.095	3967	472.262	3993	475.357
EN5	3874	461.190	3957	471.071	4006	476.905	4041	481.071	4068	484.286
ES1	3833	456.310	3916	466.190	3965	472.024	4000	476.190	4027	479.405
ES2	3840	457.143	3924	467.143	3973	472.976	4008	477.143	4035	480.357
ES3	3915	466.071	3999	476.071	4048	481.905	4083	486.071	4110	489.286
ES4	3765	448.214	3849	458.214	3898	464.048	3932	468.095	3959	471.310
ES5	3837	456.786	3921	466.786	3970	472.619	4004	476.667	4031	479.881
WN1	3937	468.690	3986	474.524	4069	484.405	4104	488.571	4131	491.786
WN2	3926	467.381	3974	473.095	4058	483.095	4093	487.262	4120	490.476
WN3	3835	456.548	3884	462.381	3968	472.381	4002	476.429	4029	479.643
WN4	3853	458.690	3902	464.524	3986	474.524	4021	478.690	4048	481.905
WN5	3985	474.405	4034	480.238	4118	490.238	4153	494.405	4180	497.619
WS1	4033	480.119	4082	485.952	4165	495.833	4200	500	4227	503.214
WS2	3936	468.571	3985	474.405	4069	484.405	4104	488.571	4131	491.786
WS3	3839	457.024	3888	462.857	3971	472.738	4006	476.905	4033	480.119
WS4	3851	458.452	3900	464.286	3984	474.286	4018	478.333	4045	481.548
WS5	3912	465.714	3961	471.548	4045	481.548	4079	485.595	4106	488.810

Table B.5: HV Settings for Trigger Bin T4.

Chn	g2k-HV	g2k-dV	g4k-HV	g4k-dV	g6k-HV	g6k-dV	g8k-HV	g8k-dV	g10k-HV	g10k-dV
EN1	3984	474.286	4067	484.167	4116	490	4151	494.167	4178	497.381
EN2	3850	458.333	3934	468.333	3983	474.167	4018	478.333	4045	481.548
EN3	3963	471.786	4047	481.786	4096	487.619	4131	491.786	4158	495
EN4	3821	454.881	3905	464.881	3954	470.714	3989	474.881	4016	478.095
EN5	3896	463.810	3980	473.810	4029	479.643	4063	483.690	4090	486.905
ES1	3855	458.929	3939	468.929	3988	474.762	4022	478.810	4049	482.024
ES2	3863	459.881	3946	469.762	3995	475.595	4030	479.762	4057	482.976
ES3	3938	468.810	4021	478.690	4070	484.524	4105	488.690	4132	491.905
ES4	3787	450.833	3871	460.833	3920	466.667	3955	470.833	3982	474.048
ES5	3859	459.405	3943	469.405	3992	475.238	4027	479.405	4054	482.619
WN1	3959	471.310	4008	477.143	4092	487.143	4126	491.190	4153	494.405
WN2	3948	470	3997	475.833	4081	485.833	4115	489.881	4142	493.095
WN3	3857	459.167	3906	465	3990	475	4025	479.167	4052	482.381
WN4	3876	461.429	3924	467.143	4008	477.143	4043	481.310	4070	484.524
WN5	4008	477.143	4057	482.976	4140	492.857	4175	497.024	4202	500.238
WS1	4055	482.738	4104	488.571	4188	498.571	4222	502.619	4249	505.833
WS2	3959	471.310	4008	477.143	4091	487.024	4126	491.190	4153	494.405
WS3	3861	459.643	3910	465.476	3994	475.476	4029	479.643	4055	482.738
WS4	3873	461.071	3922	466.905	4006	476.905	4041	481.071	4068	484.286
WS5	3934	468.333	3983	474.167	4067	484.167	4102	488.333	4129	491.548

Table B.6: HV Settings for Trigger Bin T5.

Chn	g2k-HV	g2k-dV	g4k-HV	g4k-dV	g6k-HV	g6k-dV	g8k-HV	g8k-dV	g10k-HV	g10k-dV
EN1	4006	476.905	4090	486.905	4138	492.619	4173	496.786	4200	500
EN2	3873	461.071	3956	470.952	4005	476.786	4040	480.952	4067	484.167
EN3	3986	474.524	4069	484.405	4118	490.238	4153	494.405	4180	497.619
EN4	3844	457.619	3927	467.500	3976	473.333	4011	477.500	4038	480.714
EN5	3918	466.429	4002	476.429	4051	482.262	4086	486.429	4113	489.643
ES1	3877	461.548	3961	471.548	4010	477.381	4045	481.548	4072	484.762
ES2	3885	462.500	3969	472.500	4018	478.333	4052	482.381	4079	485.595
ES3	3960	471.429	4044	481.429	4093	487.262	4127	491.310	4154	494.524
ES4	3810	453.571	3893	463.452	3942	469.286	3977	473.452	4004	476.667
ES5	3882	462.143	3965	472.024	4014	477.857	4049	482.024	4076	485.238
WN1	3981	473.929	4030	479.762	4114	489.762	4149	493.929	4176	497.143
WN2	3970	472.619	4019	478.452	4103	488.452	4138	492.619	4165	495.833
WN3	3880	461.905	3929	467.738	4012	477.619	4047	481.786	4074	485
WN4	3898	464.048	3947	469.881	4031	479.881	4065	483.929	4092	487.143
WN5	4030	479.762	4079	485.595	4163	495.595	4197	499.643	4224	502.857
WS1	4077	485.357	4126	491.190	4210	501.190	4245	505.357	4272	508.571
WS2	3981	473.929	4030	479.762	4114	489.762	4148	493.810	4175	497.024
WS3	3883	462.262	3932	468.095	4016	478.095	4051	482.262	4078	485.476
WS4	3896	463.810	3945	469.643	4028	479.524	4063	483.690	4090	486.905
WS5	3957	471.071	4006	476.905	4089	486.786	4124	490.952	4151	494.167

Appendix C

Miscellaneous Images

C.1 HBD Simulation Project

Please refer to Section 3.5.1 for a detailled discussion and results of the HBD Simulation Project. All images shown here are from the HBD HV laboratory at the Physics Bld., BNL.

Figure C.1: Overview of the hardware components of the HBD Simulation Project.

(a) LeCroy and CAEN Mainframes

**(b)** HV Test Boxes for Resistor Chain and Divider
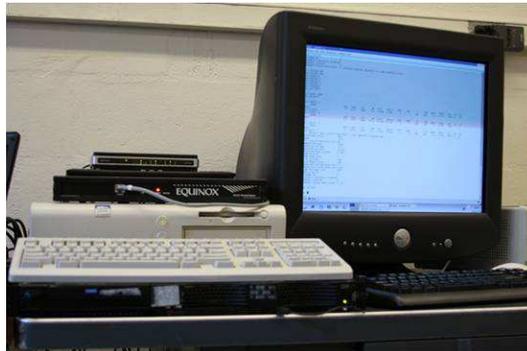
(c) HBD & Terminal Server

(d) HVC Client Control

Figure C.2: The main units of the HBD Simulation Project.

C.2 HBD Operation with HVC in PHENIX

The basic tools of the platform-independent HVC (client) version 2.0 are the *Main Control Panel*, the *Module Control* and the *P/T Control Monitor*. These tools, as shown in Fig. C.3, were most frequently used by the PHENIX Shift Crew during Run-9. The Main Control Panel provides a general overview of

the current status of the detector, e.g. the Bias Mode (RB/FB), the voltage level (Standby/Operational), the number of tripped, currently recovering, ramping and disabled HV channels as well as the PHENIX DAQ run number. The Module Control serves as the tool to activate or enable, deactivate or dis-
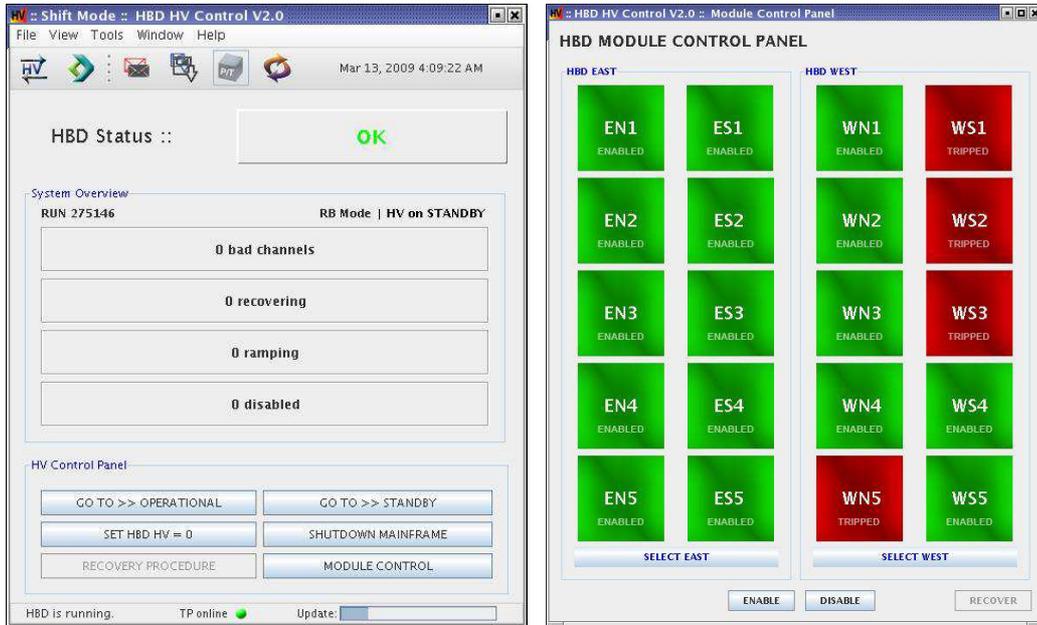
(a) Main Control Panel

(b) Module Control

(c) P/T Control Monitor

Figure C.3: The HVC's basic control tools used by the Shift Crew at PHENIX.

able and to recover either virtual trips (initiated by TPS) or hardware trips. Another important tool is the P/T Control Monitor. It allows to monitor the currently measured P/T in both detector arms and informs the Shift Crew, if the P/T has passed its current trigger bin and the adjustment of the operational voltages is necessary. The actual change of voltages can then simply performed by acknowledging the adjustment and allowing Ramp Control to update the mainframe settings; the system will then take care of everything
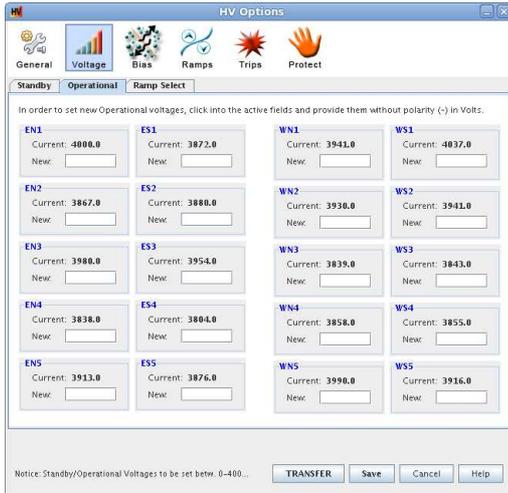
(a) HV Settings
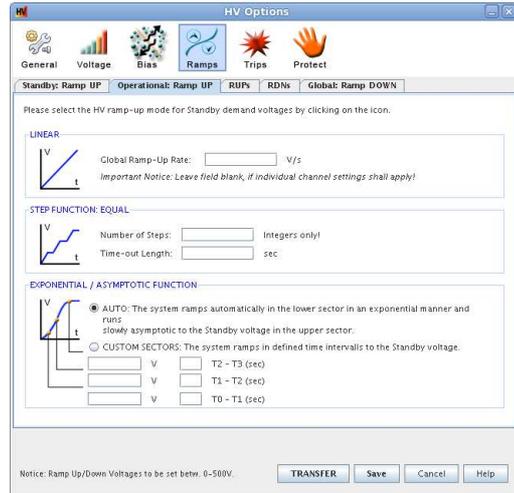
(b) Ramp Settings
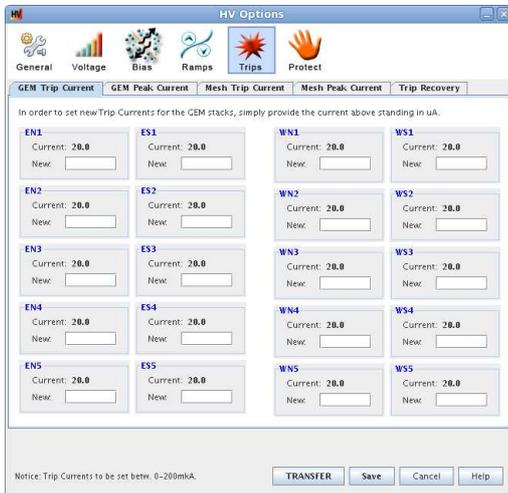
(c) Trip Settings
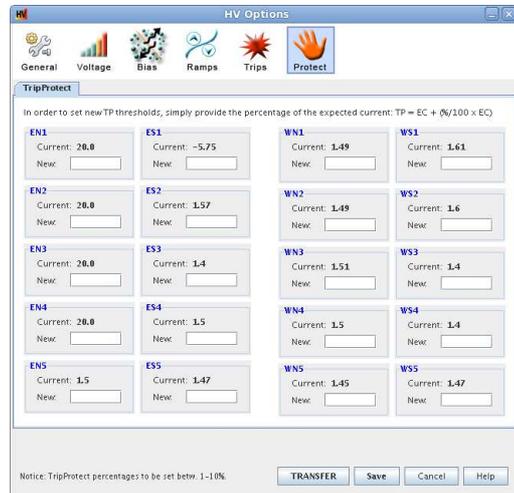
(d) TPS Settings

Figure C.4: The HV Options Tool for HBD Experts to configure the fundamental HVC control parameters.

else. The main panel for HBD Experts is the *HV Options Tool* (see Fig. C.4), which allows to configure voltage, bias and trip settings for each detector module as well as the sensitivity of the Trip Protect System (TPS).

The most important monitoring tool for both the Shift Crew and HBD Experts is the *HV Surveillance Panel*, as shown in Fig. C.5. Each GEM channel is listed with the raw settings directly from the HV mainframe, e.g. the demand voltage (DV), the measured voltage (MV), the measured current (MC), the measured peak current (MPC), the agreement of measured with expected current in percentage (MC:EC), the trip protect setting in percentage (TP), the lower and higher threshold or so-called deadzones for virtual trips (DZ_l and DZ_h), the ramp up and down speeds in V/s (RUP and RDN) as well as the hardware trip threshold for slow current and peak current (TC and TPC). The demand and measured voltage (M:DV and M:MV) and the measured current (M:MC) for the corresponding Mesh channel is listed as well. Furthermore, the currently applied dV (RB/FB), activity status (enabled and disabled) and the global trip status indicating virtual or hardware trips (OK, vtrip, htrip).

HBD HV Surveillance Panel

HBD | HV Channel Listing

Chn	DV	MV	MC	MPC	MC:EC	TP	DZ_l	DZ_h	RUP	RDN	TC	TPC	M:DV	M:MV	M:MC	dv	STATUS	TRIP
EN1	-2500.0	-2500.4	-89.605	-89.635	99.969	20.0	-71.706	-107.559	25	25	-109.619	-200.0	-2421.0	-2422.2	-0.054	20.0 RB	enabled	OK
EN2	-2500.0	-2500.4	-90.468	-90.464	101.319	20.0	-71.432	-107.149	25	25	-109.276	-200.0	-2436.3	-2436.8	0.0040	5.0 RB	enabled	OK
EN3	-2500.0	-2499.8	-89.082	-87.221	99.919	20.0	-71.324	-106.985	25	25	-109.162	-200.0	-2430.4	-2431.0	-0.013	10.0 RB	enabled	OK
EN4	-2500.0	-2500.1	-88.856	-88.858	99.067	20.0	-71.754	-107.631	25	25	-109.689	-200.0	-2435.0	-2436.5	-0.052	5.0 RB	enabled	OK
EN5	-2500.0	-2500.0	-89.528	-89.517	99.874	1.5	-88.296	-90.986	25	25	-109.641	-200.0	-2430.3	-2431.1	0.011	10.0 RB	enabled	OK
ES1	0.0	0.2	-0.015	-0.369	-210....	-5.75	0.0060	0.0070	25	25	-109.012	-200.0	0.0	0.8	-0.0020	0.0 Z	disabled	OK
ES2	-2500.0	-2499.8	-89.111	-89.215	99.934	1.57	-87.77	90.57	25	25	-109.177	-200.0	-2430.5	-2430.7	0.029	10.0 RB	enabled	OK
ES3	-2500.0	-2499.8	-89.695	-89.745	99.928	1.4	-88.503	-91.016	25	25	-109.767	-200.0	-2425.2	-2426.2	0.048	15.0 RB	enabled	OK
ES4	-2500.0	-2500.7	-89.522	-89.531	99.893	1.5	-88.274	-90.962	25	25	-109.593	-200.0	-2430.9	-2433.5	0.027	10.0 RB	enabled	OK
ES5	-2500.0	-2500.9	-89.326	-89.301	99.827	1.47	-88.165	-90.796	25	25	-109.449	-200.0	-2430.7	-2431.3	0.0070	10.0 RB	enabled	OK
WN1	-2500.0	-2500.2	-89.623	-89.594	99.94	1.49	-88.341	-91.013	25	25	-109.67	-200.0	-2430.9	-2430.7	-0.265	10.0 RB	enabled	OK
WN2	-2500.0	-2499.8	-89.551	-89.551	99.954	1.49	-88.257	-90.927	25	25	-109.599	-200.0	-2430.7	-2430.8	0.283	10.0 RB	enabled	OK
WN3	-2500.0	-2500.3	-89.615	-89.65	99.805	1.51	-88.434	-91.146	25	25	-109.78	-200.0	-2430.4	-2430.2	-0.296	10.0 RB	enabled	OK
WN4	-2500.0	-2500.3	-89.436	-89.459	99.824	1.5	-88.25	-90.938	25	25	-109.583	-200.0	-2430.5	-2430.1	-0.219	10.0 RB	enabled	OK
WN5	-2500.0	-2500.4	-89.615	-89.651	99.88	1.45	-88.422	-91.024	25	25	-109.709	-200.0	-2425.0	-2425.8	0.049	15.0 RB	enabled	OK
WS1	-2500.0	-2498.9	-89.525	-89.523	100.058	1.61	-88.033	-90.914	25	25	-109.513	-200.0	-2425.9	-2425.1	0.094	15.0 RB	enabled	OK
WS2	-2500.0	-2499.5	-89.713	-89.691	100.039	1.6	-88.243	-91.113	25	25	-109.696	-200.0	-2431.0	-2431.0	0.024	10.0 RB	enabled	OK
WS3	-2500.0	-2501.7	-89.696	-89.716	99.724	1.4	-88.685	-91.203	25	25	-109.883	-200.0	-2430.1	-2429.7	0.051	10.0 RB	enabled	OK
WS4	-2500.0	-2501.9	-89.816	-89.778	99.835	1.4	-88.705	-91.224	25	25	-109.896	-200.0	-2430.3	-2431.0	0.151	10.0 RB	enabled	OK
WS5	-2500.0	-2500.6	-89.535	-89.551	99.868	1.47	-88.335	-90.971	25	25	-109.631	-200.0	-2430.3	-2431.2	-0.0040	10.0 RB	enabled	OK

Figure C.5: The HV Surveillance Panel provides an overview of the current HV parameters and measurements for each channel.