1. Features

- Core
  - 32-bit ARM® Cortex® - M0+
  - Up to 48 MHz operating frequency
- Memories
  - Up to 64 Kbytes flash memory
  - Up to 8 Kbytes SRAM
- Clock management
  - Internal 4/8/16/ 22.12/24 MHz RC oscillator (HSI)
  - Internal 32.768 KHz RC oscillator (LSI)
  - 4 to 32 MHz crystal oscillator (HSE)
  - 32.768KHz low speed crystal oscillator (LSE)
  - PLL (supports 2 frequency multiplication of HSI or HSE)
- Reset and power management
  - Operating voltage: 1.7 to 5.5 V
  - Low power modes: Sleep and Stop
  - Power-on/Power-down reset (POR/PDR)
  - Brown-out reset (BOR)
  - Programmable voltage detection (PVD)
- General-purpose input and output (I/O)
  - Up to 30 I/Os, all available as external interrupts
  - Drive current 8 mA
  - Four GPIOs support super current sink, configurable to 80 mA/60 mA/40 mA/20 mA
- 3-channel DMA controller
- One 12-bit ADC
  - Up to 10 external input channels
  - Input voltage conversion range: 0 to VCC

- Timers
  - A 16-bit advanced control timer (TIM1)
  - Four general-purpose 16-bit timers (TIM3/TIM14/TIM16/TIM17)
  - A low-power timer (LPTIM), supports wake-up from stop mode
  - An independent watchdog timer (IWDT)
  - A window watchdog timer (WWDT)
  - A SysTick timer
  - A IRTIM
- RTC
- Communication interfaces
  - Two serial peripheral interfaces (SPI)
  - Two universal synchronous asynchronous recevicer/transmitter (USART) with automatic baud rate detection
  - A I2C interface, supports standard mode (100 kHz), fast mode (400 kHz), supports 7-bit addressing mode
- Support 4-bit 7-segment common cathode LED digital tube
  - Cycle scan 1-digit, 2-digit, 3-digit, 4-digit number
- Hardware CRC-32 module
- Two comparators
- Unique UID
- Serial wire debug (SWD)
- Working temperature: -40 to 85 ℃
- Package: LQFP32, QFN32, TSSOP20, QFN 20

Content

2. Introduction

PY32F030 series microcontrollers are MCUs with high performance 32-bit ARM® Cortex® -M0 + core, wide voltage operating range. It has embedded up to 64 Kbytes flash and 8 Kbytes SRAM memory, a maximum operating frequency of 48 MHz, and contains various products in different package types. The chip integrates multi-channel I2C, SPI, USART and other communication peripherals, one channel 12-bit ADC, five 16-bit timers, and 2-channel comparators.

PY32F030 series microcontrollers are -40 ℃ to 85 ℃, and the operating voltage range is 1.7 to 5.5 V. The chip provides sleep and stop low-power operating modes from meeting different low-power applications.

The PY32F030 series of microcontrollers are suitable for various application scenarios, such as controllers, portable devices, PC peripherals, gaming and GPS platforms, industrial applications.

Table 2-1 PY32F030 series product features and peripheral counts

Peripherals		PY32F030F					PY32F030K				
		Fx3	Fx4	Fx6	Fx7	Fx8	Kx3	Kx4	Kx6	Kx7	Kx8
Flash (Kbyte)		8	16	32	48	64	8	16	32	48	64
SRAM (Kbyte)		2	2	4	6	8	2	2	4	6	8
Timers	Advanced control	1 (16-bit)									
	General purpose	4 (16-bit)									
	Low power	1									
	SysTick	1									
	Watchdog	2									
Comm. interfaces	SPI	2									
	I2C	1									
	USART	2									
DMA		3ch									
RTC		Yes									
Universal port		18					30/28				
Number of ADC channels (external + internal)		2+2/5+2					10+2/9+2				
Comparators		2									
Max. CPU frequency		48 MHz									
Operating voltage		1.7 to 5.5 V									
Package		TSSOP20/QFN20					LQFP32/QFN32				

Figure 2-1 Block diagram

3. Functional overview

3.1. Arm® Cortex®-M0+ core

The Arm® Cortex®-M0+ is an entry-level 32-bit Arm Cortex processor designed for a wide range of embedded applications. It provides developers with significant benefits, including:

- Simple structure, easy to learn and program

- Ultra-low power consumption, energy-saving operation

- Reduced code density and more

Cortex-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. The processor offers high-end processing hardware, including single-cycle multipliers, through a streamlined but powerful instruction set and an extensively optimized design. Moreover, it delivers the superior performance expected from a 32-bit architecture computer, with a higher coding density than other 8 and 16-bit microcontrollers.

The Cortex-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

3.2. Memories

The on-chip integrated SRAM is accessed by bytes (8 bits), half-word (16bits) or word (32bits).

The on-chip integrated Flash consists of two different physical areas:

- Main flash area, which contains application and user data

- The information area has 4K bytes, and it includes the following parts:
  - ➢ Option bytes
  - ➢ UID bytes
  - ➢ System memory

The protection of Flash main memory includes the following mechanisms:

- Read protection(RDP) prevents access from outside.

- Write protection (WRP) control prevents unwanted writes (confuse by program memory pointer from PC). The minimum protection unit for write protection is 4K bytes.

- Option byte write protection, special unlocking design.

3.3. Boot mode

Through BOOT0 pin and boot configuration bit nBOOT1 (stored in Option bytes), three different boot modes can be selected, as shown in the following table:

Table 3-1Boot configuration

Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
X	0	Select Main flash as the boot area
1	1	Select System memory as the boot area
0	1	Select SRAM as the boot area

The Boot loader program is stored in the System memory and used to download the Flash program through the USART interface.

3.4. Clock system

After the CPU starts, the default system clock frequency is HSI 8 MHz, and the system clock frequency and system clock source can be reconfigured after the program runs. The high frequency clocks that can be selected are:

- A 4/8/16/22.12/24 MHz configurable internal high precision HSI clock.

- A 32.768 KHz configurable internal LSI clock.

- 4 to 32 MHz HSE clock can enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.

- A 32.768 KHz LSE clock.

- PLL clock has HSI and HSE sources. If the HSE source is selected, when CSS is enabled and CSS fails, the PLL and HSE will be turned off, and the hardware selects the system clock source as HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. AHB and APB clock frequencies up to 48 MHz.
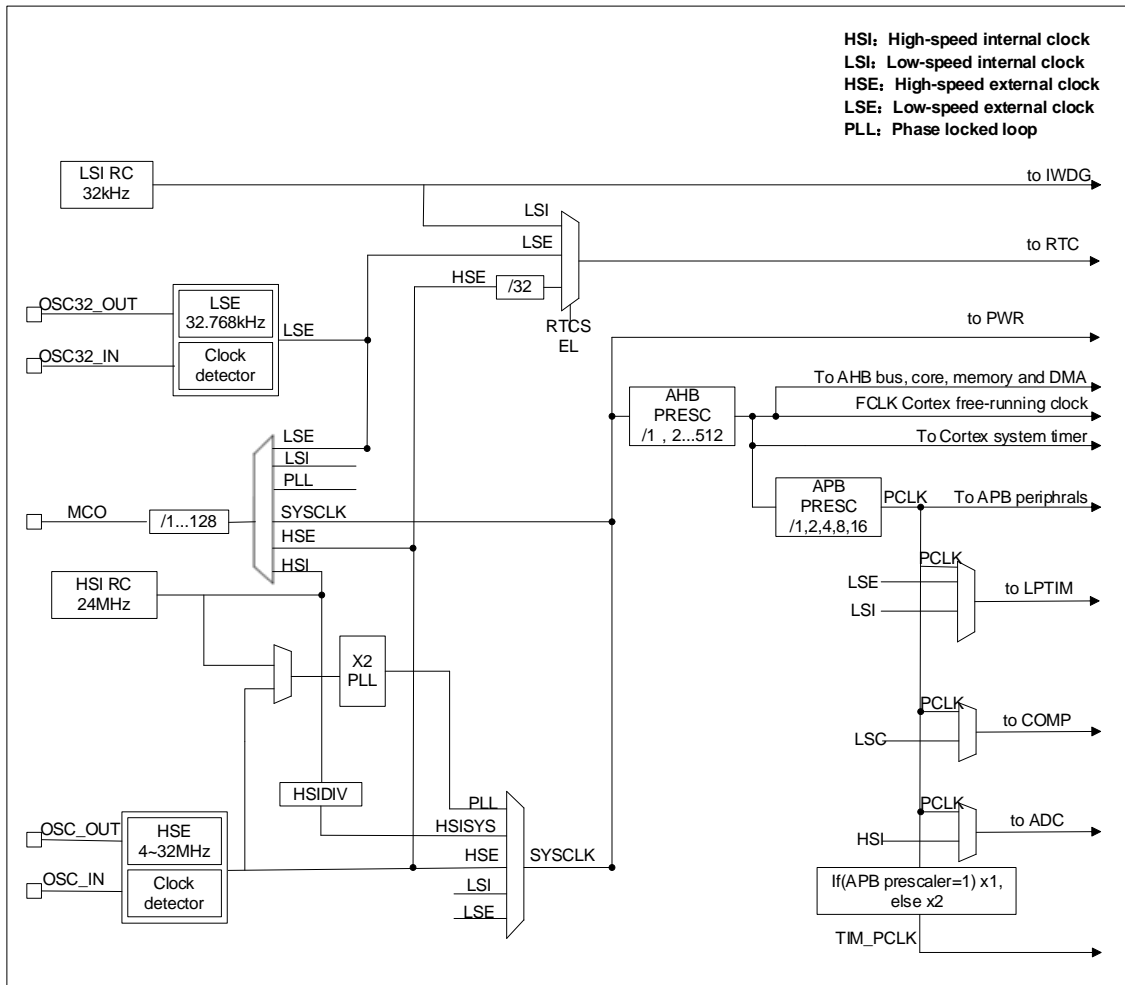
Figure 3-1 System clock structure diagram

3.5. Power management

3.5.1. Power block diagram
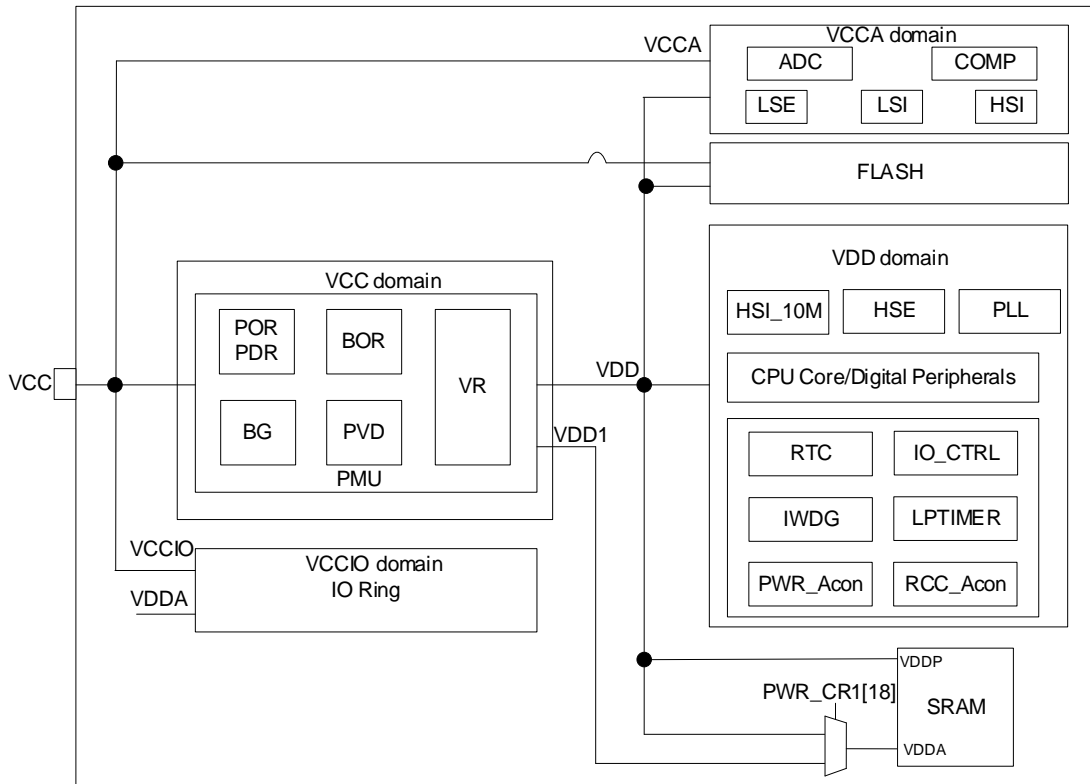
Figure 3-2 Power block diagram

Table 3-2 Power block diagram

Serial number	Power supply	Power value	Describe
1	VCC	1.7 to 5.5V	The chip is supplied with power through the power pins, and its power supply module is part of the analogue circuit.
2	VCCA	1.7 to 5.5V	Power to most analogue modules from VCC PAD (a separate power supply PAD can also be designed).
3	VCCIO	1.7 to 5.5V	Power supply to IO, from VCC PAD
4	VDD	1.2/1.0 V ± 10 %	VR supplies power to the main logic circuits and SRAM inside the chip. When the MR is powered, it outputs 1.2 V. According to the software configuration, entering the stop mode can be powered by MR or LPR, and the LPR output is determined to be 1.2 V or 1.0 V.

3.5.2. Power monitoring

3.5.2.1. Power on reset (POR/PDR)

The Power on reset (POR)/Power down reset (PDR) module is designed to provide power-on and power-off reset for the chip. The module keeps working in all modes.

3.5.2.2. Brown-out reset (BOR)

In addition to POR/ PDR, BOR (brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on, the BOR threshold can be selected by the Option byte, and both the rising and falling detection points can be configured individually.
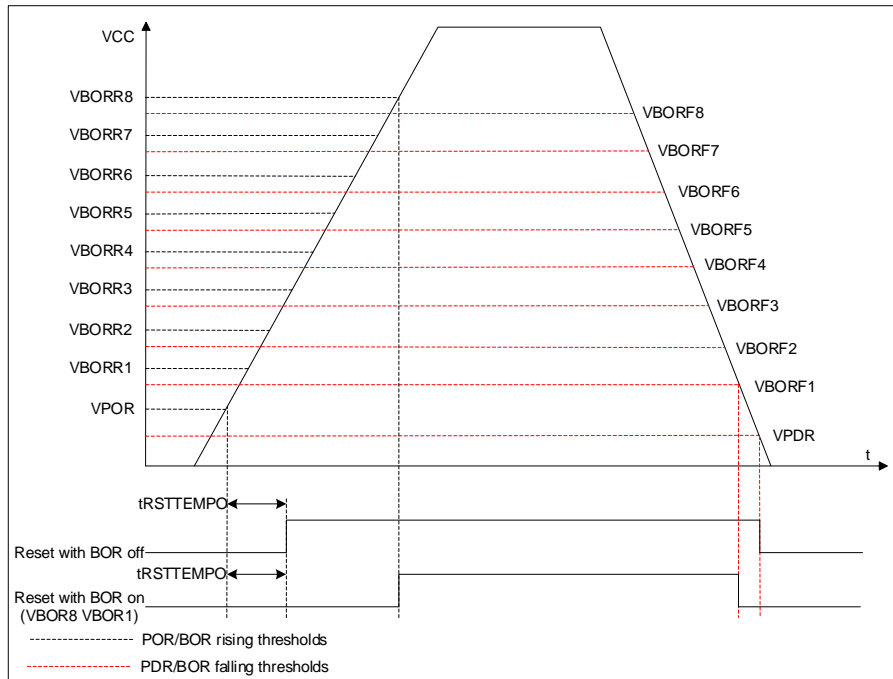
Figure 3-3 POR/PDR/BOR threshold

3.5.2.3. Programmable voltage detection (PVD)

Programmable Voltage Detector (PVD) module can be used to detect the VCC power supply (it can also detect the voltage of the PB7 pin), and the detection point can be configured through the register. When VCC is higher or lower than the detection point of PVD, a corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI , depending on the rising/falling edge configuration of EXTI line 16. When VCC rises above the PVD detection point, or VCC falls below the PVD detection point , an interrupt is generated. In the service program, users can perform urgent shutdown tasks.
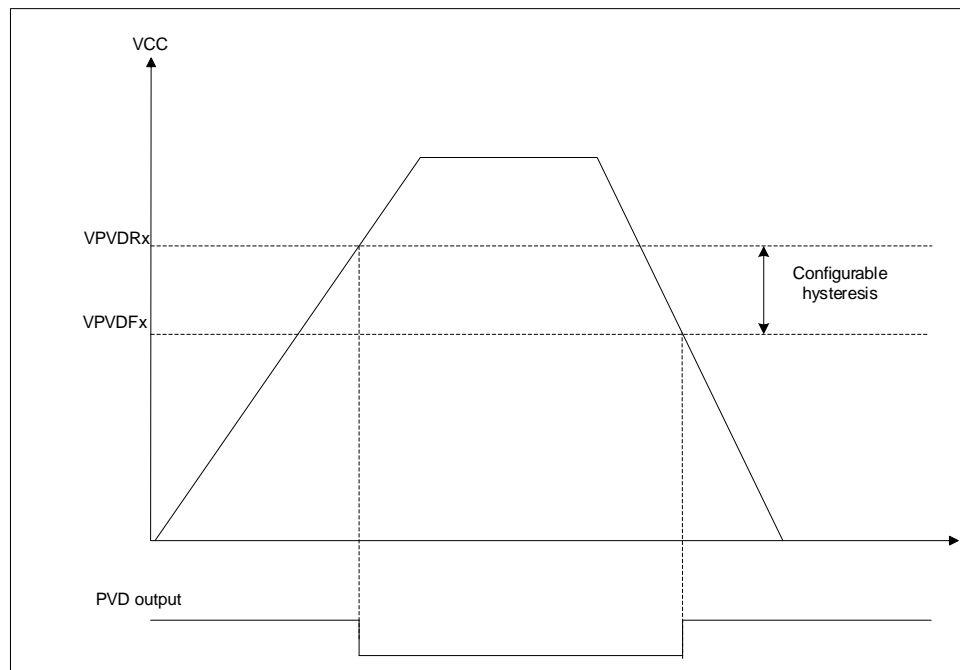
Figure 3-4 PVD threshold

3.5.3. Voltage regulator

The chip designs two voltage regulators:

- Main regulator (MR) keeps working when the chip is in normal operating state.

- Low power regulator (LPR) provides a lower power consumption option in stop mode.

3.5.4. Low power mode

In addition to the normal operating mode, the chip has two low-power modes:

- **Sleep mode**: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.

- **Stop mode**: In this mode, the contents of SRAM and registers are maintained, HSI and HSE are turned off, and most modules of clocks in the VDD domain are stopped. GPIO, PVD, COMP output, RTC and LPTIM can wake up stop mode.

3.6. Reset

Two resets are designed in the chip: power and system reset.

3.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/Power-down reset (POR/PDR)

- Brown-out reset (BOR)

3.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed Watchdog Reset (WWDG)
- Independent Watchdog Reset (IWDG)
- SYSRESETREQ software reset
- Option byte load reset (OBL)
- Power reset (POR/PDR , BOR)

3.7. General-purpose input and output (GPIOs)

The software configures each GPIO as output (push-pull or open-drain), input (floating, pull-up/down, analogue), peripheral multiplexing function, and locking mechanism freeze I/O port configuration function.

3.8. Direct memory access (DMA)

Direct Memory Access (DMA) provides high-speed data transfer between peripherals and memory or between memory and memory.

DMA controller has three channels, and each channel is responsible for managing memory access requests from one or more peripherals. The DMA controller includes an arbiter for handling DMA requests for each DMA request's priority..

DMA supports circular buffer management, eliminating the need for user code to intervene when the controller reaches the end of the buffer.

Each channel is directly connected to a dedicated hardware DMA request, and each channel also supports software triggering. These functions are configured through software.

DMA is available for peripherals: SPI, I2C, USART, all TIMx timers (except TIM14 and LPTIM) and ADC.

3.9. Interrupts and events

The PY32F030 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller and an extended interrupt/event controller.

3.9.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a high-priority interrupt event occurs and a low-priority interrupt event is just waiting to be serviced, the later-arriving high-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a high-priority ISR and then starting a pending low-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling

- Level 4 interrupt priority

- Supports one NMI interrupt

- Supports 32 maskable external interrupts

- Supports 10 Cortex-M0+ exceptions

- High-priority interrupts can interrupt low-priority interrupt responses

- Support tail-chaining optimization

- Hardware interrupt vector retrieval

3.9.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from stop mode.

The EXTI controller has multiple channels, including a maximum of 16 GPIOs, 1 PVD output, 2 COMP outputs, RTC and LPTIM wake-up signals. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 ~ 15 channel through the select signal.

Each EXTI line can be independently masked through registers.

The EXTI controller can capture pulses shorter than the internal clock period.

Registers in the EXTI controller latch each event. Even in stop mode, after the processor wakes up from stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

3.10. Analog to digital converter (ADC)

The chip has a 12-bit SARADC. The module has up to 12 channels to be measured, including 10 external channels and 2 internal channels.

The conversion mode of each channel can be set to single, continuous, sweep, discontinuous mode. Conversion results are stored in left or right-aligned 16-bit data registers.

An analogue watchdog allows the application to detect if the input voltage exceeds a user-defined high or low threshold.

The ADC has been implemented to operate at a low frequency, resulting in lower power consumption.

At the end of sampling, conversion, and continuous conversion, an interrupt request is generated when the conversion voltage exceeds the threshold when simulating the watchdog.

3.11. Timer

The characteristics of different timers of PY32F003 are shown in the following table:

Table 3-3 Timer features

Types	Timer	Couter resolution	Counting type	Prescaler factor	DMA	Capture /compare channels	Comple- mentary outputs
Advanced control	TIM1	16-bit	Up, down, center aligned	Any integer between 1 and 65536	Supported	4	3
General purpose	TIM3	16-bit	Up, down, center aligned	Any integer between 1 and 65536	Supported	4	-
	TIM14	16-bit	Up	Any integer between 1 and 65536	-	1	-
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Supported	1	1

3.11.1. Advanced-control timer (TIM1)

The advanced timer TIM1 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

TIM1 includes 4 independent channels:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If TIM1 is configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

3.11.2. General-purpose timers (TIM3, TIM14, TIM16, TIM17)

3.11.2.1. TIM3

The general-purpose timer TIM3 is based on a 16-bit auto-reload counter and a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM3 general-purpose timer can work with the TIM1 advanced-control timer by the Timer Link feature for synchronization or event chaining.

TIM3 has an independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

The counter can be frozen in debug mode.

3.11.2.2. TIM14

The general-purpose timer TIM14 is based on a 16-bit auto-reload counter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

The counter can be frozen in debug mode.

3.11.2.3. TIM16/TIM17

The general-purpose timer TIM16 and TIM17 is based on a 16-bit auto-reload counter and a 16-bit prescaler.

TIM16/TIM17 have one independent channel for input capture/output compare, PWM or one- pulse mode output.

TIM16/TIM17 have complementary outputs with dead time.

TIM16/TIM17 has an independent DMA request generation.

These counters can be frozen in debug mode.

3.11.3. Low power timer (LPTIM)

LPTIM is a 16 -bit upcounter with a 3-bit prescaler and only support a single count.

LPTIM can be configured as a stop mode wake-up source.

The counter can be frozen in debug mode.

3.11.4. Independent watchdog (IWDG)

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.

IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.

Controlling of option byte can enable IWDG hardware mode.

IWDG is the wake-up source of stop mode, which wakes up stop mode by reset.

The counter can be frozen in debug mode.

3.11.5. System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

3.11.6. SysTick timer

SysTick timer is dedicated to real-time operating systems, but could also be used as a standard downcounter.

SysTick Features:

- A 24-bit down counter

- Auto-reload capability

- Maskable system interrupt generation when the counter reaches 0

3.12. Real-time clock (RTC)

The real-time clock is an independent Timer. RTC has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

RTC is a 32-bit programmable counter with a prescale factor of up to 2^{20} bits.

The RTC counter clock source can be LSI and the stop wake-up source.

RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).

RTC supports clock calibration.

RTC can be frozen in debug mode.

3.13. I2C interface

I2C (inter-integrated circuit) bus interface connects the microcontroller and the serial I2C bus. It provides multi-master capability and controls all I2C bus specific sequences, protocols, arbitration and timing. Standard mode (Sm) and fast mode (Fm) are supported.

I2C Features:

- Slave and master mode

- Multi-host function: can be master or slave

- Support different communication speeds
  - Standard Mode (Sm): Up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz

- As master
  - Generate Clock
  - Generation of Start and Stop

- As slave
  - Programmable I2C address detection

> ➢ Discovery of the Stop bit

- 7-bit addressing mode

- General call

- Status flag

  - ➢ Transmit/receive mode flags

  - ➢ Byte transfer complete flag

  - ➢ I2C busy flag bit

- Error flag

  - ➢ Master a rbitration loss

  - ➢ ACK failure after address/data transfer

  - ➢ Start/Stop error

  - ➢ Overrun/Underrun (clock stretching function disable)

- Optional clock stretching

- Single-byte buffer with DMA capability

- Software reset

- Analogue noise filter function

3.14. Universal synchronous/asynchronous recevicer/ transmitter (USART)

PY32F030 contains 2 USARTs with precisely the same functions.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baudrate generator to provide a wide range of baudrate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baudrate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USARTs features:

- Full-duplex asynchronous communication

- NRZ standard format

- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance

- Programmable baudrate shared by transmit and receive, up to 4.5Mbit/s

- Automatic baudrate detection

- Programmable data length of 8 or 9 bits

- Configurable stop bits (1 or 2 bits)

- Synchronous mode and clock output function for synchronous communication

- Single-wire half-duplex communication

- Independent transmit and receive enable bits

- ■ Hardware flow control
- ■ Receive/transmit bytes by DMA buffer
- ■ Detection flag
  - ➢ Receive full buffer
  - ➢ Send empty buffer
  - ➢ End of transmission
- ■ Parity Control
  - ➢ Send check digit
  - ➢ Check the received data
- ■ Flagged interrupt sources
  - ➢ CTS change
  - ➢ Send empty register
  - ➢ Send completed
  - ➢ Receive full data register
  - ➢ Bus idle detected
  - ➢ Overflow error
  - ➢ Frame error
  - ➢ Noise operation
  - ➢ Error detection
- ■ Multiprocessor communication
  - ➢ If the address does not match, enter silent mode
- ■ Wake-up from silent mode: by idle detection and address flag detection

3.15. Serial peripheral interface (SPI)

PY32F030 contains two SPIs.

SPIs allow the chip to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in master mode and provides the communication clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- ■ Master or slave mode
- ■ 3 -wire full-duplex simultaneous transmission
- ■ 2-wire half-duplex synchronous transmission (with bidirectional data line)
- ■ 2-wire simplex synchronous transmission (no bidirectional data line)
- ■ 8-bit or 16-bit transmission frame selection
- ■ Support multi-master mode
- ■ 8 master mode baudrate prescaler factors (max fPCLK/ 4)
- ■ Slave mode frequency (max fPCLK/4)
- ■ Both master and slave modes can be managed by software or hardware NSS: dynamic change of master/slave operating mode

- Programmable clock polarity and phase

- Programmable data order, MSB first or LSB first

- Dedicated transmit and receive flags that can trigger interrupts

- SPI bus busy status flag

- Motorola mode

- Interrupt-causing master mode faults, overloads

- Two 32-bit Rx and Tx FIFOs with DMA capability

3.16. Serial wire debug (SWD)

The ARM SWD interface allows serial debugging tools to be connected to the PY32F030.

4. Pin configuration
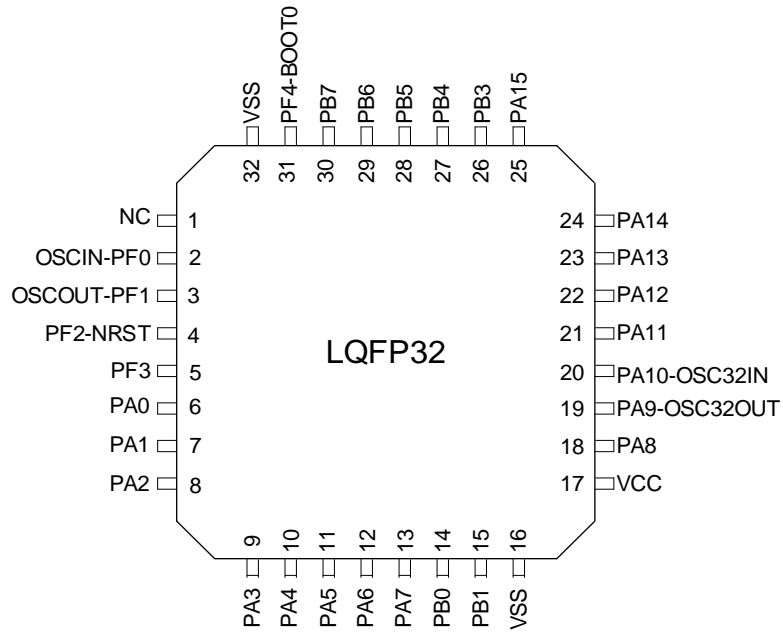
Figure 4-1LQFP32 Pinout1 PY32F030K1xT
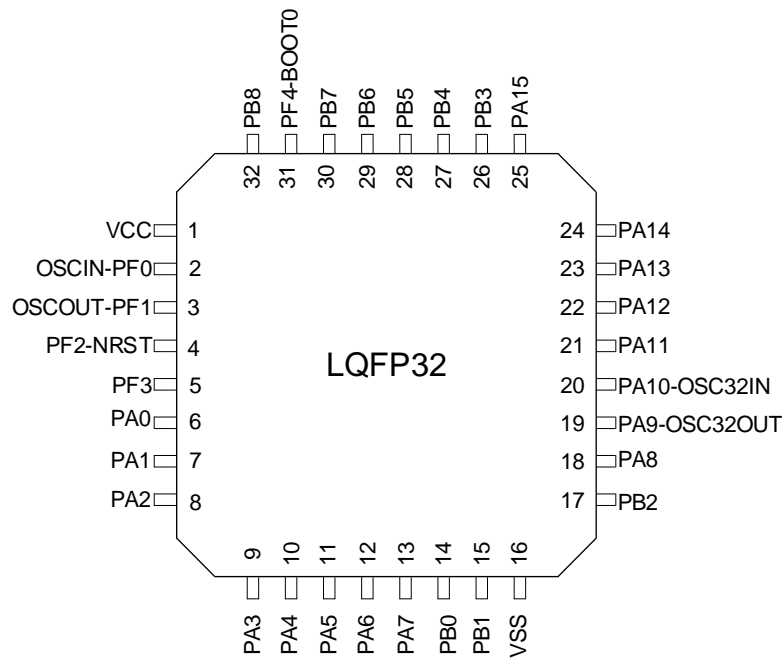
Figure 4-2LQFP32 Pinout2 PY32F030K2xT
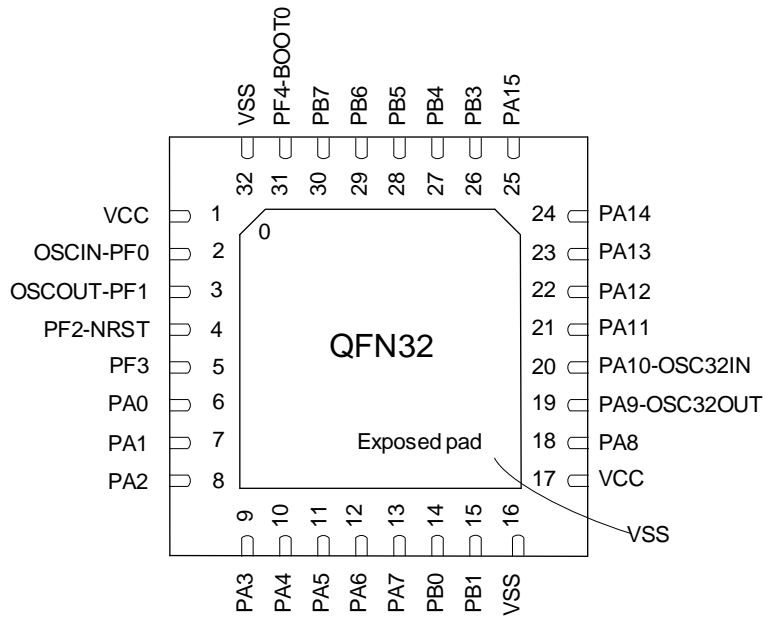
Figure 4-3QFN32 Pinout1 PY32F030K1xU
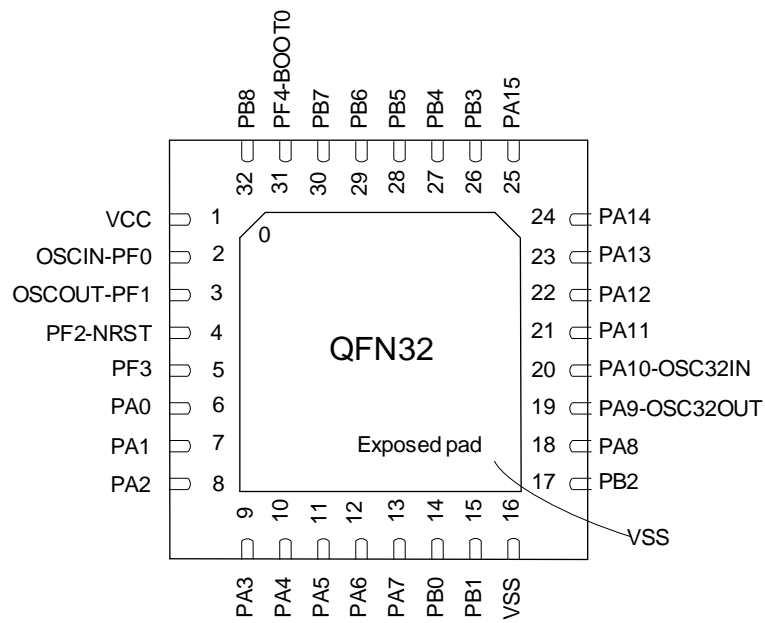
Figure 4-4QFN32 Pinout2 PY32F030K2xU
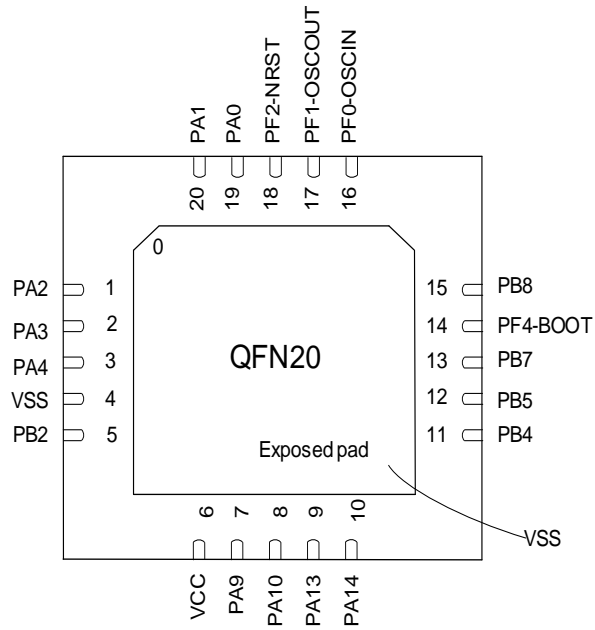
Figure 4-5QFN20 Pinout1 PY32F030F1xU
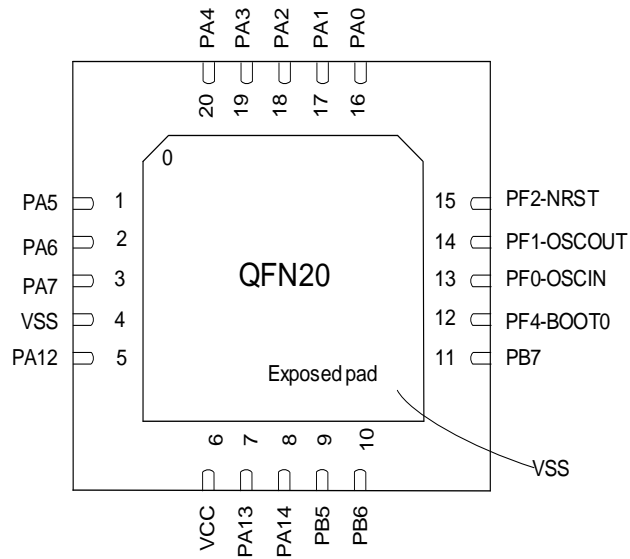
Figure 4-6QFN20 Pinout2 PY32F030F2xU

```
         OSCIN-PF0 ⊏  1        20  ⊐ PF4-BOOT0
        OSCOUT-PF1 ⊏  2        19  ⊐ PB7
          PF2-NRST ⊏  3        18  ⊐ PB6
               PF3 ⊏  4        17  ⊐ PB5
               PA2 ⊏  5  TSSOP20  16  ⊐ PB4
               PA3 ⊏  6        15  ⊐ PA14
               VSS ⊏  7        14  ⊐ PA13
               PB2 ⊏  8        13  ⊐ PA11
               VCC ⊏  9        12  ⊐ PA10-OSC32IN
               PA8 ⊏ 10        11  ⊐ PA9-OSC32OUT
```
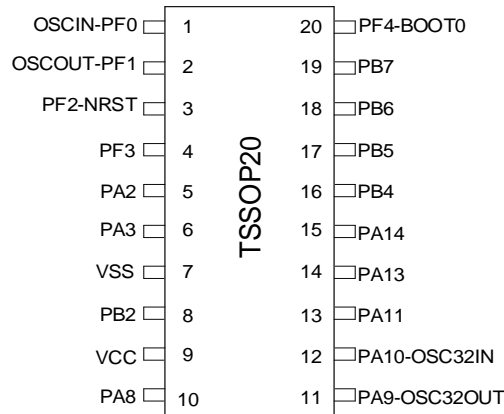
Figure 4-7TSSOP20 Pinout1 PY32F030F1xP

```
               PA2 ⊏  1        20  ⊐ PA1
               PA3 ⊏  2        19  ⊐ PA0
               PA4 ⊏  3        18  ⊐ PF2-NRST
               PA5 ⊏  4  TSSOP20  17  ⊐ PF1-OSCOUT
               PA6 ⊏  5        16  ⊐ PF0-OSCIN
               PA7 ⊏  6        15  ⊐ PF4-BOOT0
               VSS ⊏  7        14  ⊐ PB7
              PA12 ⊏  8        13  ⊐ PB6
               VCC ⊏  9        12  ⊐ PB5
              PA13 ⊏ 10        11  ⊐ PA14
```
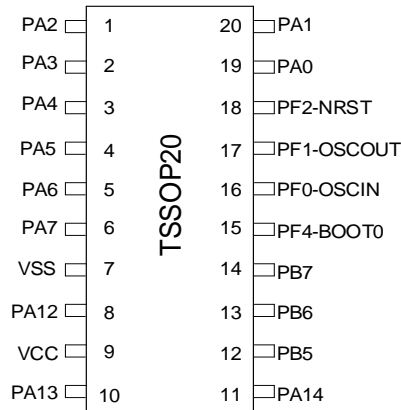
Figure 4-8TSSOP20 Pinout2 PY32F030F2xP

Table 4-1 Pin definition and symbols

Types		Symbol	Definition
Port type		S	Supply pin
		G	Ground pin
		I/O	Input / output pin
		NC	Undefined
Port structure		COM	5V port, support analogue input and output function
		RST	Reset port, with internal weak pull-up resistor, does not support analogue input and output function
		_L	LED COM port, support analogue input and output function
Notes			Unless otherwise specified by a note, all ports are set as floating inputs during and after reset.
Port functions	Alternate functions		Functions selected through GPIOx_AFR registers
	Additional functions		Functions directly selected or enabled through peripheral registers.

Table 4-2LQFP32/QFN32 pin definitions

Package type								Port functions	
LQFP32 K1	LQFP32 K2	QFN32 K1	QFN32 K2	Reset	Port type	Port structure	Notes	Alternate functions	Additional functions
1	-	-	-	NC	NC				
-	1	1	1	VCC	S			Digital power supply	
2	2	2	2	PF0-OSC_IN-(PF0)	I/O	COM		SPI2_SCK USART2_RX TIM14_CH1 USART1_RX USART2_TX I2C_SDA	OSC_IN
3	3	3	3	PF1-OSC_OUT-(PF1)	I/O	COM		SPI2_MISO USART2_TX USART1_TX USART2_RX I2C_SCL SP1_NSS TIM14_CH	OSC_OUT
4	4	4	4	PF2-NRST	I/O	RST	(1)	MCO SPI2_MOSI USART2_RX	NRST
5	5	5	5	PF3	I/O	COM		USART1_TX USART2_TX SPI2_MISO SPI1_NSS TIM3_CH3 RTC_OUT	COMP2_INP
6	6	6	6	PA0	I/O	COM		SPI2_SCK USART1_CTS LED_DATA_B USART2_CTS COMP1_OUT TIM1_CH3 TIM1_CH1N SPI1_MISO USART2_TX IR_OUT	ADC_IN0 COMP1_INM
7	7	7	7	PA1	I/O	COM		SPI1_SCK USART1_RTS USART2_RTS LED_DATA_C EVENTOUT	COMP1_INP ADC_IN1

								SPI1_MOSI	
								USART2_RX	
								TIM1_CH4	
								TIM1_CH2N	
								MCO	
8	8	8	8	PA2	I/O	COM		SPI1_MOSI	COMP2_INM ADC_IN2
								USART1_TX	
								USART2_TX	
								LED_DATA_D	
								LPUART_TX	
								COMP2_OUT	
								SPI1_SCK	
								TIM3_CH1	
								I2C_SDA	
9	9	9	9	PA3	I/O	COM		SPI2_MISO	COMP2_INP ADC_IN3
								USART1_RX	
								USART2_RX	
								LED_DATA_E	
								EVENTOUT	
								SPI1_MOSI	
								TIM1_CH1	
								I2C_SCL	
10	10	10	10	PA4	I/O	COM		SPI1_NSS	ADC_IN4
								USART1_CK	
								SPI2_MOSI	
								LED_DATA_F	
								TIM14_CH1	
								USART2_CK	
								ENENTOUT	
								RTC_OUT	
								TIM3_CH3	
								USART2_TX	
11	11	11	11	PA5	I/O	COM		SPI1_SCK	ADC_IN5
								LED_DATA_G	
								LPTIM_ETR	
								EVENTOUT	
								TIM3_CH2	
								USART2_RX	
								MCO	
12	12	12	12	PA6	I/O	COM		SPI1_MISO	ADC_IN6
								TIM3_CH1	
								TIM1_BKIN	
								LED_DATA_DP	
								TIM16_CH1	
								EVENTOUT	

								LPUART_CTS	
								COMP1_OUT	
								USART1_CK	
								RTC_OUT	
13	13	13	13	PA7	I/O	COM		SPI1_MOSI	ADC_IN7
								TIM3_CH2	
								TIM1_CH1N	
								TIM14_CH1	
								TIM17_CH1	
								EVENTOUT	
								COMP2_OUT	
								USART1_TX	
								USART2_TX	
								I2C_SDA	
								SPI1_MISO	
14	14	14	14	PB0	I/O	COM		SPI1_NSS	ADC_IN8
								TIM3_CH3	
								TIM1_CH2N	
								EVENTOUT	
								COMP1_OUT	
15	15	15	15	PB1	I/O	COM		TIM14_CH1	COMP1_INM ADC_IN9
								TIM3_CH4	
								TIM1_CH3N	
								LPUART_RTS	
								EVENTOUT	
16	16	16	16	VSS	S			Ground	
-	17	-	17	PB2	I/O	COM		USART1_RX	COMP1_INP
								USART2_RX	
								SPI2_SCK	
17	-	17	-	VCC	S			Digital power supply	
18	18	18	18	PA8	I/O	COM		SPI2_NSS	-
								USART1_CK	
								TIM1_CH1	
								USART2_CK	
								MCO	
								EVENTOUT	
								USART1_RX	
								USART2_RX	
								SPI1_MOSI	
								I2C_SCL	
19	19	19	19	PA9	I/O	COM		SPI2_MISO	OSC32OUT
								USART1_TX	
								TIM1_CH2	
								MCO	
								I2C_SCL	

								EVENTOUT	
								I2C_SDA	
								TIM1_BK	
								SPI1_SCK	
								USART1_RX	
20	20	20	20	PA10	I/O	COM		SPI2_MOSI	OS32IN
								USART1_RX	
								TIM1_CH3	
								TIM17_BKIN	
								USART2_RX	
								I2C_SDA	
								EVENTOUT	
								I2C_SCL	
								SPI1_NSS	
								USART1_TX	
								IR_OUT	
21	21	21	21	PA11	I/O	COM		SPI1_MISO	-
								USART1_CTS	
								TIM1_CH4	
								TIM1_CH4	
								EVENTOUT	
								USART2_CTS	
								I2C_SCL	
								COMP1_OUT	
22	22	22	22	PA12	I/O	COM		SPI1_MOSI	-
								USART1_RTS	
								TIM1_ETR	
								USART2_RTS	
								EVENTOUT	
								I2C_SDA	
								COMP2_OUT	
23	23	23	23	PA13(SWDIO)	I/O	COM	(2)	SWDIO	-
								IR_OUT	
								EVENTOUT	
								SPI1_MISO	
								TIM1_CH2	
								USART1_RX	
								MCO	
24	24	24	24	PA14(SWCLK)	I/O	COM	(2)	SWCLK	-
								USART1_TX	
								USART2_TX	
								EVENTOUT	
								MCO	
25	25	25	25	PA15	I/O	COM_L		SPI1_NSS	-
								USART1_RX	

								USART2_RX	
								LED_COM0	
								EVENTOUT	
26	26	26	26	PB3	I/O	COM_L		SPI1_SCK	COMP2_INM
								TIM1_CH2	
								USART1_RTS	
								USART2_RTS	
								LED_COM1	
								EVENTOUT	
27	27	27	27	PB4	I/O	COM_L		SPI1_MISO	COMP2_INP
								TIM3_CH1	
								USART2_CTS	
								USART1_CTS	
								TIM17_BKIN	
								LED_COM2	
								EVENTOUT	
28	28	28	28	PB5	I/O	COM_L		SPI1_MOSI	-
								TIM3_CH2	
								TIM16_BKIN	
								USART2_CK	
								USART1_CK	
								LPTIM_IN1	
								LED_COM3	
								COMP1_OUT	
29	29	29	29	PB6	I/O	COM		USART1_TX	COMP2_INP
								TIM1_CH3	
								TIM16_CH1N	
								USART2_TX	
								SPI2_MISO	
								I2C_SCL	
								LPTIM_ETR	
								EVENTOUT	
30	30	30	30	PB7	I/O	COM		USART1_RX	COMP2_INM PVD_IN
								SPI2_MOSI	
								TIM17_CH1N	
								USART2_RX	
								I2C_SDA	
								EVENTOUT	
31	31	31	31	PF4-BOOT0	I/O	COM	(3)	-	BOOT0
-	32	-	32	PB8	I/O	COM		SPI2_SCK	COMP1_INP
								TIM16_CH1	
								I2C1_SCL	
								USART2_TX	
								EVENTOUT	
								LED_DATA_A	

							USART1_TX	
							SPI2_NSS	
							I2C_SDA	
							TIM17_CH1	
							IR_OUT	
32	-	32	-	VSS	S		Ground	

Table 4-3QFN20/TSSOP20 pin definitions

Package type				Reset	Port type	Port structure	Notes	Port functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2					Altenate functions	Additional functions
-	-	-		NC	NC				
-	-	-		VCC	S			Digital power supply	
16	13	1	16	PF0-OSC_IN-(PF0)	I/O	COM		SPI2_SCK	OSC_IN
								USART2_RX	
								TIM14_CH1	
								USART1_RX	
								USART2_TX	
								I2C_SDA	
17	14	2	17	PF1-OSC_OUT-(PF1)	I/O	COM		SPI2_MISO	OSC_OUT
								USART2_TX	
								USART1_TX	
								USART2_RX	
								I2C_SCL	
								SP1_NSS	
								TIM14_CH	
18	15	3	18	PF2-NRST	I/O	RST	(1)	MCO	NRST
								SPI2_MOSI	
								USART2_RX	
-	-	4	-	PF3	I/O	COM		USART1_TX	COMP2_INP
								USART2_TX	
								SPI2_MISO	
								SPI1_NSS	
								TIM3_CH3	
								RTC_OUT	
19	16	-	19	PA0	I/O	COM		SPI2_SCK	ADC_IN0 COMP1_INM
								USART1_CTS	
								LED_DATA_B	
								USART2_CTS	
								COMP1_OUT	
								TIM1_CH3	
								TIM1_CH1N	

								SPI1_MISO	
								USART2_TX	
								IR_OUT	
20	17	-	20	PA1	I/O	COM		SPI1_SCK	COMP1_INP ADC_IN1
								USART1_RTS	
								USART2_RTS	
								LED_DATA_C	
								EVENTOUT	
								SPI1_MOSI	
								USART2_RX	
								TIM1_CH4	
								TIM1_CH2N	
								MCO	
1	18	5	1	PA2	I/O	COM		SPI1_MOSI	COMP2_INM ADC_IN2
								USART1_TX	
								USART2_TX	
								LED_DATA_D	
								LPUART_TX	
								COMP2_OUT	
								SPI1_SCK	
								TIM3_CH1	
								I2C_SDA	
2	19	6	2	PA3	I/O	COM		SPI2_MISO	COMP2_INP ADC_IN3
								USART1_RX	
								USART2_RX	
								LED_DATA_E	
								EVENTOUT	
								SPI1_MOSI	
								TIM1_CH1	
								I2C_SCL	
3	20	-	3	PA4	I/O	COM		SPI1_NSS	ADC_IN4
								USART1_CK	
								SPI2_MOSI	
								LED_DATA_F	
								TIM14_CH1	
								USART2_CK	
								ENENTOUT	
								RTC_OUT	
								TIM3_CH3	
								USART2_TX	
-	1	-	4	PA5	I/O	COM		SPI1_SCK	ADC_IN5
								LED_DATA_G	
								LPTIM_ETR	
								EVENTOUT	
								TIM3_CH2	

								USART2_RX	
								MCO	
-	2	-	5	PA6	I/O	COM		SPI1_MISO	ADC_IN6
								TIM3_CH1	
								TIM1_BKIN	
								LED_DATA_DP	
								TIM16_CH1	
								EVENTOUT	
								LPUART_CTS	
								COMP1_OUT	
								USART1_CK	
								RTC_OUT	
-	3	-	6	PA7	I/O	COM		SPI1_MOSI	ADC_IN7
								TIM3_CH2	
								TIM1_CH1N	
								TIM14_CH1	
								TIM17_CH1	
								EVENTOUT	
								COMP2_OUT	
								USART1_TX	
								USART2_TX	
								I2C_SDA	
								SPI1_MISO	
-	-	-	-	PB0	I/O	COM		SPI1_NSS	ADC_IN8
								TIM3_CH3	
								TIM1_CH2N	
								EVENTOUT	
								COMP1_OUT	
-	-	-	-	PB1	I/O	COM		TIM14_CH1	COMP1_INM ADC_IN9
								TIM3_CH4	
								TIM1_CH3N	
								LPUART_RTS	
								EVENTOUT	
4	4	7	7	VSS	S			Ground	
5	-	8	-	PB2	I/O	COM		USART1_RX	COMP1_INP
								USART2_RX	
								SPI2_SCK	
6	6	9	9	VCC	S			Digital power supply	
-	-	10	-	PA8	I/O	COM		SPI2_NSS	-
								USART1_CK	
								TIM1_CH1	
								USART2_CK	
								MCO	
								EVENTOUT	
								USART1_RX	

								USART2_RX	
								SPI1_MOSI	
								I2C_SCL	
7	-	11	-	PA9	I/O	COM		SPI2_MISO	OSC32OUT
								USART1_TX	
								TIM1_CH2	
								MCO	
								I2C_SCL	
								EVENTOUT	
								I2C_SDA	
								TIM1_BK	
								SPI1_SCK	
								USART1_RX	
8	-	12	-	PA10	I/O	COM		SPI2_MOSI	OS32IN
								USART1_RX	
								TIM1_CH3	
								TIM17_BKIN	
								USART2_RX	
								I2C_SDA	
								EVENTOUT	
								I2C_SCL	
								SPI1_NSS	
								USART1_TX	
								IR_OUT	
-	-	13	-	PA11	I/O	COM		SPI1_MISO	-
								USART1_CTS	
								TIM1_CH4	
								TIM1_CH4	
								EVENTOUT	
								USART2_CTS	
								I2C_SCL	
								COMP1_OUT	
-	5	-	8	PA12	I/O	COM		SPI1_MOSI	-
								USART1_RTS	
								TIM1_ETR	
								USART2_RTS	
								EVENTOUT	
								I2C_SDA	
								COMP2_OUT	
9	7	14	10	PA13(SWDIO)	I/O	COM	(2)	SWDIO	-
								IR_OUT	
								EVENTOUT	
								SPI1_MISO	
								TIM1_CH2	
								USART1_RX	

								MCO	
10	8	15	11	PA14(SWCLK)	I/O	COM	(2)	SWCLK	-
								USART1_TX	
								USART2_TX	
								EVENTOUT	
								MCO	
-	-	-	-	PA15	I/O	COM_L		SPI1_NSS	-
								USART1_RX	
								USART2_RX	
								LED_COM0	
								EVENTOUT	
-	-	-	-	PB3	I/O	COM_L		SPI1_SCK	COMP2_INM
								TIM1_CH2	
								USART1_RTS	
								USART2_RTS	
								LED_COM1	
								EVENTOUT	
11	-	16	-	PB4	I/O	COM_L		SPI1_MISO	COMP2_INP
								TIM3_CH1	
								USART2_CTS	
								USART1_CTS	
								TIM17_BKIN	
								LED_COM2	
								EVENTOUT	
12	9	17	12	PB5	I/O	COM_L		SPI1_MOSI	-
								TIM3_CH2	
								TIM16_BKIN	
								USART2_CK	
								USART1_CK	
								LPTIM_IN1	
								LED_COM3	
								COMP1_OUT	
-	10	18	13	PB6	I/O	COM		USART1_TX	COMP2_INP
								TIM1_CH3	
								TIM16_CH1N	
								USART2_TX	
								SPI2_MISO	
								I2C_SCL	
								LPTIM_ETR	
								EVENTOUT	
13	11	19	14	PB7	I/O	COM		USART1_RX	COMP2_INM PVD_IN
								SPI2_MOSI	
								TIM17_CH1N	
								USART2_RX	
								I2C_SDA	

								EVENTOUT	
14	12	20	15	PF4-BOOT0	I/O	COM	(3)	-	BOOT0
15	-	-	-	PB8	I/O	COM		SPI2_SCK TIM16_CH1 I2C1_SCL USART2_TX EVENTOUT LED_DATA_A USART1_TX SPI2_NSS I2C_SDA TIM17_CH1 IR_OUT	COMP1_INP
-	-	-	-	VSS	S			Ground	

Note :

(1) Selecting PF2 or NRST is configured through option bytes .

(2) After reset, the two pins of PA13 and PA14 are configured as SWDIO and SWCLK AF function, the former internal pull-up resistor, the latter internal pull-down resistor is activated.

(3) PF4-BOOT0 is the default digital input mode, and the pull-down is enabled.

4.1.   Port A alternate functions mapping

Table 4-4 Port A alternate functions mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK	USART1_CTS	-	LED_DATA_B	USART2_CTS	-	-	COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_TX	SPI1_MISO	-	-	TIM1_CH3	TIM1_CH1N	IR_OUT
PA1	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	USART1_RTS	-	LED_DATA_C	USART2_RTS	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_RX	SPI1_MOSI	-	-	TIM1_CH4	TIM1_CH2N	MCO
PA2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	USART1_TX	-	LED_DATA_D	USART2_TX	-	-	COMP2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_SCK	-	I2C_SDA	TIM3_CH1	-	-
PA3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_MISO	USART1_RX	-	LED_DATA_E	USART2_RX	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_MOSI	-	I2C_SCL	TIM1_CH1	-	-
PA4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_NSS	USART1_CK	SPI2_MOSI	LED_DATA_F	TIM14_CH1	USART2_CK	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_TX	-	-	-	TIM3_CH3	-	RTC_OUT
PA5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	-	-	LED_DATA_G	-	LPTIM1_ETR	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_RX	-	-	-	TIM3_CH2	-	MCO
PA6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	TIM3_CH1	TIM1_BKIN	LED_DATA_DP	-	TIM16_CH1	-	COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_CK	-	-	-	-	-	-	RTC_OUT

PA7

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
USART1_TX	USART2_TX	SPI1_MISO	-	I2C_SDA	-	-	-

PA8

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SPI2_NSS	USART1_CK	TIM1_CH1	-	USART2_CK	MCO	-	EVENTOUT
AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
USART1_RX	USART2_RX	SPI1_MOSI	-	I2C_SCL	-	-	-

PA9

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SPI2_MISO	USART1_TX	TIM1_CH2	-	USART2_TX	MCO	I2C_SCL	EVENTOUT
AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
USART1_RX	-	SPI1_SCK	-	I2C_SDA	TIM1_BKIN	-	-

PA10

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SPI2_MOSI	USART1_RX	TIM1_CH3	-	USART2_RX	TIM17_BKIN	I2C_SDA	EVENTOUT
AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
USART1_TX	-	SPI1_NSS	-	I2C_SCL	-	-	-

PA11

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SPI1_MISO	USART1_CTS	TIM1_CH4	-	USART2_CTS	EVENTOUT	I2C_SCL	COMP1_OUT

PA12

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SPI1_MOSI	USART1_RTS	TIM1_ETR	-	USART2_RTS	EVENTOUT	I2C_SDA	COMP2_OUT

PA13

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT
AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
USART1_RX	-	SPI1_MISO	-	-	TIM1_CH2	-	MCO

PA14

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SWCLK	USART1_TX	-	-	USART2_TX	-	-	EVENTOUT
AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
-	-	-	-	-	-	-	MCO

PA15

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
SPI1_NSS	USART1_RX	-	-	USART2_RX	-	LED_COM0	EVENTOUT

4.2. Port B alternate functions mapping

Table 4-5 Port B alternate functions mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS	TIM3_CH3	TIM1_CH2N	-	-	EVENTOUT	-	COMP1_OUT
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	EVENTOUT
PB2	USART1_RX	SPI2_SCK	-	USART2_RX	-	-	-	-
PB3	SPI1_SCK	TIM1_CH2	-	USART1_RTS	USART2_RTS	-	LED_COM1	EVENTOUT
PB4	SPI1_MISO	TIM3_CH1	-	USART1_CTS	USART2_CTS	TIM17_BKIN	LED_COM2	EVENTOUT
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	USART1_CK	USART2_CK	LPTIM_IN1	LED_COM3	COMP1_OUT
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	SPI2_MISO	USART2_TX	LPTIM_ETR	I2C_SCL	EVENTOUT
PB7	USART1_RX	SPI2_MOSI	TIM17_CH1N	-	USART2_RX	-	I2C_SDA	EVENTOUT

PB8

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
-	SPI2_SCK	TIM16_CH1	LED_DATA_A	USART2_TX	-	I2C_SCL	EVENTOUT
AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
USART1_TX	-	-	SPI2_NSS	I2C_SDA	TIM17_CH1	-	IR_OUT

4.3. Port F alternate functions mapping

Table 4-6 Port F alternate functions mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0-OSC_IN	-	-	TIM14_CH1	SPI2_SCK	USART2_RX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	USART2_TX	-	-	I2C_SDA	-	-	-
PF1_OSC_OUT	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	SPI2_MISO	USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	USART2_RX	SPI1_NSS	-	I2C_SCL	TIM14_CH1	-	-
PF2-NRST	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	SPI2_MOSI	USART2_RX	-	MCO	-
PF3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_TX	-	-	SPI2_MISO	USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_NSS	-	-	TIM3_CH3	-	RTC_OUT
PF4-BOOT0	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	-	-	-	-	-

5. Memory mapping
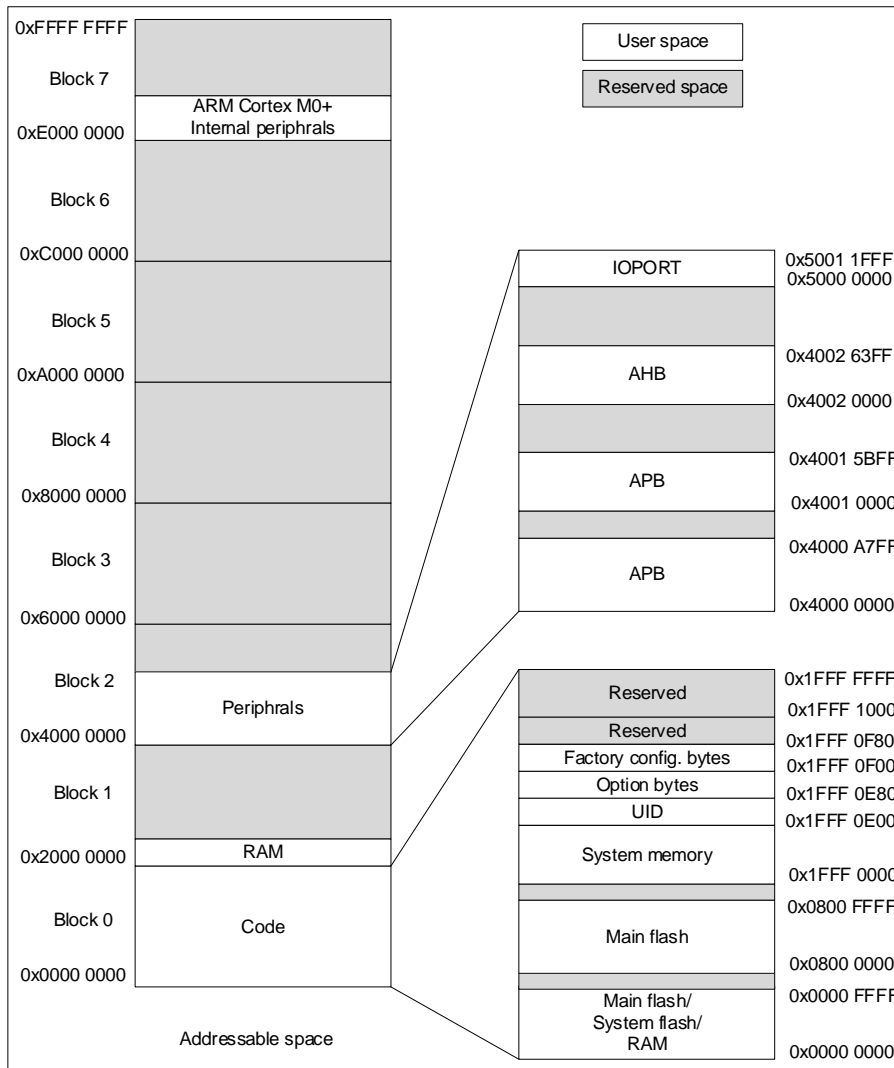
Figure 5-1 Memory map

Table 5-1 Memory address

Type	Boundary Address	Size	Memory area	Description
SRAM	0x2000 2000 - 0x3FFF FFFF	512 MBytes	Reserved	
	0x2000 0000 - 0x2000 1FFF	8 KBytes	SRAM	Depending on the hardware, the SRAM is up to 8 KBytes
Code	0x1FFF 1000 - 0x1FFF FFFF	4 KBytes	Reserved	
	0x1FFF 0F80 - 0x1FFF 0FFF	128 Bytes	Reserved	
	0x1FFF 0F00 - 0x1FFF 0F7F	128 Bytes	Factory config	Store HSI triming data, flash erasing time configuration parameters
	0x1FFF 0E80 - 0x1FFF 0EFF	128 Bytes	Option bytes	Option bytes
	0x1FFF 0E00 - 0x1FFF 0E7F	128 Bytes	UID	Unique ID
	0x1FFF 0000 - 0x1FFF 0DFF	3.5 KBytes	System memory	Store the boot loader

	0x0801 0000 - 0x1FFF FFFF	384 MBytes	Reserved	
	0x0800 0000 - 0x0800 FFFF	64 KBytes	Main flash memory	
	0x0001 0000 - 0x07FF FFFF	8 MBytes	Reserved	
	0x0000 0000 - 0x0000 FFFF	64 KBytes	According to the Boot configuration: 1) Main flash memory 2) System memory 3) SRAM	

Note:

Except for 0 x1FFF 0E00 - 0x1FFF 0E7F, the above spaces are marked as reserved spaces, which cannot be written and read as 0 with response error.

Table 5-2 Peripheral register address

Bus	Boundary Address	Size	Peripheral
	0xE000 0000 - 0xE00F FFFF	1 MBytes	M0+
IOPORT	0x5000 1800 - 0x5FFF FFFF	256 MBytes	Reserved[1]
	0x5000 1400 - 0x5000 17FF	1 KBytes	GPIOF
	0x5000 1000 - 0x5000 13FF	1 KBytes	Reserved
	0x5000 0C00 - 0x5000 0FFF	1 KBytes	Reserved
	0x5000 0800 - 0x5000 0BFF	1 KBytes	Reserved
	0x5000 0400 - 0x5000 07FF	1 KBytes	GPIOB
	0x5000 0000 - 0x5000 03FF	1 KBytes	GPIOA
AHB	0x4002 3400 - 0x4FFF FFFF		Reserved
	0x4002 300C - 0x4002 33FF	1 KBytes	Reserved
	0x4002 3000 - 0x4002 3008		CRC
	0x4002 2400 - 0x4002 2FFF		Reserved
	0x4002 2124 - 0x4002 23FF	1 KBytes	Reserved
	0x4002 2000 - 0x4002 2120		Flash
	0x4002 1C00 - 0x4002 1FFF	3 KBytes	Reserved
	0x4002 1888 - 0x4002 1BFF	1 KBytes	Reserved
	0x4002 1800 - 0x4002 1884		EXTI[2]
	0x4002 1400 - 0x4002 17FF	1 KBytes	Reserved
	0x4002 1064 - 0x4002 13FF	1 KBytes	Reserved
	0x4002 1000 - 0x4002 1060		RCC[2]
	0x4002 0C00 - 0x4002 0FFF	1 KBytes	Reserved
	0x4002 0040 - 0x4002 03FF	1 KBytes	Reserved
	0x4002 0000 - 0x4002 003C		DMA
APB	0x4001 5C00 - 0x4001 FFFF	32 KBytes	Reserved
	0x4001 5880 - 0x4001 5BFF	1 KBytes	Reserved
	0x4001 5800 - 0x4001 587F		DBG
	0x4001 4C00 - 0x4001 57FF	3 KBytes	Reserved
	0x4001 4850 - 0x4001 4BFF	1 KBytes	Reserved
	0x4001 4800 - 0x4001 484C		TIM17
	0x4001 4450 - 0x4001 47FF	1 KBytes	Reserved
	0x4001 4400 - 0x4001 404C		TIM16
	0x4001 3C00 - 0x4001 43FF	2 KBytes	Reserved
	0x4001 381C - 0x4001 3BFF	1 KBytes	Reserved

Address	Size	Peripheral
0x4001 3800 - 0x4001 3018		USART1
0x4001 3400 - 0x4001 37FF	1 KBytes	Reserved
0x4001 3010 - 0x4001 33FF	1 KBytes	Reserved
0x4001 3000 - 0x4001 300C		SPI1
0x4001 2C50 - 0x4001 2FFF	1 KBytes	Reserved
0x4001 2C00 - 0x4001 2C4C		TIM1
0x4001 2800 - 0x4001 2BFF	1 KBytes	Reserved
0x4001 270C - 0x4001 27FF	1 KBytes	Reserved
0x4001 2400 - 0x4001 2708		ADC
0x4001 0400 - 0x4001 23FF	8 KBytes	Reserved
0x4001 0220 - 0x4001 03FF		Reserved
0x4001 0200 - 0x4001 021F	1 KBytes	COMP1 and COMP2
0x4001 0000 - 0x4001 01FF		SYSCFG
0x4000 B400 - 0x4000 FFFF	19 KBytes	Reserved
0x4000 B000 - 0x4000 B3FF	1 KBytes	Reserved
0x4000 8400 - 0x4000 AFFF	11 KBytes	Reserved
0x4000 8000 - 0x4000 83FF	1 KBytes	Reserved
0x4000 7C28 - 0x4000 7FFF	1 KBytes	Reserved
0x4000 7C00 - 0x4000 7C24		LPTIM
0x4000 7400 - 0x4000 7BFF	2 KBytes	Reserved
0x4000 7018 - 0x4000 73FF	1 KBytes	Reserved
0x4000 7000 - 0x4000 7014		PWR[3]
0x4000 5800 - 0x4000 6FFF	6 KBytes	Reserved
0x4000 5434 - 0x4000 57FF	1 KBytes	Reserved
0x4000 5400 - 0x4000 5430		I2C
0x4000 4800 - 0x4000 53FF	3 KBytes	Reserved
0x4000 441C - 0x4000 47FF	1 KBytes	Reserved
0x4000 4400 - 0x4000 4418		USART2
0x4000 3C00 - 0x4000 43FF	1 KBytes	Reserved
0x4000 3810 - 0x4000 3BFF	1 KBytes	Reserved
0x4000 3800 - 0x4000 380C		SPI2
0x4000 3400 - 0x4000 37FF	1 KBytes	Reserved
0x4000 3014 - 0x4000 33FF	1 KBytes	Reserved
0x4000 3000 - 0x4000 0010		IWDG
0x4000 2C0C - 0x4000 2FFF	1 KBytes	Reserved
0x4000 2C00 - 0x4000 2C08		WWDG
0x4000 2830 - 0x4000 2BFF	1 KBytes	Reserved
0x4000 2800 - 0x4000 282C		RTC[3]
0x4000 2420 - 0x4000 27FF	1 KBytes	Reserved
0x4000 2400 - 0x4000 241C		LED
0x4000 2054 - 0x4000 23FF	1 KBytes	Reserved
0x4000 2000 - 0x4000 0050		TIM14
0x4000 1800 - 0x4000 1FFF	2 KBytes	Reserved
0x4000 1400 - 0x4000 17FF	1 KBytes	Reserved
0x4000 1030 - 0x4000 13FF	1 KBytes	Reserved
0x4000 1000 - 0x4000 102C		Reserved
0x4000 0800 - 0x4000 0FFF	2 KBytes	Reserved
0x4000 0450 - 0x4000 07FF	1 KBytes	Reserved
0x4000 0400 - 0x4000 044C		TIM3

	0x4000 0000 - 0x4000 03FF	1 KBytes	Reserved

Note:

（1） The address space marked as Reserved by AHB in the above table cannot be written, read is 0, and a hardfault is generated. The address space marked as Reserved by APB cannot be written, read back as 0, but no hardfault will be generated.

（2） Not only supports 32 bit word access, but also supports halfword and byte access.

（3） Not only supports 32 bit word access, but also supports half word access.

6. Electrical characteristics

6.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to VSS.

6.1.1. Minimum and maximum values

Unless otherwise specified, the mimimum and maximum values are guaranteed in the worst condotions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A =25°C and T_A =$T_{A(max)}$ (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology charateristics are indicated in the table footnotes and are not tested in production. Based on charaterization, the minimum and maximum values refer to sample tests and represent the mean vaule plus or minus three times the standard deviation.

6.1.2. Typical value

Unless otherwise specified, typical data is based on T_A =25°C and VCC = 3.3V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by cgaracterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than equal to the value indicated.

6.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional opeartion of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6-1 Voltage characteristics[1]

Symbol	Ratings	Minimum value	Maximum value	Unit
VCC	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	VCC+0.3	V

（1） Power supply VCC and ground VSS pins must always be connected to the external power supply within the allowable range.

Table 6-2 Current characteristics

Symbol	Describe	Maximum value	Unit
I_{VCC}	Flowing into VCC pin (supply current)[1]	100	mA
I_{VSS}	Total current flowing out of VSS pin (outflow current)[1]	100	
$I_{IO(PIN)}$	Output sink current of COM IO[2]	20	
	Output sink current of COM_L IO[2]	80	
	Source current for all IOs	-20	

（1） Power supply VCC and ground VSS pins must always be connected to the external power supply within the allowable range.

（2） These I/O types refer to the terms and symbols defined by pins.

Table 6-3 Thermal characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	℃
T_O	Range of working temperature	-40 to +85	℃

6.3. Operating conditions

6.3.1. General working conditions

Table 6-4 General working conditions

Symbol	Parameter	Condition	Minimum vaule	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB Clock frequency	-	0	48	MHz
VCC	Standard operating voltage	-	1.7	5.5	V
VIN	I/O input voltage	-	-0.3	VCC+0.3	V
T_A	Ambient temperature	-	-40	85	℃
T_J	Junction temperature	-	-40	90	℃

6.3.2. Operating conditions at power-up / power-down

Table 6-5 Operating conditions at power-up / power-down

Symbol	Parameter	Condition	Minimum vaule	Maximum value	Unit
t_{VCC}	VCC rise time rate	-	0	∞	us/V
	VCC fall time rate	-	20	∞	

6.3.3. Embedded reset and LVD module features

Table 6-6 Embedded reset module features

Symbol	Parameter	Condition	Minimum vaule	Typical value	Maximum value	Unit
$t_{RSTTEMPO}$[1]	Reset time	-	-	4.0	7.5	ms
$V_{POR/PDR}$	POR/PDR reset threshold	Rising edge	1.50[2]	1.60	1.70	V
		Falling edge	1.45[1]	1.55	1.65[2]	V
V_{BOR1}	BOR threshold 1	Rising edge	1.70[2]	1.80	1.90	V
		Falling edge	1.60	1.70	1.80[2]	V
V_{BOR2}	BOR threshold 2	Rising edge	1.90[2]	2.00	2.10	V
		Falling edge	1.80	1.90	2.00[2]	V
V_{BOR3}	BOR threshold 3	Rising edge	2.10[2]	2.20	2.30	V

		Falling edge	2.00	2.10	2.20[2]	V
V_{BOR4}	BOR threshold 4	Rising edge	2.30[2]	2.40	2.50	V
		Falling edge	2.20	2.30	2.40[2]	V
V_{BOR5}	BOR threshold 5	Rising edge	2.50[2]	2.60	2.70	V
		Falling edge	2.40	2.50	2.60[2]	V
V_{BOR6}	BOR threshold 6	Rising edge	2.70[2]	2.80	2.90	V
		Falling edge	2.60	2.70	2.80[2]	V
V_{BOR7}	BOR threshold 7	Rising edge	2.90[2]	3.00	3.10	V
		Falling edge	2.80	2.90	3.00[2]	V
V_{BOR8}	BOR threshold 8	Rising edge	3.10[2]	3.20	3.30	V
		Falling edge	3.00	3.10	3.20[2]	V
V_{PVD0}	PVD threshold 0	Rising edge	1.70[2]	1.80	1.90	V
		Falling edge	1.60	1.70	1.80[2]	V
V_{PVD1}	PVD Threshold 1	Rising edge	1.90[2]	2.00	2.10	V
		Falling edge	1.80	1.90	2.00[2]	V
V_{PVD2}	PVD Threshold 2	Rising edge	2.10[2]	2.20	2.30	V
		Falling edge	2.00	2.10	2.20[2]	V
V_{PVD3}	PVD Threshold 3	Rising edge	2.30[2]	2.40	2.50	V
		Falling edge	2.20	2.30	2.40[2]	V
V_{PVD4}	PVD Threshold 4	Rising edge	2.50[2]	2.60	2.70	V
		Falling edge	2.40	2.50	2.60[2]	V
V_{PVD5}	PVD threshold 5	Rising edge	2.70[2]	2.80	2.90	V
		Falling edge	2.60	2.70	2.80[2]	V
V_{PVD6}	PVD threshold 6	Rising edge	2.90[2]	3.00	3.10	V
		Falling edge	2.80	2.90	3.00[2]	V
V_{PVD7}	PVD threshold 7	Rising edge	3.10[2]	3.20	3.30	V
		Falling edge	3.00	3.10	3.20[2]	V
$V_{POR\_PDR\_hyst}$[1]	POR / PDR hysteresis voltage	-		50		mV
$V_{PVD\_BOR\_hyst}$[1]	PVD hysteresis voltage			100		mV
$Idd_{(PVD)}$	PVD power consumption			0.6		uA
$Idd_{(BOR)}$	BOR power consumption			0.6		uA

（1） Guaranteed by design, not tested in production.

（2） Data is based on assessment results and is not tested in production.

6.3.4. Operating current characteristics

Table 6-7 Operating mode current

Symbol	Condition						Typical value[1]	Maximum value	Unit
	System clock	Frequency	Code	Run	Peripheral clock	FLASH sleep			
$I_{DD}(run)$	HSI	48 MHz	While(1)	Flash	ON	DISABLE	2.6	-	mA
					OFF	DISABLE	1.7	-	
		24 MHz			ON	DISABLE	1.5	-	
					OFF	DISABLE	0.9	-	

Frequency				Typical	Max	Unit
16 MHz	ON	DISABLE	1.1	-		
	OFF	DISABLE	0.7	-		
8 MHz	ON	DISABLE	0.7	-		
	OFF	DISABLE	0.5	-		
4 MHz	ON	DISABLE	0.5	-		
	OFF	DISABLE	0.35	-		
LSI 32.768 KHz	ON	DISABLE	170	-	uA
	OFF	DISABLE	170	-	
LSI 32.768 KHz	ON	ENABLE	95	-	uA
	OFF	ENABLE	95	-	

（1） Data is based on assessment results and is not tested in production.

Table 6-8 Sleep mode current

Symbol	Condition				Typical value[1]	Maximum value	Unit
	System clock	Frequency	Peripheral clock	FLASH sleep			
I_{DD}(sleep)	HSI	48 MHz	ON	DISABLE	1.8	-	mA
			OFF	DISABLE	1.1	-	mA
		24 MHz	ON	DISABLE	1	-	mA
			OFF	DISABLE	0.6	-	mA
		16 MHz	ON	DISABLE	0.75	-	mA
			OFF	DISABLE	0.5	-	mA
		8 MHz	ON	DISABLE	0.5	-	mA
			OFF	DISABLE	0.35	-	mA
		4 MHz	ON	DISABLE	0.4	-	mA
			OFF	DISABLE	0.35	-	mA
	LSI	32.768 KHz	ON	DISABLE	170	-	uA
			OFF	DISABLE	170	-	uA
	LSI	32.768 KHz	ON	ENABLE	95	-	uA
			OFF	ENABLE	96	-	uA

（1） Data is based on assessment results and is not tested in production.

Table 6-9 Stop mode current

Symbol	Condition					Typical value[1]	Maximum value	Unit
	VCC	VDD	MR/LPR	LSI	Peripheral clock			
I_{DD}(stop)	1.7 to 5.5V	1.2V	MR	-	-	70	-	uA
		1.2V	LPR	ON	RTC+IWDG+LPTIM	6	-	
					IWDG	6	-	
					LPTIM	6	-	
					RTC	6	-	
				OFF	No	6	-	
		1.0V		ON	RTC+IWDG+LPTIM	4.5	-	
					IWDG	4.5	-	
					LPTIM	4.5	-	
					RTC	4.5	-	
				OFF	No	4.5	-	

（1） Data is based on assessment results and is not tested in production.

6.3.5. Wake-up time for low power mode

Table 6-10 Low power mode wake-up time

Symbol	Parameters[1]		Condition		Typical value[2]	Maximum value	Unit
$T_{WUSLEEP}$	Wake-up from sleep mode		-		1.65		us
T_{WUSTOP}	Wake-up from stop mode	Powered by MR	Execute program in Flash, HSI (24 MHz) as system clock		3.5		us
		Powered by LPR	Execute program in Flash, HSI as system clock	VDD=1.2V	6		us
				VDD=1.0V	6		

（1） The wake-up time is measured from the wake-up time until the first instruction is read by the user program.

（2） Data is based on assessment results and is not tested in production.

6.3.6. External Clock Source Characteristics

6.3.6.1. External high-speed clock

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the chip stops working, the corresponding I/O is used as a standard GPIO.
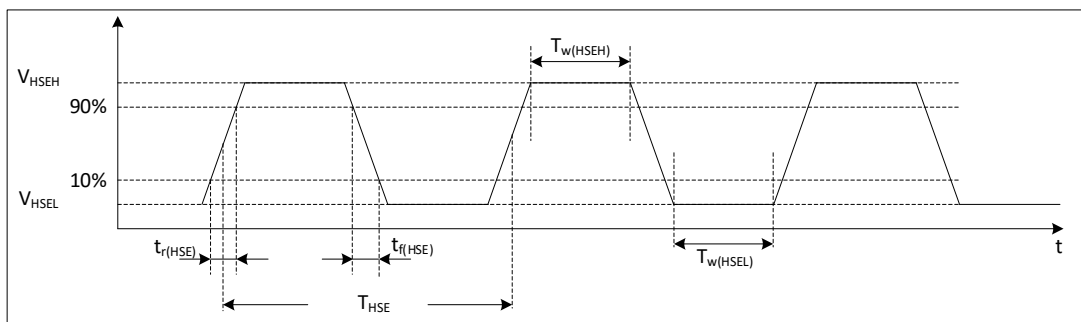

Figure 6-1 External high-speed clock timing diagram

Table 6-11 External high-speed clock features

Symbol	Parameters[1]	Minimum value	Typical value	Maximum value	Unit
f_{HSE_ext}	User external clock source frequency	0	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7VCC		VCC	V
V_{HSEL}	Input pin low level voltage	Vss		0.3VCC	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	Enter high or low time	15			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Enter the rise/fall time	-		20	ns

（1） Guaranteed by design, not tested in production.

6.3.6.2. External low-speed clock

In the bypass mode of LSE (the LSE BYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO .
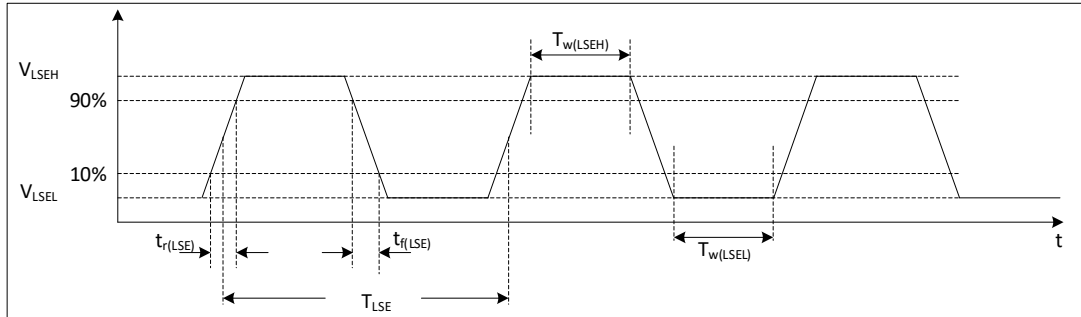

Figure 6-2 External low-speed clock timing diagram

Table 6-12 External low-speed clock characteristics

Symbol	Parameters[1]	Minimum value	Typical value	Maximum value	Unit
f_{LSE_ext}	User external clock frequency		32.768	1000	KHz
V_{LSEH}	Input pin high level voltage	0.7VCC			V
V_{LSEL}	Input pin low level voltage			0.3VCC	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	Enter high or low time	450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Enter the rise/fall time	-		50	ns

（1） Guaranteed by design, not tested in production .

6.3.6.3. External high-speed crystal

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 6-13 External high-speed crystal characteristics

Symbol	Parameter	Condition[1]	Minimum value[2]	Typical value	Maximum value[2]	Unit
f_{OSC_IN}	Oscillation frequency	-	4		32	MHz
IDD[4]	HSE current consumption	During startup			5.5	mA
		VCC = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz		0.58		
		VCC = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz		0.59		
		VCC = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz		0.89		
		VCC = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz		1.14		
		VCC = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz		1.94		

| $t_{SU(HSE)}$[3][4] | Startup Time | f_{OSC_IN} = 32 MHz | | 3 | | ms |
| | | f_{OSC_IN} = 4 MHz | | 15 | | ms |

（1） Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.

（2） Guaranteed by design, not tested in production.

（3） $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state , measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another .

（4） Data is based on assessment results and is not tested in production.

6.3.6.4. External low-speed crystal

The low-speed external (LSE) clock can be supplied with a 32.768 KHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 6-14 External low-speed crystal characteristics

Symbol	Parameter	Condition[1]	Minimum value[2]	Typical value	Maximum value[2]	Unit
IDD[4]	LSE current consumption	LSE_DRIVER [1:0] = 00		-		nA
		LSE_DRIVER [1:0] = 01		560		
		LSE_DRIVER [1:0] = 10		920		
		LSE_DRIVER[1:0] = 11		1260		
$t_{SU(LSE)}$[3][4]	Startup Time			3		s

（1） Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.

（2） Guaranteed by design, not tested in production.

（3） $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable , measured for a standard crystal/resonator , which may vary greatly from crystal to resonator.

（4） Data is based on assessment results and is not tested in production.

6.3.7. Internal high frequency clock source HSI characteristics

Table 6-15 Internal high frequency clock source characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HSI}	HSI frequency	T_A = 25 °C, VCC = 3.3 V	23.83[2]	24	24.17[2]	MHz
			21.97[2]	22.12	22.27[2]	MHz
			15.89[2]	16	16.11[2]	MHz
			7.94[2]	8	8.06[2]	MHz
			3.97[2]	4	4.03[2]	MHz
$\Delta T_{emp(HSI)}$	HSI frequency temperature drift	VCC = 1.7 to 5.5 V, T_J = 0 to 85 °C	-2[2]		2[2]	%
		VCC = 1.7 to 5.5 V, T_J = -40 to 85 °C	-4[2]		2[2]	%

f_{TRIM}[1]	HSI fine-tuning accuracy			0.1			%
D_{HSI}[1]	Duty cycle		45[1]		55[1]		%
$t_{Stab(HSI)}$	HSI stabilization time			2	4[1]		us
$I_{DD(HSI)}$[2]	HSI current consumption	4 MHz		100			uA
		8 MHz		105			uA
		16 MHz		150			uA
		22.12 MHz, 24 MHz		180			uA

（1） Guaranteed by design, not tested in production.

（2） Data is based on assessment results and is not tested in production.

6.3.8. Internal low frequency clock source LSI characteristics

Table 6-16 Internal low frequency clock characteristics

Symbol	Parameter	Condition	Minimum vaule	Typical value	Maximum value	Unit
f_{LSI}	LSI frequency	T_A = 25 °C, VCC = 3.3 V	-3		+3	%
$\Delta T_{emp(LSI)}$	LSI frequency temperature drift	VCC = 1.6 to 5.5 V, T_J = 0 to 85 °C	-10[2]		10[2]	%
		VCC = 1.6 to 5.5 V, T_J = -40 to 85°C	-20[2]		20[2]	%
f_{TRIM}[1]	LSI fine-tuning accuracy			0.2		%
$t_{Stab(LSI)}$[1]	LSI stabilization time			150		us
$I_{DD(LSI)}$[1]	LSI current consumption			210		nA

（1） Guaranteed by design, not tested in production.

（2） Data is based on assessment results and is not tested in production.

6.3.9. Phase locked loop (PLL) characteristics

Table 6-17 Phase locked loop characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{PLL_IN}	input frequency	T_A = 25 °C, VCC = 3.3 V	16[1]		24[1]	MHz
f_{PLL_OUT}	Output frequency	T_A = 25 °C, VCC = 3.3 V	32[1]		48	MHz
Jitter	Period jitter				0.3[1]	ns
t_{LOCK}	Latch time	f_{PLL_IN} = 24 MHz		15	40[1]	us

（1） Guaranteed by design, not tested in production.

6.3.10. Memory characteristics

Table 6-18 Memory characteristics

Symbol	Parameter	Condition	Typical value	Maximum value[1]	Unit
t_{prog}	Page program	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase	-	3.0	4.5	ms
I_{DD}	Page programe		2.1	2.9	mA
	Page/sector/mass erase		2.1	2.9	mA

（1） Guaranteed by design, not tested in production.

Table 6-19 Memory erase times and data retention

Symbol	Parameter	Condition	Minimum[1]	Unit
N_{END}	Erase and write times	T_A = -40 to 85 ℃	100	Kcycle
t_{RET}	Data retention period	10 Kcycle T_A = 55 ℃	20	Year

（1） Data is based on assessment results and is not tested in production.

6.3.11. EFT characteristics

Symbol	Parameter	Condition	Grade	Typical value	Unit
EFT to IO		IEC61000-4-4	B	2	KV
EFT to Power		IEC61000-4-4	B	4	KV

6.3.12. ESD & LU Characteristics

Table 6-20ESD & LU characteristics

Symbol	Parameter	Condition	Typical value	Unit
$V_{ESD(HBM)}$	Static discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	6	KV
$V_{ESD(CDM)}$	Static discharge voltage (charging equipment model)	ESDA/JEDEC JS-002-2018	1	KV
$V_{ESD(MM)}$	Static discharge voltage (machine model)	JESD22-A115C	200	V
LU	Static latch-up	JESD78E	200	mA

6.3.13. Port Characteristics

Table 6-21IO static characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IH}	Input high level voltage	VCC = 1.7 to 5.5 V	0.7VCC			V
V_{IL}	Input low level voltage	VCC = 1.7 to 5.5 V			0.3VCC	V
V_{hys}[1]	Schmitt hysteresis voltage			200		mV
I_{lkg}	Input leakage current				1	uA
R_{PU}	Pull-up resistor		30	50	70	kΩ
R_{PD}	Pull-down resistor		30	50	70	kΩ
C_{IO}[1]	Pin capacitance			5		pF

（1） Guaranteed by design, not tested in production.

Table 6-22 Output voltage characteristics

Symbol	Parameters[1]	Condition	Minimum	Maximum	Unit

V_{OL}	COM IO output low level	I_{OL} = 8 mA, VCC ≥ 2.7 V	-		0.4	V
V_{OL}		I_{OL} = 4 mA, VCC = 1.8 V	-		0.5	V
V_{OL}[3]	COM_L IO[2] output low level	I_{OL} = 20 mA, VCC ≥ 2.7 V	-		0.4	V
V_{OL}[3]		I_{OL} = 10 mA, VCC = 1.8 V	-		0.5	V
V_{OL}[3]		I_{OL} = 40 mA, VCC ≥ 2.7 V	-		0.4	V
V_{OL}[3]		I_{OL} = 20 mA, VCC = 1.8 V	-		0.5	V
V_{OL}[3]		I_{OL} = 60 mA, VCC ≥ 2.7 V	-		0.4	V
V_{OL}[3]		I_{OL} = 30 mA, VCC = 1.8 V	-		0.5	V
V_{OL}[3]		I_{OL} = 80 mA, VCC ≥ 2.7 V	-		0.4	V
V_{OL}[3]		I_{OL} = 40 mA, VCC = 1.8 V	-		0.5	V
V_{OH}	COM IO output high level	I_{OH} = 8 mA, VCC ≥ 2.7 V	VCC–0.4	-		V
V_{OH}		I_{OH} = 4 mA, VCC = 1.8 V	VCC–0.5	-		V
V_{OL}[3]	COM_L IO[2] output high level	I_{OH} = 20 mA, VCC ≥ 2.7 V	VCC–0.4	-		V
V_{OL}[3]		I_{OH} = 10 mA, VCC = 1.8 V	VCC–0.5	-		V
V_{OL}[3]		I_{OH} = 40 mA, VCC ≥ 2.7 V	VCC–0.4	-		V
V_{OL}[3]		I_{OH} = 20 mA, VCC = 1.8 V	VCC–0.5	-		V
V_{OL}[3]		I_{OH} = 60 mA, VCC ≥ 2.7 V	VCC–0.4	-		V
V_{OL}[3]		I_{OH} = 30 mA, VCC = 1.8 V	VCC–0.5	-		V
V_{OL}[3]		I_{OH} = 80 mA, VCC ≥ 2.7 V	VCC–0.4	-		V
V_{OL}[3]		I_{OH} = 40 mA, VCC = 1.8 V	VCC–0.5	-		V

（1） IO types can refer to the terms and symbols defined by the pins.

（2） COM_L IO current 80mA/60mA/40mA/20mA can be set by software .

（3） Data is based on assessment results and is not tested in production.

6.3.14. NRST pin characteristics

Table 6-23NRST pin characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IH}	Input high level voltage	VCC = 1.7 to 5.5 V	0.7VCC			V
VIL	Input low level voltage	VCC = 1.7 to 5.5 V			0.2VCC	V
V_{hys}[1]	Schmitt hysteresis voltage			300		mV
I_{lkg}	Input leakage current				1	uA
RPU[1]	Pull-up resistor		30	50	70	kΩ
RPD[1]	Pull-down resistor		30	50	70	kΩ
$C_{IO\_}$	Pin capacitance			5		pF

（1） Guaranteed by design, not tested in production.

6.3.15. ADC characteristics

surface 6-24ADC characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$I_{DD\_}$	Current consumption	@0.75MSPS		1.0		mA
C_{IN}[1]	Internal sample and hold capacitors			5		pF

F_{ADC}	Convert clock frequency	VCC = 1.7 to 2.3 V	1	4	6[2]	MHz
		VCC = 2.3 to 5.5 V	1	8	12[2]	MHz
T_{samp}[1]		VCC = 1.7 to 2.3 V	0.2			us
		VCC = 2.3 to 5.5 V	0.1			us
T_{conv}[1]				12*Tclk		
T_{eoc}[1]				0.5*Tclk		
DNL[2]				±2		LSB
INL[2]				±3		LSB
Offset[2]				±2		LSB

（1） Guaranteed by design, not tested in production.

（2） Data is based on assessment results and is not tested in production.

6.3.16. Comparator Characteristics

Table 6-25 Comparator features[1]

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
VIN	Input voltage range			0		VCC	V
VBG	Scale input voltage				VREFINT		V
VSC	Scaler offset voltage				±5	± 10	mV
IDD(SCALER)	Scaler static consumption	BRG_EN=0 (bridge disable)			200	300	nA
		BRG_EN=1(bridge enable)			0.8	1	uA
tSTART_SCALER	Scaler startup time				100	200	us
tSTART	Startup time to reach propagation delay specification	High-speed mode				5	us
		Medium-speed mode				15	
tD	Propagation delay	200 mV step, 100 mV overdrive	High-speed mode			30	50	ns
			Medium-speed mode			0.3	0.6	us
		>200 mV step, 100 mV overdrive	High-speed mode				10	us
			Medium-speed mode				1.2	ns
Voffset	Offset error				±5		mV
Vhys	Hysteresis	No hysteresis			0		mV
		Low hysteresis			10		
		Medium hysteresis			20		
		High hysteresis			30		

		Medium-speed mode, no de-glitcher	Static		5		uA
IDD	Consumption		With 50 KHz and ±100 mv overdrive square sig-nal		6		uA
		Medium-speed mode, with de-glitcher	Static		7		uA
			With 50 KHz and ±100 mv overdrive square sig-nal		8		u A
		High-speed mode, no de-glitcher	Static		250		u A
			With 50 KHz and ±100 mv overdrive square sig-nal		250		u A

（1） Guaranteed by design, not tested in production.

6.3.17. Temperature sensor characteristics

Table 6-26 Temperature sensor characteristics

Symbol	Parameter	Mini-mum value	Typi-cal value	Maximum value	Unit
T_L[1]	VTS linearity with temperature		±1	±2	℃
Avg_Slope[1]	Average slope	2.3	2.5	2.7	mV/℃
V_{30}	Voltage at 30 ℃ (±5 ℃)	0.742	0.76	0.785	V
t_{START}[1]	Start up time entering in continuous mode		7 0	1 20	us
t_{s_temp}[1]	ADC sampling time when reading the tempera-ture	9			us

（1） Guaranteed by design, not tested in production.

（2） Data is based on assessment results and is not tested in production.

6.3.18. Timer features

Table 6-27 Timer features

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution time	-	1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.833		ns
f_{EXT}		-		$f_{TIMxCLK}$/2	MHz

	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 48 MHz		24	
R_{esTIM}	Timer resolution	TIM1/3/14/16/17		16	Bit
$t_{COUNTER}$	16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.020833	1365	us

Table 6-28LPTIM characteristics (clock selection LSI)

Prescaler	PRESC [2:0]	Minimum overflow value	Maximum overflow value	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 6-29IWDG characteristics (clock selection LSI)

Prescaler	PR[2:0]	Minimum overflow value	Maximum overflow value	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 6-30 WWDG characteristics (clock select 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Minimum overflow value	Maximum overflow value	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

6.3.19. Communication interfaces

6.3.19.1. I2C interface features

The I2C interface meets the timing requirements of the I2C-bus specification and user manual:

■ Standard-mode (Sm): 100 Kbit/s

■ Fast-mode (Fm): 400 Kbit/s

The I2C timings requirements is guaranteed by design, provided the I2C peripheral is properly configured and the I2C CLK frequency is greater than the minimum required in the table below.

Table 6-31 Minimum I2C CLK frequency

Symbol	Parameter	Condition	Minimum	Unit
$f_{I2CCLK(min)}$	Minimum I2CCLK frequency	Standard-mode	2	MHz
		Fast-mode	9	

I2C SDA and SCL pins have analogue filtering, see table below.

Table 6-32I2C filter characteristics

Symbol	Parameter	Minimum	Maximum	Unit
t_{AF}	Lmiting duration of spikes suppressed by the filter (spikers shorter than the limiting duration are suppressed)	50	260	ns

6.3.19.2. Serial Peripheral Interface (SPI) Characteristics

Table 6-33SPI characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	12	MHz
		Slave mode	-	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, fPCLK = 36 MHz, presc = 4	Tpclk*2 - 2	Tpclk*2 + 1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode, fPCLK = 48 MHz, presc = 4	Tpclk + 5[1]	-	ns
		Slave mode, fPCLK = 48 MHz, presc = 4	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	ns
$t_{h(SI)}$		Slave mode	Tpclk + 5	-	
$t_{a(SO)}$	Data output access time	Slave mode, presc = 4	0	3Tpclk	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	2Tpclk + 5	4Tpclk + 5	ns
$t_{v(SO)}$	Data output valid ime	Slave mode (after enable edge), presc = 4	0	1.5Tpclk[2]	ns
$t_{v(MO)}$	Data output valid ime	Master mode (after enable edge)	-	6	ns
$t_{h(SO)}$	Data output hold time	Slave mode, presc = 4	0[3]	-	ns
$t_{h(MO)}$		Master mode	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

（1） The Master generates a 1pclk receive control signal before the receive edge.

（2） Slave has a maximum of 1pclk based on the sending edge of SCK delay, considering IO delay, etc., define 1.5pclk.

（3） In the case that the SCK duty cycle sent by the Master is wide between the receiving edge and the sending edge, the Slave updates the data before the sending edge.
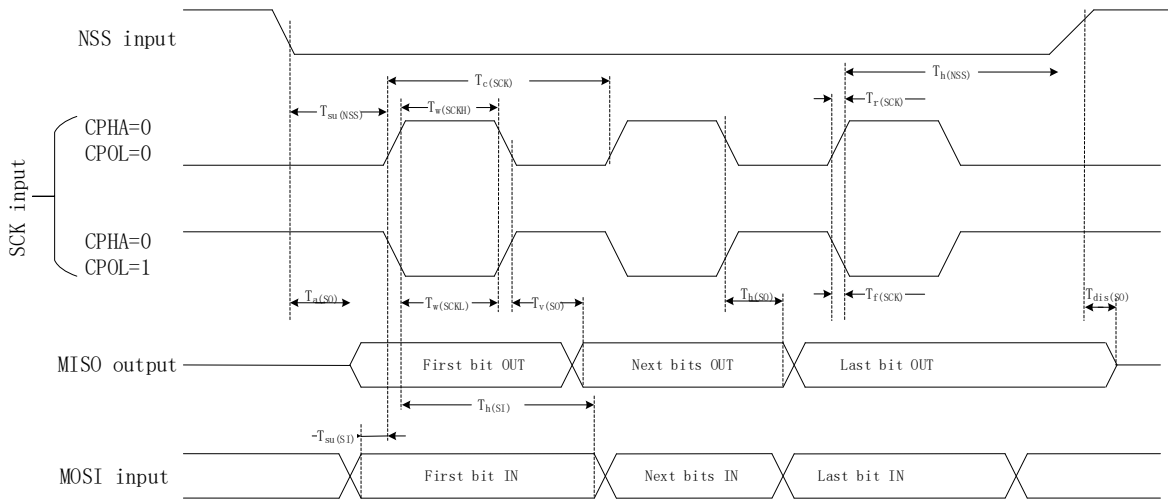
Figure 6-3SPI timing diagram – slave mode and CPHA=0
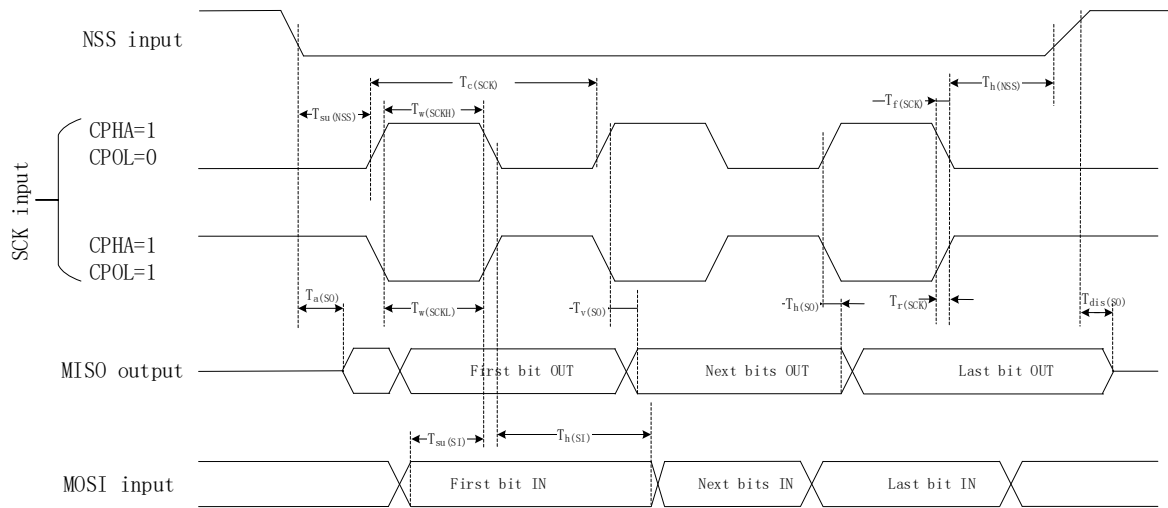
Figure 6-4SPI timing diagram – slave mode and CPHA=1
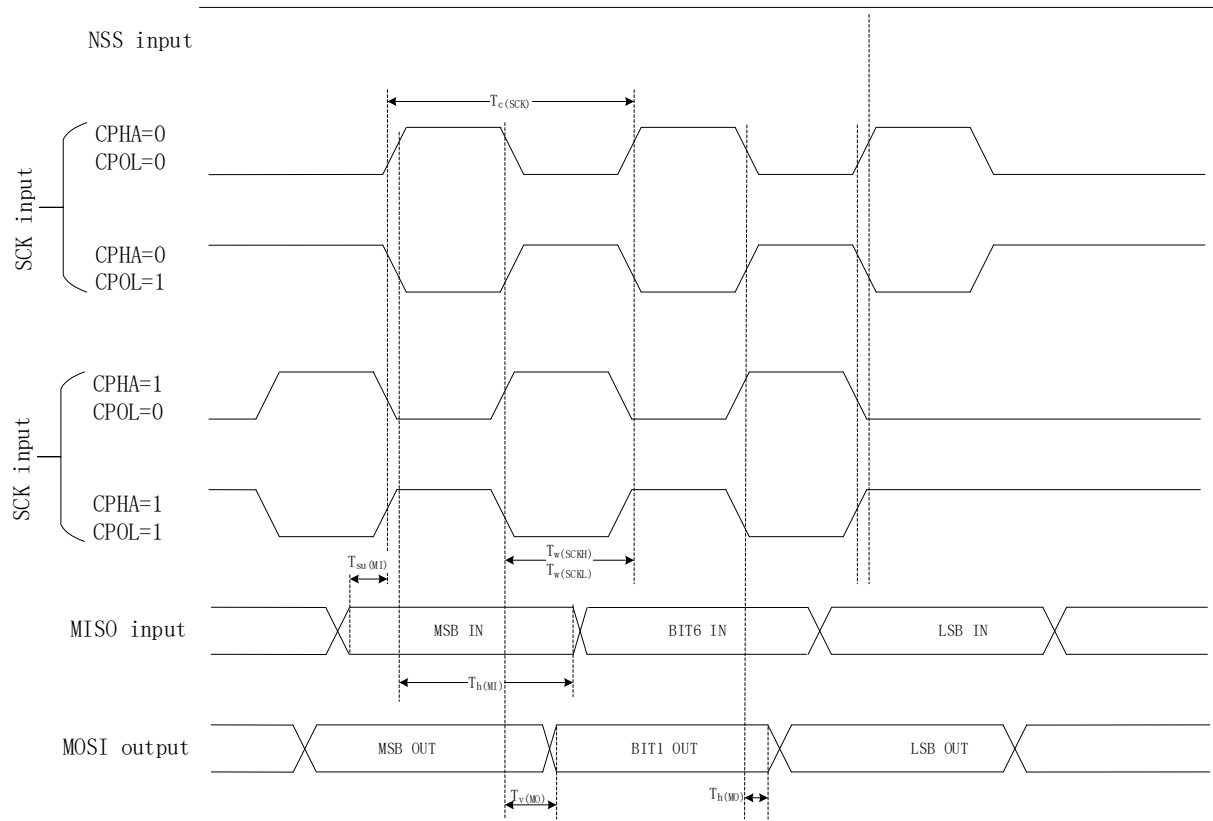
Figure 6-5SPI timing diagram – master mode

7. Package information

7.1. LQFP32 package size

Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
A3	0.590	0.640	0.690
b	0.330	-	0.410
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
e	0.800BSC		
L	0.450	-	0.750
L1	1.000REF		
θ	0	-	7°

Note：1. Dimensions are not to scale
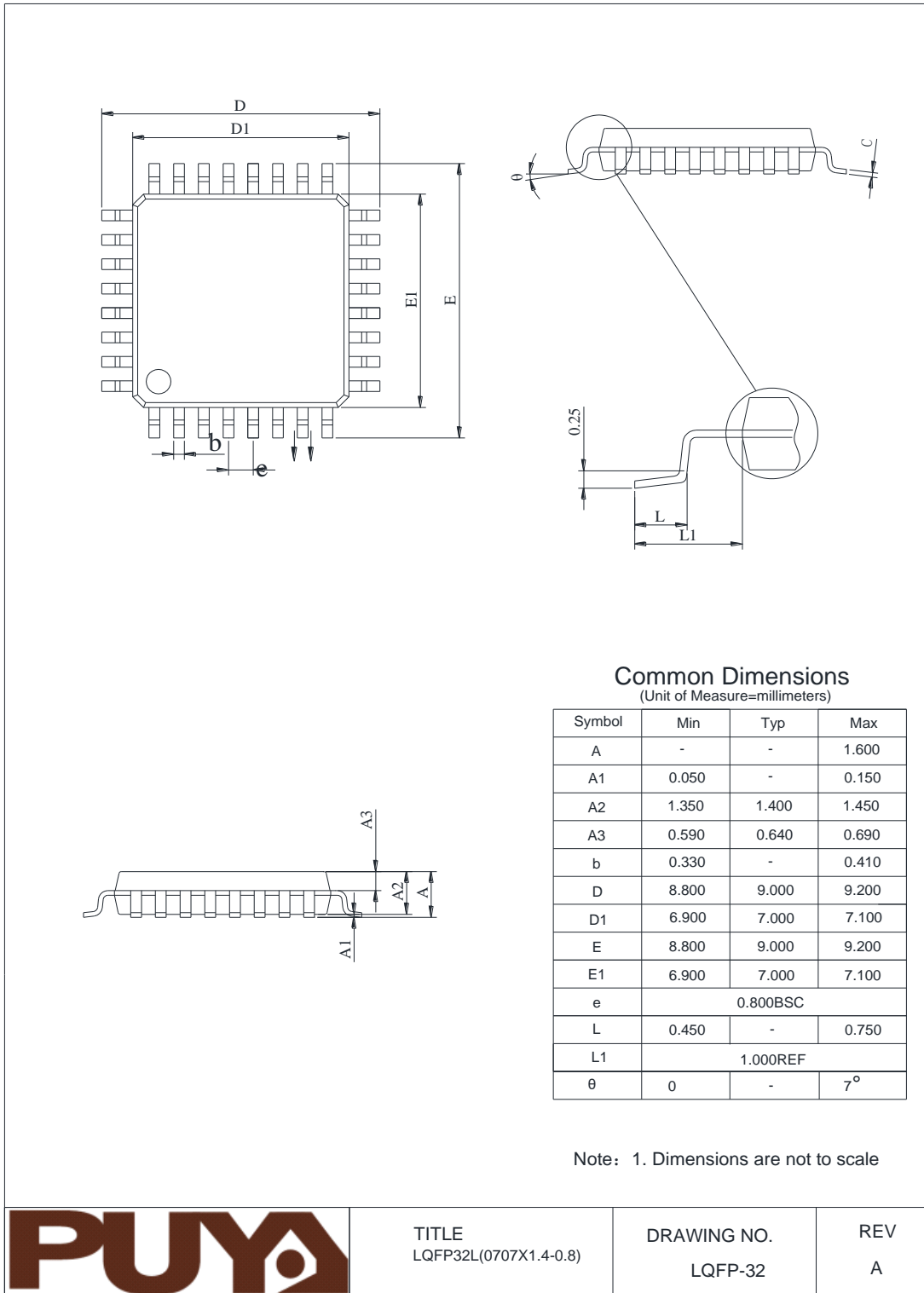
	TITLE LQFP32L(0707X1.4-0.8)	DRAWING NO. LQFP-32	REV A

7.2. QFN32 package size

TOP VIEW   SIDE VIEW

Pin1

BOTTOM VIEW

Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0	0.020	0.050
b	0.180	0.250	0.300
c	0.200REF		
D	4.900	5.000	5.100
D2	3.400	3.500	3.600
E	4.900	5.000	5.100
E1	3.400	3.500	3.600
e	0.500BSC		
Nd	3.500BSC		
L	0.350	0.400	0.450
h	0.300	0.350	0.400

BOTTOM VIEW

Note：1. Dimensions are not to scale
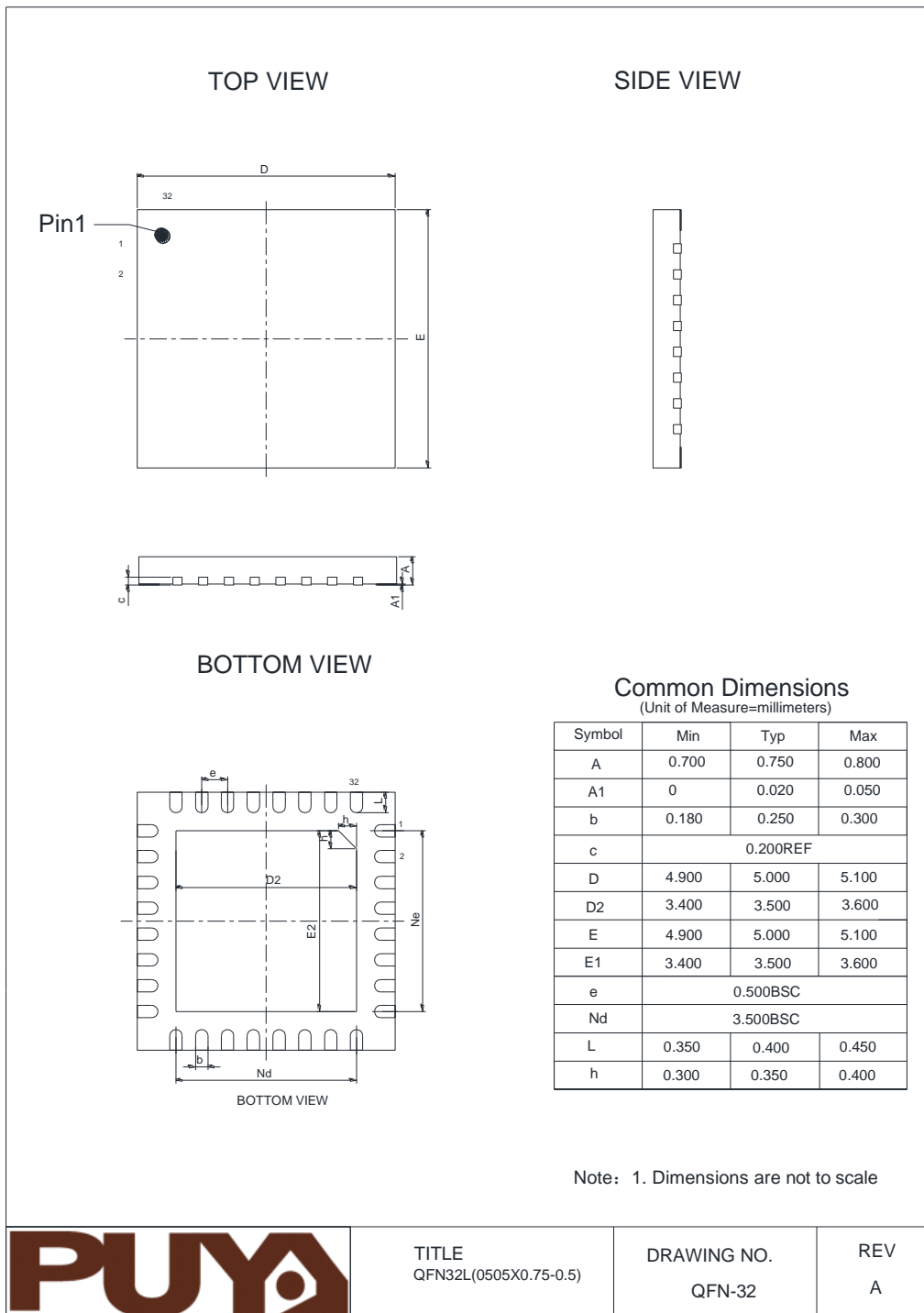
PUYA	TITLE QFN32L(0505X0.75-0.5)	DRAWING NO. QFN-32	REV A

7.3. QFN20 Package Dimensions

TOP VIEW

SIDE VIEW

Pin1

BOTTOM VIEW

Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.500	0.550	0.600
A1	0	0.020	0.050
b	0.150	0.200	0.250
b1	0.140REF		
c	0.150REF		
D	2.900	3.000	3.100
D2	1.550	1.650	1.750
E	2.900	3.000	3.100
E2	1.550	1.650	1.750
e	0.400BSC		
Nd	1.600BSC		
Ne	1.600BSC		
L	0.350	0.400	0.450
h	0.200	0.250	0.300

Note：1. Dimensions are not to scale
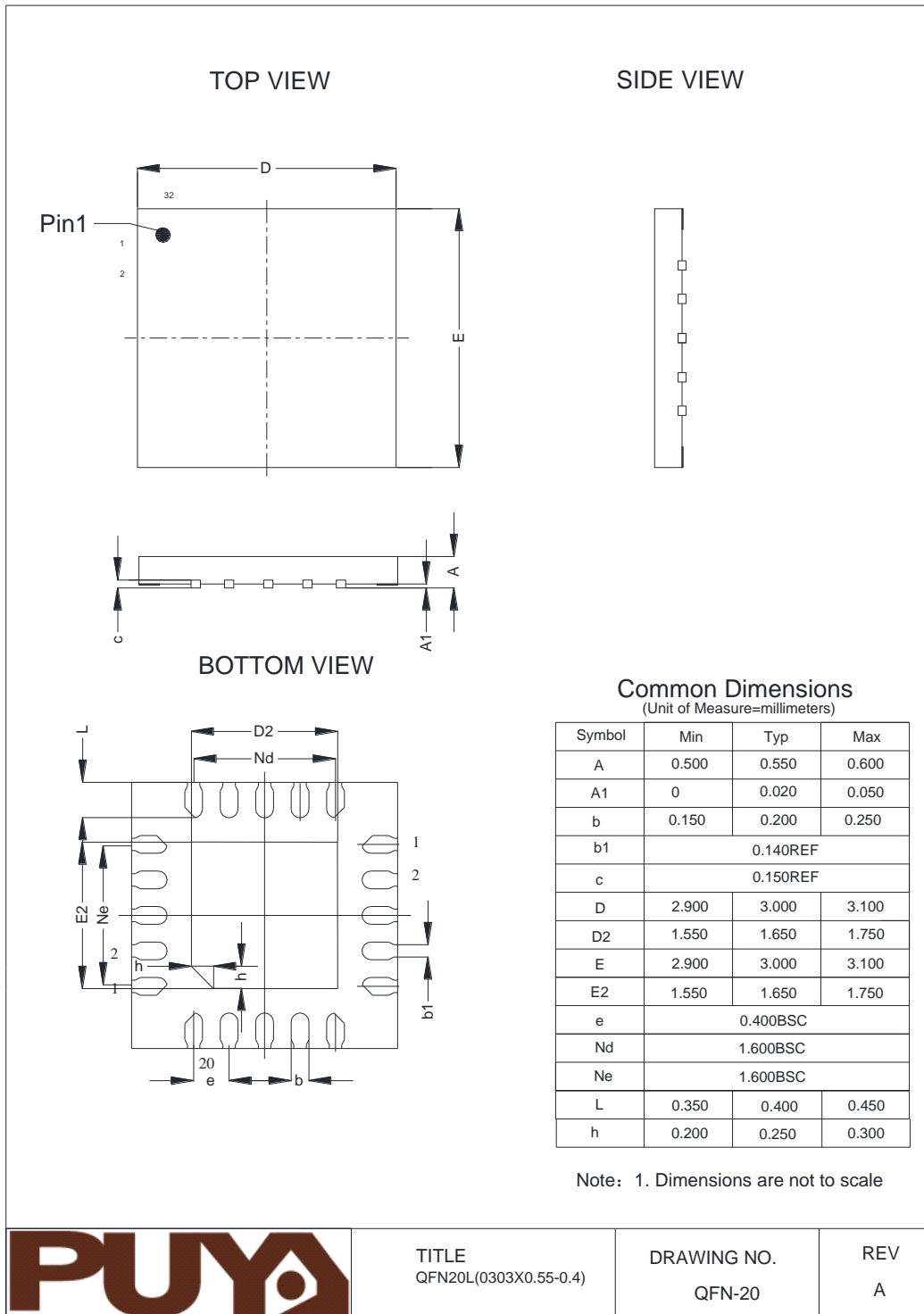
PUYA	TITLE QFN20L(0303X0.55-0.4)	DRAWING NO. QFN-20	REV A

7.4. TSSOP20 package size

Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
A3	0.390	0.440	0.490
b	0.200	-	0.280
c	0.130	-	0.170
D	6.400	6.500	6.600
E	6.200	6.400	4.500
E1	4.300	4.400	
e		0.650BSC	0.750
L	0.450	-	
L1		1.000REF	
θ	0	-	8°

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	TSSOP20	TSSOP-20	A

8.　Ordering information

Example:

| PY | 32 | F | 030 | K1 | 8 | T | 6 | x |

Company

Product family
32bit MCU

Product type
F = General purpose

Sub-family
030 = PY32F030xx

Pin count
F1 = 20 pins Pinout1
E1 = 24 pins Pinout1
G1 = 28 pins Pinout1
K1 = 32 pins Pinout1
K2 = 32 pins Pinout2

User code memory size
3 = 8Kbytes
4 = 16 Kbytes
6 = 32 Kbytes
7 = 48 Kbytes
8 = 64 Kbytes
Package
P = TSSOP
U = QFN
T = LQFP
Y = WLCSP

Temerature range

6 = -40℃ to +85℃

Options

xxx = code ID of programmed parts(includes packing type)
TR = tape and reel packing
TU = Tube Packing
blank = tray packing

9. Version history

Version	Date	Description	Note
V1.0	2021.10.20	Initial version	-
V1.1	2021.12.09	1. Delete SSOP24 package information 2. Add "TU= Tube Packing" to ordering information 3. Section 6.3.9, modifying parameters	-
V1.2	2021.12.28	1. Modify the format 2. Section 6.3.4 , modifying parameters 3. Section 6.3.16, modifying parameters 4. Chapter 4, LQFP32 Pinout1 pin configuration modification	-
V1.3	2022.1.13	1. Added chapter 6.3.11 2. Modify chapter 3.15, modify parameters 3. Add TSSOP20/QFN20 Pinout2 package	-
V1.4	2022.1.24	1. Table 6-18, modify parameters 2. Table 6-33, modify parameters 3. Chapter 8, modifying parameters	-