Multiplexers are used to create complex signal routing, such as in the ALU of processor. There are other applications as well, two of them are presented below.

Increasing the number of address bits by one doubles the number of possible inputs. Thus, 4 bit multiplexer is the result of two selector bits (Fig. 3 and Fig 4.). The truth table of 4 bit multiplexer can be found below:

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

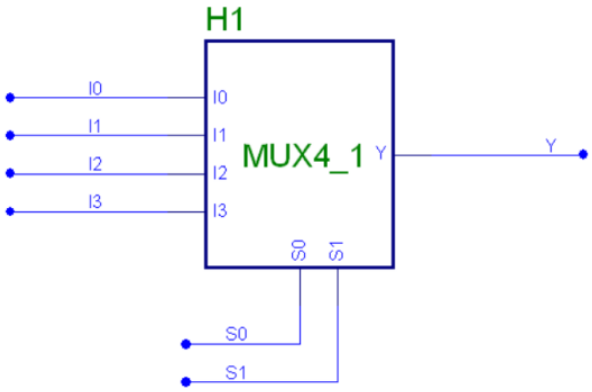

Figure 3. –Block scheme of 4 bit multiplexer

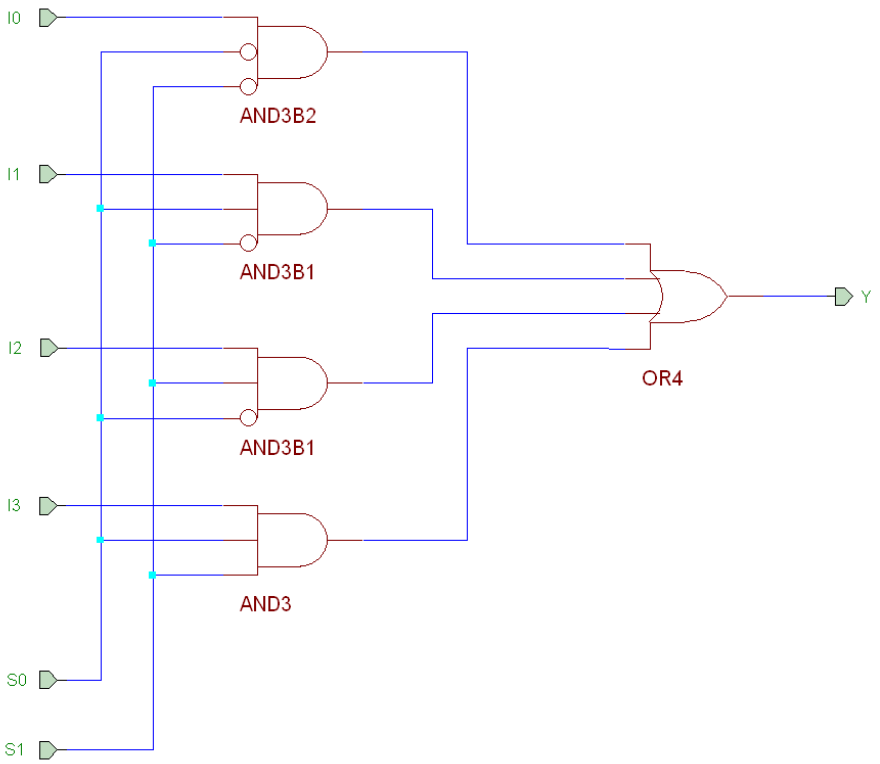

Figure 4. – Schematic of 4 bit multiplexer

Multiplexer with increased number of inputs can be designed in two ways. You can design it by using the necessary amount of gates or you can create it from multiplexers with less inputs.

Multiplexer helps in the implementation of look-up tables (see introductory lab description). The used FPGA (on the Basys panel) utilize 4 bit LUTs in its CLB to implement logic functions up to 4 variables. If this would be solved by containers, then each CLB would need 64k bit memory. Instead, it is enough to use e.g. a 16 bit register with a 16 bit multiplexer. The address bits of the multiplexer are connected to 4 variables of the logic function. The software calculates, based on the schematic, which logic function is needed for implementation and it connects the 16 input bits to the given input of the multiplexer in every combination of the mentioned 4 input variables. It can be seen that such realization requires less resources.