Computational Microelectronics HW.8

EECS, 20204003

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1. Double Gate FET with Non-linear Poisson

1) Numerical Expression

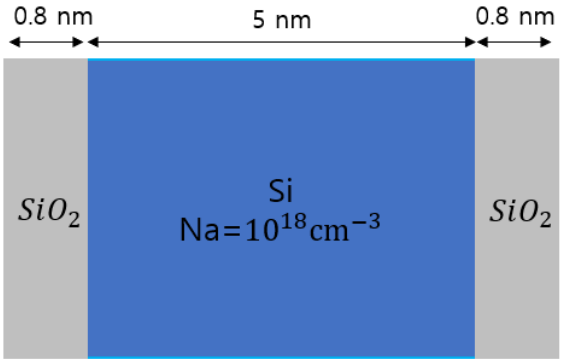

Fig. 1 Double Gate FET

$qN_{dop}^{+} = -qN_{Acceptor}$

a) At Si:

$$r_i = \frac{\varepsilon_{si}}{\Delta x}(\phi_{i+1} - 2\phi_i + \phi_{i-1}) + (\Delta x)qN_{dop}^{+} - (\Delta x)qn_{int}\exp\left(\frac{q\phi_i}{k_BT}\right)$$

$$J_{i,i+1} = \frac{\varepsilon_{si}}{\Delta x}\ ,\quad J_{i,i} = \frac{-2\varepsilon_{si}}{\Delta x} - (\Delta x)qn_{int}\frac{q}{k_BT}\exp\left(\frac{q\phi_i}{k_BT}\right)\ ,\ J_{i,i-1} = \frac{\varepsilon_{si}}{\Delta x}$$

b) At Oxide:

$$r_i = \frac{\varepsilon_{ox}}{\Delta x}(\phi_{i+1} - 2\phi_i + \phi_{i-1})$$

$$J_{i,i+1} = \frac{\varepsilon_{ox}}{\Delta x}\ ,\quad J_{i,i} = \frac{-2\varepsilon_{ox}}{\Delta x},\ J_{i,i-1} = \frac{\varepsilon_{ox}}{\Delta x}$$

c) At Oxide-Si interface:

$$r_i = \frac{\varepsilon_{si}}{\Delta x}(\phi_{i+1} - \phi_i) - \frac{\varepsilon_{ox}}{\Delta x}(\phi_i - \phi_{i-1}) + \left(\frac{\Delta x}{2}\right)qN_{dop}^{+} - \left(\frac{\Delta x}{2}\right)qn_{int}\exp\left(\frac{q\phi_i}{k_BT}\right)$$

$$J_{i,i+1} = \frac{\varepsilon_{si}}{\Delta x}\ ,\quad J_{i,i} = \frac{-\varepsilon_{si}-\varepsilon_{ox}}{\Delta x} - \left(\frac{\Delta x}{2}\right)qn_{int}\frac{q}{k_BT}\exp\left(\frac{q\phi_i}{k_BT}\right)\ ,\ J_{i,i-1} = \frac{\varepsilon_{ox}}{\Delta x}$$

d) At Si-Oxide interface:

$$r_i = \frac{\varepsilon_{ox}}{\Delta x}(\phi_{i+1} - \phi_i) - \frac{\varepsilon_{si}}{\Delta x}(\phi_i - \phi_{i-1}) + \left(\frac{\Delta x}{2}\right)qN_{dop}^{+} - \left(\frac{\Delta x}{2}\right)qn_{int}\exp\left(\frac{q\phi_i}{k_BT}\right)$$

$$J_{i,i+1} = \frac{\varepsilon_{ox}}{\Delta x}\ ,\quad J_{i,i} = \frac{-\varepsilon_{si}-\varepsilon_{ox}}{\Delta x} - \left(\frac{\Delta x}{2}\right)qn_{int}\frac{q}{k_BT}\exp\left(\frac{q\phi_i}{k_BT}\right)\ ,\ J_{i,i-1} = \frac{\varepsilon_{si}}{\Delta x}$$

HW8 is using same model that we used in HW5. However, in HW6, the problem was about linear Poisson solver. However, HW8 is about non-linear Poisson. As a result, Newton-Raphson method is used to solve above problem. All of elements which are needed are represented above.

Finally, by solving below equation and update the potential many time, the numerical solution can be solved.

$$\mathbf{J}\,\boldsymbol{\delta\phi} = -\mathbf{r}$$

$$\boldsymbol{\phi}_{new} = \boldsymbol{\phi} + \boldsymbol{\delta\phi}_{old}$$

2) Results

a) Electrostatic Potential ($\mathbf{V_{gs}} = \mathbf{0V}, \mathbf{0.5V}, \mathbf{1V}$)

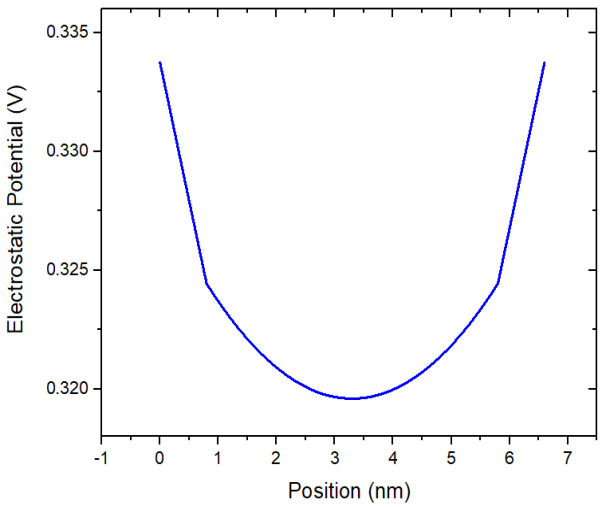

Fig 2. Position vs. Potential graph which is solved numerically when $\mathbf{V_{gs}} = 0\text{V}$.

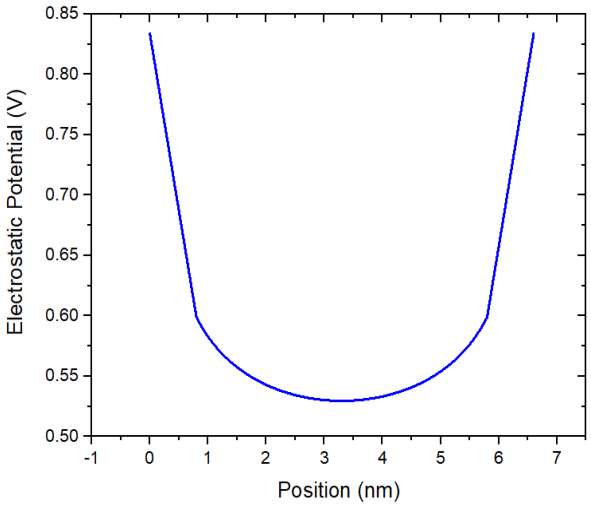

Fig 3. Position vs. Potential graph which is solved numerically when $\mathbf{V_{gs}} = 0.5\text{V}$.

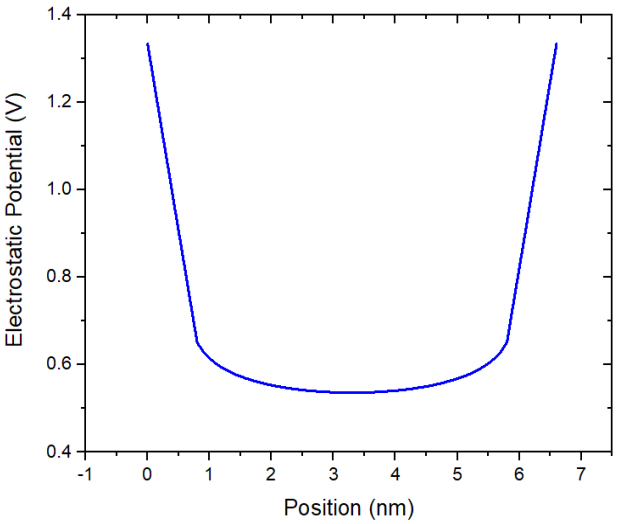

Fig 4. Position vs. Potential graph which is solved numerically when $\mathbf{V_{gs}} = 1\text{V}$.

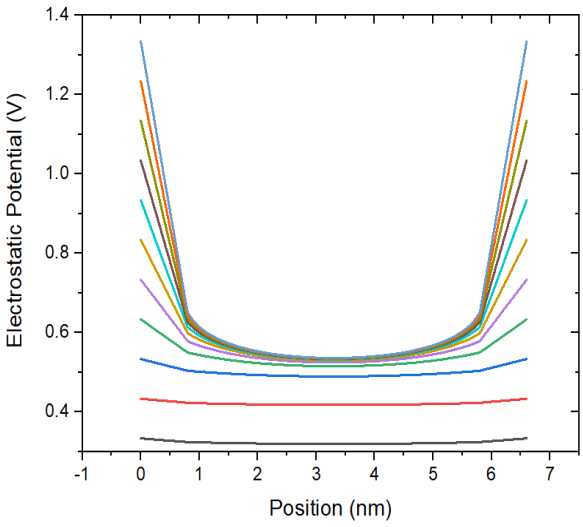

Fig 5. Position vs. Potential graph which is solved numerically when $\mathbf{V_{gs}} = 0\sim1\text{V}$.

As gate voltage increases, potential in Oxide layer increases much faster than that of in Silicon layer. When gate voltage becomes close to 1V, there are almost no changes of potential in Silicon. Most of changes are appear in Oxide layer as theory.

b) Integrated Electron Density ($\mathbf{V_{gs}} = \mathbf{0V \sim 1V}$)

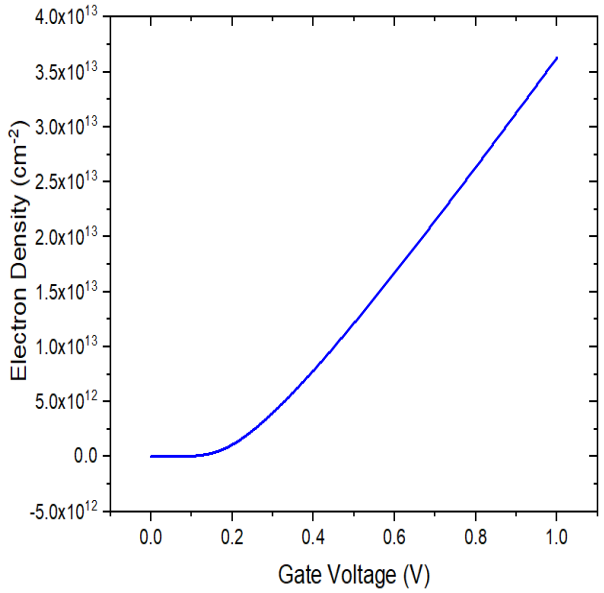

Fig 6. Gate voltage vs. integrated electron density which is solved numerically for $\mathbf{V_{gs}}$ = 0~1V.

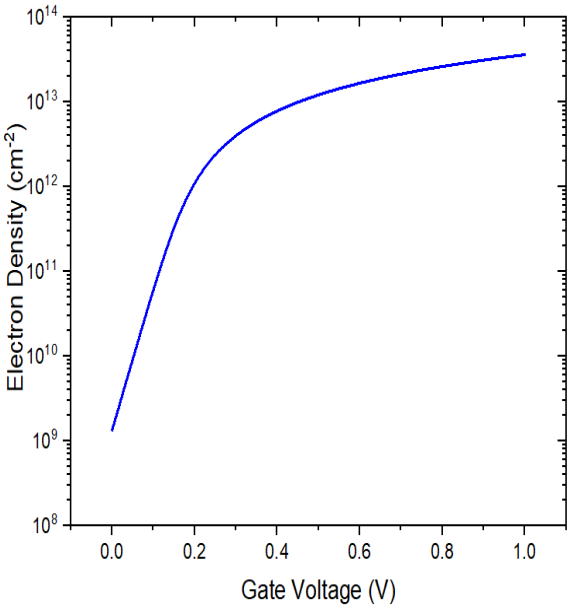

Fig 7. Gate voltage vs. integrated electron density log scaled graph for $\mathbf{V_{gs}}$ = 0~1V.