

RGB LED, 2x switches, 1x button, E-STOP



## BOARD I/O

24 channels  
5V/3.3V  
I/O



### GPIO

16 channels  
+/-10V diff.  
pair inputs



### ANALOG INPUTS

8 full inverters



### DRIVE OUTPUTS

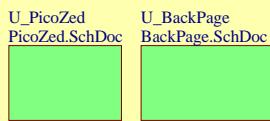
Quadrature  
input (A,B,Z)



### ENCODER

# PicoZed

7030



### JTAG



### ETHERNET



### USB OTG



### USB UART



Power inputs  
to board



24V



VDRIVE

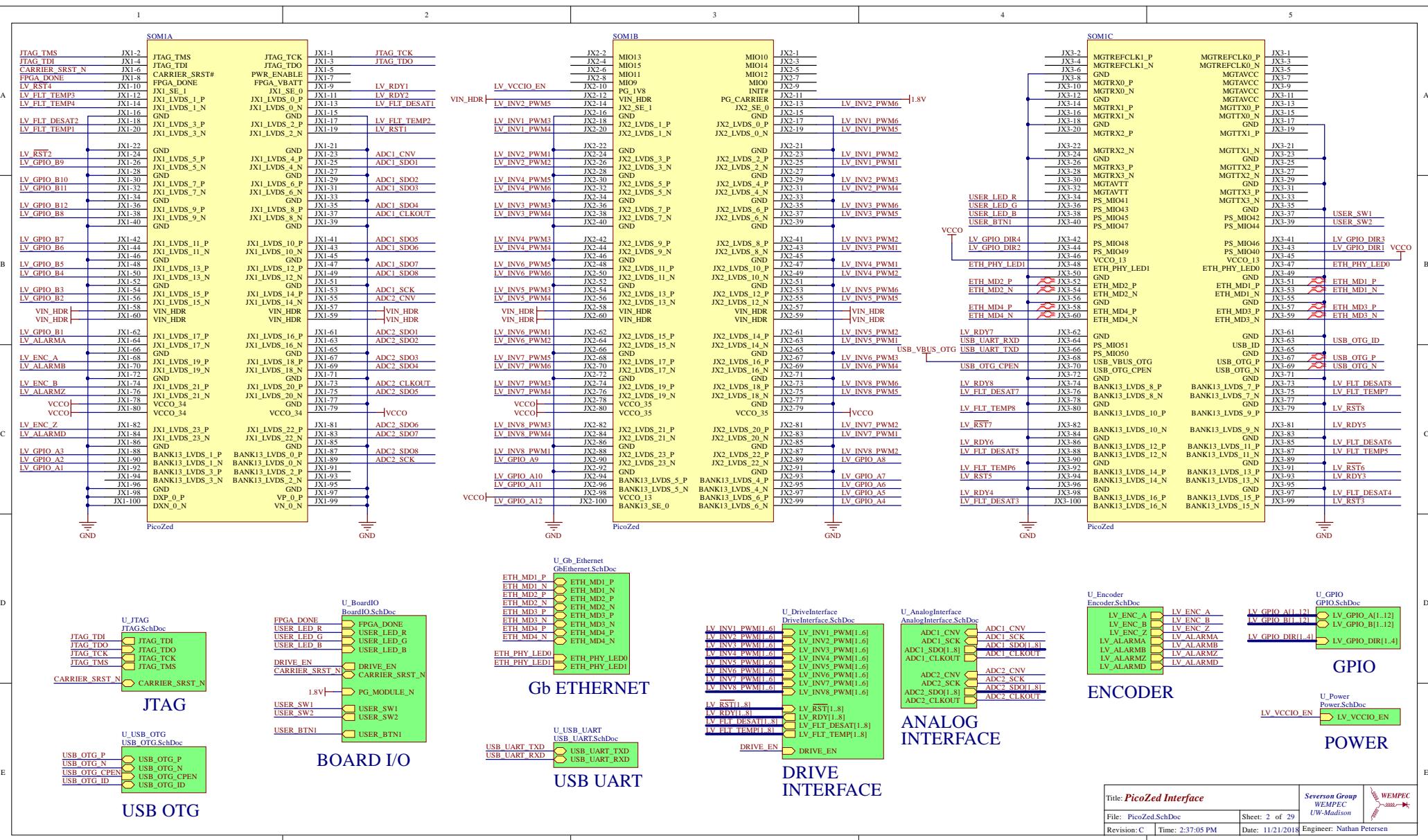
## POWER

-15V +15V 5V 3.3V 2.048V 1.8V

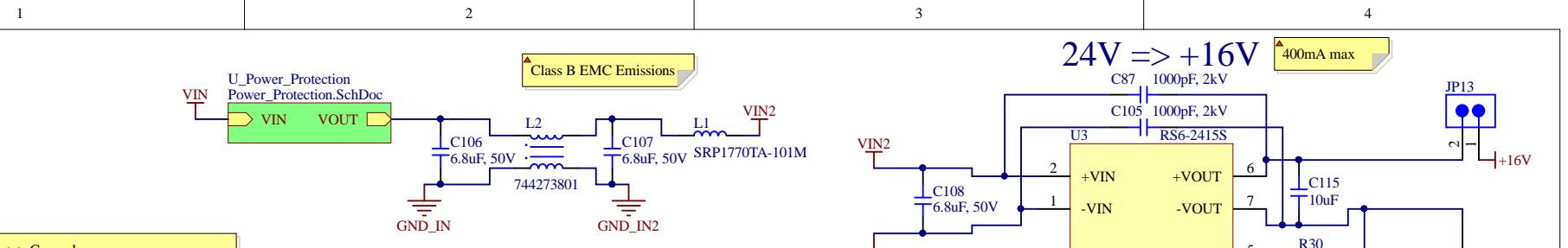
VDRIVE

Title: <b>AMDC</b>		Severson Group WEMPEC UW-Madison
File: <b>AMDC.SchDoc</b>	Sheet: 1 of 29	
Revision: C	Time: 2:37:05 PM	
Date: 11/21/2018		Engineer: Nathan Petersen

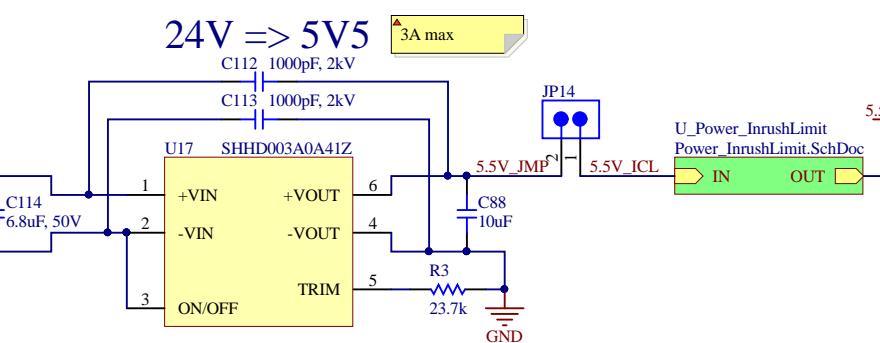
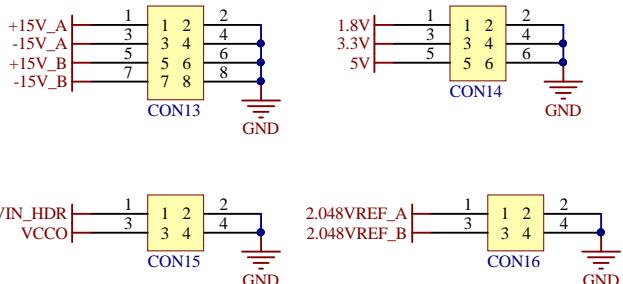




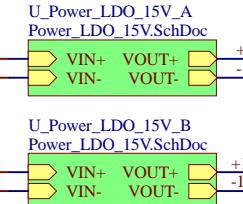
Title: PicoZed Interface		Severson Group	WEMPEC
File: PicoZed.SchDoc		Sheet: 2 of 29	
Revision: C		Time: 2:37:05 PM	Date: 11/21/2018
			Engineer: Nathan Petersen



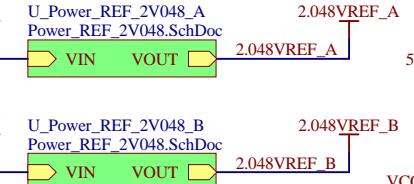
## VOLTAGE HEADERS



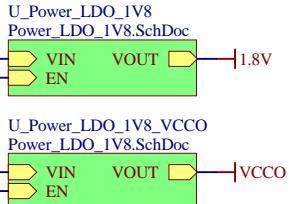
## +/-15V LDOs 200mA max each



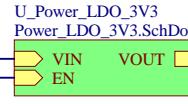
## 2.048V REF 25mA max



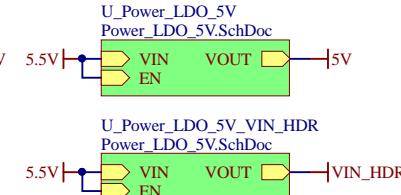
## 1.8V LDOs 3A max each



## 3.3V LDO 3A max each



## 5V LDOs 3A max each



Title: **Power**

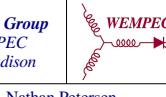
File: Power.SchDoc

Sheet: 3 of 29

Revision: C Time: 2:37:06 PM

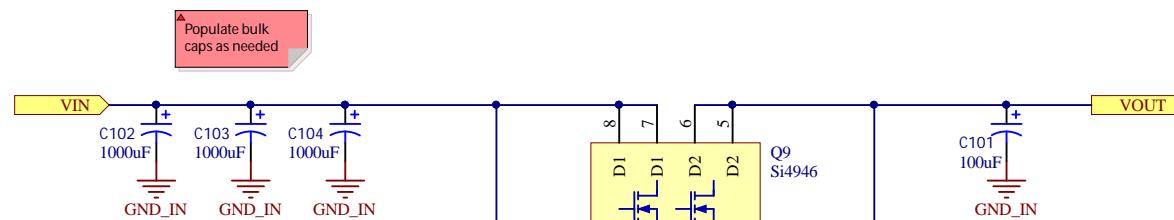
Date: 11/21/2018

Severson Group  
WEMPEC  
UW-Madison



Engineer: Nathan Petersen

A



B

**RANGE: 20V - 34V**

$R_1 + R_2 = 3mV / 100nA = 30k$   
 $R_3 = 2 \cdot 3mV / 10nA \cdot (20V - 0.5V) = 1.17M$

Closest 1% val:  $R_3 = 1.15M$

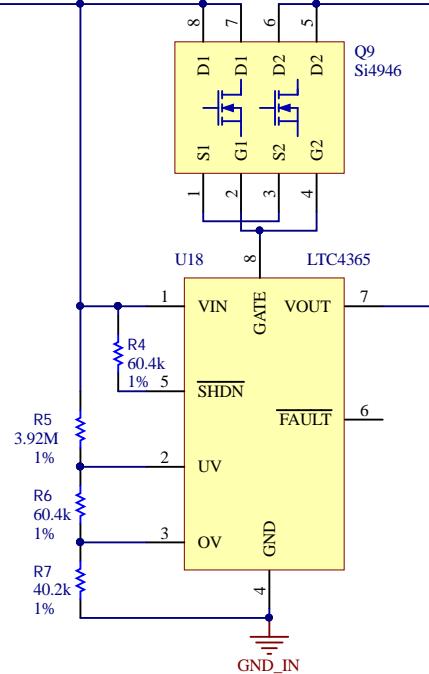
$R_1 = (30k + 1.15M) / (2 \cdot 34V) \approx 17k$

$R_2 = 30k - 17k \approx 13k$

$R_1=243K$   
 $R_2=57.6k$   
 $R_3=7.5M$

$OV = (R_1+R_2+R_3)/2 \cdot R_1 = 16.04V$   
 $UV = ((R_3/2) \cdot (R_1+R_2)) + 0.5 = 13V$

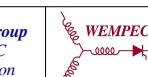
C



D

Title: **Power Protection**File: **Power\_Protection.SchDoc**Sheet: **4 of 29**Revision: **C** Time: **2:37:06 PM**Date: **11/21/2018**

**Severson Group**  
**WEMPEC**  
**UW-Madison**



A

A

B

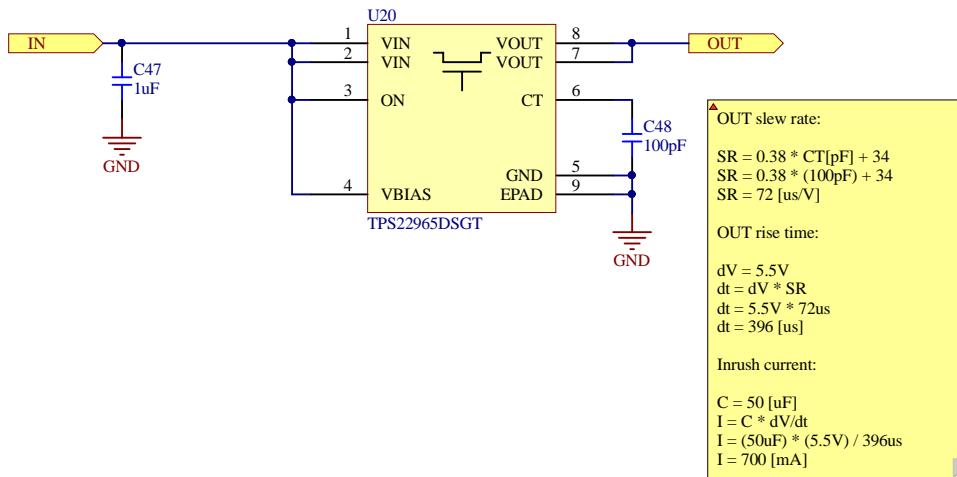
B

C

C

D

D

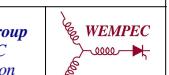


Title: **Inrush Current Limiter**

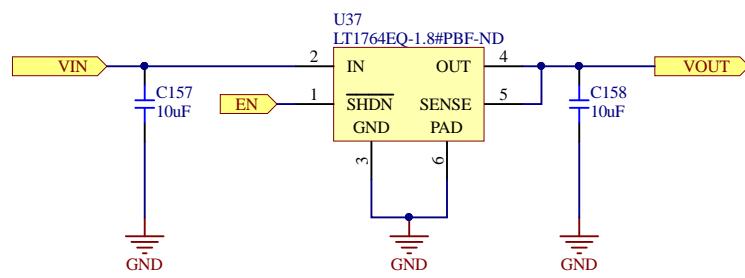
File: Power\_InrushLimit.SchDoc Sheet: 5 of 29

Revision: C Time: 2:37:06 PM Date: 11/21/2018

Severson Group  
WEMPEC  
UW-Madison



Engineer: Nathan Petersen

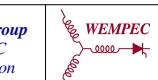


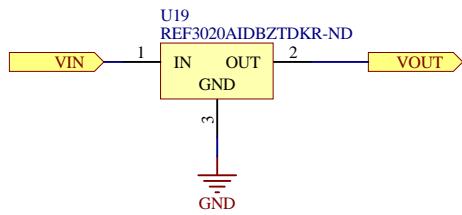
Title: ***1.8V LDO***

File: ***Power\_LDO\_1V8.SchDoc*** Sheet: ***6 of 29***

Revision: ***C*** Time: ***2:37:06 PM*** Date: ***11/21/2018***

***Severson Group***  
***WEMPEC***  
***UW-Madison***





Title: **2.048V Reference**

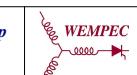
File: Power\_REF\_2V048.SchDoc

Sheet: **7** of 29

Revision: C Time: 2:37:06 PM

Date: 11/21/2018

*Severson Group*  
WEMPEC  
UW-Madison

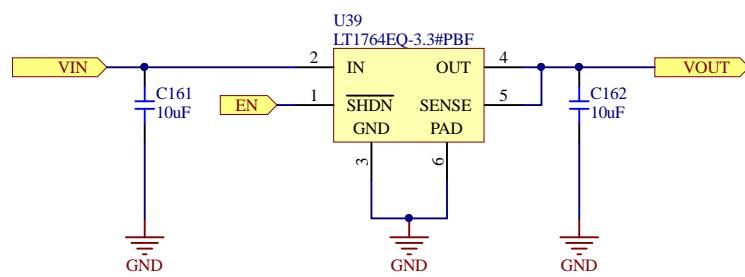
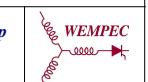


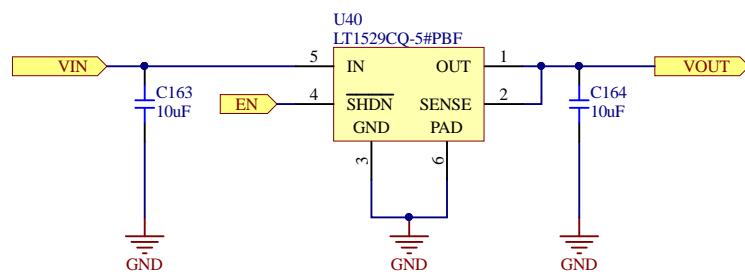
A

B

C

D

Title: **3.3V LDO**File: **Power\_LDO\_3V3.SchDoc** Sheet: **8 of 29**Revision: **C** Time: **2:37:06 PM**Date: **11/21/2018** Engineer: **Nathan Petersen**
**Severson Group**  
**WEMPEC**  
**UW-Madison**


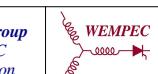


Title: **5V LDO**

File: Power\_LDO\_5V.SchDoc Sheet: **9** of **29**

Revision: **C** Time: **2:37:06 PM** Date: **11/21/2018**

*Severson Group*  
WEMPEC  
UW-Madison



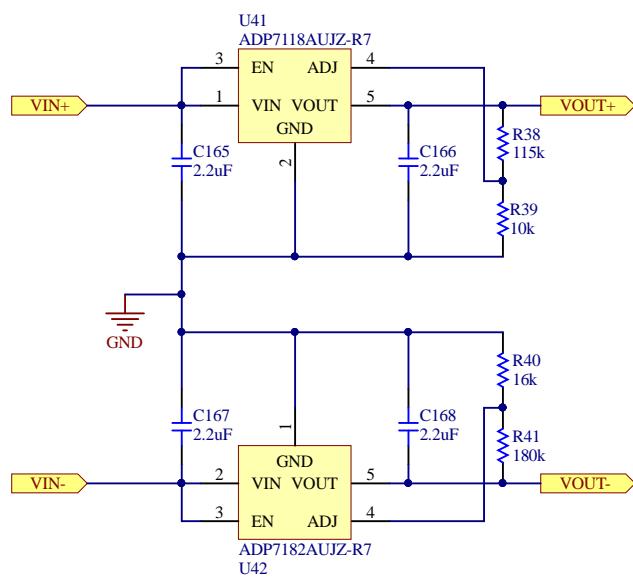
Engineer: Nathan Petersen

A

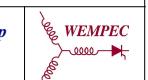
B

C

D

Title: **+/-15V LDO**File: **Power\_LDO\_15V.SchDoc** | Sheet: **10 of 29**Revision: **C** | Time: **2:37:06 PM**Date: **11/21/2018**

**Severson Group**  
**WEMPEC**  
**UW-Madison**



A

A

B

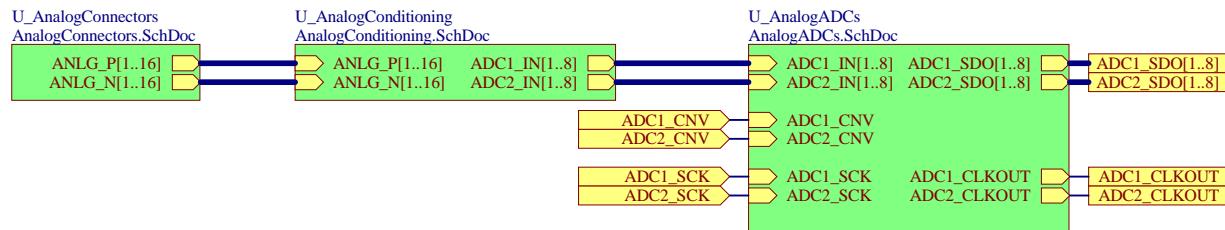
B

C

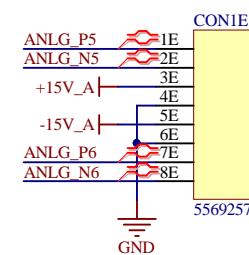
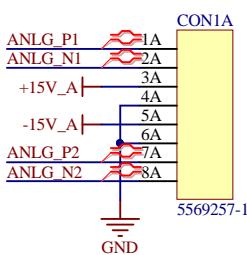
C

D

D

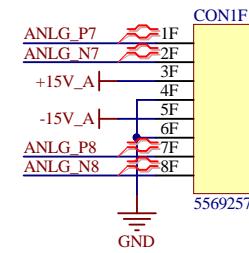
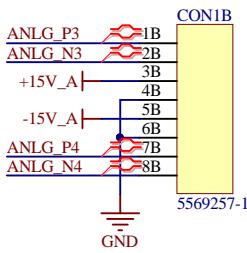


A

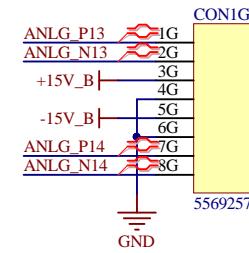
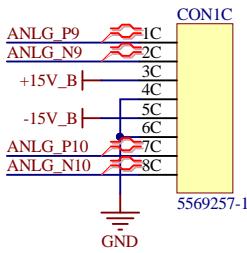


B

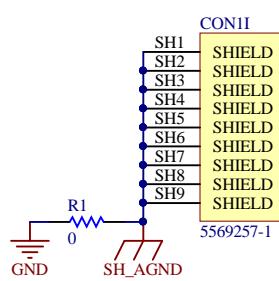
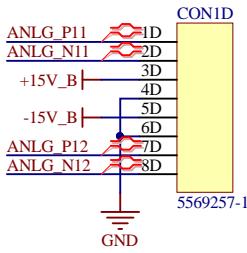
ANLG\_P[1..16] ANLG\_P[1..16]  
 ANLG\_N[1..16] ANLG\_N[1..16]



C



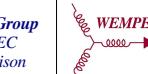
D

Title: **Analog RJ45 Connectors**

File: AnalogConnectors.SchDoc

Revision: C Time: 2:37:06 PM

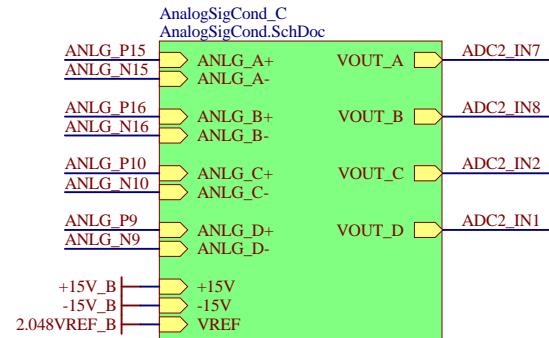
Date: 11/21/2018

Severson Group  
WEMPEC  
UW-Madison

Engineer: Nathan Petersen

A

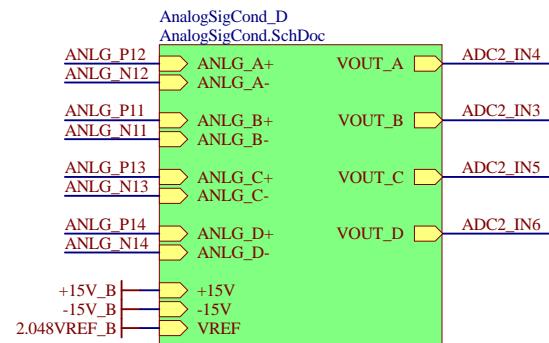
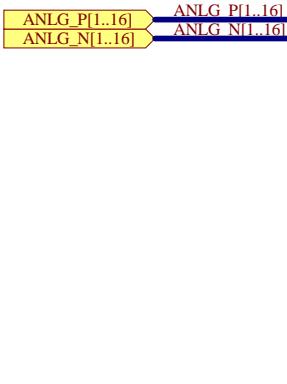
A



ADC1\_IN[1..8]  
ADC2\_IN[1..8]  
ADC2\_IN[1..8]

B

B



C

C

D

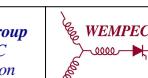
D

Title: **Analog Signal Conditioning**

File: **AnalogConditioning.SchDoc** Sheet: **13 of 29**

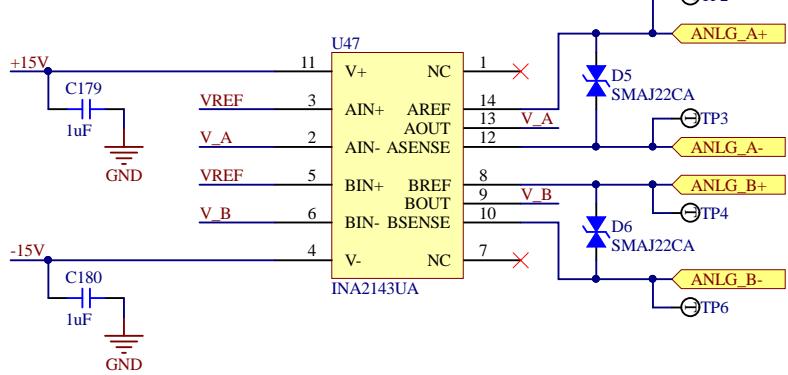
Revision: **C** Time: **2:37:06 PM** Date: **11/21/2018**

**Severson Group**  
**WEMPEC**  
**UW-Madison**

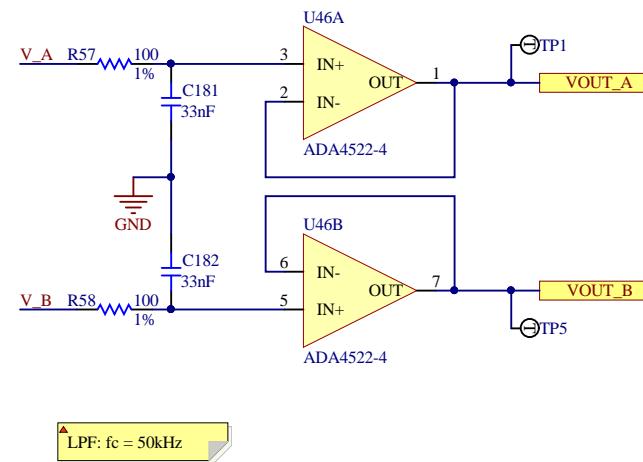


Engineer: **Nathan Petersen**

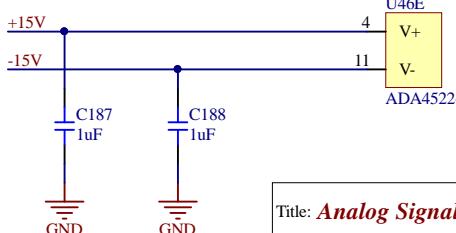
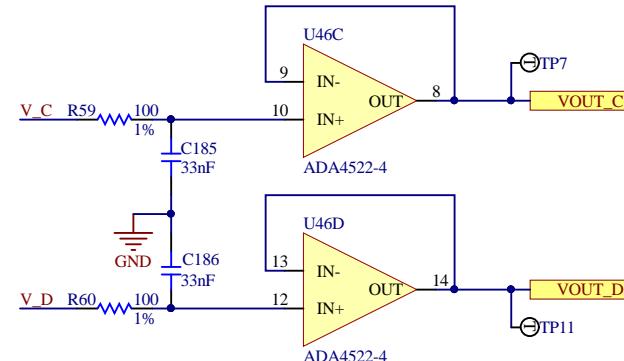
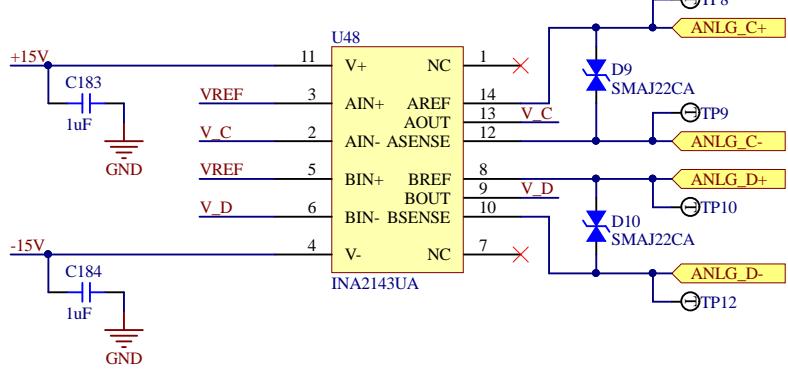
A



B



C



Title: Analog Signal Front-End

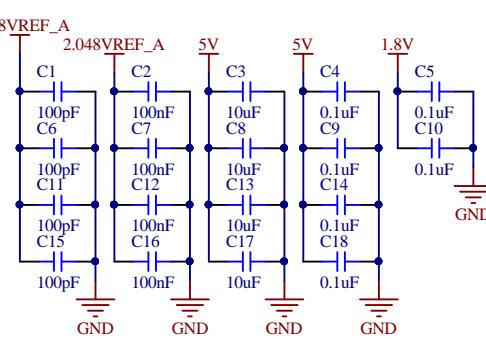
File: AnalogSigCond.SchDoc Sheet: 14 of 29

Revision: C Time: 2:37:06 PM Date: 11/21/2018

Severson Group  
WEMPEC  
UW-MadisonWEMPEC  

Engineer: Nathan Petersen

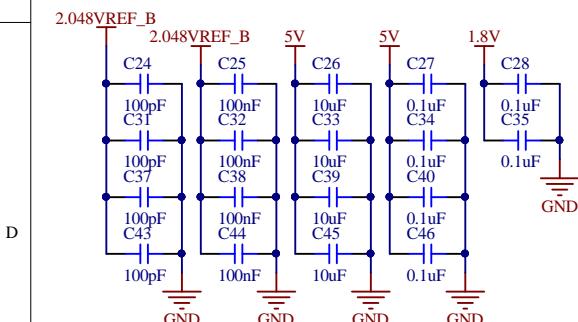
A



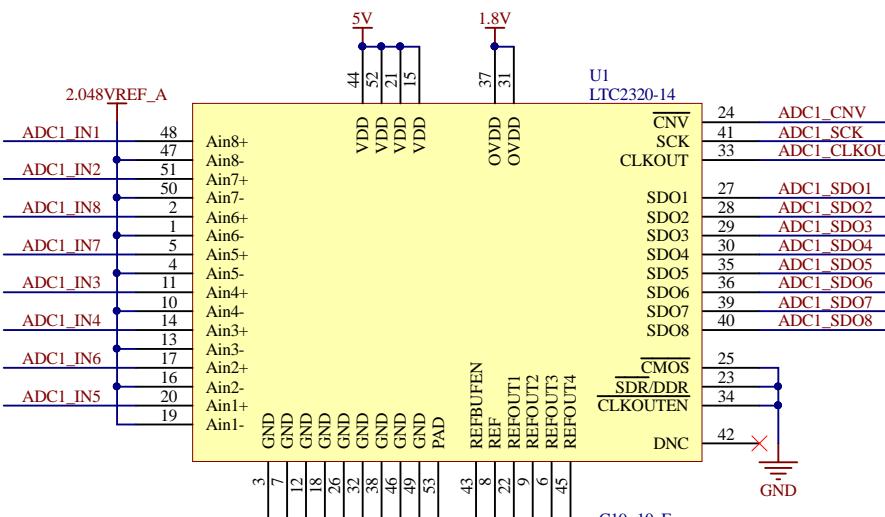
B

**ADC1\_IN[1..8]** **ADC1\_IN[1..8]**  
**ADC2\_IN[1..8]** **ADC2\_IN[1..8]**

C

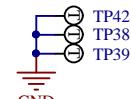


D



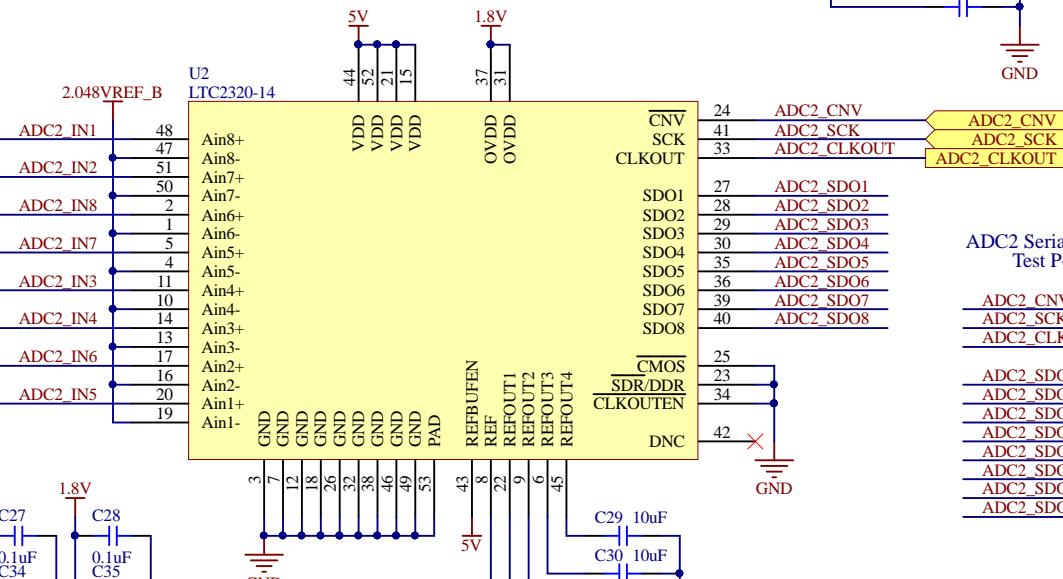
**ADC1 Serial Interface Test Points**

ADC1_CNV	TP14
ADC1_SCK	TP16
ADC1_CLKOUT	TP18
ADC1_SDO1	TP19
ADC1_SDO2	TP20
ADC1_SDO3	TP21
ADC1_SDO4	TP22
ADC1_SDO5	TP23
ADC1_SDO6	TP24
ADC1_SDO7	TP25
ADC1_SDO8	TP26



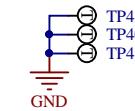
**ADC1\_SDO[1..8]** **ADC1\_SDO[1..8]**  
**ADC2\_SDO[1..8]** **ADC2\_SDO[1..8]**

E



**ADC2 Serial Interface Test Points**

ADC2_CNV	TP27
ADC2_SCK	TP28
ADC2_CLKOUT	TP29
ADC2_SDO1	TP30
ADC2_SDO2	TP31
ADC2_SDO3	TP32
ADC2_SDO4	TP33
ADC2_SDO5	TP34
ADC2_SDO6	TP35
ADC2_SDO7	TP36
ADC2_SDO8	TP37



Title: **ADCs**

File: **AnalogADCs.SchDoc** Sheet: **15 of 29**

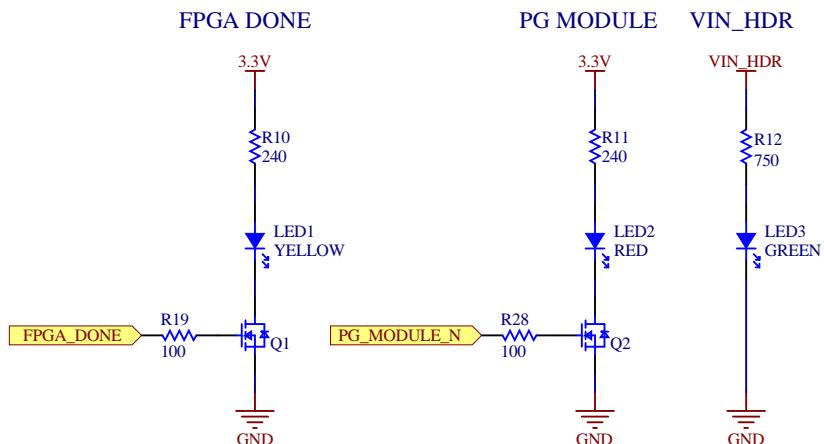
Revision: **C** Time: **2:37:07 PM**

Date: **11/21/2018** Engineer: **Nathan Petersen**

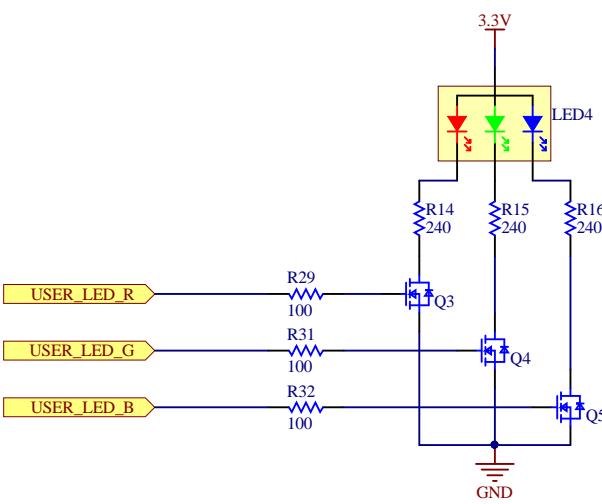
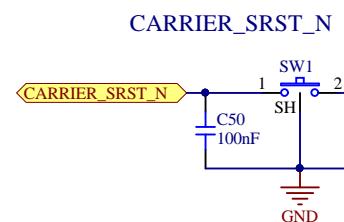
**Severson Group**  
**WEMPEC**  
**UW-Madison**



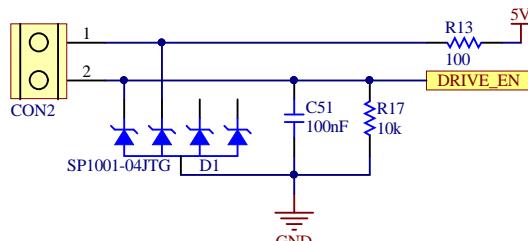
## STATUS LEDS



## CONTROL BUTTON

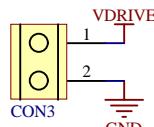


## DRIVE ENABLE (ESTOP)

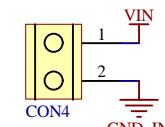


## POWER CONNECTORS

### VDRIVE



### VIN (assumed 24V DC)



Title: **Board I/O**

File: **BoardIO.SchDoc**

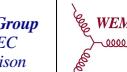
Sheet: **16 of 29**

Revision: **C**

Time: **2:37:07 PM**

Date: **11/21/2018**

Severson Group  
WEMPEC  
UW-Madison



A

A

B

B

C

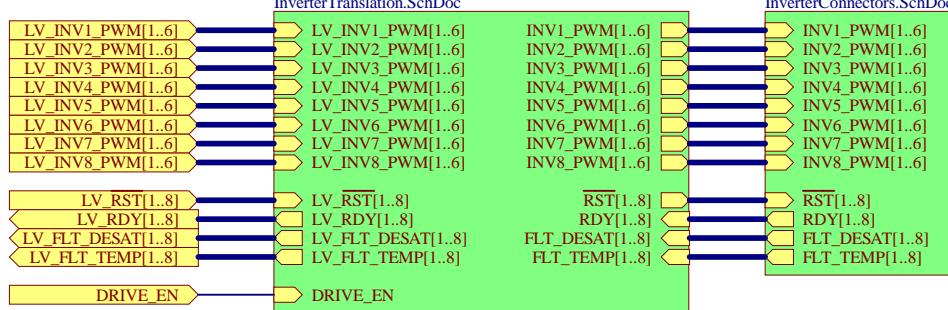
C

D

D

**U\_InverterTranslation**  
InverterTranslation.SchDoc

**U\_InverterConnectors**  
InverterConnectors.SchDoc

Title: **Drive Interface**

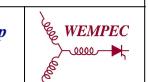
File: DriveInterface.SchDoc

Sheet: 17 of 29

Revision: C Time: 2:37:07 PM

Date: 11/21/2018

**Severson Group**  
WEMPEC  
UW-Madison



1

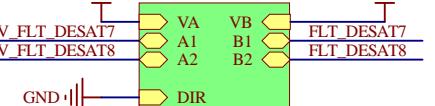
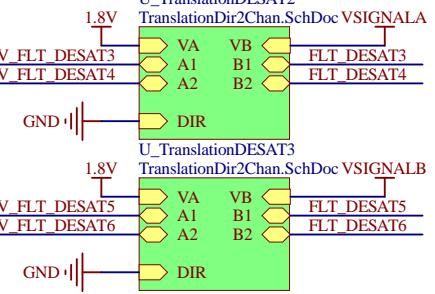
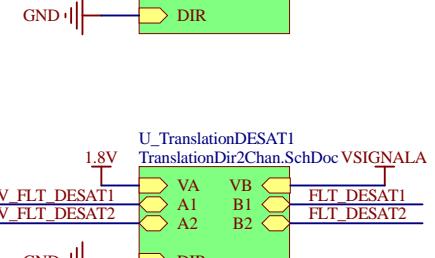
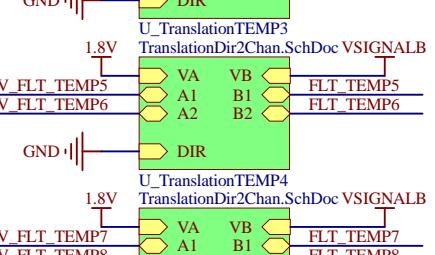
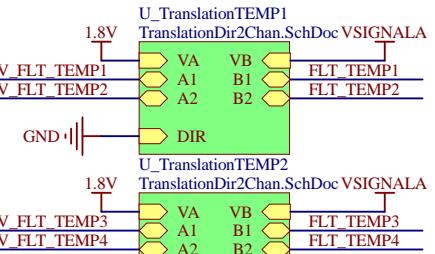
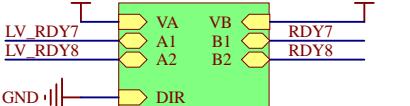
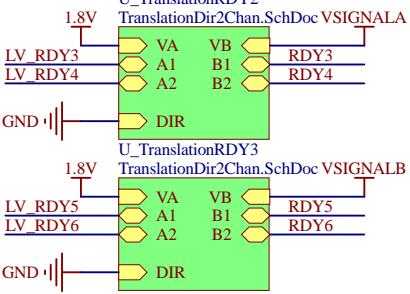
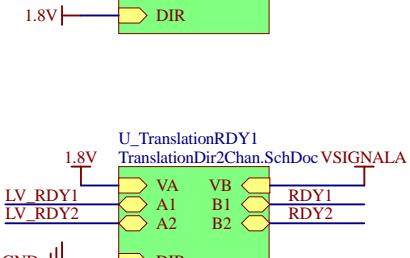
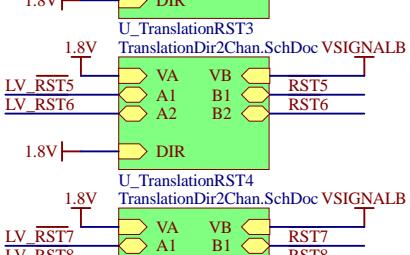
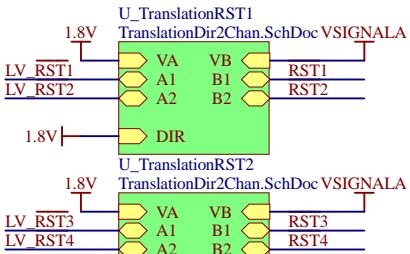
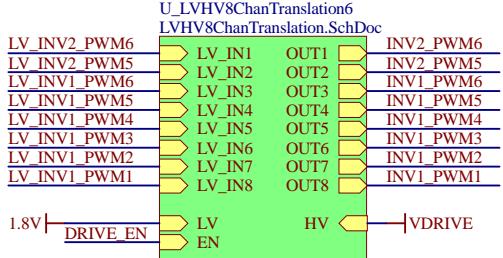
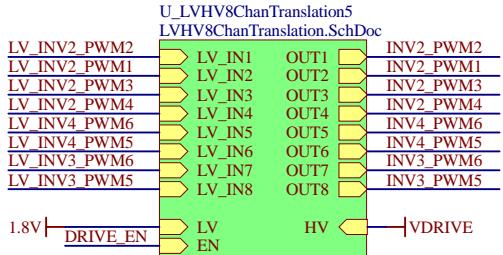
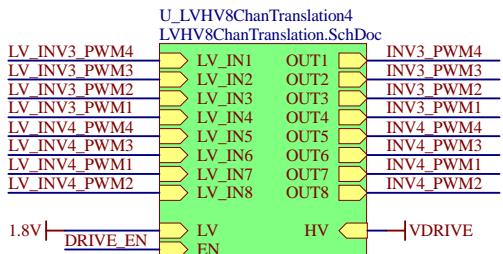
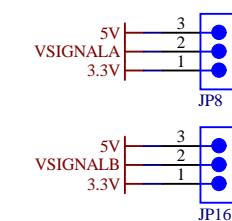
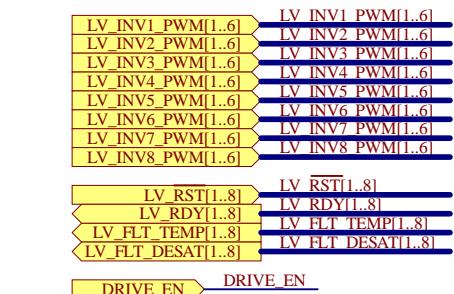
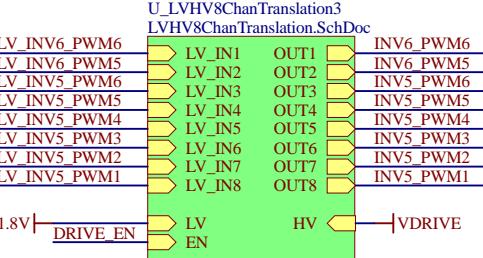
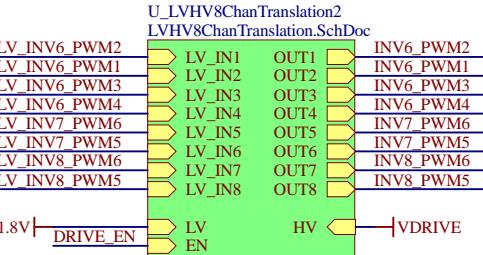
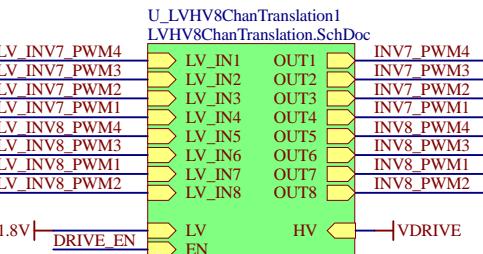
2

3

4

A

A



1

2

3

4

Title: **Inverter Level Translation**Severson Group  
WEMPEC  
UW-Madison

File: InverterTranslation.SchDoc Sheet: 18 of 29

Revision: C Time: 2:37:07 PM Date: 11/21/2018

Engineer: Nathan Petersen

A

A

B

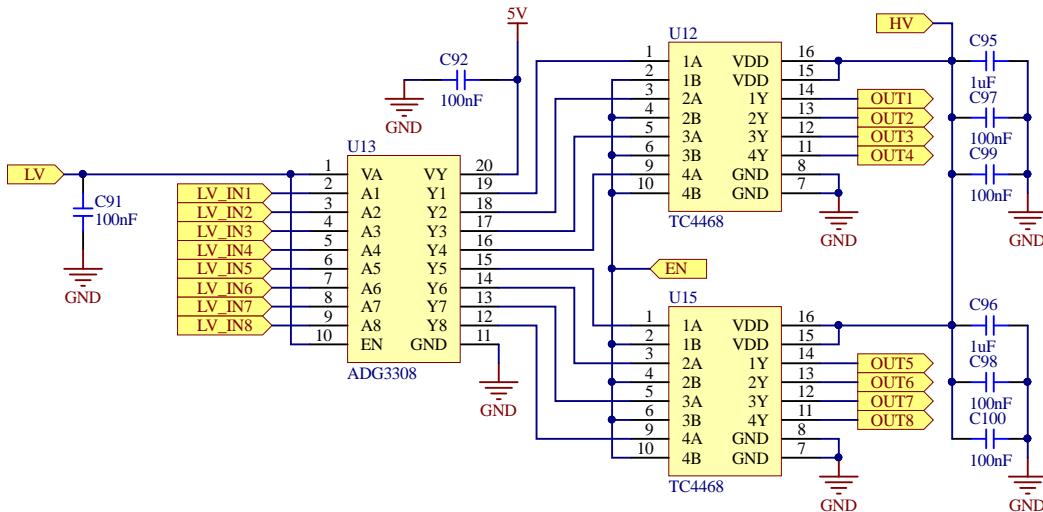
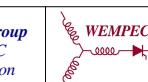
B

C

C

D

D

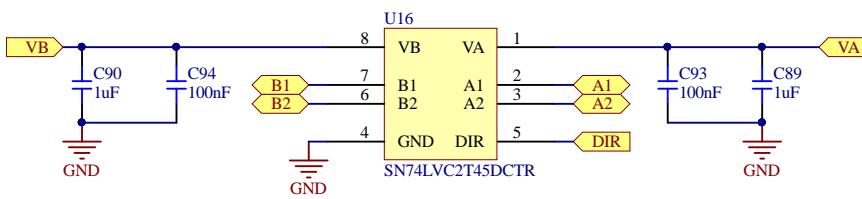
Title: **8-channel LV to HV Translation**File: **LVHF8ChanTranslation.SchDoc** | Sheet: **19 of 29**Revision: **C** | Time: **2:37:07 PM**Date: **11/21/2018** | Engineer: **Nathan Petersen**
**Severson Group**  
**WEMPEC**  
**UW-Madison**


A

B

C

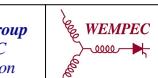
D

Title: **2-Channel Directional Translation**

File: TranslationDir2Chan.SchDoc | Sheet: 20 of 29

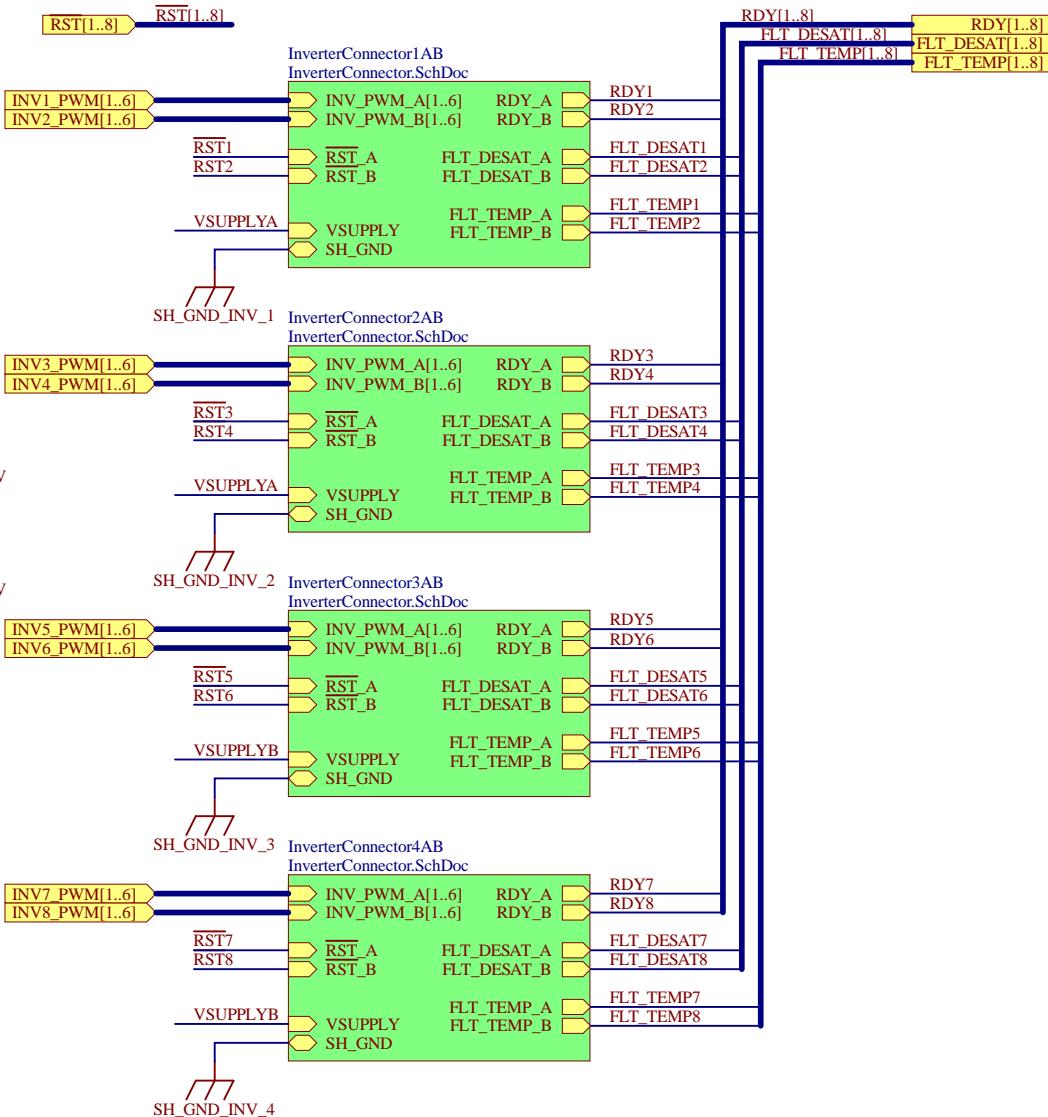
Revision: C | Time: 2:37:07 PM | Date: 11/21/2018

*Severson Group*  
WEMPEC  
UW-Madison



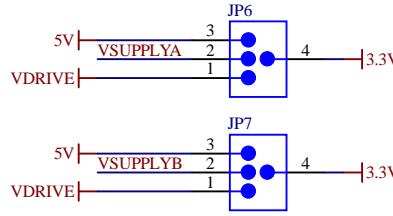
Engineer: Nathan Petersen

A



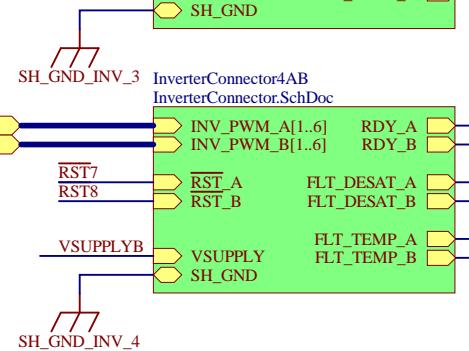
A

B



B

C



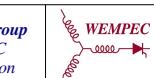
C

D

Title: **Inverter Connectors**

File: InverterConnectors.SchDoc | Sheet: 21 of 29

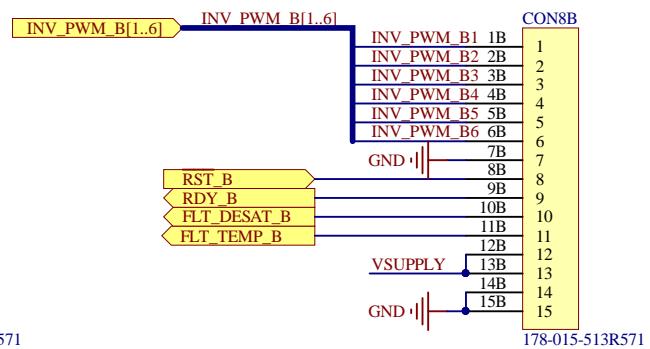
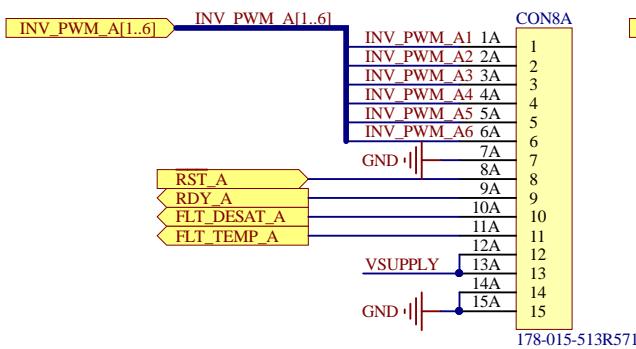
Revision: C | Time: 2:37:08 PM | Date: 11/21/2018

Severson Group  
WEMPEC  
UW-Madison

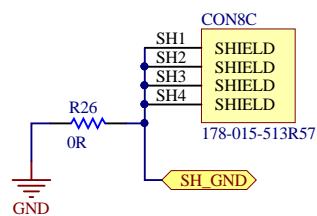
Engineer: Nathan Petersen

A

VSUPPLY



C



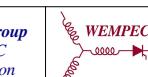
D

Title: **Inverter Connector**

File: InverterConnector.SchDoc Sheet: 22 of 29

Revision: C Time: 2:37:08 PM Date: 11/21/2018

Severson Group  
WEMPEC  
UW-Madison



Engineer: Nathan Petersen

A

A

B

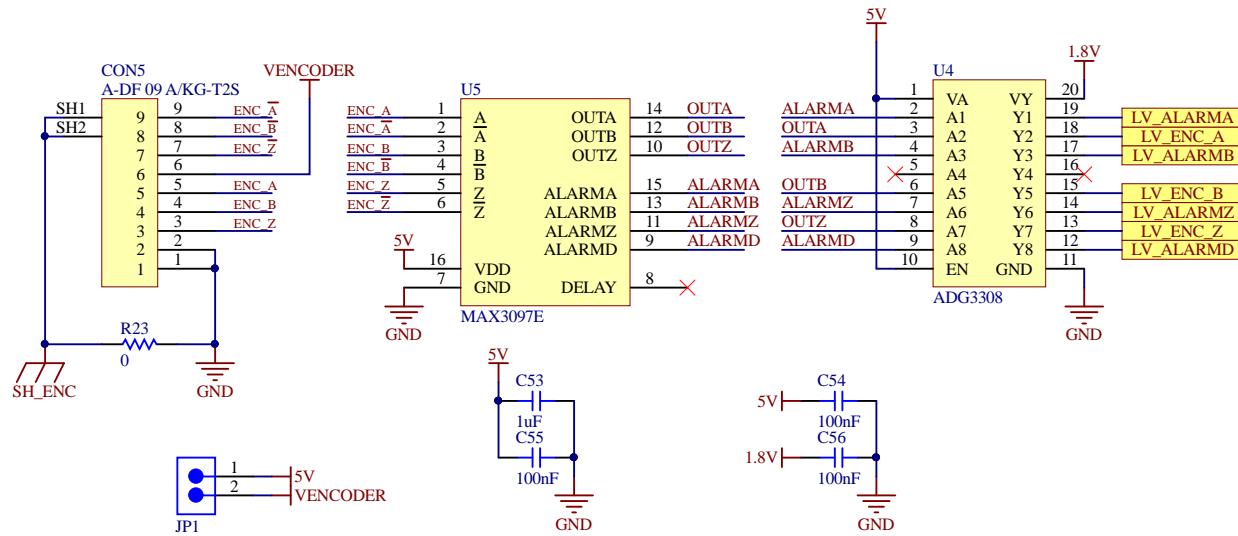
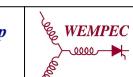
B

C

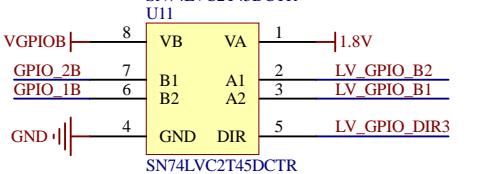
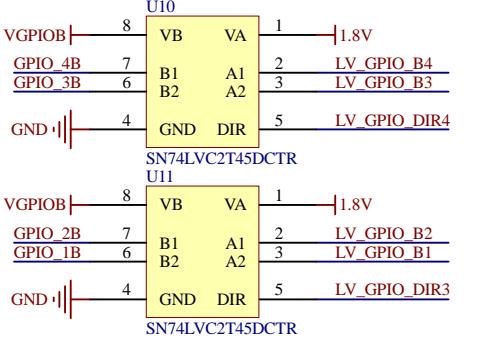
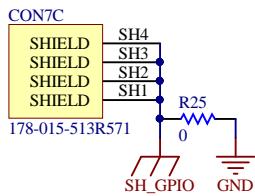
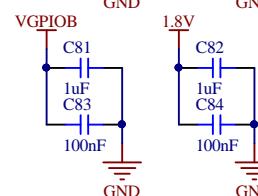
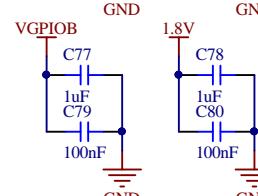
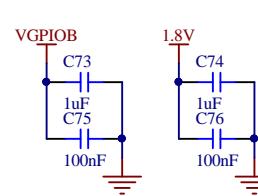
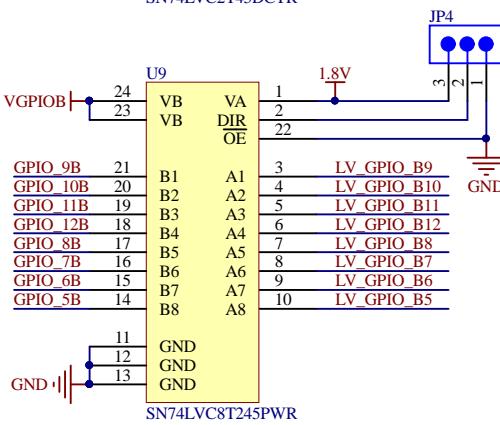
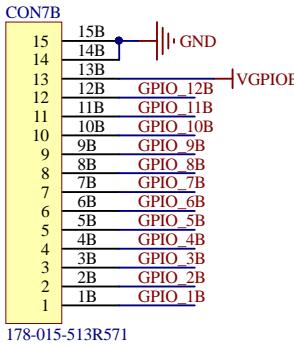
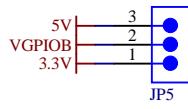
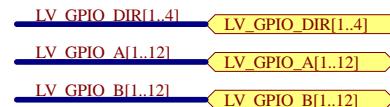
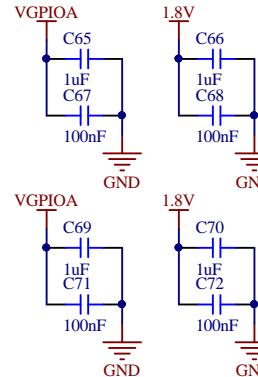
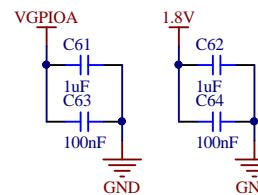
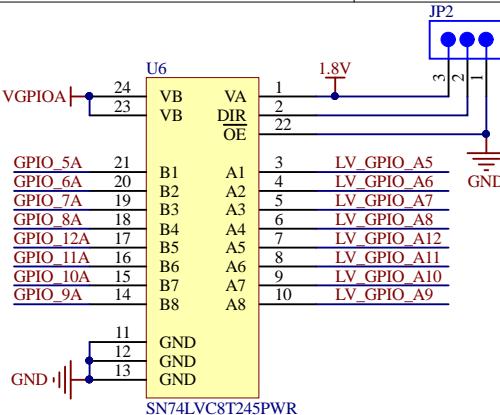
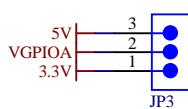
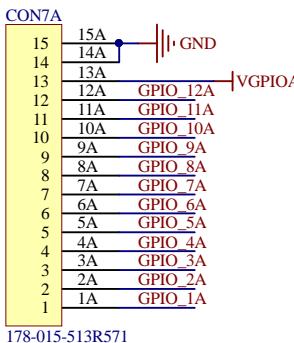
C

D

D

Title: **Encoder**File: **Encoder.SchDoc**Sheet: **23 of 29**Revision: **C** Time: **2:37:08 PM**Date: **11/21/2018**
**Severson Group**  
**WEMPEC**  
**UW-Madison**


A

Title: **GPIO**File: **GPIO.SchDoc**Revision: **C**Sheet: **24** of **29**Time: **2:37:08 PM**Date: **11/21/2018**Severson Group  
WEMPEC  
UW-MadisonEngineer: **Nathan Petersen**

A

A

B

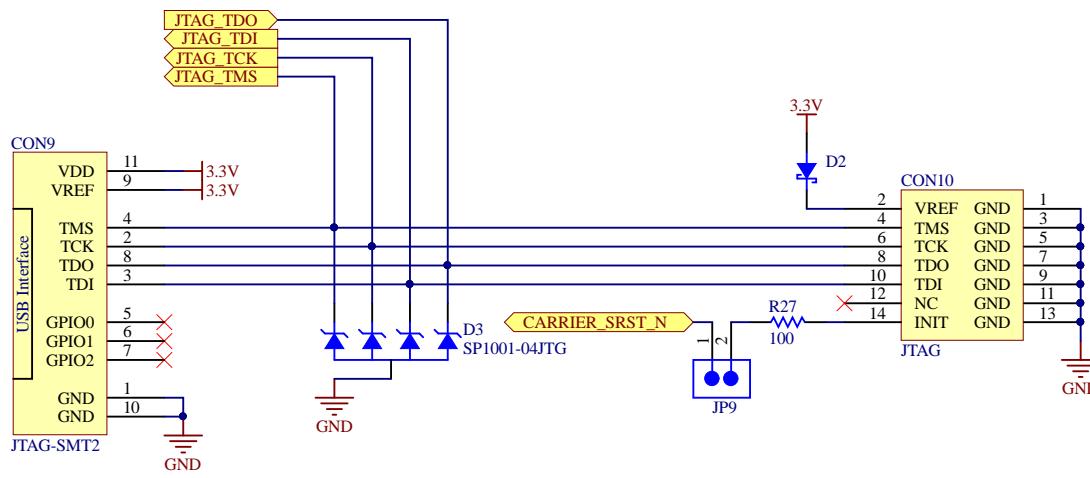
B

C

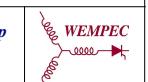
C

D

D

Title: **JTAG**File: **JTAG.SchDoc**Sheet: **25 of 29**Revision: **C** Time: **2:37:08 PM**Date: **11/21/2018**

**Severson Group**  
WEMPEC  
UW-Madison



A

A

B

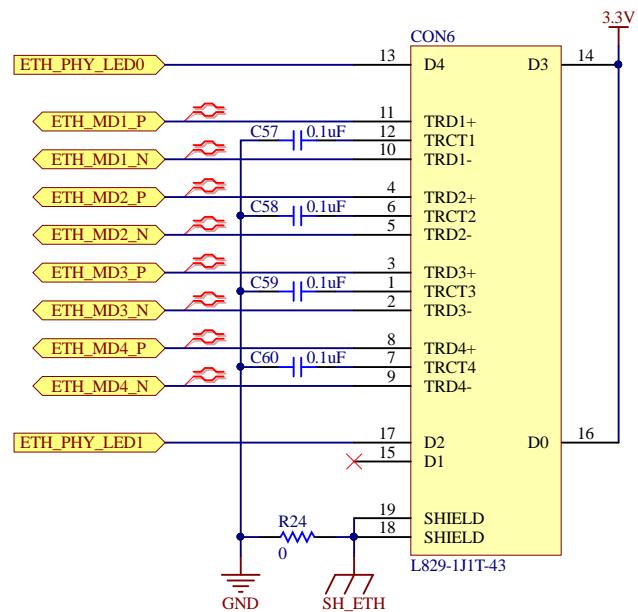
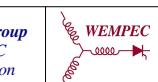
B

C

C

D

D

Title: **SoM Gb Ethernet**File: **GbEthernet.SchDoc**Sheet: **26 of 29**Revision: **C** Time: **2:37:08 PM**Date: **11/21/2018****Severson Group**  
WEMPEC  
UW-MadisonEngineer: **Nathan Petersen**

A

A

B

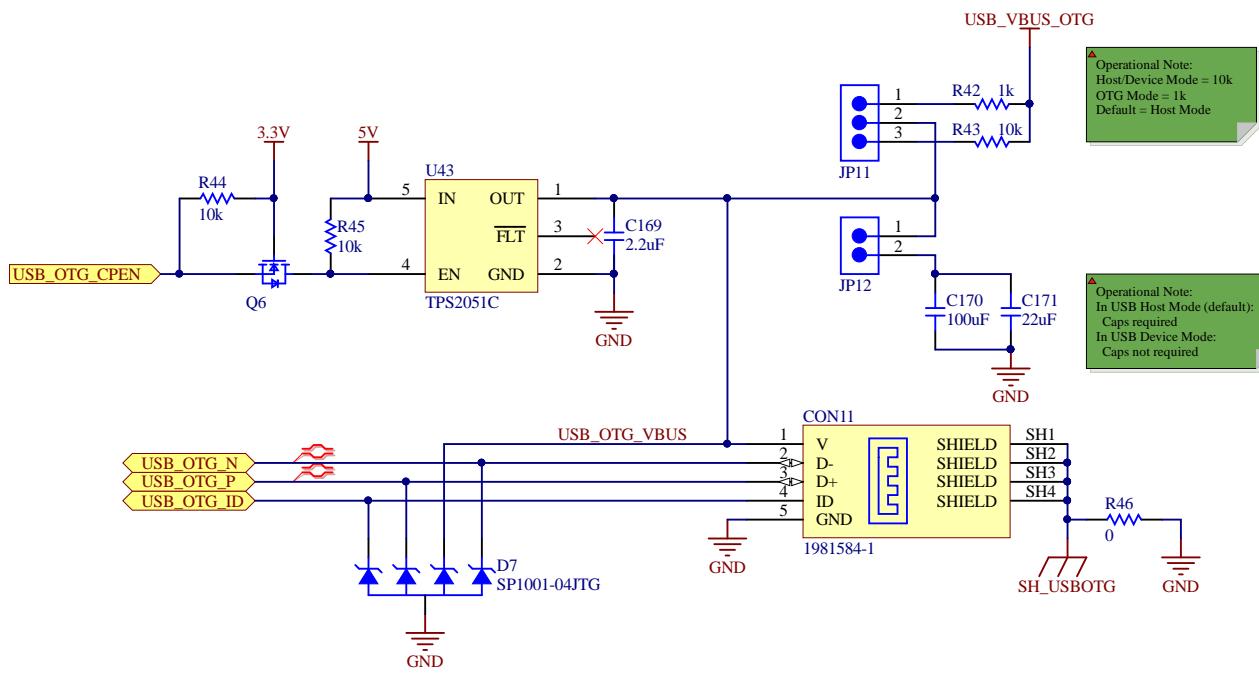
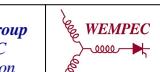
B

C

C

D

D

Title: **USB OTG**File: **USB\_OTG.SchDoc** Sheet: **27 of 29**Revision: **C** Time: **2:37:08 PM** Date: **11/21/2018****Severson Group**  
**WEMPEC**  
**UW-Madison**

A

A

B

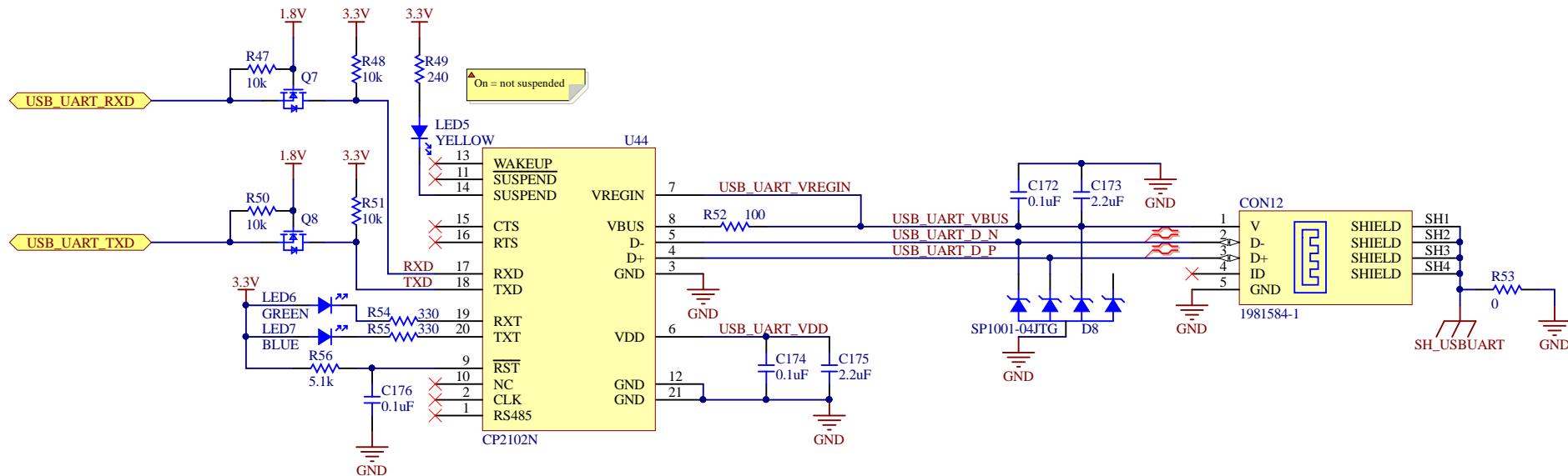
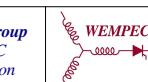
B

C

C

D

D

Title: **USB UART**File: **USB\_UART.SchDoc**Sheet: **28 of 29**Revision: **C** Time: **2:37:08 PM**Date: **11/21/2018**
**Severson Group**  
**WEMPEC**  
**UW-Madison**
Engineer: **Nathan Petersen**

A

B

C

D

**4-40 Screws:****4-40 Standoffs:****Mouting Holes:**