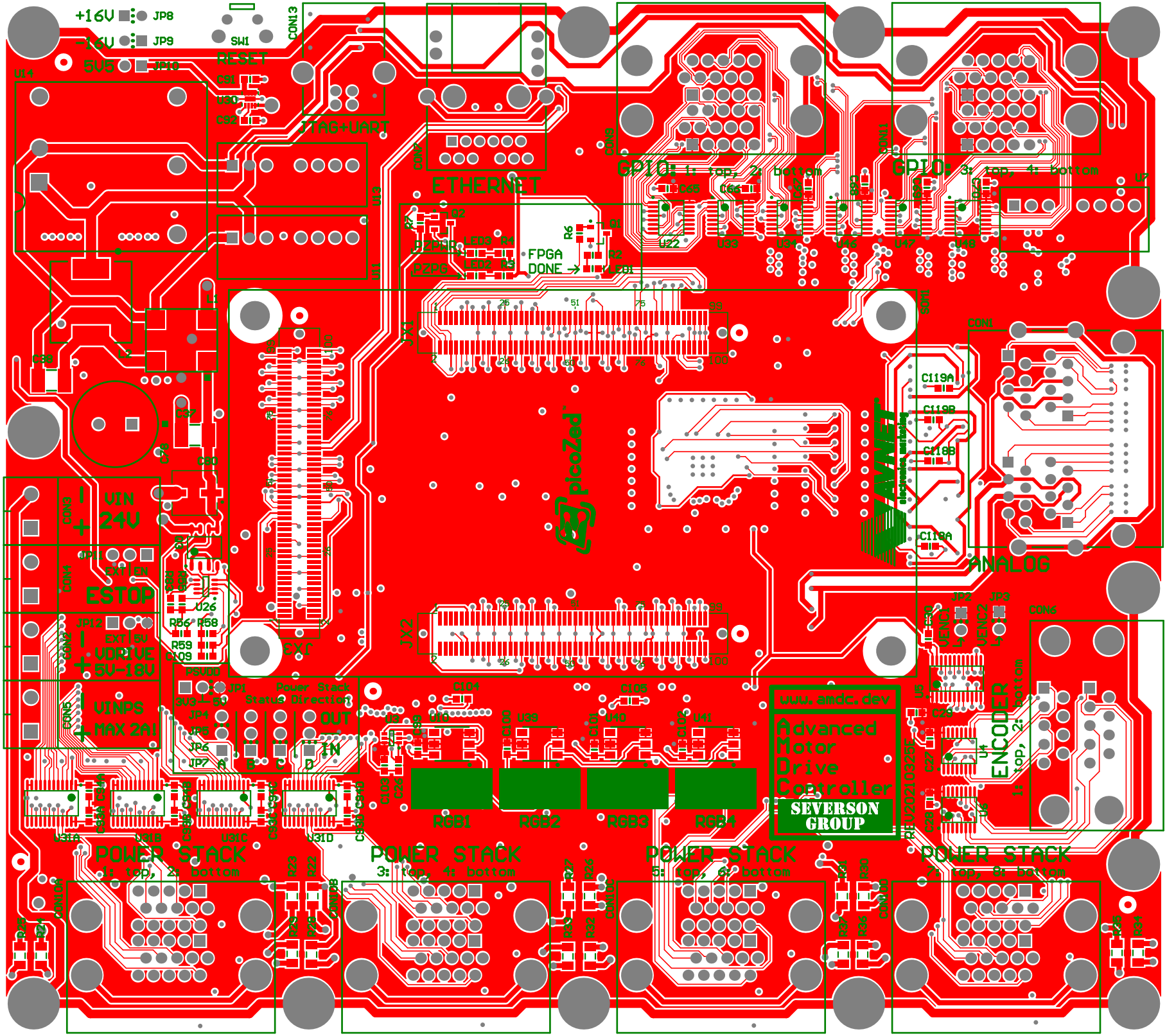
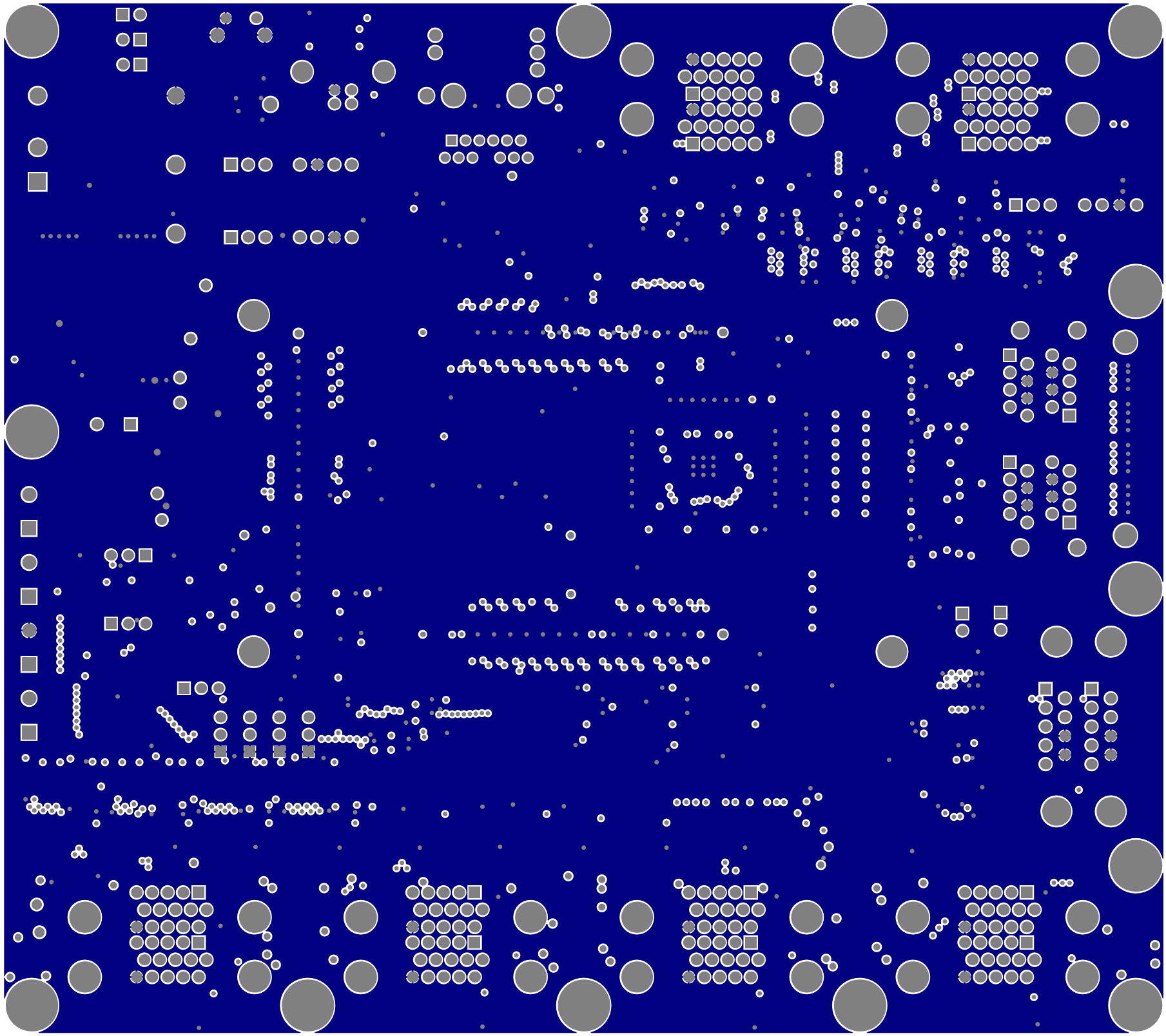
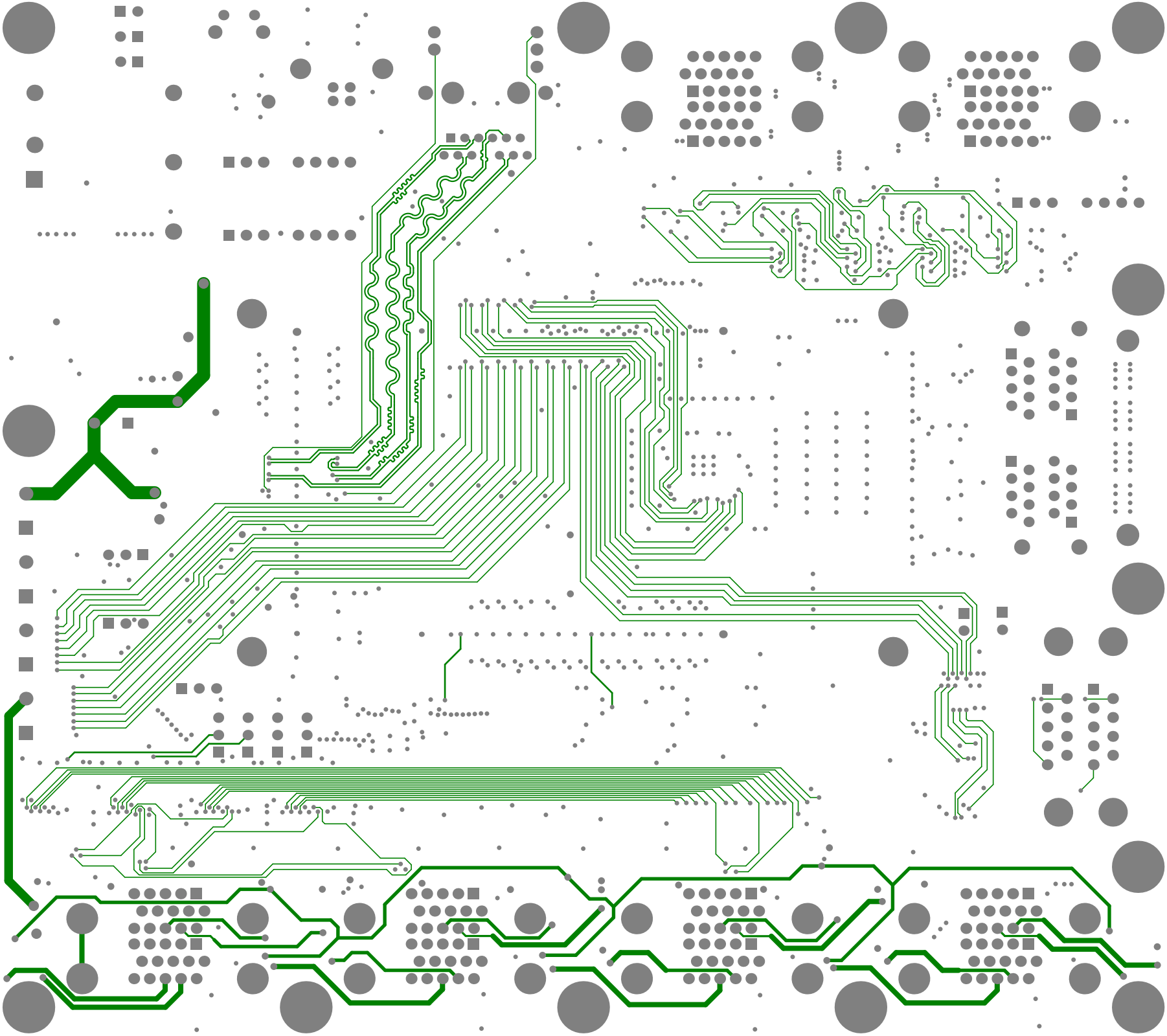
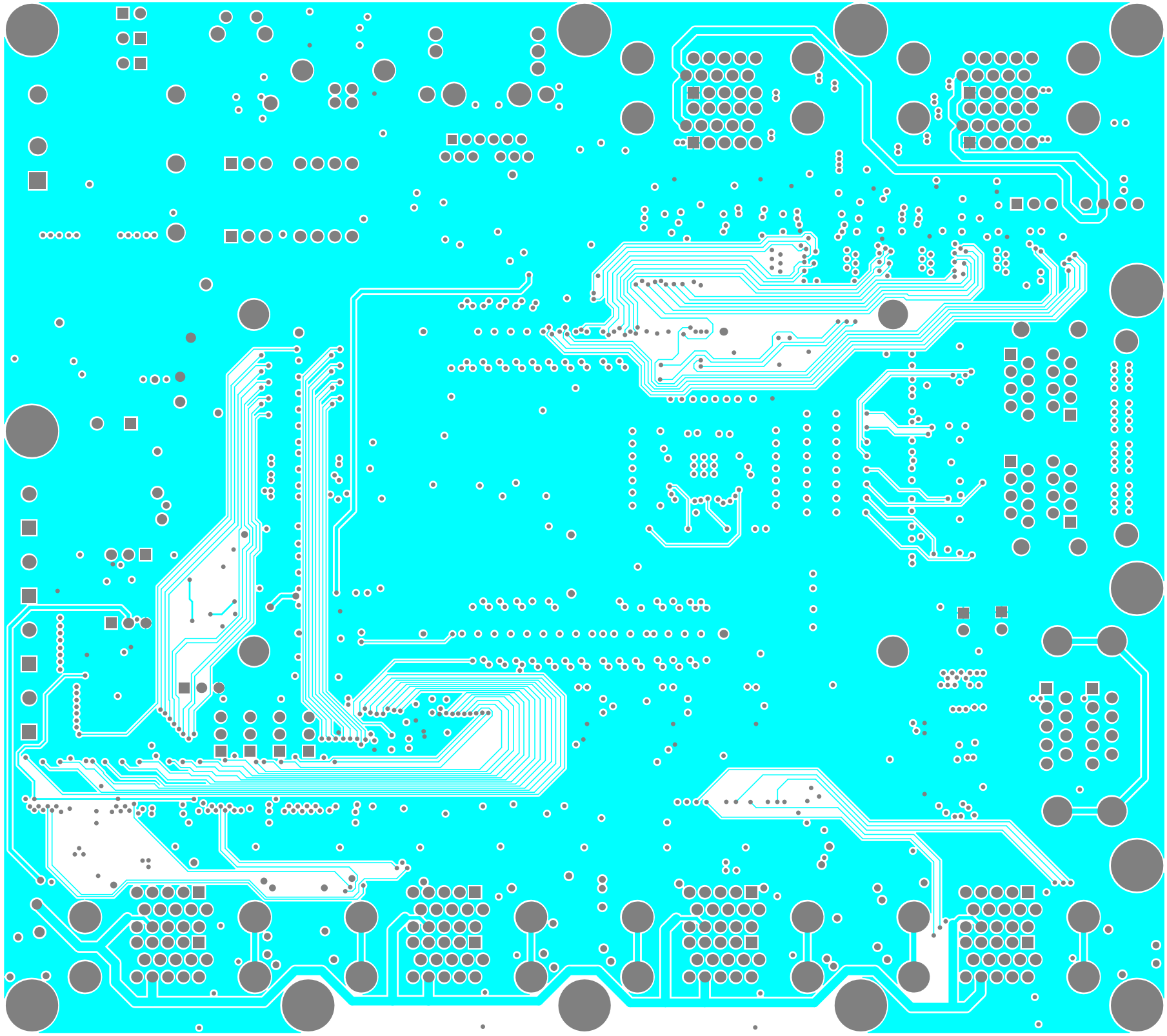
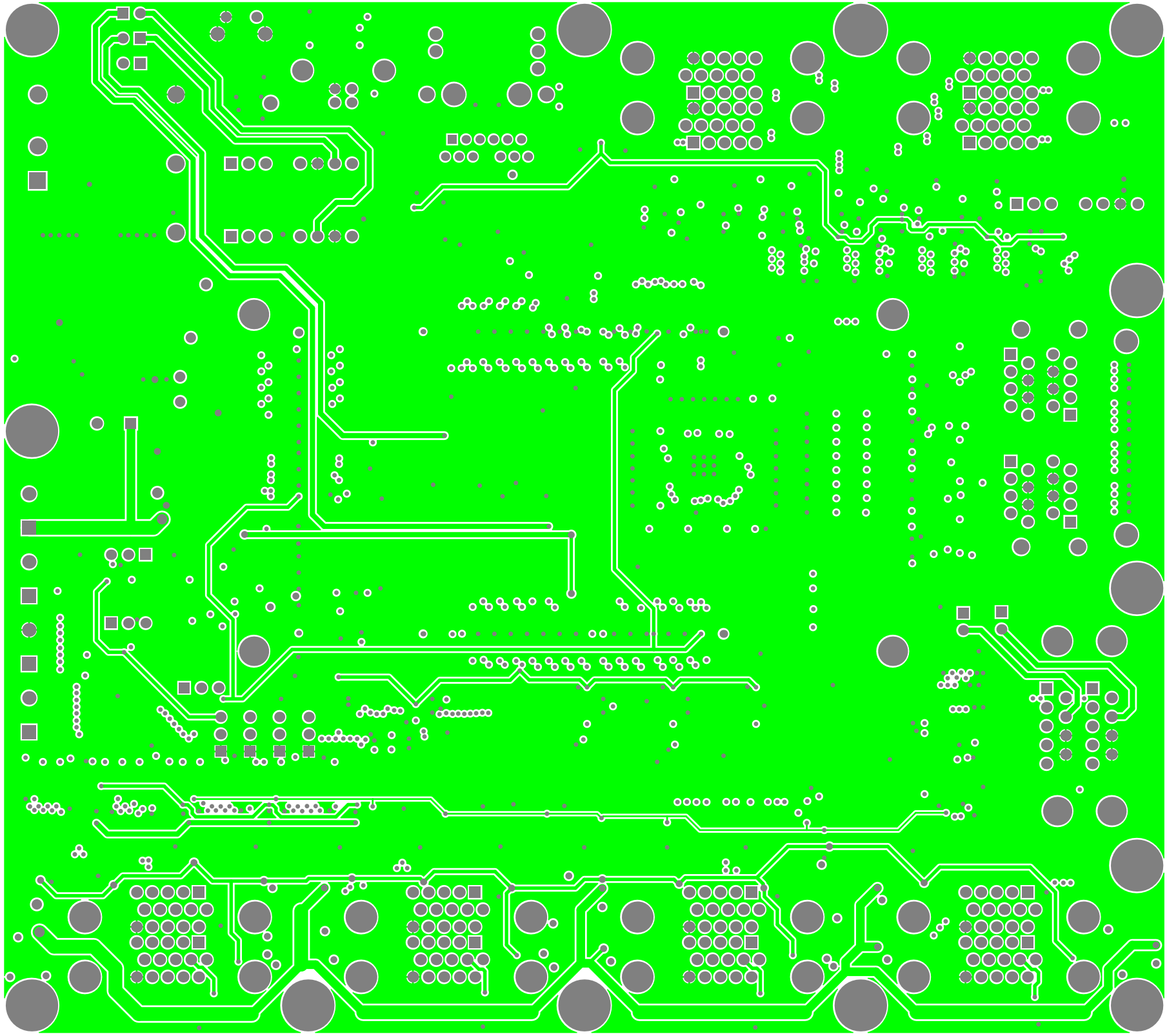

+16V
JP8
-16V
JP9
5V5
JP10
SW1
RESET
JTAG+UART
ETHERNET
GPIO: 1: top, 2: bottom
GPIO: 3: top, 4: bottom
FPGA
DONE
picoZed
JX1
JX2
JX3
VIN
24V
ESTOP
VDRIVE
5V-18V
VINPS
MAX 2A!
Power Stack
Status Direction
OUT
IN
RGB1
RGB2
RGB3
RGB4
www.amdc.dev
Advanced
Motor
Drive
Controller
SEVERSON
GROUP
ANALOG
ENCODER
1: top, 2: bottom
POWER STACK
1: top, 2: bottom
POWER STACK
3: top, 4: bottom
POWER STACK
5: top, 6: bottom
POWER STACK
7: top, 8: bottom









NXP