

4x RGB LEDs, E-STOP



BOARD I/O

A
4x GPIO ports each with 3 diff inputs, 3 diff outputs**GPIO**B
8x channel +/-10V diff. pair inputs**ANALOG INPUTS**C
8x full 3-phase 2-level inverters**DRIVE OUTPUTS**C
2x quadrature input (A,B,Z)**ENCODER**

PicoZed

7030

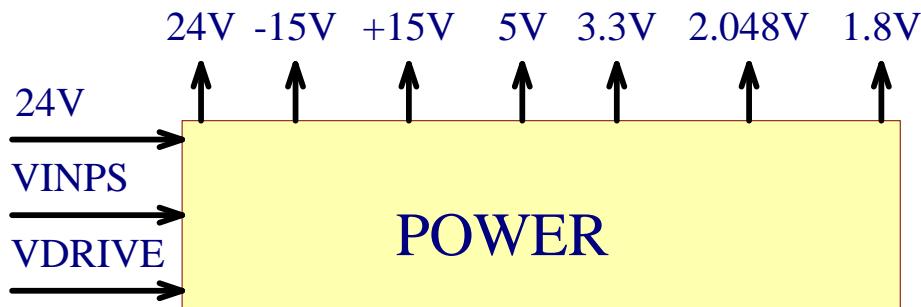
U_PicoZed

PicoZed.SchDoc

JTAG / UART**ETHERNET****EEPROM**

D

Power inputs to board



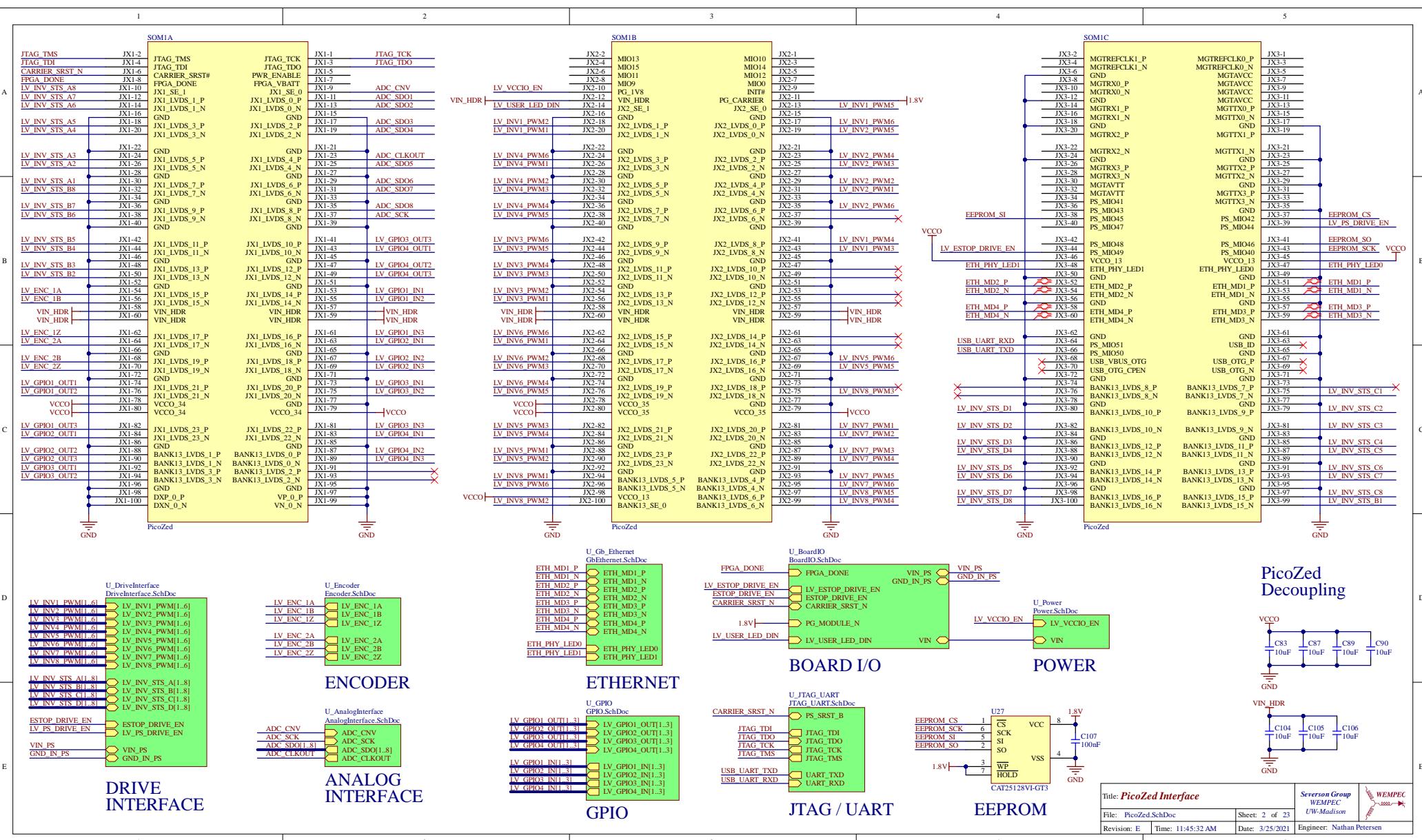
U_BackPage

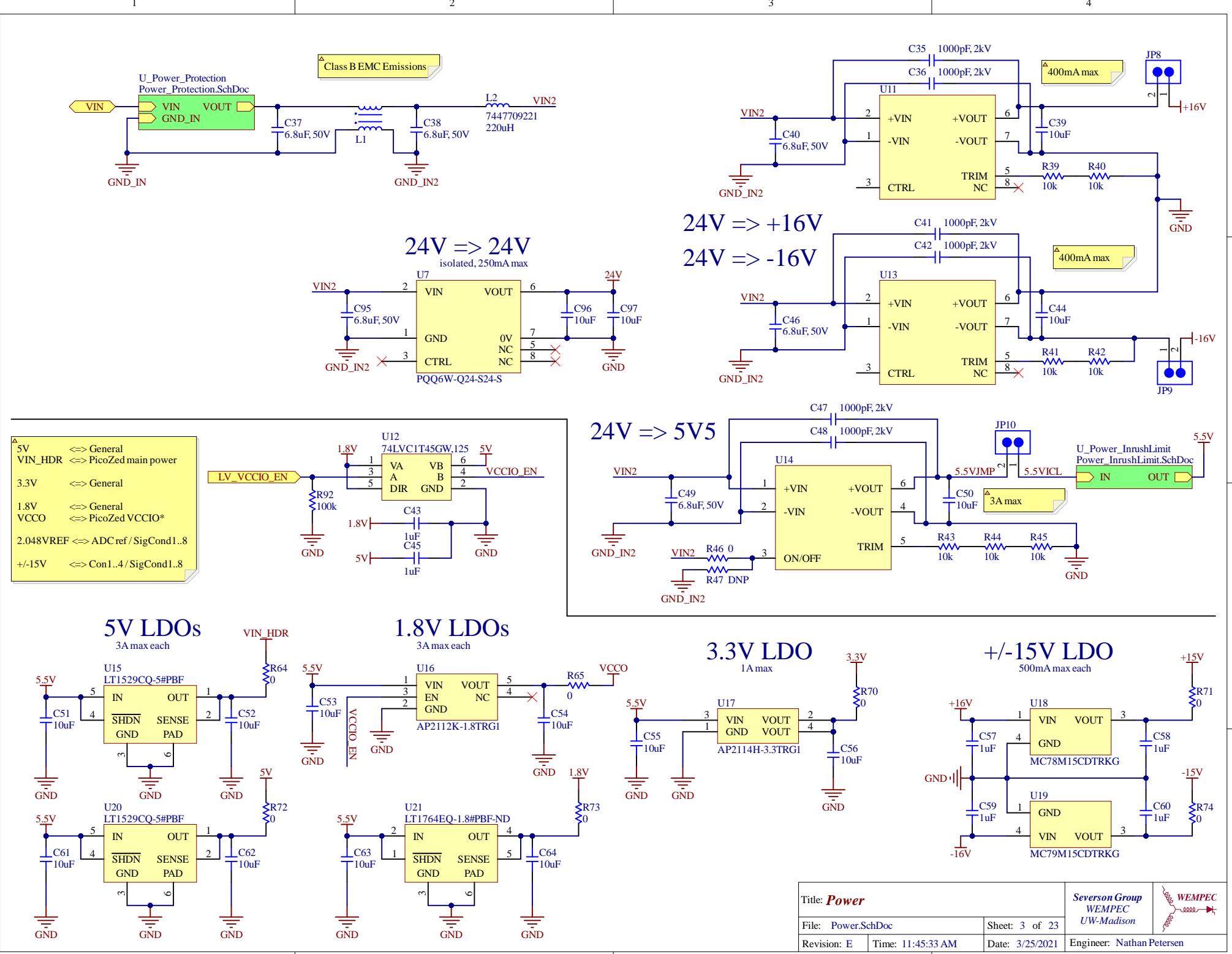
BackPage.SchDoc

U_RevisionChanges

RevisionChanges.SchDoc

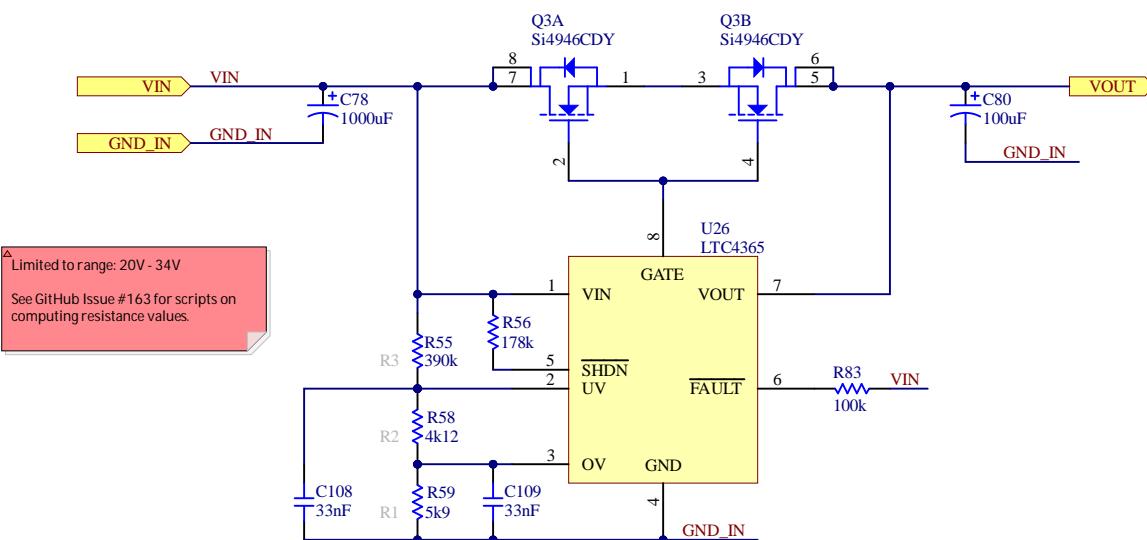
Title: **Advanced Motor Drive Controller**File: **AMDC.SchDoc** Sheet: **1 of 23**Revision: **E** Time: **11:45:32 AM** Date: **3/25/2021**Severson Group
WEMPEC
UW-MadisonEngineer: **Nathan Petersen**





A

A



B

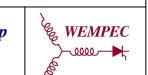
B

C

C

D

D

Title: **Power Protection**File: **Power_Protection.SchDoc**Sheet: **4 of 23**Revision: **E** Time: **11:45:33 AM**Date: **3/25/2021**
Severson Group
WEMPEC
UW-Madison
Engineer: **Nathan Petersen**

A

A

B

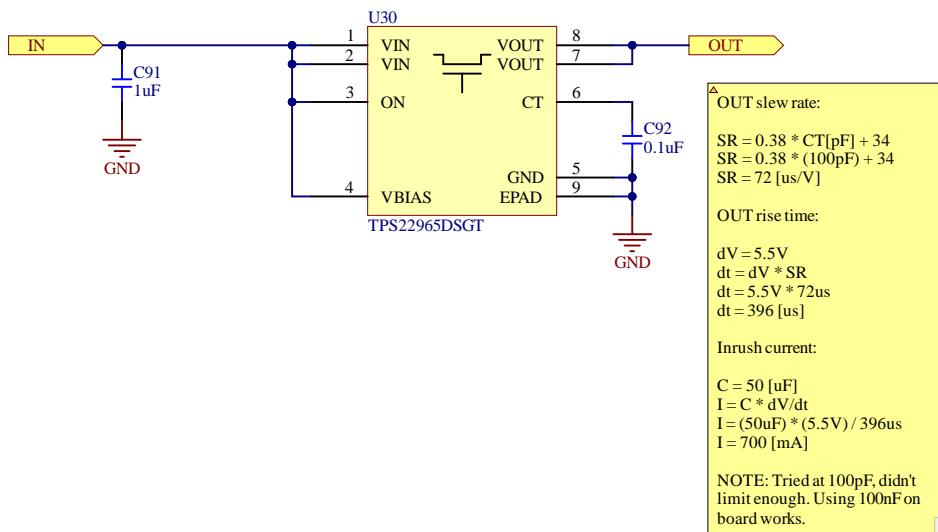
B

C

C

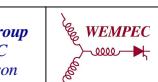
D

D

Title: **Inrush Current Limiter**

File: Power_InrushLimit.SchDoc Sheet: 5 of 23

Revision: E Time: 11:45:33 AM Date: 3/25/2021

Severson Group
WEMPEC
UW-Madison

Engineer: Nathan Petersen

A

A

B

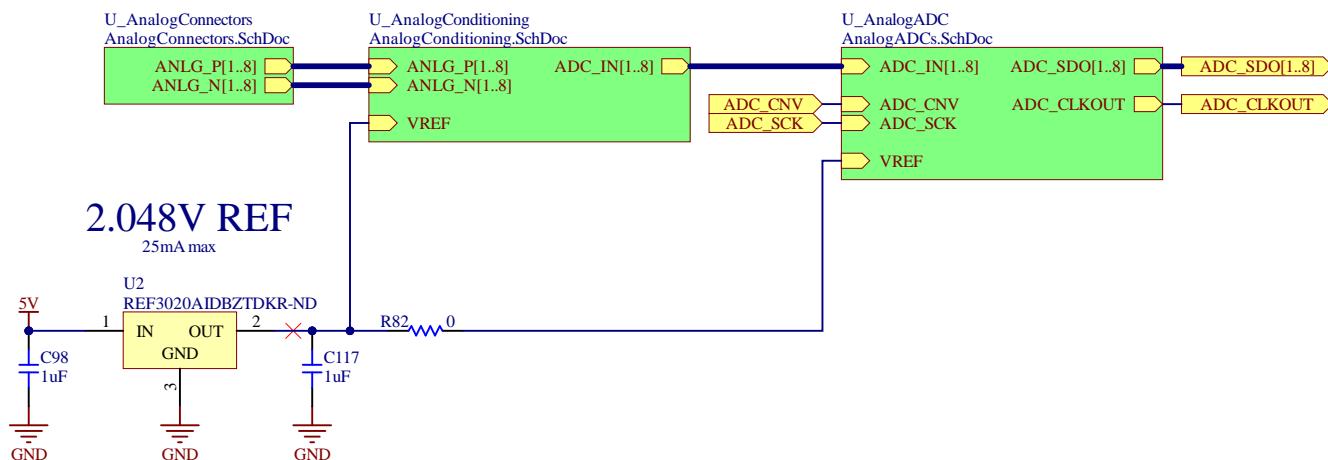
B

C

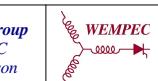
C

D

D

Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **6 of 23**Revision: **E** Time: **11:45:33 AM**Date: **3/25/2021**

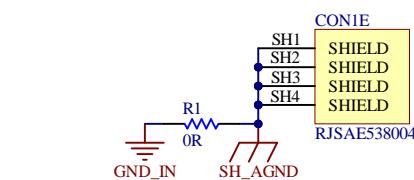
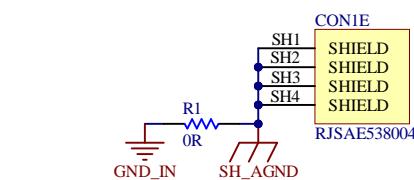
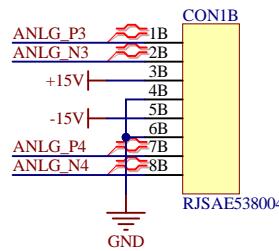
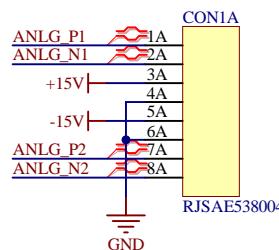
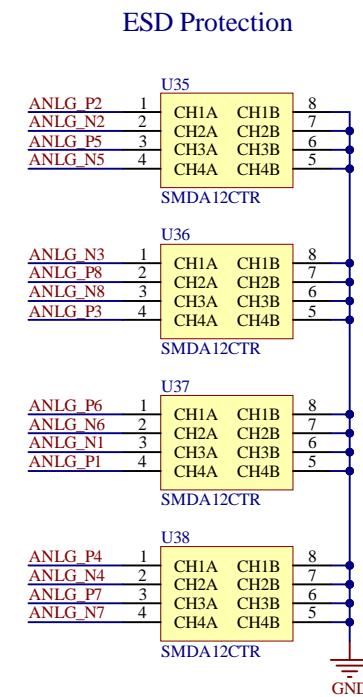
Severson Group
WEMPEC
UW-Madison

Engineer: **Nathan Petersen**

A



B



Force no input to 0V

ANLG_P1	R84 100k	ANLG_N1
ANLG_P2	R85 100k	ANLG_N2
ANLG_P3	R86 100k	ANLG_N3
ANLG_P4	R87 100k	ANLG_N4
ANLG_P5	R88 100k	ANLG_N5
ANLG_P6	R89 100k	ANLG_N6
ANLG_P7	R90 100k	ANLG_N7
ANLG_P8	R91 100k	ANLG_N8

A

A

B

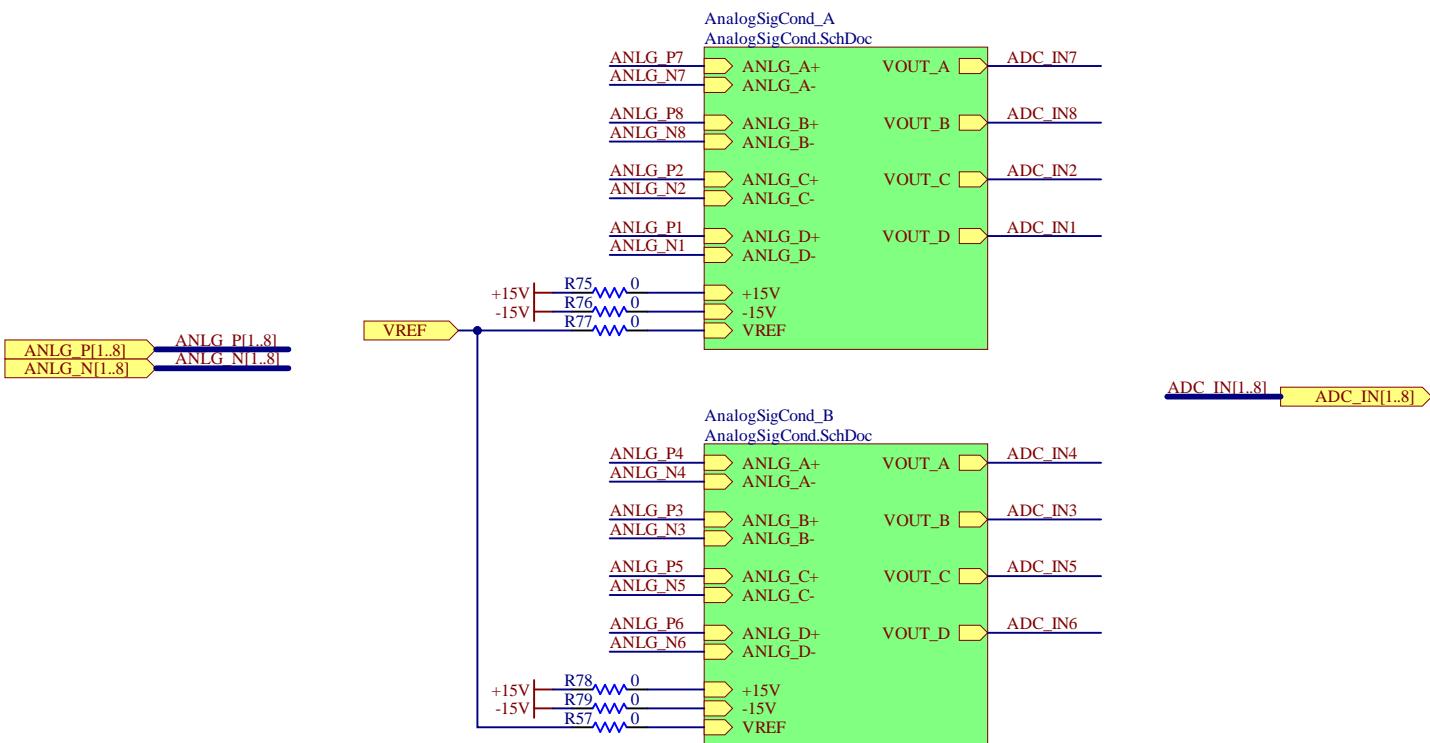
B

C

C

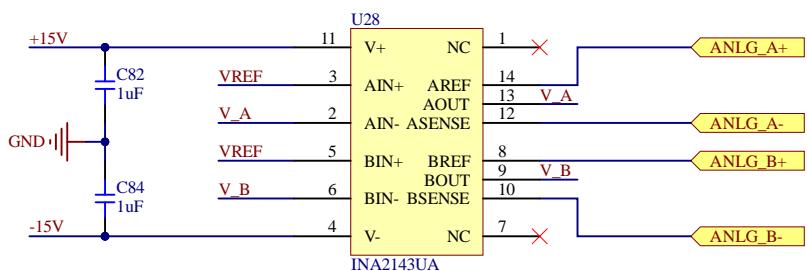
D

D

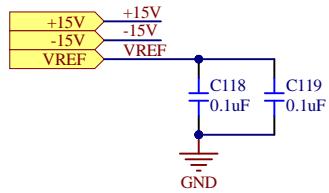
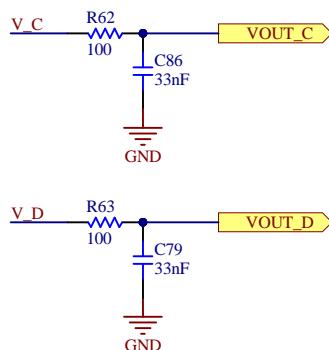
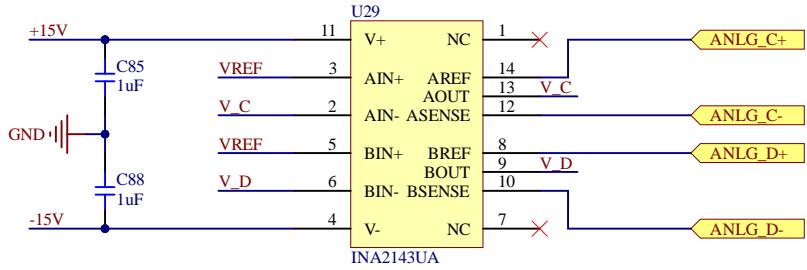
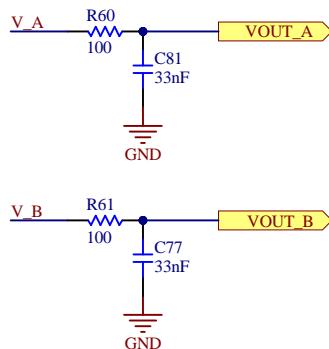


A

A



LPF: $f_c = 50\text{kHz}$



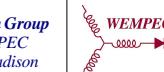
Title: **Analog Signal Front-End**

File: AnalogSigCond.SchDoc

Sheet: 9 of 23

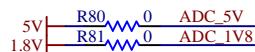
Revision: E Time: 11:45:33 AM Date: 3/25/2021

Severson Group
WEMPEC
UW-Madison



Engineer: Nathan Petersen

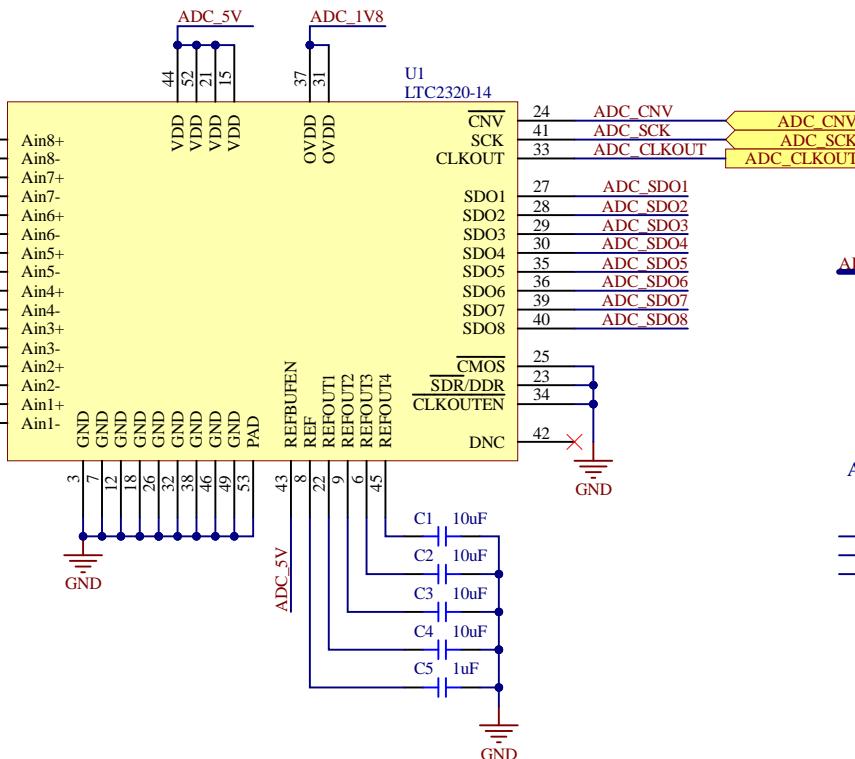
A



VREF

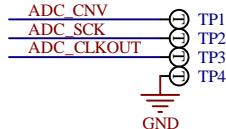
ADC_IN[1..8]

VREF
ADC_IN8 47
ADC_IN7 51
ADC_IN6 50
ADC_IN5 2
ADC_IN4 1
ADC_IN3 5
ADC_IN2 11
ADC_IN1 10
ADC_IN1 14
ADC_IN2 13
ADC_IN3 17
ADC_IN4 16
ADC_IN5 20
ADC_IN6 19

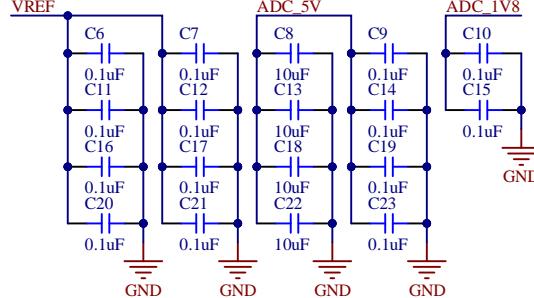


ADC_SDO[1..8] ADC_SDO[1..8]

ADC Serial Interface Test Points



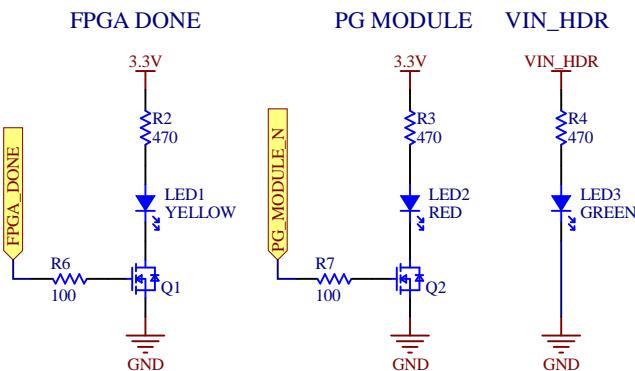
B



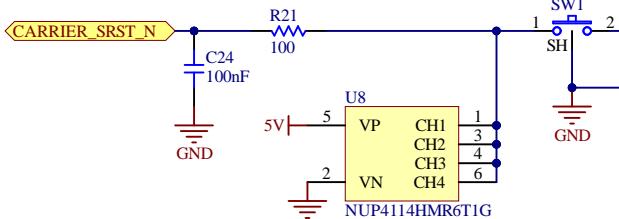
C

D

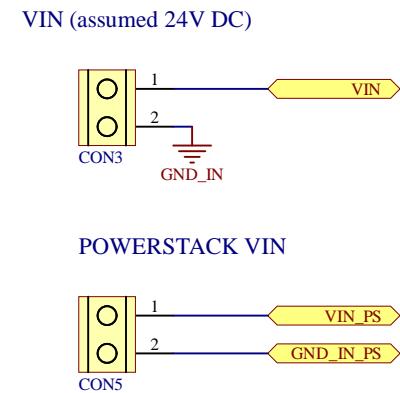
STATUS LEDS



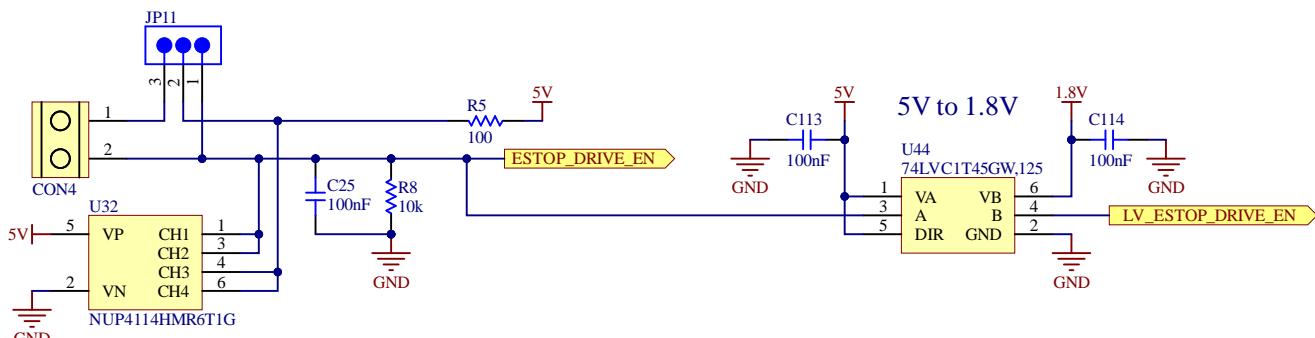
RESET BUTTON



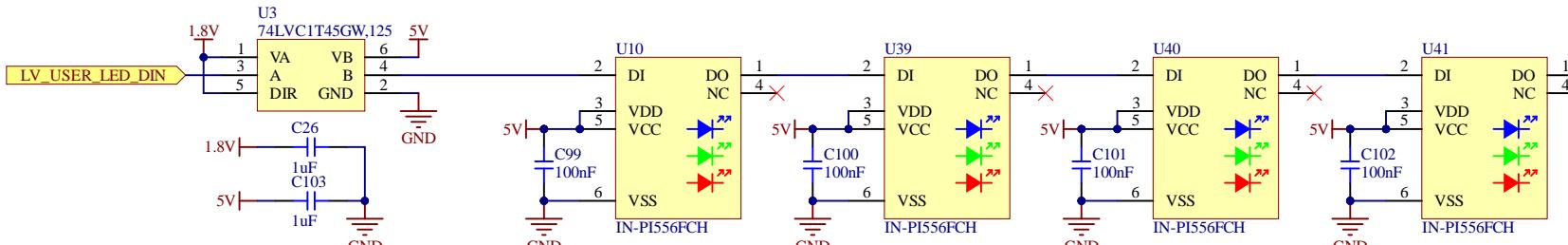
POWER CONNECTORS



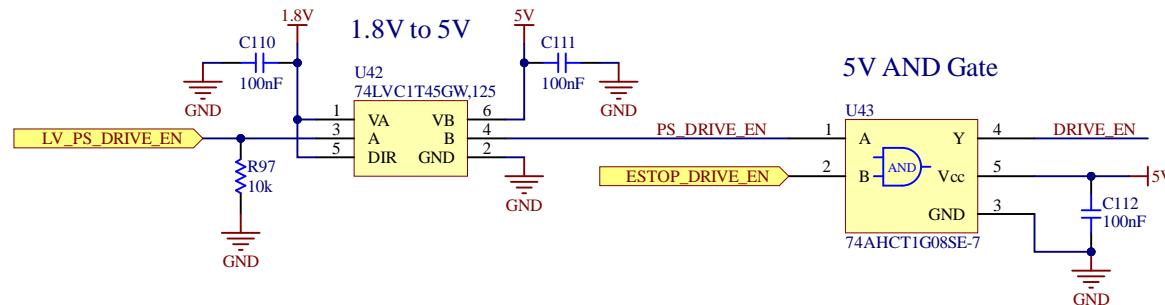
DRIVE ENABLE (ESTOP)



USER RGB LEDs

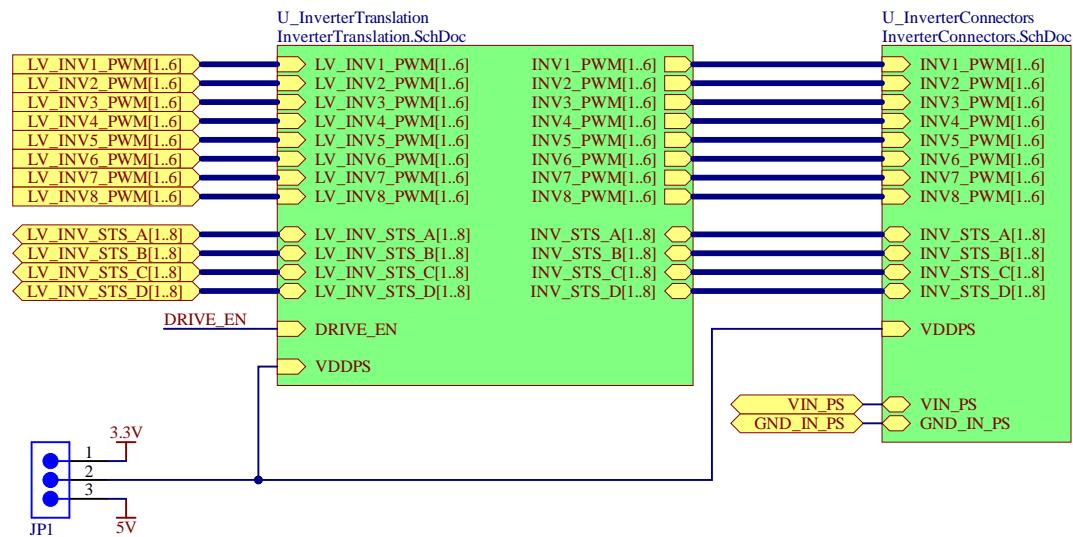


A



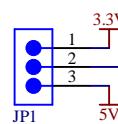
A

B



B

C



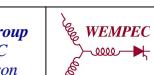
C

D

Title: **Drive Interface**File: **DriveInterface.SchDoc**

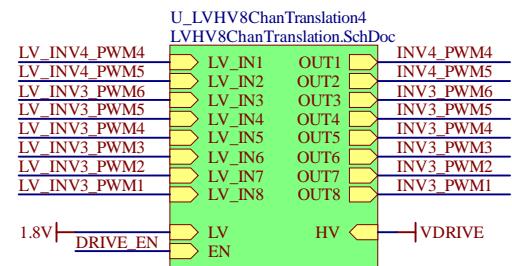
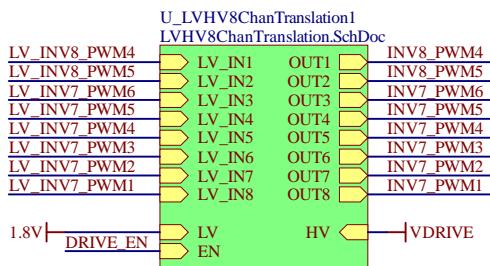
Sheet: 12 of 23

Revision: E Time: 11:45:33 AM Date: 3/25/2021

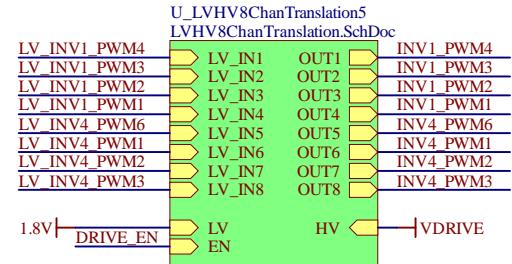
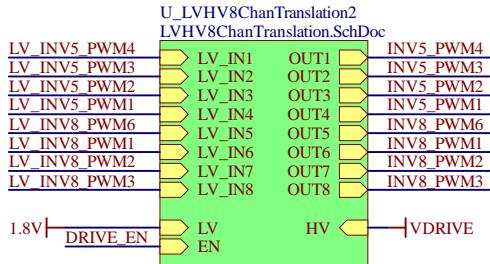
Severson Group
WEMPEC
UW-Madison

Engineer: Nathan Petersen

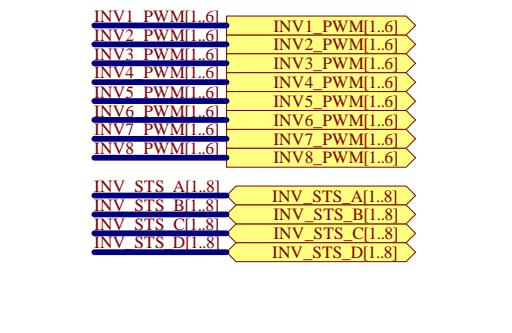
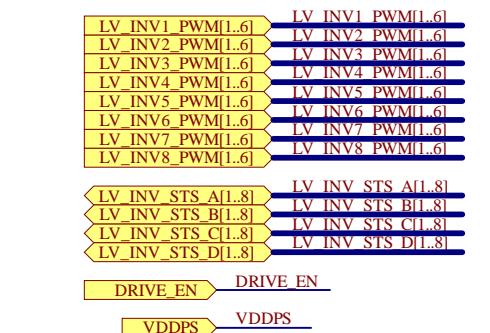
A



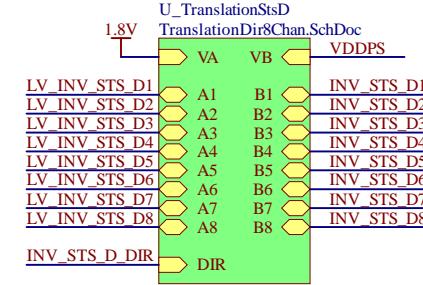
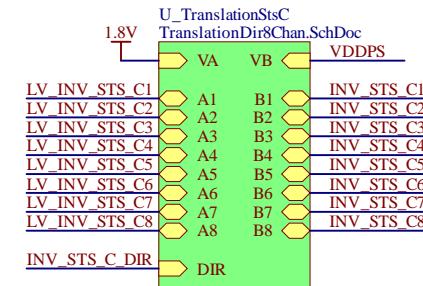
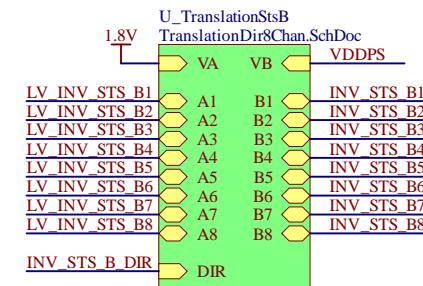
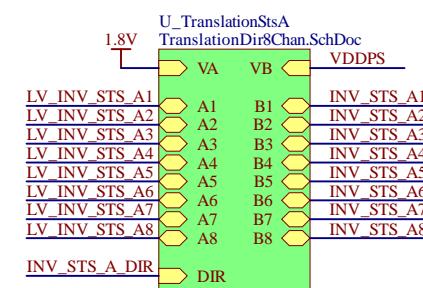
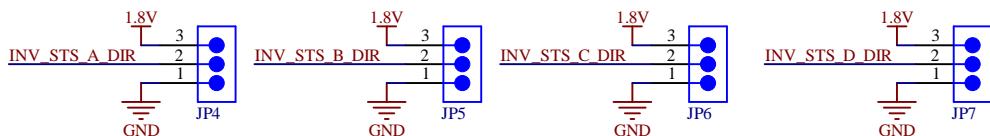
B



C



D

Title: **Inverter Level Translation**Severson Group
WEMPEC
UW-Madison

File: InverterTranslation.SchDoc | Sheet: 13 of 23

Revision: E | Time: 11:45:33 AM | Date: 3/25/2021

Engineer: Nathan Petersen

A

A

B

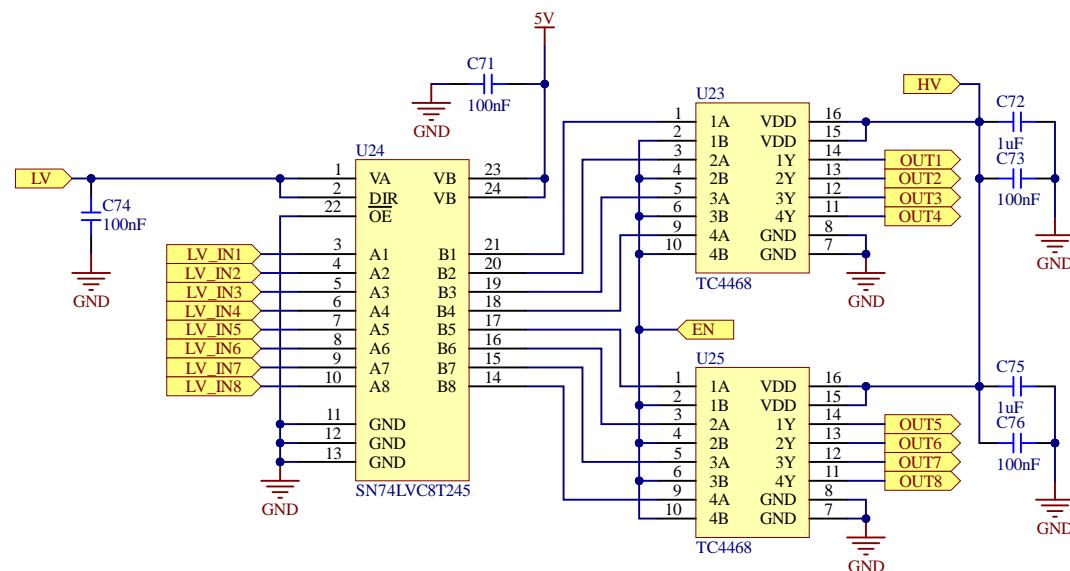
B

C

C

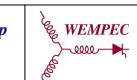
D

D

Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: 14 of 23

Revision: E | Time: 11:45:33 AM | Date: 3/25/2021

Severson Group
WEMPEC
UW-Madison



Engineer: Nathan Petersen

A

A

B

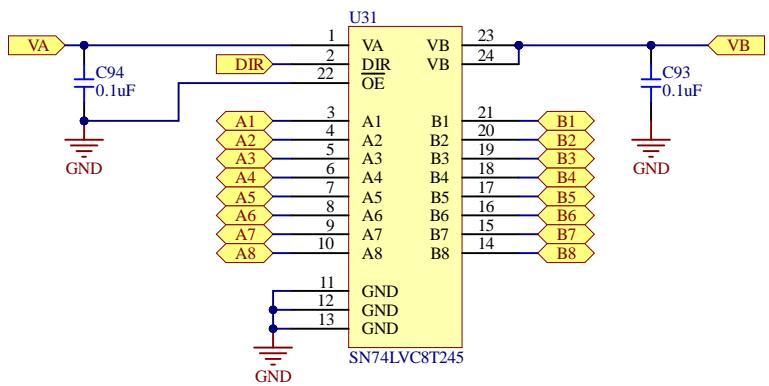
B

C

C

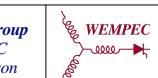
D

D

Title: **8-Channel Directional Translation**

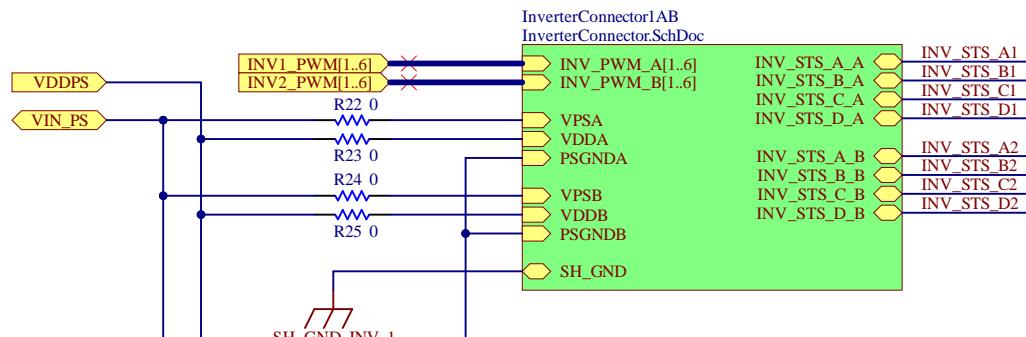
File: TranslationDir8Chan.SchDoc | Sheet: 15 of 23

Revision: E | Time: 11:45:33 AM | Date: 3/25/2021

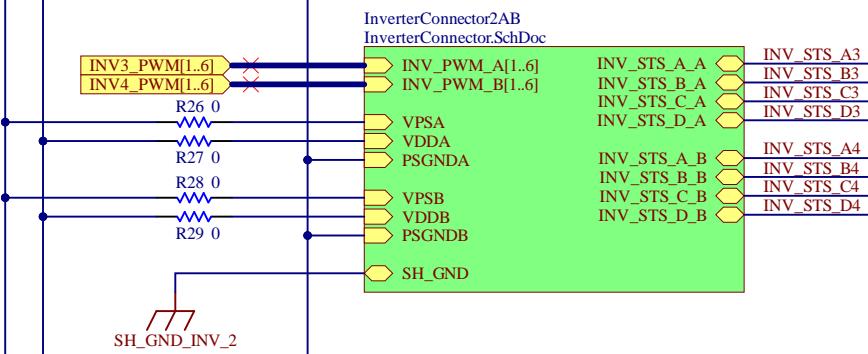
Severson Group
WEMPEC
UW-Madison

Engineer: Nathan Petersen

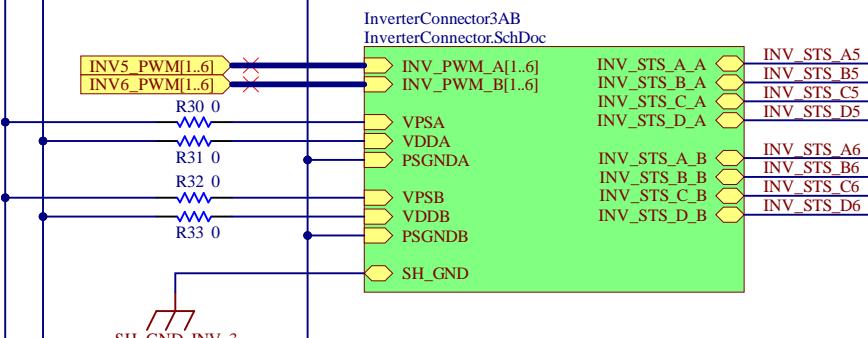
A



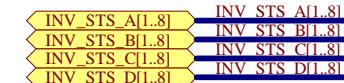
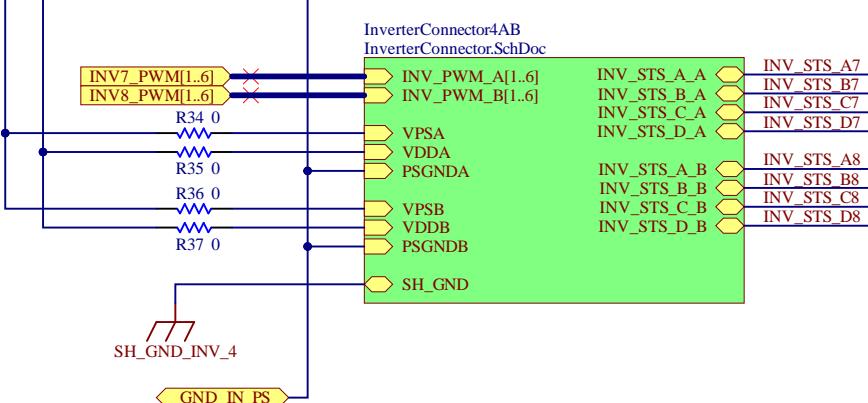
B



C

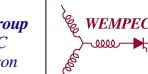


D

Title: **Inverter Connectors**

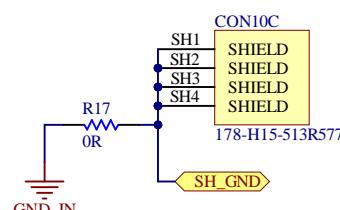
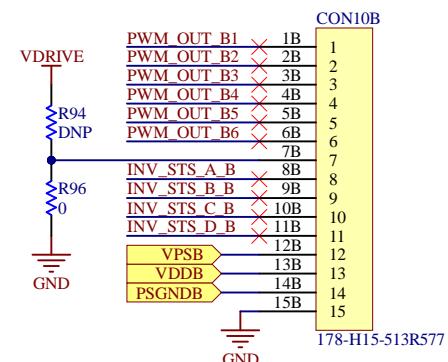
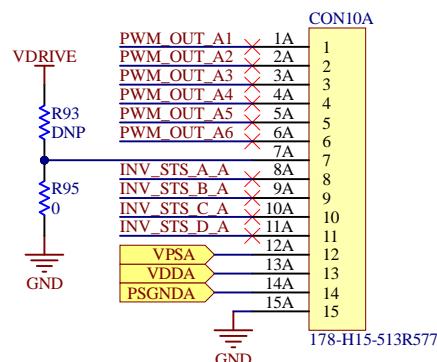
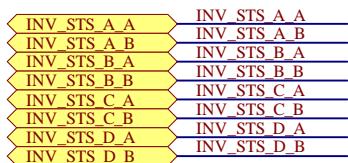
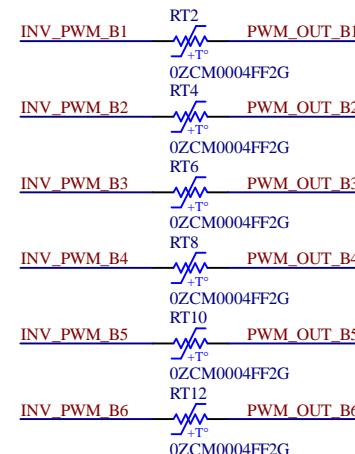
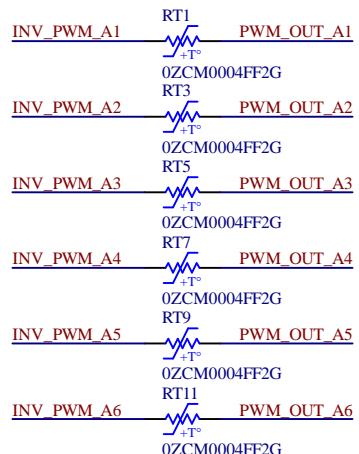
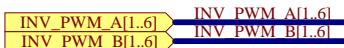
File: InverterConnectors.SchDoc | Sheet: 16 of 23

Revision: E | Time: 11:45:33 AM | Date: 3/25/2021

Severson Group
WEMPEC
UW-Madison

Engineer: Nathan Petersen

Short Circuit Protection

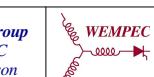


Title: **Inverter Connector**

File: InverterConnector.SchDoc | Sheet: 17 of 23

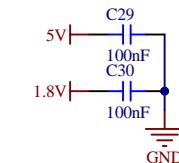
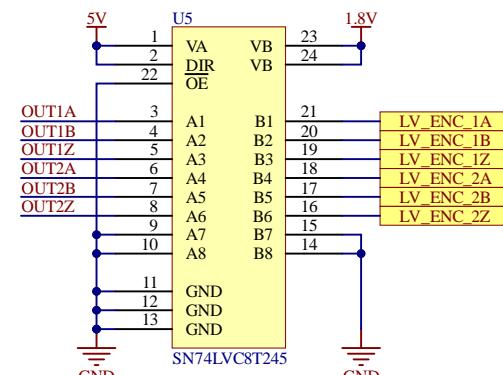
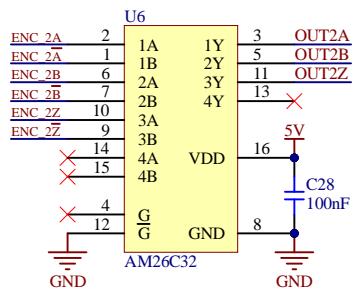
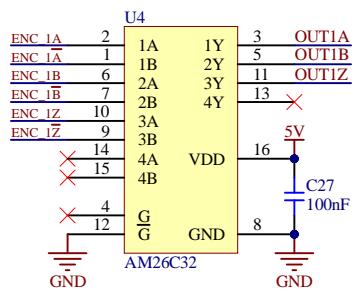
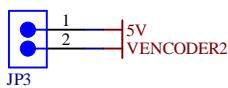
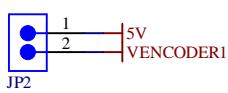
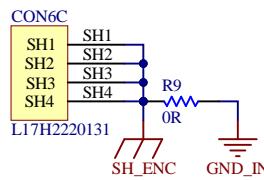
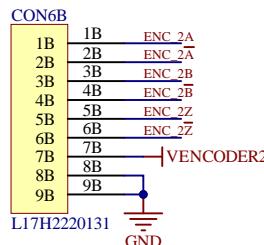
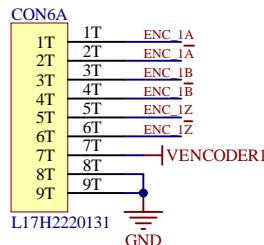
Revision: E | Time: 11:45:33 AM | Date: 3/25/2021

Severson Group
WEMPEC
UW-Madison



Engineer: Nathan Petersen

A

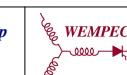
Title: **Encoders**

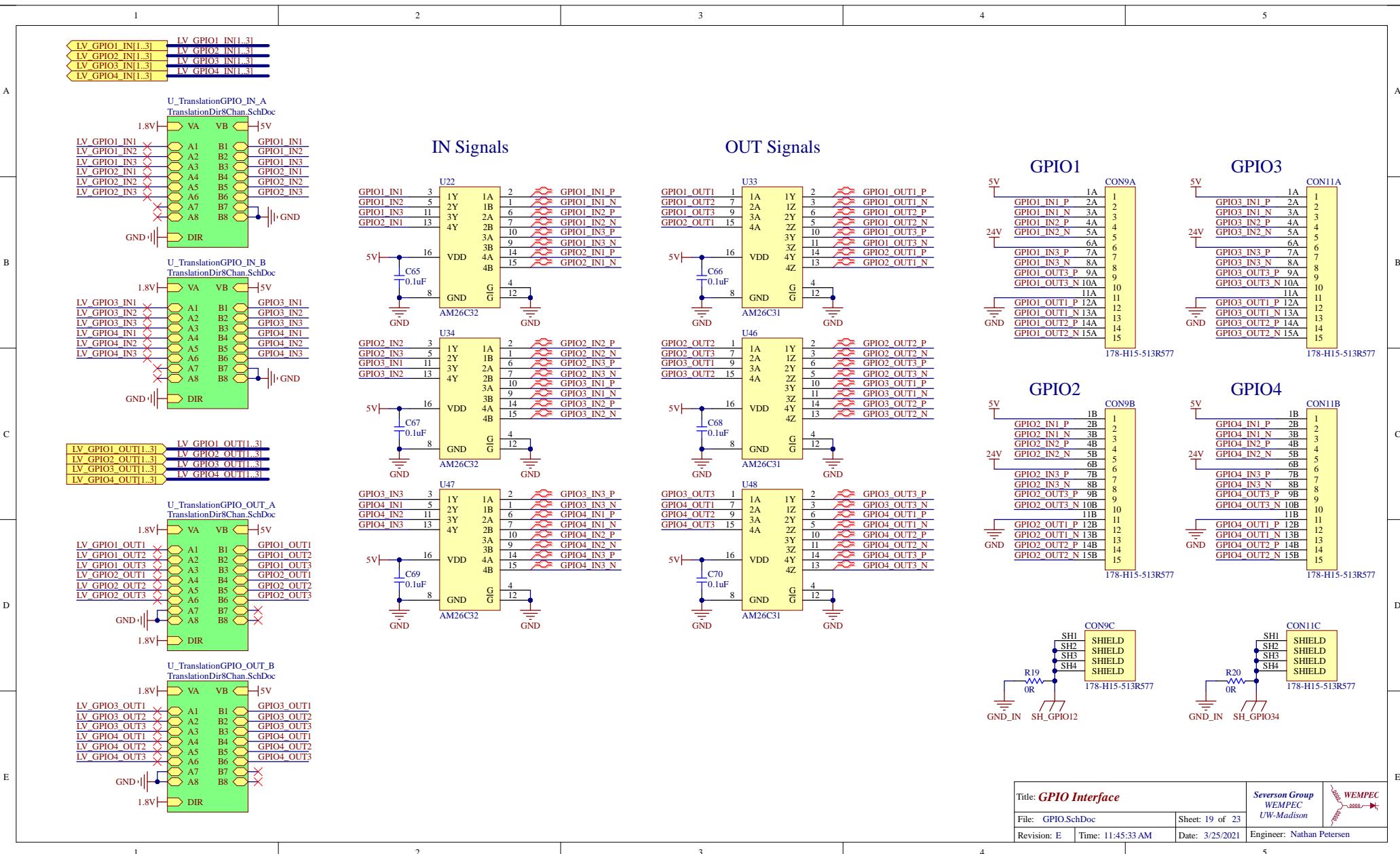
File: Encoder.SchDoc

Sheet: 18 of 23

Revision: E Time: 11:45:33 AM

Date: 3/25/2021

Severson Group
WEMPEC
UW-Madison




A

A

B

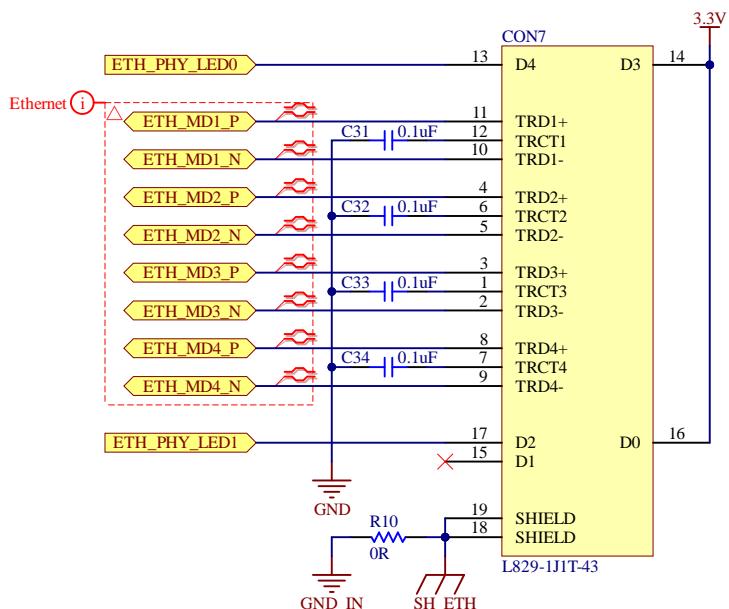
B

C

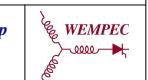
C

D

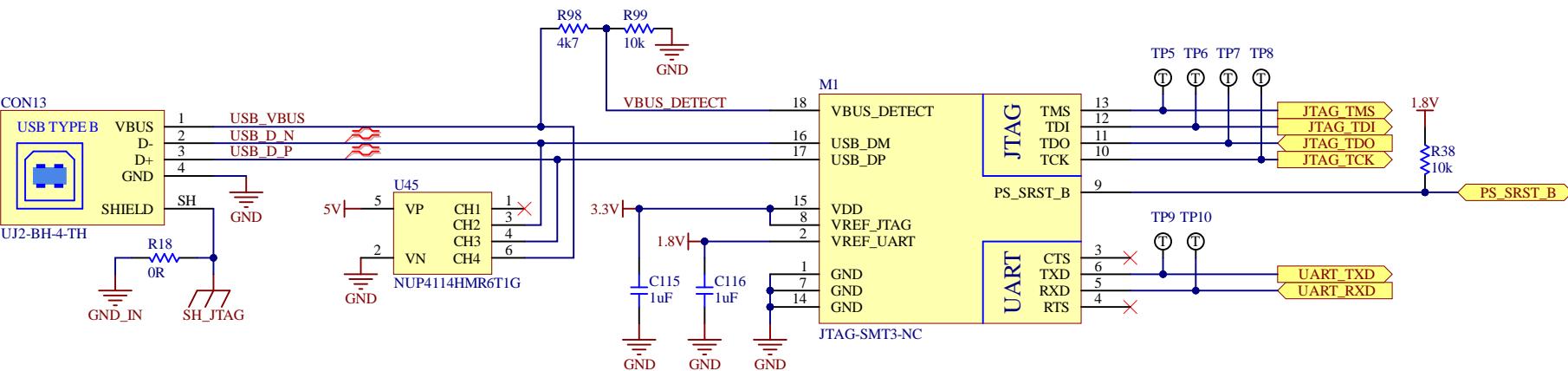
D

Title: **SoM Gb Ethernet**File: **GbEthernet.SchDoc** Sheet: **20 of 23**Revision: **E** Time: **11:45:34 AM** Date: **3/25/2021**

Severson Group
WEMPEC
UW-Madison



Engineer: Nathan Petersen

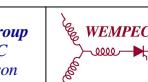


Title: **Host Interface: JTAG and UART**

File: **JTAG_UART.SchDoc** Sheet: 21 of 23

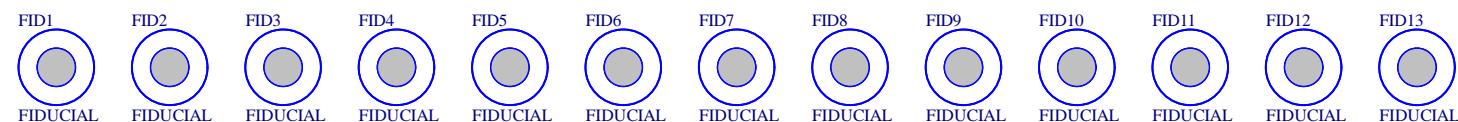
Revision: E Time: 11:45:34 AM Date: 3/25/2021

Severson Group
WEMPEC
UW-Madison



Engineer: Nathan Petersen

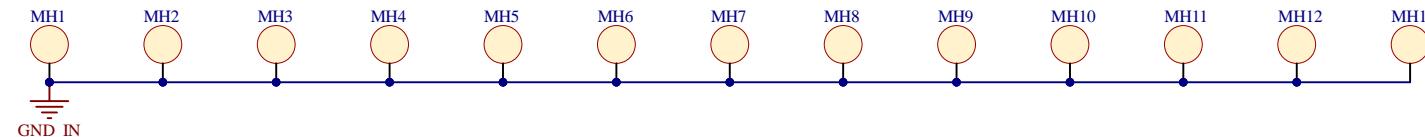
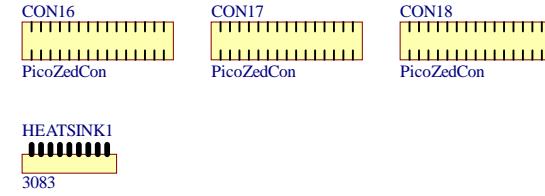
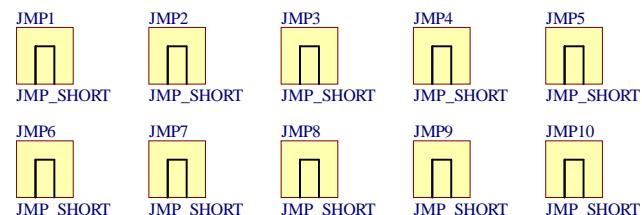
A

Fiducials:

B

4-40 Screws:**4-40 Standoffs:**

C

Mouting Holes:**PicoZed hardware:****Jumpers:**
Silkscreen marked with default locationsTitle: **Back Page**

File: BackPage.SchDoc

Sheet: 22 of 23

Revision: E Time: 11:45:34 AM

Date: 3/25/2021

Severson Group
WEMPEC
UW-Madison

Engineer: Nathan Petersen

A

REV A: design finalized 2018-05-25

- Initial design

REV B: design finalized 2018-07-17

- Add power input protection
- Add test points
- Add TVS to analog inputs
- Change power input DC/DC modules
- Fix BOM with correct part numbers
- Fix footprints

REV C: design finalized 2018-11-21

- Add inrush current limiting to 5V5 rail
- Add more silkscreen labels
- Add test points
- Change ADC reference from 2.5V to 2.048V
- Change trim resistors for +/-16V DC/DCs
- Swap UART Tx / Rx pins
- Separate power stack shields between connectors
- Fix footprints

REV D: design finalized 2020-01-29

- New PCB form factor (6" x 6.75", 6 layers)
- Add power stack supply rail distribution
- Add isoSPI ports
- Add extra encoder port
- Add 0R resistors to subsection power for debugging
- Add 100k resistors across analog inputs
- Add serially addressable RGB LEDs
- Add EEPROM
- Add fiducials to layout
- Remove user button / switch
- Remove discrete RGB LED
- Remove ADC2, now just one ADC
- Remove unity gain op-amp driving ADC inputs
- Reduce bulk input
- Reduce 24V power filter component current ratings
- Reduce 3V3 LDO current rating
- Change level-shifter IC for UART signals
- Change JTAG to NC module
- Change JTAG pin headers to pads
- Change values for inrush limiting circuitry
- Change FPGA driven MOSFETs to lower V_{th}
- Change FPGA pin-out mapping
- Change power stack connector I/O
- Change encoder input signal chain
- Change Ethernet routing to correct diff. impedance
- Fix footprints

REV E: design finalized 2021-03-25

- Remove isoSPI
- Add shared UART and JTAG interface
- Add more GPIO ports
- Add mechanical parts to BOM
- Add website to PCB silkscreen
- Add reset signal pull-up and ESD protection
- Add local decoupling to VREF
- Add local decoupling to 2.048V
- Add E-STOP logic signal to FPGA
- Add PTC resettable fuses to PWM outputs
- Add VDRIVE signal to PS interface
- Add jumpers for default VDRIVE and ESTOP
- Add pull-down to VCCIO_EN
- Change power wiring in schematics
- Change shield termination to VIN-
- Change mounting holes to VIN- from GND
- Change DB15 P/N to include screw posts
- Change to USB type B receptacle
- Update top-level block diagram
- Fix 24V supply to GPIO port
- Fix power protection circuitry
- Fix board start-up PWM issues
- Fix P/N for RC filter caps
- Fix BOM components for DFM
- Fix footprints

See www.github.com/Severson-Group/AMDC-Hardware/issues for more discussion on design changes

B

A

C

B

D

C

Title: Revision Changes		Severson Group WEMPEC UW-Madison
File: RevisionChanges.SchDoc	Sheet: 23 of 23	
Revision: E	Time: 11:45:34 AM	Date: 3/25/2021
Engineer: Nathan Petersen		