1 Features

- **Light to Digital Converter Integrated Circuit for SteamVR™ Tracking**
- Convert infrared light pulses to digital envelope pulses used to track position.
- Convert infrared light pulses to digital pulses that follow the optical carrier.
- 1MHz to 10MHz optical carrier frequencies
- 50Hz/60Hz ambient noise rejection
- Two-wire control bus shares E/D pins
  - Sleep command
  - Configuration
- DVDD: 3.3V
- Small Package Size simplifies industrial design of tracked objects
  - 9 Bump WLCSP Package
  - 1.66mm x 1.66mm

2 Applications

- SteamVR Tracking Applications
- Room-scale Virtual Reality Tracking
- Virtual Reality Controllers
- Tracking of Physical Objects in VR
- Adding SteamVR Tracking to VR Head Mounted Displays
- Robotics Positioning
- Volumetric Entertainment Systems
- Optical Ranging
- Optical Detection
- Free-Space Optical Communication

3 Description

Triad Semiconductor's TS4231 enables cost effective deployment of Valve Corporation's SteamVR Tracking System. Working with a photodiode, the TS4231 converts infrared light pulses into position-indicating digital envelope signals. The device also includes a digital output, data pin that is a representation of the optical carrier waveform applied to the photodiode. The TS4231 includes circuits for photodiode biasing and provides high gain, noise filtering and envelope detection of pulsed IR light sources. The Envelope output of the TS4231 is a digital signal that tracks the envelope of the amplitude modulated (OOK or ASK) infrared light that is incident on the photodiode. The data output is a digital signal that tracks the modulated light input. The TS4231 is configured by a two-wire bus that shares the E/D pins of the device.

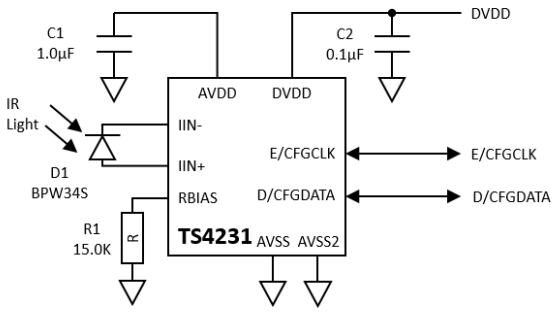
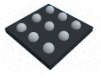


Figure 1: Simplified Application Circuit



TS4231 Device Size
1.66mm x 1.66mm

4 Device Overview

The TS4231 is a mixed-signal integrated circuit for use in optical position tracking applications. Utilizing Wafer Level Chip Scale Packaging (WLCSP), it achieves a minimal footprint size for use in space-constrained assemblies. The TS4231 provides pulse detection circuitry for use in room scale tracking/positioning for virtual reality gaming and other applications which require millimeter position accuracy. The signal path is driven from an external photodiode which is connected directly to the IIN+ and IIN- package inputs, then AC coupled to the inputs of a differential TIA. Internal bias blocks provide the necessary biasing for the photodiode. The output of the differential TIA is followed by filtering and gain blocks to limit noise before the signal drives an envelope detector and data slicer to generate the output signals. Figure 2 shows the block diagram of the TS4231. The TS4231 is available in a 9-bump WLCSP package.

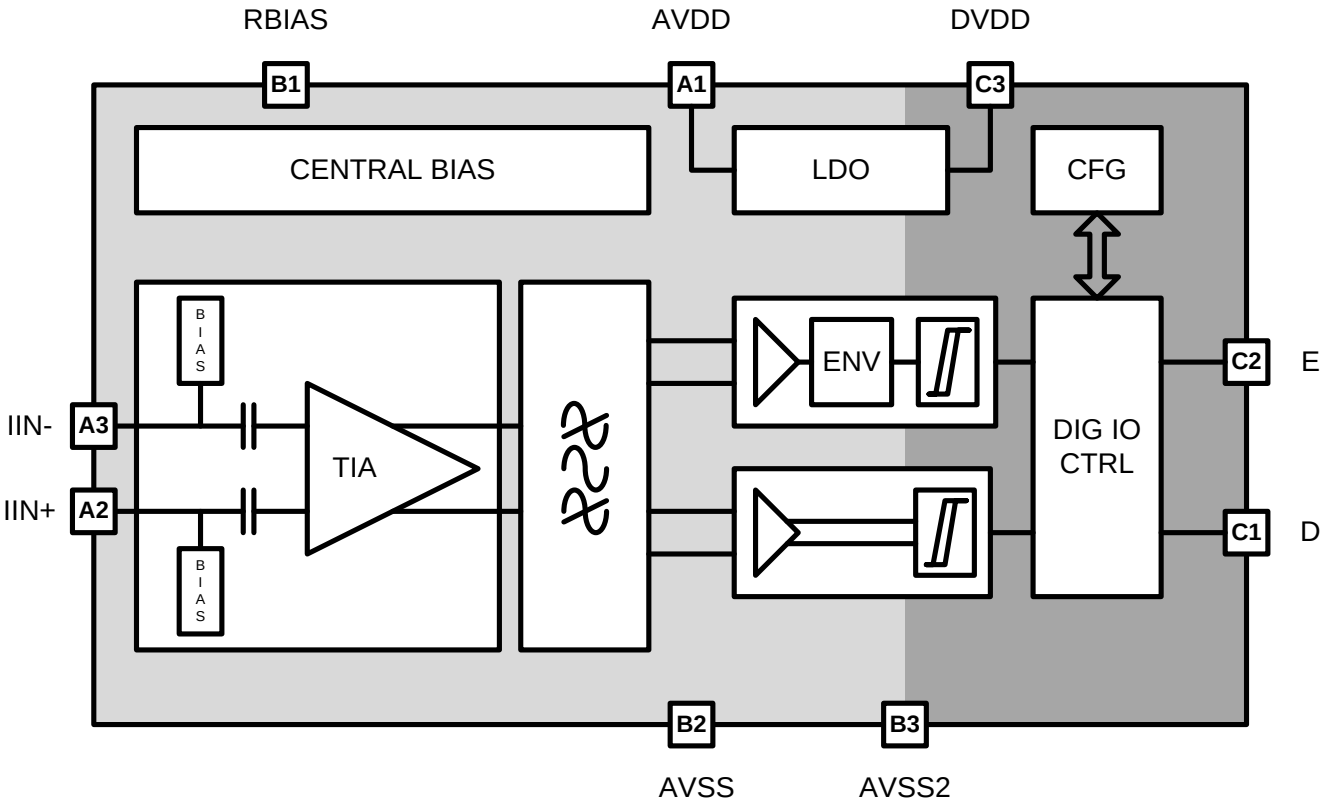


Figure 2: TS4231 Basic Block Diagram

5 Bias Circuitry

The TS4231 contains an internal reference system that controls the device's internal detection levels. An external resistor connected to the RBIAS input is used to set the internal reference. The internal reference will remain constant (within the resistor and reference tolerance) over process corners.

6 Signal Path

6.1 TIA & Filter Amplifier

The TIA is designed to amplify a differential input current pulse, created by an optical detector diode, into an output voltage pulse. A detector diode input load of 30 pF is expected for nominal operation. Detector sensitivity will vary with diode input load and can also be affected by stray capacitance due to PCB layout at the IIN+, IIN- and RBIAS inputs. The Filter Amplifier is implemented using successive band limiting gain stages.

6.2 Envelope and Data Detectors

The Envelope Detector is triggered by a filtered and detected signal crossing a configured threshold. The Envelope output is asserted during detection of light pulses incident on the external photodiode. The data detector is implemented using a comparator with controlled hysteresis. The Data pin low time is qualified with an internal one-shot and is forced to return low if the low duration exceeds a 600-900ns timeout. See Figure 3.

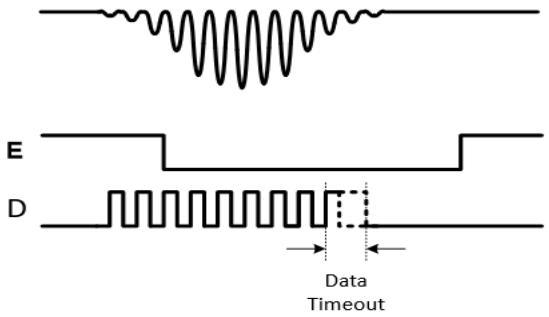


Figure 3: Output Waveforms for Modulated IR light with Gaussian Envelope

7 Digital Control Interface

The TS4231 provides a digital control interface (see Figure 4) that can be controlled by the Valve SteamVR Tracking HDK FPGA. After device power on, the SteamVR Tracking HDK communicates with the TS4231 over the E and D pins to configure the device. After device power on, the device must detect modulated infrared light prior to configuration as shown in Figure 5. After light detection, the SteamVR Tracking HDK communicates with the TS4231 over the E and D pins to configure the device. After being configured, the device will be in normal watch mode looking for modulated IR light. When the device's photodiode is exposed to modulated IR light within the frequency range of the device, the envelope output is asserted on the E pin and the carrier data is output on the D pin.

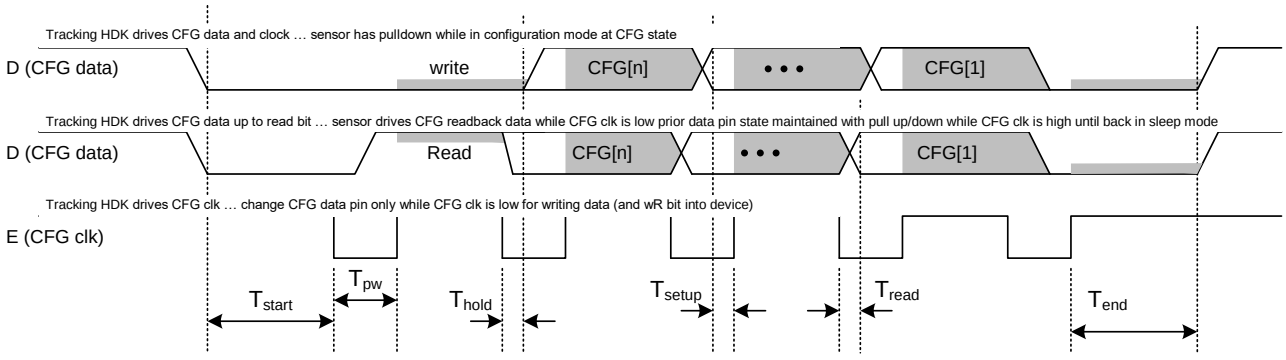


Figure 4: Configuration Interface Timing

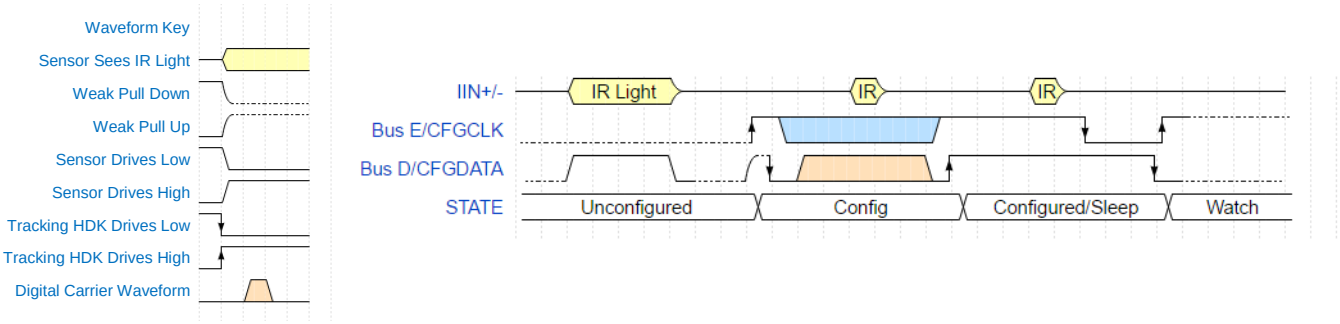


Figure 5: TS4231 powers up Un-configured then the SteamVR Tracking HDK configures the device

7.1 Sleep Mode

After the device has been configured to detect the optical carrier, the SteamVR Tracking HDK transitions the device back to Watch state by driving E pin low, then D pin low, then E pin back high. Once in Watch state the SteamVR Tracking HDK promptly releases the E/D bus so that the TS4231 can drive the E and D outputs when IR light is detected. While configured to pulse out the carrier on the D pin, the SteamVR Tracking HDK can put the device to sleep by driving E pin low. To transition back to Watch mode, the SteamVR Tracking HDK sets the D pin low and then the E pin high providing for quick transitions between Watch and Sleep to support dynamic power control.

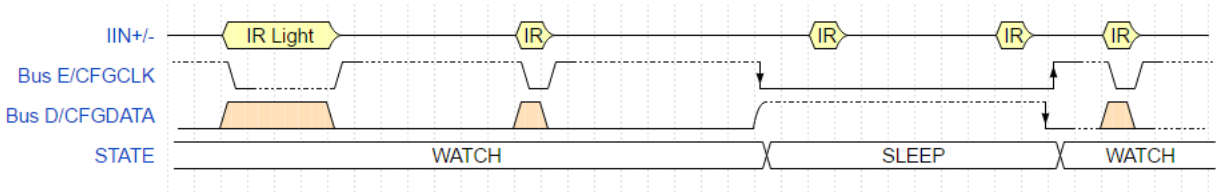


Figure 6: Sleep Timing

8 Performance Characteristics

8.1 Absolute Maximum Ratings

Parameter(1)(2)	Notes/Conditions	MIN	MAX	units
DVDD			3.6	V
Digital Input Voltage		-0.3	3.6	V
Junction Temperature T_{JMAX}	Maximum junction temperature		150	°C
Storage Temperature, T_{STOR}	Storage temperature range	-40	150	°C
Soldering Information: infrared or convection (30 sec)	Peak body temperature (reflow)		260	°C

(1) All Voltages are specified with respect to GND = 0Vdc
(2) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

8.2 ESD Ratings

Parameter	Notes/Conditions	Value	Units
$V_{(ESD)}$ Electrostatic Discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001-2014 (1)	2000	V

(1) JEDEC document JEP155 States that 500-V HBM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

Parameter	Notes/Conditions	MIN	TYP	MAX	units
DVDD	Supply voltage	3.0	3.3	3.6	V
T_{AMB}(1)	Operating temperature range	0		85	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, Θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)}$ – T_{AMB})/ Θ_{JA}. All numbers apply for packages soldered directly onto a PC Board

8.4 Thermal Information

Parameter	Thermal Metric	9 Ball WLCSP	units
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	60	°C/W

8.5 Electrical Characteristics

Operating conditions: DVDD = 3.3V, T_{AMB} = 25 °C unless otherwise noted(1).

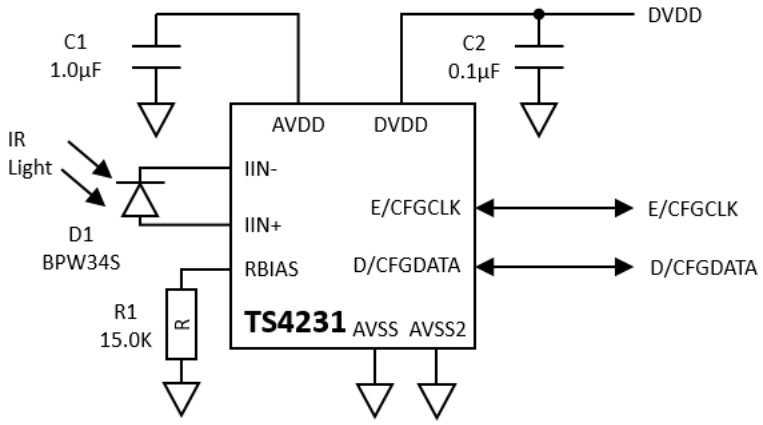
Parameter	Notes/Conditions		MIN(2)	TYP(3)	MAX(2)	units
Power Supply						
I_{VDD}	Operating current			5.0	7	mA
Sleep_I_{VDD}	Sleep mode current			0.75	1.0	mA
Digital IO						
V_{IL}	Input Low Voltage				0.3 * VDD	V
V_{IH}	Input High Voltage		0.7 * VDD			V
V_{OL}	Output Low Voltage	@ 2 mA load			0.1 * VDD	V
V_{OH}	Output High Voltage	@ 2 mA load	0.9 * VDD			V
I_{PU}	Output Pullup Current		60	100	140	µA
I_{PD}	Output Pulldown Current		60	100	140	µA
Rise(2)	10/90% Output Rise Time	Slew rate limited 5-20pF load	7		15	nS
Fall	10/90% Output Fall Time	Slew rate limited 5-20pF load	7		15	ns

Parameter	Notes/Conditions		MIN(2)	TYP(3)	MAX(2)	units
T_{start}			80			ns
T_{pw}			40			ns
T_{setup}			15			ns
T_{hold}			15			ns
T_{end}			80			ns
T_{read}					20	ns
System						
Freq	Input pulse frequency	HiPass – LoPass 3dB corners	1		10	MHz
I_{INDET}	In band detection input current level (max gain)	w/ App Schematic	0.2			µA
I_{INMAX}	In band input current level max	w/ App Schematic			100	µA
$Sleep_{RCVRY}$	Sleep Mode Recovery timing E and D outputs should be ignored during recovery time	10 – 90% on I_{VDD}			50	µS
$Sleep_{PDN}$	Sleep Mode Power Down timing	10 – 90% on I_{VDD}			50	µS
REJ_{50KHz}	50KHz Rejection	@ filter output	40			dB
	RBIAS pin stray capacitance				10	pF
	RBIAS resistor value	1% tolerance		15		kΩ

(1) Electrical Characteristic values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested
(2) Rise and Fall Times are ensured by design and not production tested.
(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material

9 Applications and Design Considerations

9.1 Application Schematic(1)



(1) Minimize stray capacitance at device pins IIN+, IIN-, RBIAS, and at D1.

Figure 7: TS4231 Application Schematic

9.2 Power Supply Recommendations

The TS4231 was designed to be operated from a 3.3V power supply. The voltage range for DVDD is shown in *Recommended Operating Conditions*. Power supply accuracy of 10% or better is advised. The internal LDO output at the AVDD pin should be bypassed with a 1µF capacitor.

9.3 Capacitor Selection

To achieve the best performance, C1 and C2 should have low ESR / ESL, and a self-resonant frequency above the maximum input signal bandwidth. Typically, size 0402 or smaller is better for high self-resonance.

9.4 Layout Guidelines

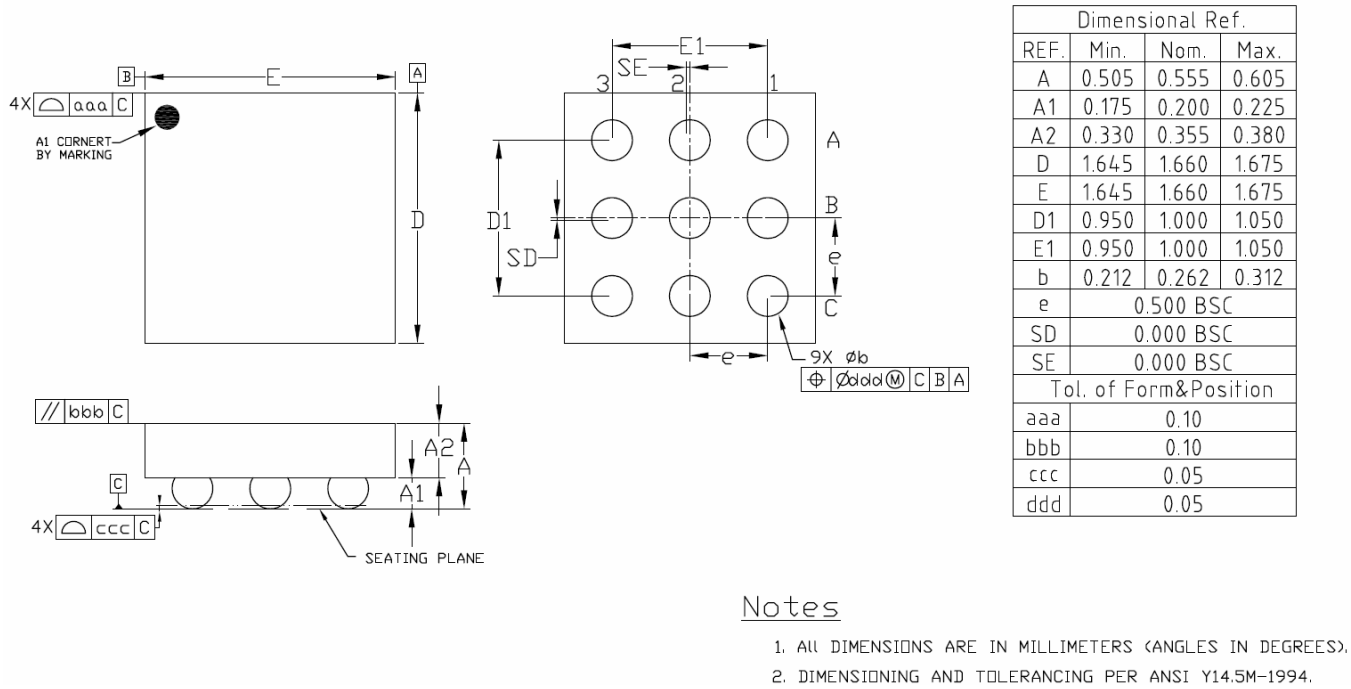
Optimum performance can be achieved with the TS4231 by adhering to the following layout guidelines which will help minimize performance degradation due to layout parasitics and noise. The following guidelines are assuming the implementation of the application schematic shown in Figure 7.

1) C1 and C2 should be placed as close as practical to their respective AVDD and DVDD package bumps
2) Shield the IIN- and IIN+ nets with ground fills
3) Minimize routing lengths on the IIN-, IIN+ and RBIAS nets
4) The D and E outputs should be routed over a solid ground plane

10 Part Packaging Information

10.1 Package Drawing

The TS4231 – Light to Digital Converter is packaged as a 9 bump WLCSP. Figure 8 shows the WLCSP configuration. Recommended Land Pattern is 0.200mm for each bump (per IPC 7351A guidelines).



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.505	0.555	0.605
A1	0.175	0.200	0.225
A2	0.330	0.355	0.380
D	1.645	1.660	1.675
E	1.645	1.660	1.675
D1	0.950	1.000	1.050
E1	0.950	1.000	1.050
b	0.212	0.262	0.312
e	0.500 BSC		
SD	0.000 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

Figure 8: TS4231 Outline Drawing

10.2 Date Code

The manufacturing date code is printed on the package as described in Section 14 of this document. The date code has the format of YYWW where YY is the last 2 digits of the manufacturing year, and WW is the week of manufacture in the year.

11 Pin List

#	Pin Name	Pin Type	Pin Description
A1	AVDD	Supply	Power (bypass with 1uF)
A2	IIN+	Input	TIA Input (TS4231 internally provides bias to AVSS for photodiode Anode and has internal AC coupling cap)
A3	IIN-	Input	TIA Input (TS4231 internally provides bias to AVDD for photodiode Cathode and has internal AC coupling cap)
B1	RBIAS	Input	1% 15k Resistor for current reference
B2	AVSS	Supply	Ground (must be connected)
B3	AVSS2	Supply	Ground (connect for best performance and to access middle bump without buried/blind via in FPC or PCB landing site)
C1	D	Digital I/O	Data Output / Configuration Data I/O
C2	E	Digital I/O	Envelope Output / Configuration Clock input
C3	DVDD	Digital Supply	LDO input supply and Digital IO power (bypass with 0.1uF)

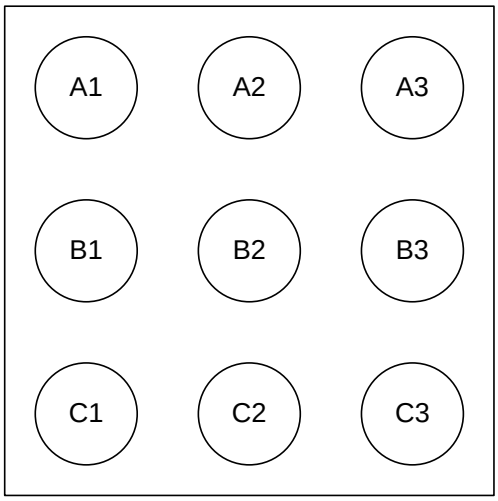


Figure 9: Top View Pin Location

12 IOMAP

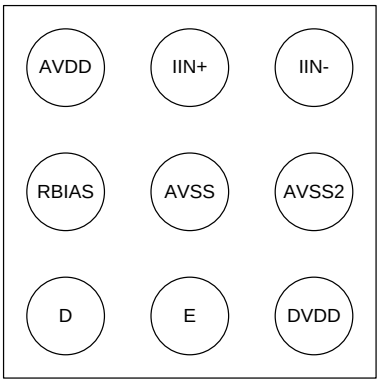
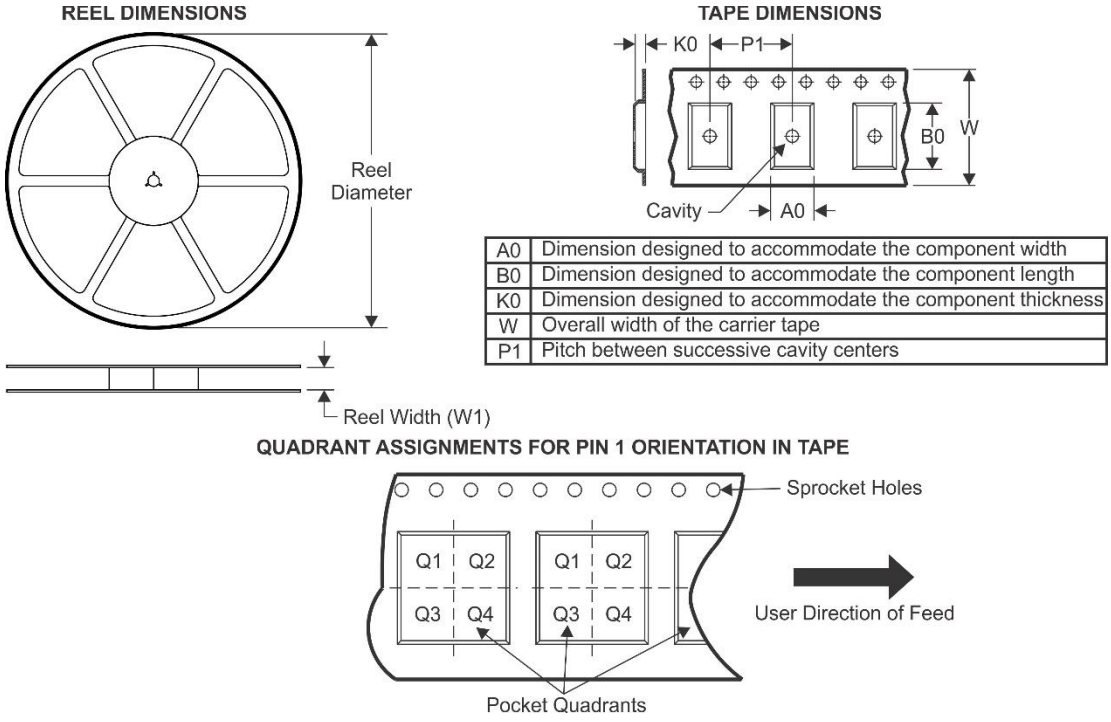


Figure 10: Top View – 3x3 Bump WLCSP IO MAP

13 Tape and Reel Packaging

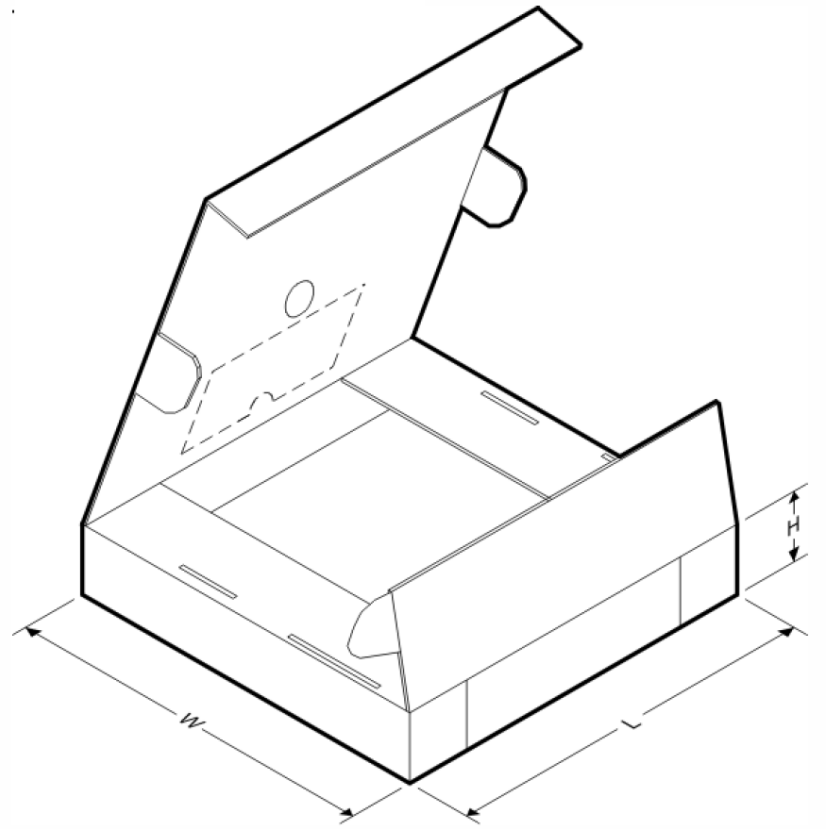
13.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Bumps	Qty / Reel	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
TS4231	WLCSP	9	4000	178.0	9.0	1.85	1.85	0.7	4.0	8.0	Q1

13.2 Tape and Reel Box Dimensions



Device	Package Type	Bumps	Qty / Reel	Length (mm)	Width (mm)	Height (mm)
TS4231	WLCSP	9	4000	215.0	200.0	40.0

Note: All dimensions are nominal

14 Branding

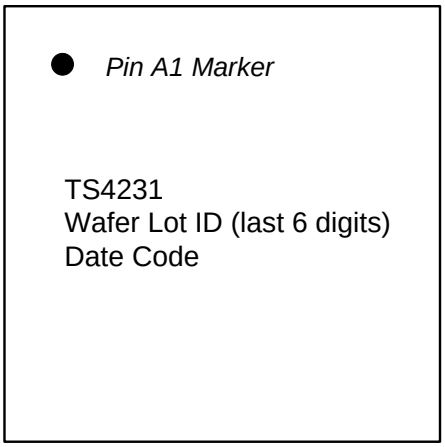


Figure 11: TS4231 Branding Diagram

15 Mechanical, Packaging and Handling Information

Device	Package Type	Bumps	Package Qty	RoHS Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Storage Temp (°C)	Device Marking
TS4231	WLCSP	9	4000	RoHS & no Sb/Br	Cu Sn Ag	Level-1-260C-168 HR	0 to 85	-40 to 150	TS4231

15.1 Electrostatic Discharge Caution

TS4231 is an ESD sensitive device with an HBM rating of Class 1C (2,000V) per JS-001-2014. The device should be placed in conductive foam during storage or handling to prevent damage due to electrostatic discharge. Refer to JESD625 for handling precautions.

15.2 MSL

TS4231 is an MSL1 device per J-STD-020. Refer to J-STD-033 for specific handling requirements and conditions.

15.3 Shelf Life

Shelf life is 12 months as per J-STD-033. Refer to J-STD-033 for additional shelf life information.

16 RoHS

TS4231 fully complies with the RoHS Directive 002/95/EC requirements without exemption and is Halogen-Free as defined by IEC 61249-2-21.

Revision History

Revision	Modifications	Modification Date
A	Initial release Rev A Datasheet	2 Jun 2017

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Triad Semiconductor designs and manufactures analog and mixed signal integrated circuits. Founded in 2002, Triad provides custom IC, ASSP and standard product solutions to customers in all major markets.

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