02-MIPS

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- MIPS
- 2 Exercises

- Microprocessor without Interlocked Pipeline Stages
- Developed in 1981 by John L. Hennessy
- One of the first RISC archetectures
- Common in embedded systems

Signed v. Unsigned

- Signed integers are stored as 2's complement
- Unsigned integers are stored as binary
- The different formats can not be
 - compared
 - used in the same expression
 - safely converted

Co-processor

- Floating point instructions on floating point co-processor
- Co-processor has a separate set of instructions
- For simplicity CPSL does not have floating point support

Load / Store

- li
- la
- lw
- SW

Arithmetic

- add, addi, addu, addiu
- sub, subu
- mult, multu
- div, divu
- mfhi, mflo Used to get results of mult and div

Conditionals

- slt, sltu, slti, sltiu
- and, andi
- or, ori
- nor

Branching

- beq, bne
- j, jr, jal

- 32 registers \$0 \$31
- mnemonic names to help remember usage

Reserved

- \$zero Always 0
- \$at Assembler Temporary
- \$k0, \$k1 Reserved for Kernal

MIPS Exercises

- \$s0-\$s7 Saved Registers
- \$t0-\$t9 Temporary Registers

Function Calls

- \$v0, \$v1 Return values
- \$a0-\$a3 Arguments
- \$ra return address set by jal

Memory Management

- \$gp Global pointer
- \$sp Stack pointer
- \$fp Frame pointer

- The following registers must have the same value after a function call returns as they had before the function call:
 - Saved registers
 - Global pointer
 - Stack pointer
 - Frame pointer
 - Return address
- All other registers are in an unknown state after a function call

- I/O provided by simulator
- put system call number into \$v0
- 1 print integer \$a0 contains integer to print
- 4 print string \$a0 contains address of string
- 5 read integer \$v0 contains integer value
- 8 read string \$a0 contains buffer, \$a1 contains length
- 10 exit

Sum of an Array

Recursive Factorial