NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2021-2022

EE4341 – ADVANCED ANALOG CIRCUITS

November / December 2021 | Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 4 pages.
2. Answer all 4 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.

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1. A common emitter amplifier (biasing circuit not shown) is shown in Figure 1 on page 2. Assume Boltzmann's constant k = 1.38 ×10^{-23} J/K, q =1.6 ×10 $^{-19}$ C, T = 300 K, V_T = 26 mV, I_e = 0.303 mA, $\beta = 100$, $r_{bb'}$ = 100 Ω, R_E = 300 kΩ, R_L = 20 kΩ, R_S = 50 Ω, R_M = 60 kΩ, and the equivalent noise bandwidth is 40 kHz. Neglect flicker noise and capacitive effect.

   Note: For the BJT biased on forward active region: $r_\pi = \frac{V_T}{I_B}$, $g_m = \frac{I_C}{V_T}$.

   (a) Draw the noisy equivalent circuit by looking from point "***a***" to the output.

   (5 Marks)

   (b) Calculate the equivalent input RMS noise voltage and noise current sources of the circuit by looking from point "***a***" to the output.

   (15 Marks)

   (c) Between R_S and the transistor Q (i.e. at point "a"), a transformer can be inserted for noise matching. Determine the optimum transformer turns ratio 1 : N so that the total output noise of the amplifier can be minimized.

   (5 Marks)

Note: Question No. 1 continues on page 2.

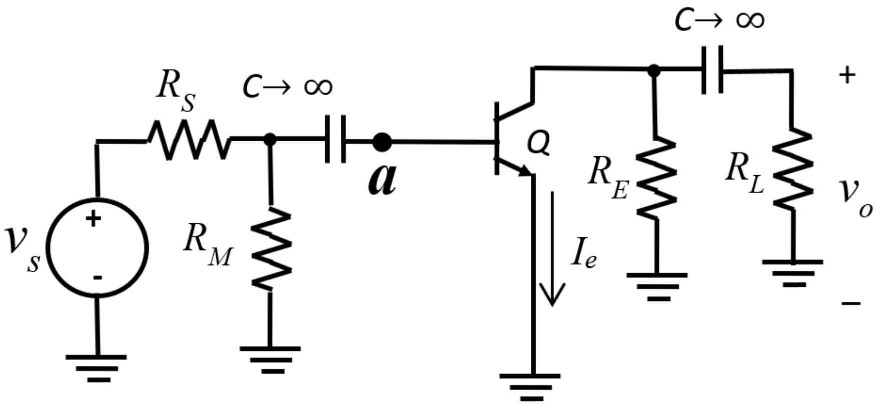


Figure 1

2. For the MOSFET amplifier shown in Figure 2, assume that $V_{DD} = 15$ V, $V_{TN} = 1$ V, $K_n = 1$ mA/V^2, $r_o = \infty$, $R_S = 1$ kΩ, $R_1 = 7$ MΩ, $R_2 = 3$ MΩ, $R_D = 1.5$ kΩ, $R_L = 10$ kΩ, $C_{gd} = 1.2$ pF, $C_{gs} = 0.5$ pF, $C_{ds} = 0.2$ pF and $C_L = 1$ pF. The transistor M_1 is same as the transistor M_2.

Note: For the MOSFET biased on saturation region: $I_D = \frac{K_N}{2}(V_{GS} - V_{TN})^2$, $g_m = \sqrt{2K_N I_D}$.

(a) Determine the Q-point for the transistor.

(8 Marks)

(b) Determine the middle-band gain A_v, and the break frequency f_1, f_2 and f_3.

(12 Marks)

(c) Draw the frequency response based on the calculations in (b).

(5 Marks)

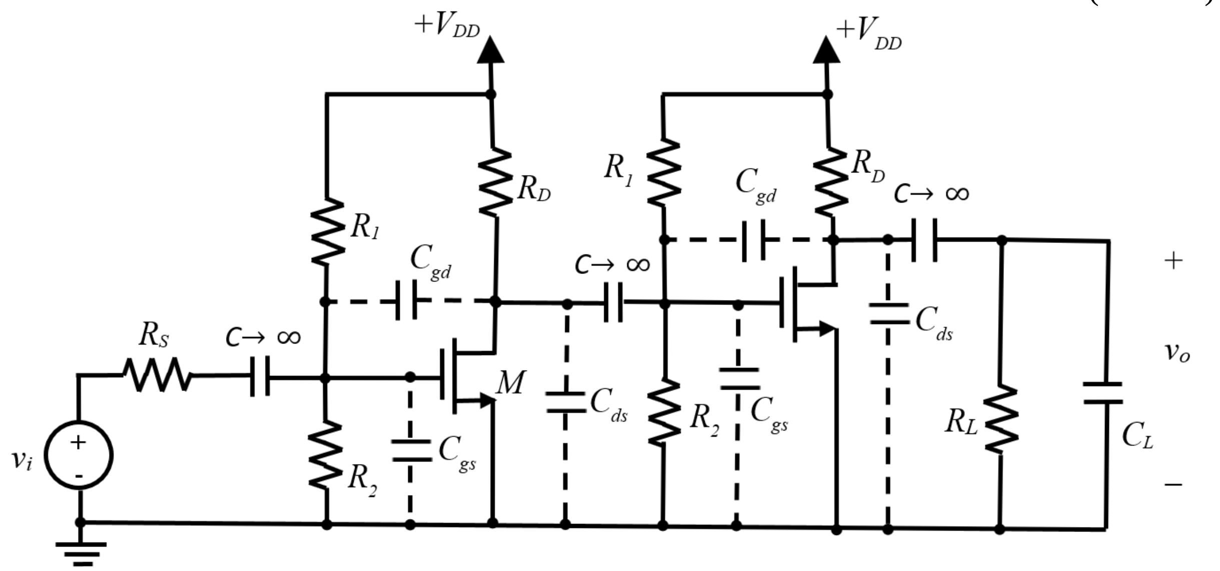


Figure 2

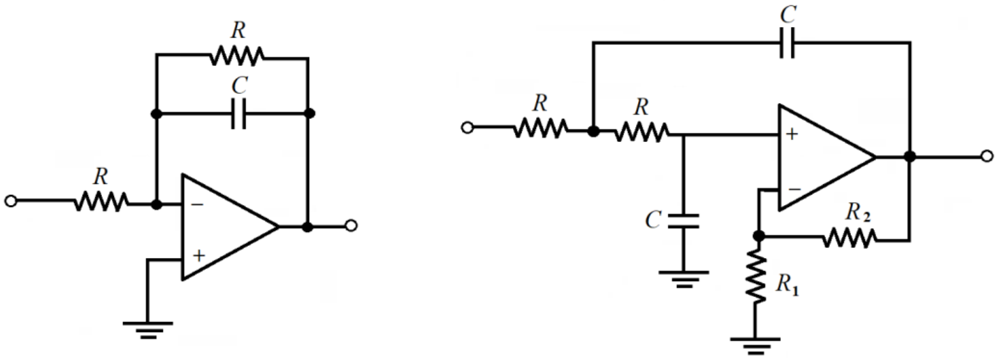
3. Design a Butterworth low pass filter with –3 dB bandwidth of 5 kHz and attenuates an unwanted signal at 30 kHz by at least 50 dB. The transfer function of the Butterworth filter is given by $T(s) = 1/B(s)$, where $B(s)$ for n^{th} order filter is given in Table 1.

   (a) Use one or more of the first order and the second order low-pass filters shown in Figure 3 and additional op-amp circuits to realize the Butterworth low pass filter. In the design, use as many 10 kΩ standard resistors as possible.

   (17 Marks)

   (b) Draw the final Butterworth filter circuit with the values of all capacitors and resistors clearly indicated.

   (8 Marks)



First order low-pass filter   Second order Sallen-Key low-pass filter

Figure 3

Table 1

n	$B(s)$
1	$(s + 1)$
2	$(s^2 + 1.4142s + 1)$
3	$(s + 1)\ (s^2 + s + 1)$
4	$(s^2 + 0.7654s + 1)\ (s^2 + 1.8478s + 1)$
5	$(s + 1)\ (s^2 + 0.61804s + 1)\ (s^2 + 1.6180s + 1)$
6	$(s^2 + 0.5176s + 1)\ (s^2 + 1.4142s + 1)\ (s^2 + 1.9318s + 1)$

4. (a) Figure 4 on page 4 shows an emitter follower that serves as an output stage of a power amplifier to drive a load R_L. It is powered by ± 10 V power supply and R = 1 kΩ. All the transistors are identical with very large current gain. Assume V_{BE} = 0.7 V and $V_{CE(sat)}$ = 0.2 V.

   (i) Determine the value of R_L to achieve maximum possible output voltage swing.

   (6 Marks)

Note: Question No. 4 continues on page 4.

(ii) If the value of R_L is half the value determined in part (i), plot the v_o versus v_i transfer function.

(6 Marks)

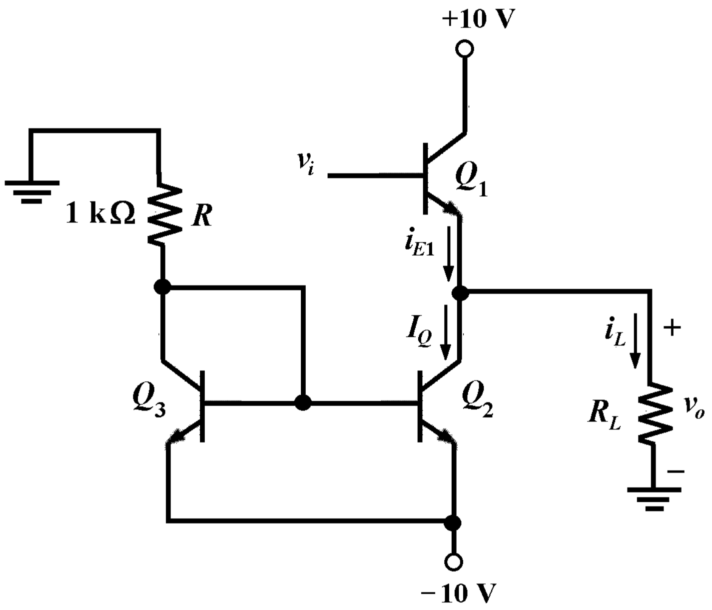


Figure 4

(b) Figure 5 shows a DC-DC Buck converter with an input voltage of 10 V and a load resistor R_L = 10 Ω. The switching frequency f_s of the power MOSFET is 100 kHz. The inductor L = 150 μH and the capacitor C = 6.8 μF. Assume that all the components in the converter circuit are ideal and lossless.

(i) Determine the DC output voltage V_o and the ripple voltage for a duty ratio D = 0.4.

(8 Marks)

(ii) For the same duty ratio given in part (i), will the converter still operate in continuous current mode if the switching frequency f_s reduces to 10 kHz?

(5 Marks)

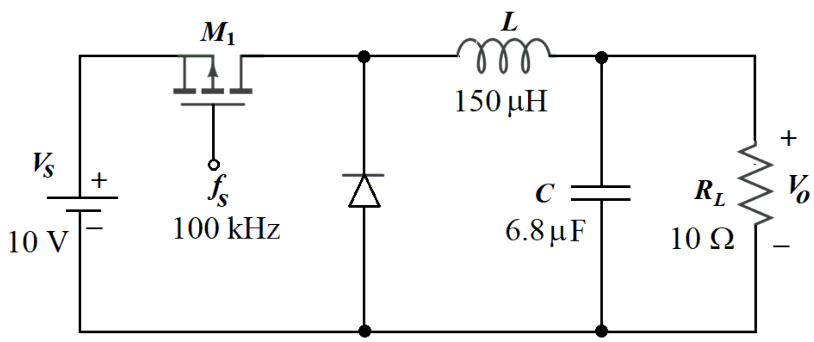


Figure 5

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