NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2023-2024

EE4341 – ADVANCED ANALOG CIRCUITS

November / December 2023 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 5 pages.
2. Answer all questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.

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1. A common emitter amplifier is shown in Figure 1 on page 2 (biasing circuit not shown). Assume Boltzmann's constant $k = 1.38 \times 10^{-23}$ J/K, $q = 1.6 \times 10^{-19}$ C, $T = 300$ K, $V_T = 26$ mV, the equivalent noise bandwidth is 100 kHz, $I_C = 0.4$ mA, $\beta = 100$, $r_{bb'} = 100\ \Omega$, $R_S = 100\ \Omega$, $R_B = 1.2\ \text{M}\Omega$, $R_C = 15\ \text{k}\Omega$, and $R_L = 500\ \text{k}\Omega$. Neglect flicker noise and capacitive effect.

   Note: For the BJT biased on forwards active region: $r_\pi = \frac{V_T}{I_B}$, $g_m = \frac{I_C}{V_T}$.

   (a) Draw the noisy equivalent circuit from point "***b***" to the output.

   (5 Marks)

   (b) Calculate the equivalent input rms noise voltage and noise current sources of the circuit looking from point "***b***" to the output.

   (14 Marks)

   (c) Derive the relationship between N and R_I so that the total output noise of the amplifier can be minimized.

   (3 Marks)

   (d) What is the condition and the value of R_I that the minimal N can be achieved? What is the minimal N?

   (3 Marks)

Note: Question 1 continues on page 2.

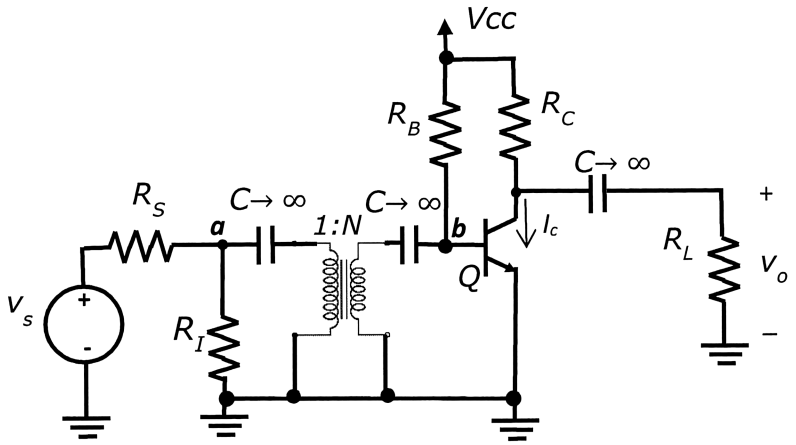

Figure 1

2. For the MOSFET amplifier shown in Figure 2 on page 3, assume that V_{DD} = 10 V, V_{TN} = 1 V, K_n = 2.5 mA/V^2, $r_o = \infty$, R_S = 10 kΩ, R_1 = 3.95 MΩ, R_2 = 1.406 MΩ, R_D = 2.42 kΩ, R_L = 1 MΩ, C_{gd}= 1 pF, C_{gs}= 0.5 pF, C_{ds}= 0.3 pF, and C_L= 1 pF.

   Note: For the MOSFET biased on saturation region: $I_D = \frac{K_N}{2}(V_{GS} - V_{TN})^2$, $g_m = \sqrt{2K_N I_D}$.

   (a) Determine the Q-point for the transistor.

   (8 Marks)

   (b) Determine the middle-band gain A_v, and the break frequency f_1 and f_2.

   (10 Marks)

   (c) Draw the frequency response based on the calculations in (b).

   (5 Marks)

   (d) Discuss the range of C_L that will significantly affect the bandwidth.

   (2 Marks)

Note: Question 2 continues on page 3.

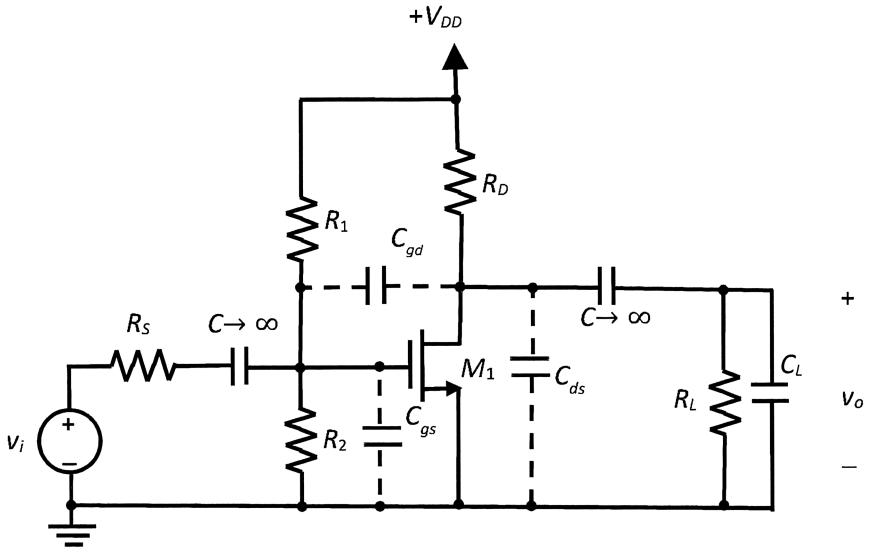

Figure 2

3. Design a Butterworth low pass filter with the frequency response that meets the attenuation requirements shown in Figure 3 on page 4. The transfer function of the Butterworth filter is given by $T(s)=1/B(s)$, where $B(s)$ for n^{th} order filter is given in Table 1 on page 4.

(a) Use one or more first order and second order Salle-Key low-pass filters with other necessary circuits to design the Butterworth low pass filter. Use as many 10 kΩ standard resistors as possible in your design.

(17 Marks)

(b) Draw the final Butterworth filter circuit and clearly indicate the values of all components.

(4 Marks)

(c) What are the advantage and the disadvantage of the Chebyshev low pass filter as compared with the Butterworth low pass filter?

(4 Marks)

Note: Question 3 continues on page 4.

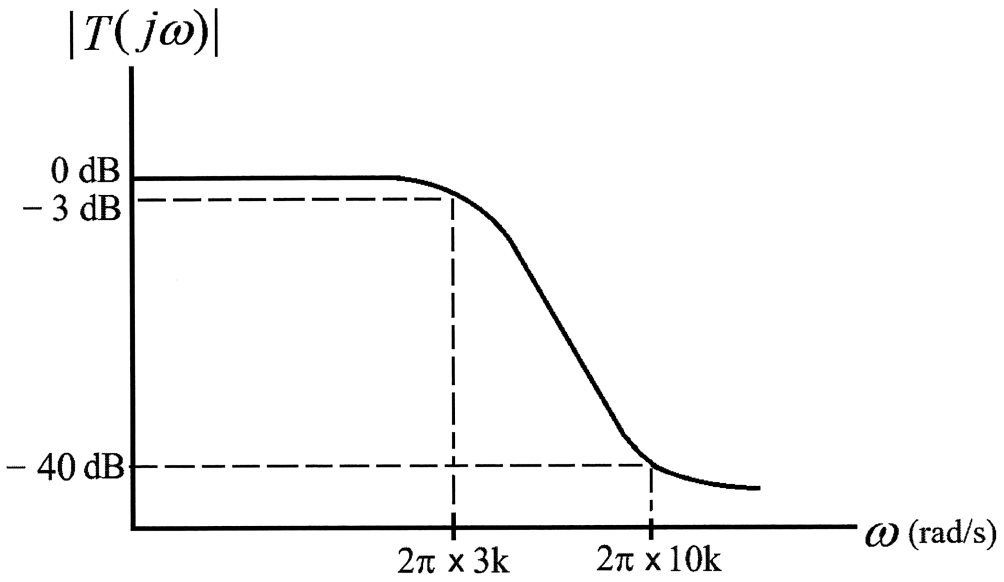

Figure 3

Table 1

n	*B*(*s*)
1	$(s + 1)$
2	$(s^2 + 1.4142s + 1)$
3	$(s + 1)(s^2 + s + 1)$
4	$(s^2 + 0.7654s + 1)(s^2 + 1.8478s + 1)$
5	$(s + 1)(s^2 + 0.61804s + 1)(s^2 + 1.6180s + 1)$
6	$(s^2 + 0.5176s + 1)(s^2 + 1.4142s + 1)(s^2 + 1.9318s + 1)$

4. (a) Figure 4 on page 5 shows an output stage of a power amplifier to drive a load R_L. It is powered by ± 9 V power supply with a biasing resistor R = 830 Ω. All the three transistors Q_1, Q_2 and Q_3 are identical with very large current gain. Assume V_{BE} = 0.7 V and $V_{CE(sat)}$ = 0.2 V for all the three transistors.

(i) What is the value of R_L to achieve maximum possible output voltage swing?
(6 Marks)

(ii) For the value of R_L determined in part (i), calculate the conversion efficiency of the output stage?
(6 Marks)

Note: Question 4 continues on page 5.

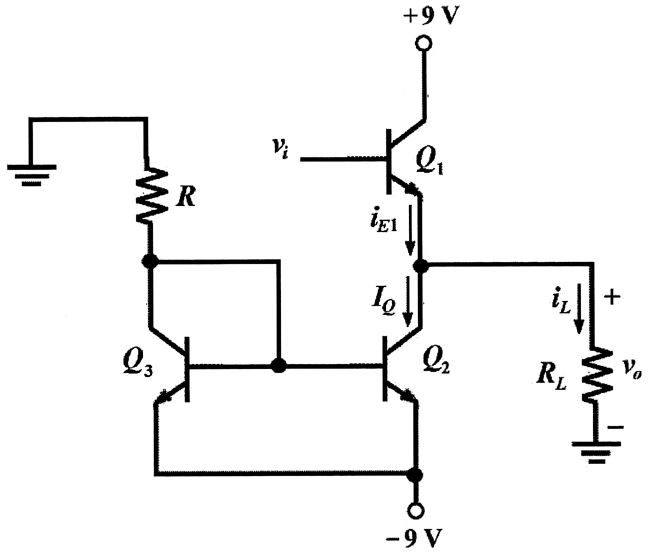

Figure 4

(b) Figure 5 shows a buck-boost DC-DC converter operating at a switching frequency f_s = 100 kHz. The input DC voltage V_s = 10 V and the load resistance R = 20 Ω. The values of the inductor L and the capacitor C are 100 μH and 50 μF respectively. Both L and C are assumed to be lossless. The diode D_1 and the transistor Q_1 are assumed to be ideal.

(i) For DC output voltage V_o = – 4.5 V, what is the required duty ratio D of the switching cycle? Determine the output ripple voltage.

(7 Marks)

(ii) Plot the waveform of the inductor current i_L and clearly indicate its maximum and minimum values.

(6 Marks)

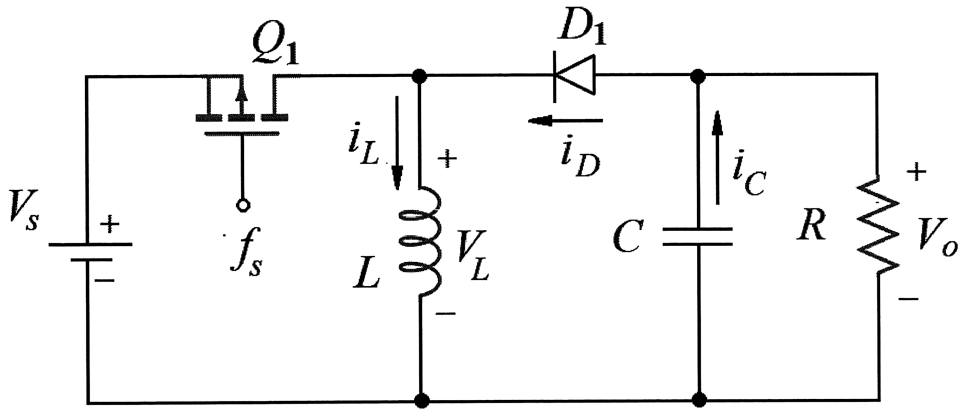

Figure 5

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.