OpenPCells

A Technology-Indendent Layout Generator for Integrated Circuits

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Introduction

Technology Mapping

Code

Examples

Motivation

- Design re-use quite poor in analog design
- Still many repetitive tasks, especially in layout
- Designs usually subject to restrictive non-disclosure agreements

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Goals

- Enable design re-use
- Provide reference implementations of common circuits
- Port complex systems to other technology nodes
- Share circuits with other researchers/companies/...

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Difficulties in Layout Automation for Integrated Circuits

- Integrated circuits are complex
- Many, many, many different ways to do the same thing
- Even more design rules, especially in modern technology nodes

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Principles of Maintainable Circuit Layouts

- 1. Simplify the schematic
- 2. Simplify the schematic
- 3. Simplify the schematic
- 4. DRY in layout (don't repeat yourself)
 - ► Draw everything only once (instances, vias, etc.)
 - ▶ Make extensive use of symmetry, only draw half/quarter/... layouts
 - Find minimum common representation of sub-blocks (e.g. transistors without implants)
 - ► Hard to do and can result in very steep instance hierarchies
 - More special cases make this even harder

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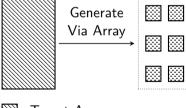
Examples

Vias and Contacts

Resolve via cuts with set of simple rules

• Fit via:
$$R = \left[\frac{W + S_{\min} - 2 \cdot E_{\min}}{C + S_{\min}}\right]$$

• Continuous via: $R = \left\lfloor \frac{W + S_{\min} - 2 \cdot E_{\min}}{C + S_{\min}} \right\rfloor$



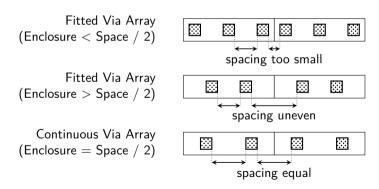
Target Area

🔯 Via Cut Layer

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Continuous Vias

- Simple cut fitting not suitable in some applications (for example merging/aligning guard rings)
- Specialized via translation ensures equal spacing



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Basic Cell Code

```
function parameters()
    -- parameter definitions go here
end
function layout (cell, P, env)
    -- layout descriptions go here
end
function config()
    -- special stuff
end
```

- Cells are described by defining public (global) functions
- Every cell *must* define layout()
- parameters() defines the parameters of the cell (and some minor other things)
- A cell without any parameters always represents the same layout
- In rare cases, config() is used, but this is only required for special cells

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Adding Parameters

```
function parameters()
   pcell.add_parameter("width", 100)
   pcell.add_parameter("height", 100)
end
```

or with a shorthand:

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Parameters - Allowed Values

- Per default, numeric parameters can take any values
- Allowed parameters can be limited to even or odd values, intervals (interval) or explicit sets (set)

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The Layout Function

- First argument is the cell buing built (it is created by the calling code)
- The first argument is in theory optional, but a cell without a cell argument makes no sense
- Second (optional) argument is the table holding all parameters with their current value (default or user-given values)
- Third (optional) argument is the environment, similar to parameters but concerns values that are defined by cell higher up in the hierarchy

```
function layout(cell, _P, env)
end
```

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Adding Shapes

- Basic shapes are added with the geometry module
- All geometry functions take the cell as first argument
- The layer as second argument
- Shape parameters (for example width and height for a rectangle) as remaining parameters

```
function layout(cell)
    geometry.rectangle(cell, layer, 100, 100)
end
```

But what do we put into the layer?

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- Shapes need to have layer information
- Can't put in specific technology layers (for example metal 1)
- Can't put in layers for the specific format (for example GDSII)
- Need a system to represent chip layers technology-independent and format-independent
- This is achieved by using *generic* layers

```
function layout(cell)
    geometry.rectangle(cell, generics.metal(1), 100, 100)
end
```

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- Metals indexed by a number (1 being at the bottom of the metal stack, closest to the bulk wafer)
- Generic layers for gates, active regions, implants, threshold voltage markings, oxide thickness
- Generics layers are translated into specific technology-bound layers
- Mapping described in layermap file with simple syntax
- Layermap has to be created for every technology node

Layermap example with only one layer (gate):

```
return {
    gate = { layer = { gds = { layer = 6, purpose = 0 } } },
    -- more layers here
}
```

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- The technology layermap can define various export types (output formats)
- Most important is currently gds (GDSII)

More complex layermap example with only one layer (gate):

```
return {
    gate = {
        name = "poly",
        layer = {
            gds = { layer = 6, purpose = 0 },
            SKILL = { layer = "poly", purpose = "drawing" },
            svg = { style = "gate", order = 3, color = "ff0000" },
        }
    }
}
```

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- Unused layers can be marked as empty
- For example, non-SOI (silicon-on-insulator) technology nodes don't need a buried-oxide break (soiopen)

```
return {
    soiopen = {}, -- will be skipped
}
```

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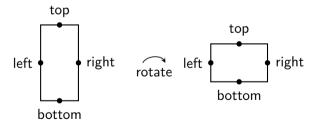
Cell Hierarchies

- Often-used cells more efficiently represented by hierarchies (re-use)
- Put sub-layouts in objects (object.create()) or re-use existing cells with (pcell.create_layout())
- Create a reference handle with pcell.add_cell_reference(ref, name)
- Use object.add child() to instantiate this reference
- The (light/proxy) object returned by object.add_child() can be use as a regular object (transformed, aligned, etc.)

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Object Alignment Boxes

- Define an object's main boundary (rectangular)
- Align with other similar objects (for example digital standard cells)
- Provide standardized means of object positioning
- Alignment boxes are not transformed (rotated, mirrored, flipped)



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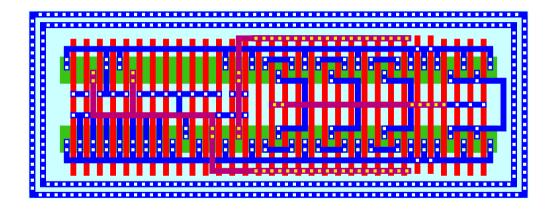
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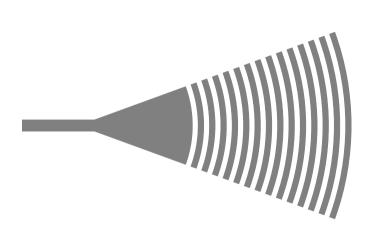
Examples

Current-Starved Ring Oscillator



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Grated Coupler



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