Scalar Efficiency SIG Meeting

April 18, 2024

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Agenda

- Update on charter
- Discuss processor types / metrics / workloads
- Introduction to instruction database

Charter

- Krste considers instructions expected to be **handwritten and applicable to multiple domains** out of scope.
- Derek's recommendation:
  - Revert to **targetable by a compiler code generator or builtin function**
  - If we discuss any instructions that do not fit that scope, we can assist in setting up a TG under a different SIG/HC/IC.

Processor types

Microcontroller	App
1. In-order implementation 2. (Relatively) low frequency 3. First-order constraints (metrics): ◦ Static code size ◦ Area 4. Second-order constraints (metrics): ◦ Dynamic code size ◦ Performance ◦ Power 5. Suggested workloads: ◦ EEMBC ◦ Zephyr OS (for code size)?	1. Up to wide out-of-order implementation 2. High frequency 3. First-order constraints (metrics): ◦ Performance ◦ Power 4. Second-order constraints (metrics); ◦ Dynamic code size ◦ Area 5. Third-order constraints (metrics): ◦ Static code size 6. Suggested workloads: ◦ SPEC CPU 2017 ◦ Android Open Source Project (AOSP) — For code size ◦ Speedometer (browser)

Metrics

Breadth

- Workload
  - Individual benchmark?
    - What’s an "important" benchmark?
  - Average on a suite?
- Per-instruction or per-extension?

Code Size

- % reduction per codepoint (*e.g.*, 1% / 0.1% SROS)?

Performance

- Need accepted performance model **or** real hardware (*e.g.* from vendor custom extension) *

Instruction database

- Instruction database has been started:
  1. Review fields
- Looking for contributions

Next steps

- Submit charter + call for Chair/Vice-chair
- Collect instructions, start dedup + categorizing
- Discuss methodology