National Semiconductor

June 1989

9602/DM9602 Dual Retriggerable, Resettable One Shots

General Description

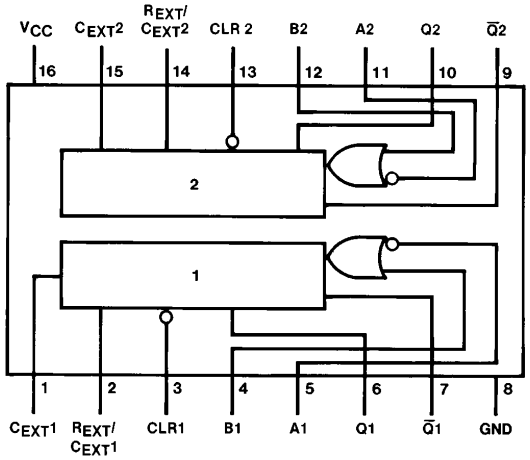
These dual resettable, retriggerable one shots have two inputs per function; one which is active high, and one which is active low. This allows the designer to employ either leading-edge or trailing-edge triggering, which is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is allowed to rapidly discharge and then charge again. The retriggerable feature permits output pulse widths to be extended. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. The output pulse may then be terminated at any time by applying a low logic level to the RESET pin. Retriggering may be inhibited by either connecting the Q output to an active high input, or the $\overline{Q}$ output to an active low input.

Features

- 70 ns to ∞ output width range
- Resettable and retriggerable—0% to 100% duty cycle
- TTL input gating—leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for V_{CC} and temperature variations
- Alternate Military/Aerospace device (54xxx) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6611–1

Order Number 9602DMQB, 9602FMQB or DM9602N
See NS Package Number J16A, N16E or W16A

Function Table

Pin No's.			Operation
A	B	CLR	
H → L	L	H	Trigger
H	L → H	H	Trigger
X	X	L	Reset

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	$T_A = -55°C$	2						V
		$T_A = 0°C$				1.9			
		$T_A = 25°C$	1.7			1.8			
		$T_A = 75°C$				1.65			
		$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage	$T_A = -55°C$			0.85				V
		$T_A = 0°C$						0.85	
		$T_A = 25°C$			0.9			0.85	
		$T_A = 75°C$						0.85	
		$T_A = 125°C$			0.85				
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
T_A	Free Air Operating Temperature		−55		125	0		75	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min (Note 4)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 4)	MIL			0.4	V
			COM			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V				60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	MIL V_I = 0.40V			−1.6	mA
			COM V_I = 0.45V			−1.6	
		V_{CC} = Min	MIL V_I = 0.40V			−1.24	
			COM V_I = 0.45V			−1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max, V_{OUT} = 1V (Notes 2 and 4)	MIL			−25	mA
			COM			−35	
I_{CC}	Supply Current	V_{CC} = Max	MIL		39	45	mA
			COM		39	50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

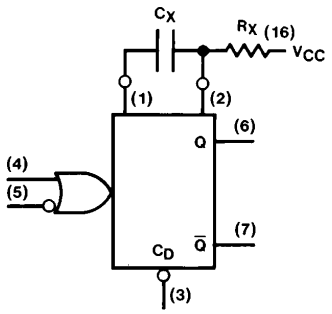
Note 3: Unless otherwise noted, R_X = 10k for all tests.

Note 4: Ground PIN 1(15) for V_{OL} on PIN 7(9) or V_{OH} and I_{OS} on PIN 6(10) and apply momentary ground to PIN 4(12). Open PIN 1(15) for V_{OL} on PIN 6(10) or V_{OH} and I_{OS} on PIN 7(9).

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		Conditions	Military		Commercial		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Negative Trigger Input to True Output	$C_L = 15$ pF, $C_X = 0$, $R_X = 5$ kΩ		35		40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Negative Trigger Input To Complement Output			43		48	ns
t_{PW}(MIN)	Minimum True Output Pulse Width				90		100	ns
	Minimum Complement Pulse Width				100		110	
t_{PW}	Pulse Width		$R_X = 10$ kΩ, $C_X = 1000$ pF	3.08	3.76	3.08	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pins 2, 14 to GND		50		50	pF
R_X	External Timing Resistor			5	25	5	50	kΩ

Logic Diagrams



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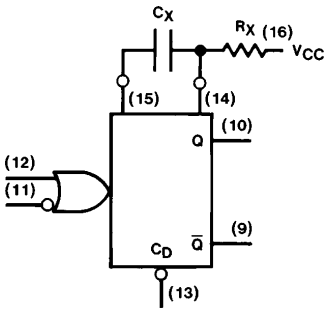

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Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
3. The output pulse with (t) is defined as follows:

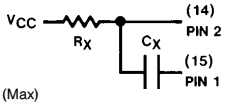
$$t = K R_X C_X \left[1 + \frac{1}{R_X}\right] \quad \text{for } C_X > 10^3 \text{ pF}, \; K \simeq 0.34$$

where: R_X is in kΩ, C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see *Figure 1.*
for K vs C_X see *Figure 6.*

4. If electrolytic type capacitors are to be used, the following three configurations are recommended:

A. Use with low leakage capacitors:

The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0V is less than 3 μA, and the inverse capacitor leakage at 1.0V is less than 5 μA over the operational temperature range.



$R < 0.6\ R_X$ (Max)

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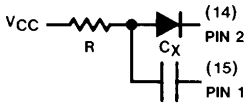
Operating Rules (Continued)

B. Use with high inverse leakage current electrolytic capacitors:

The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$$t \approx 0.3\ RC_X$$



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C. Use to obtain extended pulse widths:

This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

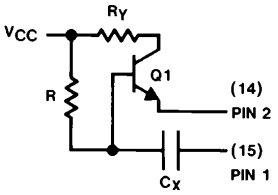
$R < R_X$ (0.7) (h_{FE} Q1) or $< 2.5\ M\Omega$, whichever is the lesser

R_X (min) $< R_Y < R_X$ (max)

($5\ k\Omega \leq R_Y \leq 10\ k\Omega$ is recommended)

Q1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962.

$$t \approx 0.3\ RC_X$$



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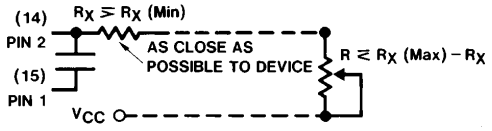
This configuration is not recommended with retriggerable operation.

5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



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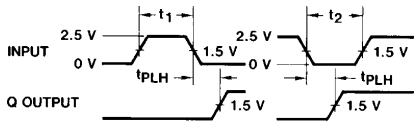
6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

7. Input Trigger Pulse Rules (See Triggering Truth Table)



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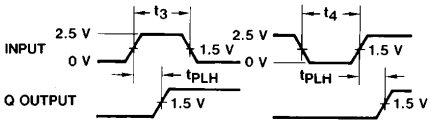
Input to Pin 5(11), (Pin 3(13) = HIGH)

Pin 4(12) = LOW

t_1, t_3 = Min. Positive Input Pulse Width > 40 ns

t_2, t_4 = Min. Negative Input Pulse Width > 40 ns



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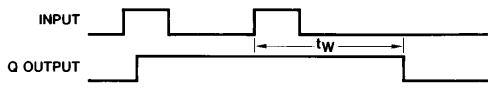
Input to Pin 4(12) (Pin 3(13) = HIGH)

Pin 5(11) = HIGH

8. The retriggerable pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = K\,R_X\,C_X\left(1 + \frac{1}{R_X}\right) + t_{PLH}$$



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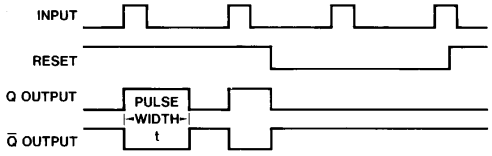
The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t. Retriggering will not occur if the retrigger pulse comes within $\approx 0.3\ C_X$ (ns) after the initial trigger pulse (i.e., during the discharge cycle).

9. Reset Operation—An overriding clear (active LOW level) is provided on each one shot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



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10. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the DM9602 is recommended.

*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

Typical Performance Characteristics

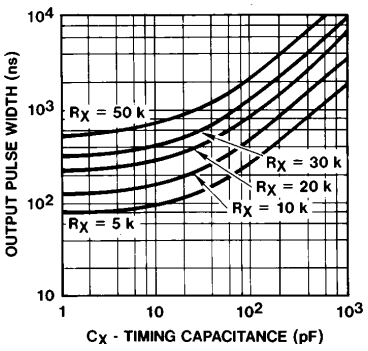

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FIGURE 1. Output Pulse Width vs Timing Resistance and Capacitance for $C_X < 10^3$ pF

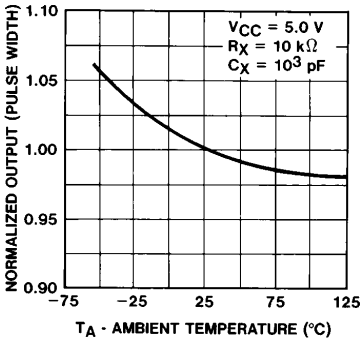

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FIGURE 2. Normalized Output Pulse Width vs Ambient Temperature

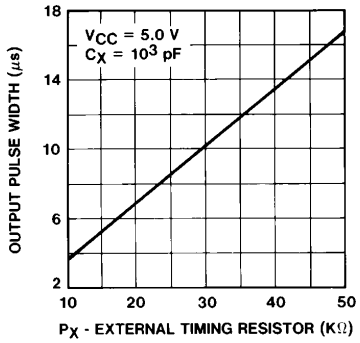

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FIGURE 3. Pulse Width vs Timing Resistor

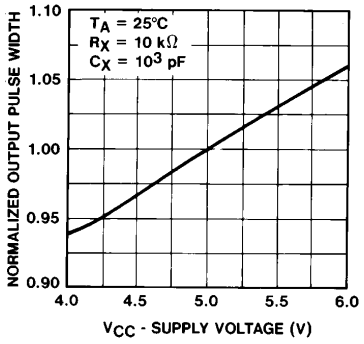

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FIGURE 4. Normalized Output Pulse Width vs Supply Voltage

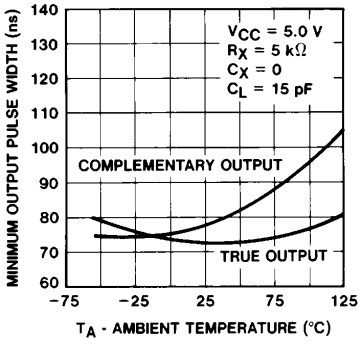

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FIGURE 5. Minimum Output Pulse Width vs Ambient Temperature

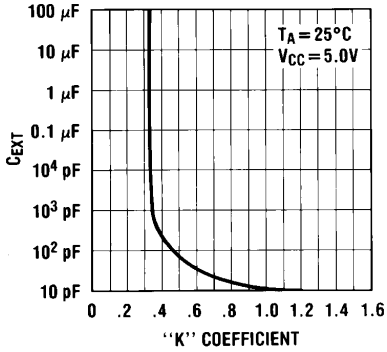

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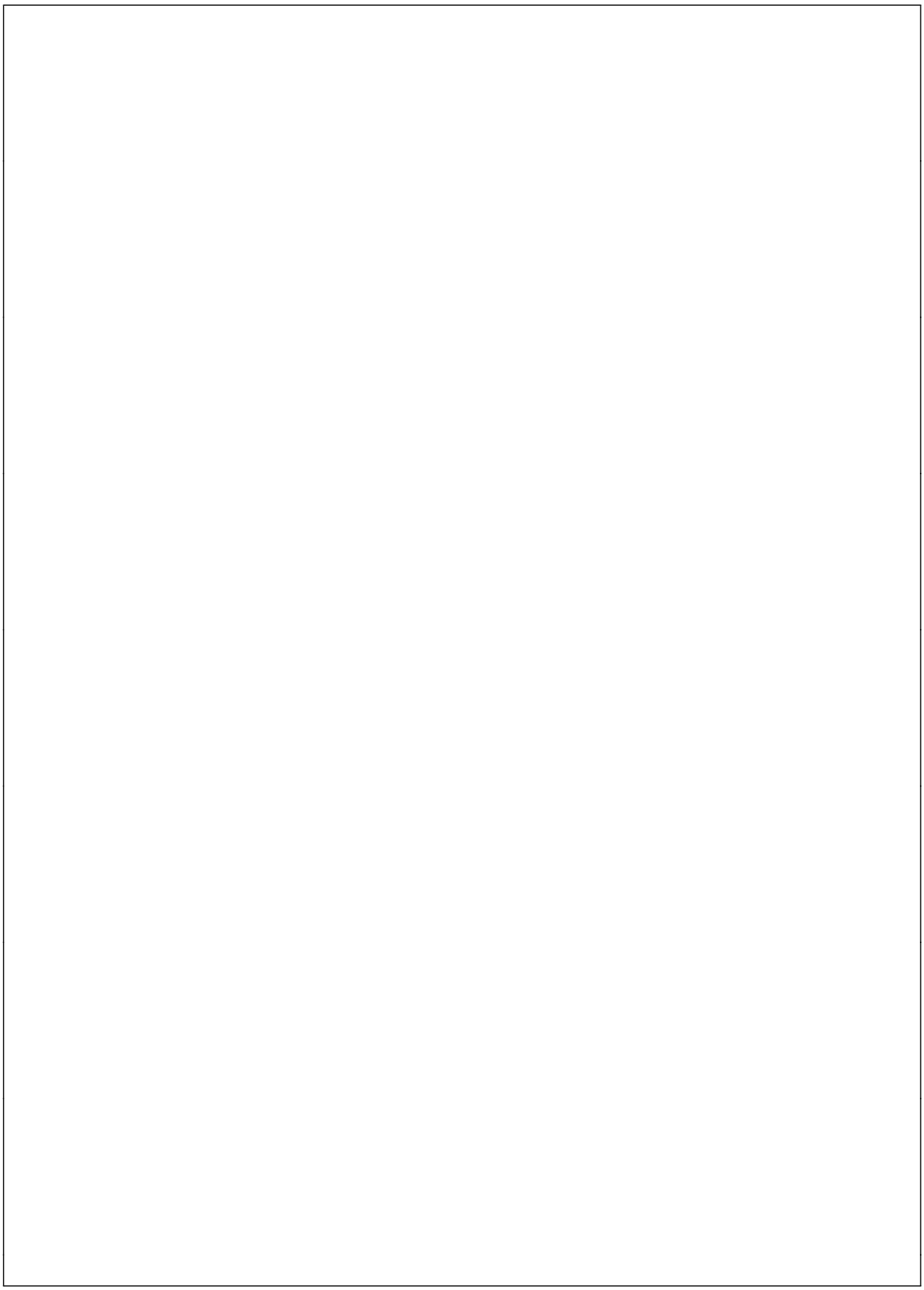
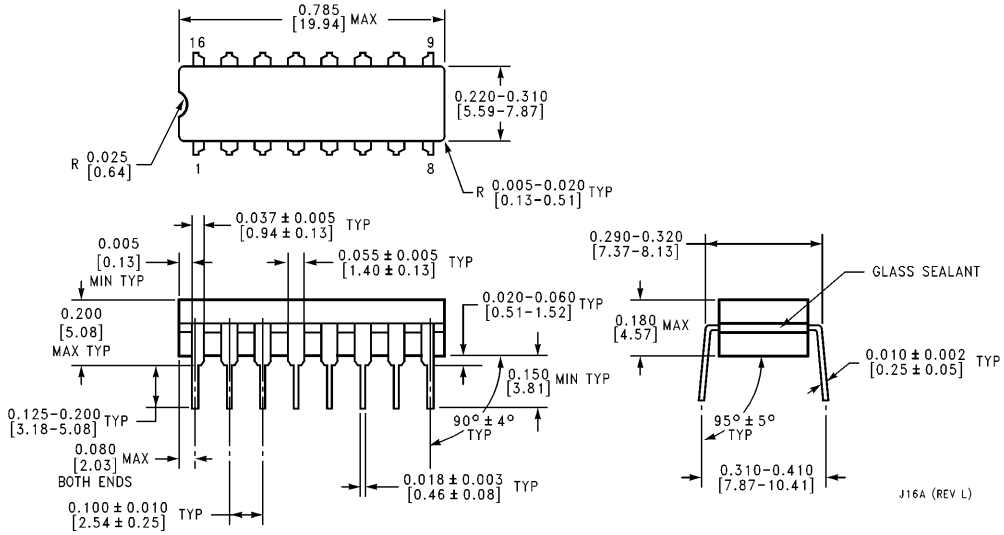
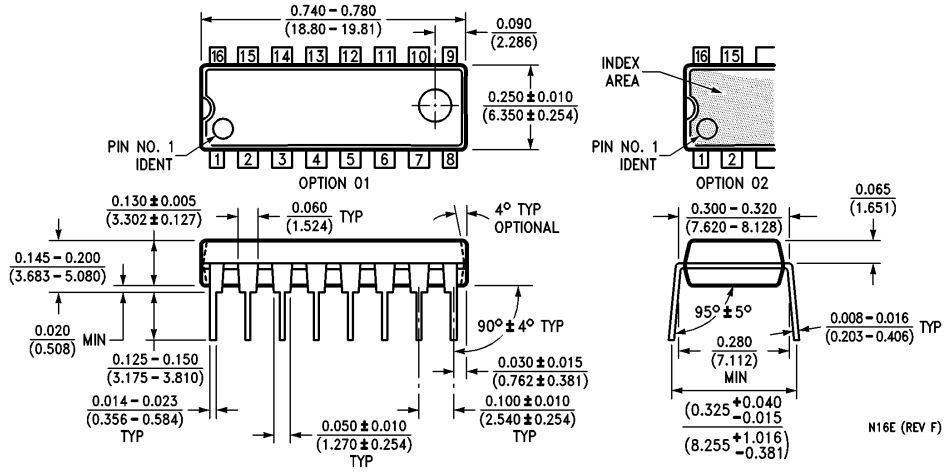
FIGURE 6. Typical "K" Coefficient Variation vs Timing Capacitance



Physical Dimensions inches (millimeters)

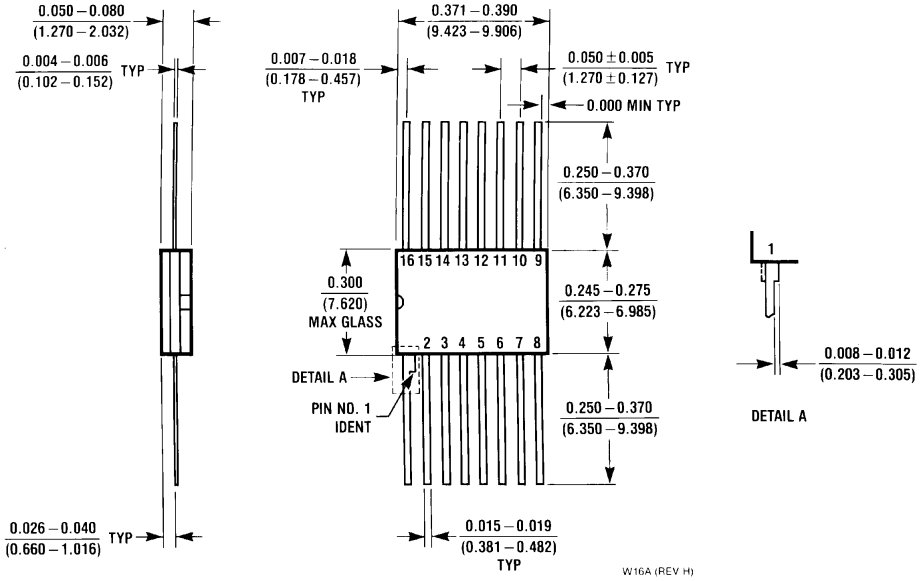


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9602DMQB
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9602N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9602FMQB
NS Package Number W16A

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408