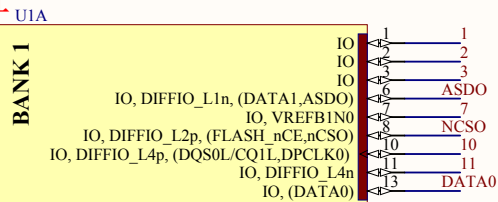
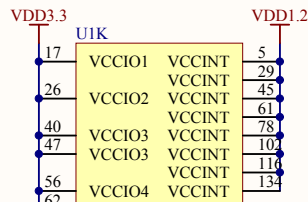


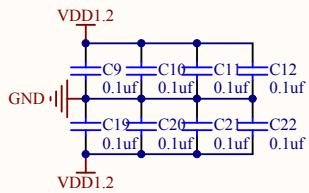
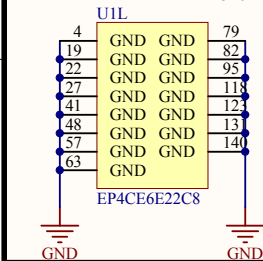
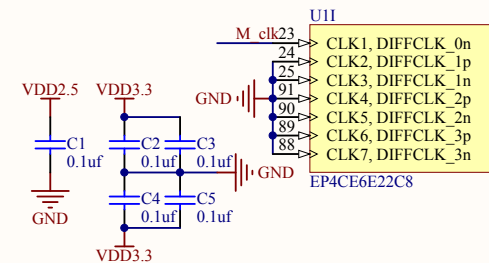
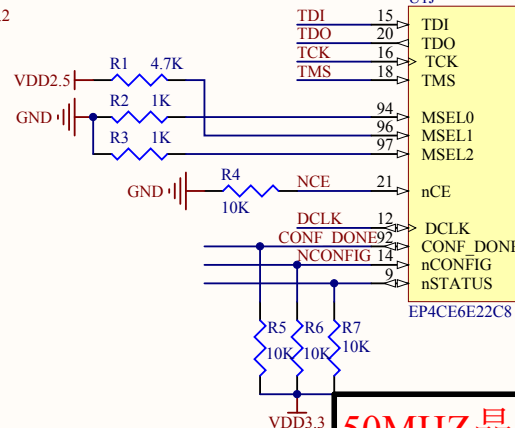
## FPGA配置



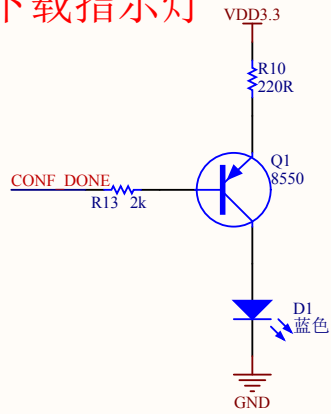
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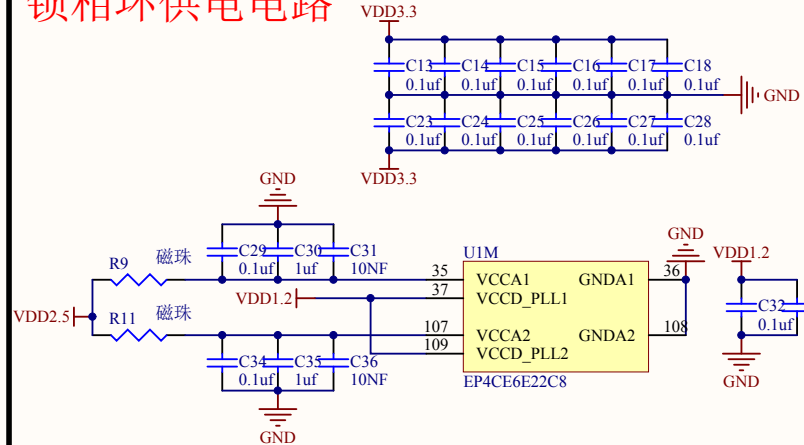
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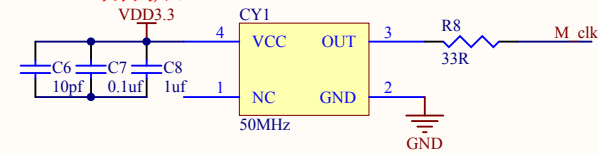
## 下载指示灯



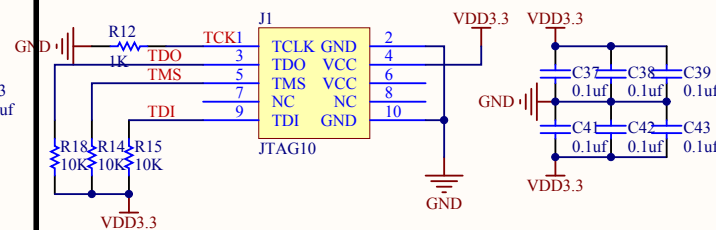
## 锁相环供电电路



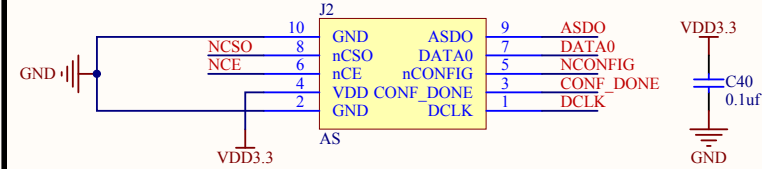
## 50MHZ晶振



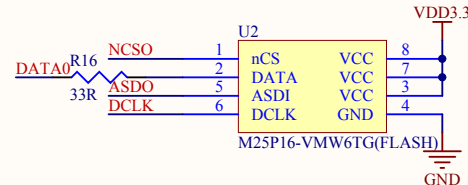
## JTAG配置接口



## AS配置接口



## FPGA程序存储器配置电路



U1B

<b>BANK 2</b>	IO, DIFFIO_L6n	28	28
	IO, DIFFIO_L8p, (DQS1L/CQ1L#,DPCLK1)	30	30
	IO, VREFB2N0	31	31
	IO, RUP1	32	32
	IO, RDN1	33	33
	IO	34	34

EP4CE6E22C8

U1F

<b>BANK 6</b>	IO, DIFFIO_R4n, (INIT_DONE)	98	98
	IO, DIFFIO_R4p, (CRC_ERROR)	99	99
	IO	100	100
	IO, DIFFIO_R3n, (nCEO)	101	101
	IO, DIFFIO_R3p, (CLKUSR)	103	103
	IO, (DQS0R/CQ1R,DPCLK5)	104	104
	IO, VREFB6N0	105	105
	IO, DIFFIO_R1n	106	106

EP4CE6E22C8

U1E

<b>BANK 5</b>	IO	73	73
	IO	74	74
	IO	75	75
	IO, RUP3	76	76
	IO, RDN3	77	77
	IO, VREFB5N0	80	80
	IO	83	83
	IO, DIFFIO_R8n	84	84
	IO, DIFFIO_R8p, (DQS1R/CQ1R#,DPCLK4)	85	85
	IO, DIFFIO_R7n, (DEV_OE)	86	86
	IO, DIFFIO_R7p, (DEV_CLRn)	87	87

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U1D

<b>BANK 4</b>	IO, DIFFIO_B12p	54	54
	IO, DIFFIO_B12n	55	55
	IO, DIFFIO_B15p, (DQ1B)	58	58
	IO, DIFFIO_B16p, (DQ1B)	59	59
	IO, DIFFIO_B16n, (DQ1B)	60	60
	IO	64	64
	IO, VREFB4N0	65	65
	IO, RUP2, (DQ1B)	66	66
	IO, RDN2, (DQ1B)	67	67
	IO, DIFFIO_B20n, (DQS0B/CQ1B,DPCLK3)	68	68
	IO	69	69
	IO, DIFFIO_B21p	70	70
	IO, DIFFIO_B21n	71	71
	IO, DIFFIO_B22p	72	72

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U1G

<b>BANK 7</b>	IO, DIFFIO_T20p, (DQS0T/CQ1T,DPCLK6)	110	110
	IO, DIFFIO_T19p	111	111
	IO, PLL2_CLKOUTn	112	112
	IO, PLL2_CLKOUTp	113	113
	IO, RUP4, (DQ1T)	114	114
	IO, RDN4, (DQ1T)	115	115
	IO, VREFB7N0	119	119
	IO, DIFFIO_T16n, (DQ1T)	120	120
	IO, DIFFIO_T16p	121	121
	IO, DIFFIO_T13p	124	124
	IO	125	125
	IO, DIFFIO_T12n	126	126
	IO, DIFFIO_T12p	127	127

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U1C

<b>BANK 3</b>	IO, DIFFIO_B1p	38	38
	IO, DIFFIO_B1n	39	39
	IO, (DQS1B/CQ1B#,DPCLK2)	42	42
	IO, PLL1_CLKOUTp	43	43
	IO, PLL1_CLKOUTn	44	44
	IO, VREFB3N0	46	46
	IO, DIFFIO_B9p, (DQ1B)	49	49
	IO, DIFFIO_B9n, (DQ1B)	50	50
	IO, DIFFIO_B10p, (DQ1B)	51	51
	IO, DIFFIO_B11p	52	52
	IO, DIFFIO_B11n	53	53

EP4CE6E22C8

U1H

<b>BANK 8</b>	IO, DIFFIO_T11n	128	128
	IO, DIFFIO_T11p	129	129
	IO, DIFFIO_T10n, (DATA2), (DQ1T)	132	132
	IO, DIFFIO_T10p, (DATA3), (DQ1T)	133	133
	IO, DIFFIO_T8n, (DQ1T)	135	135
	IO, VREFB8N0	136	136
	IO, (DATA5), (DQ1T)	137	137
	IO, (DATA6)	138	138
	IO, DIFFIO_T5p	141	141
	IO, DIFFIO_T2p, (DQS1T/CQ1T#,DPCLK7)	142	142
	IO, DIFFIO_T1n, (DQ1T)	143	143
	IO, DIFFIO_T1p, (DM1T)	144	144

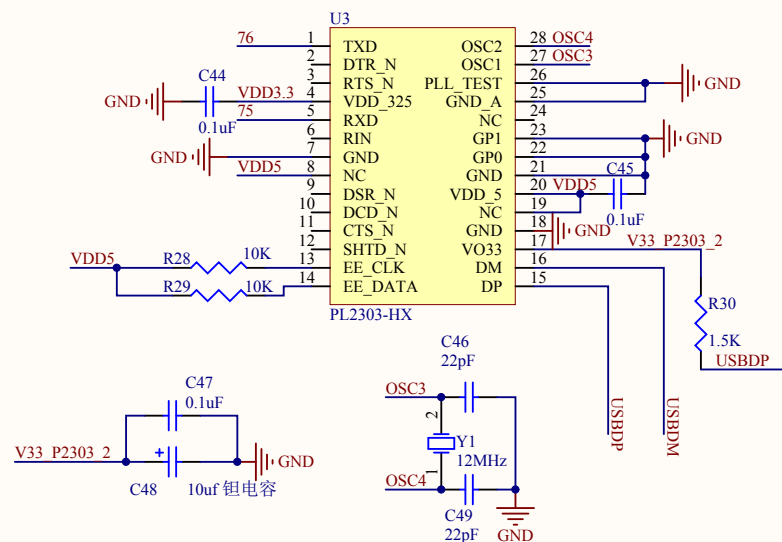
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FPGA管脚分配

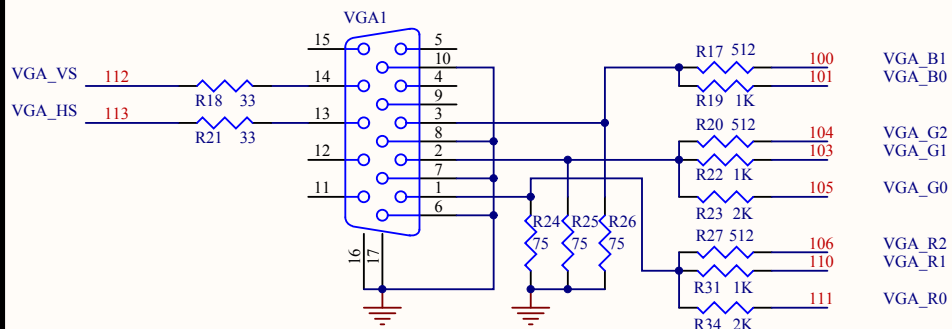


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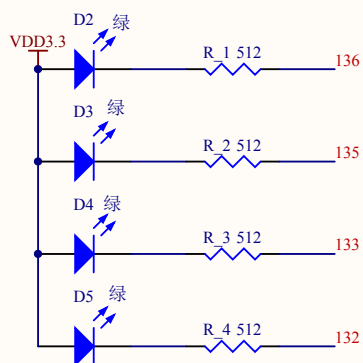
## USB转串口电路



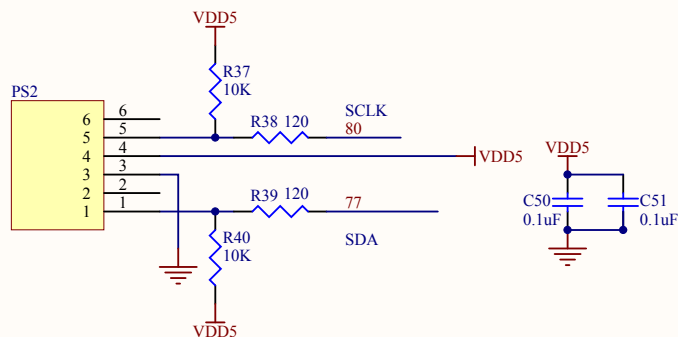
## 256色VGA接口



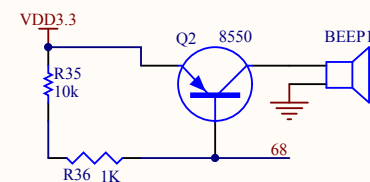
## LED



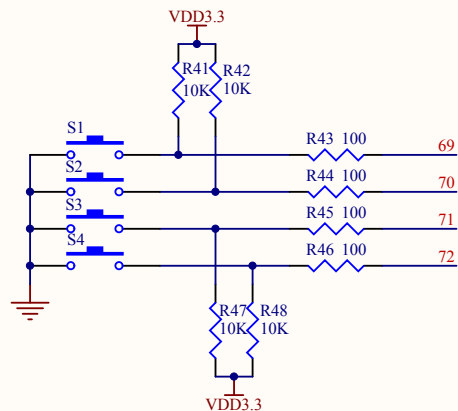
## PS2接口



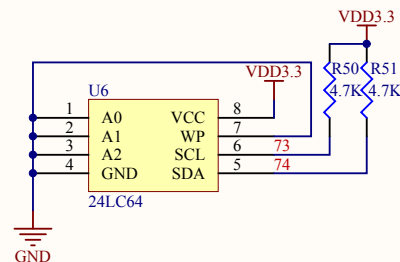
## 蜂鸣器



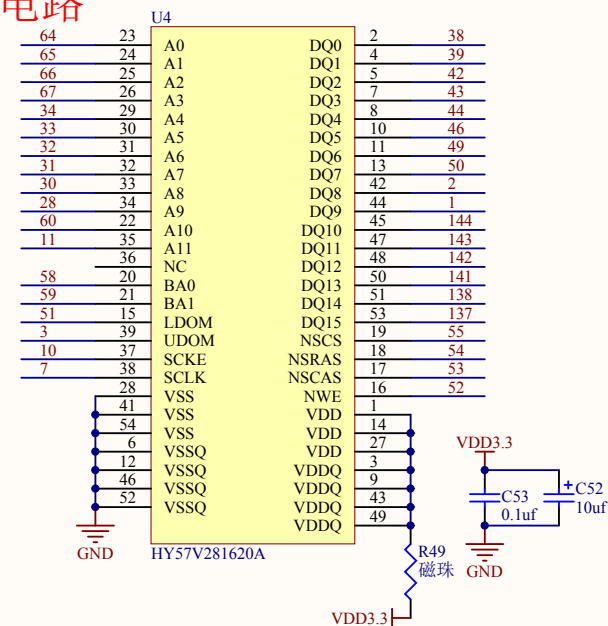
## 四位按键



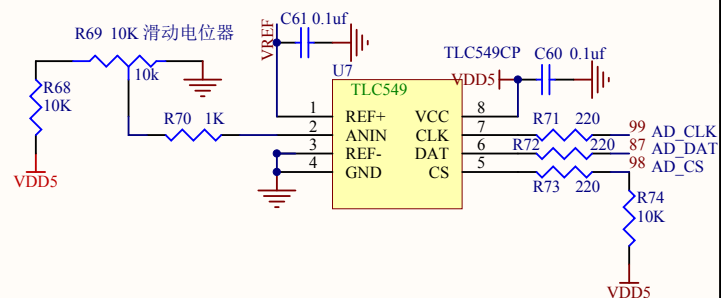
## EEPROM



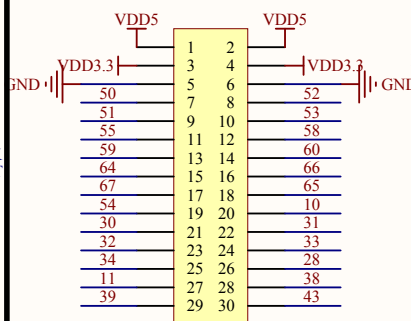
## SDRAM电路



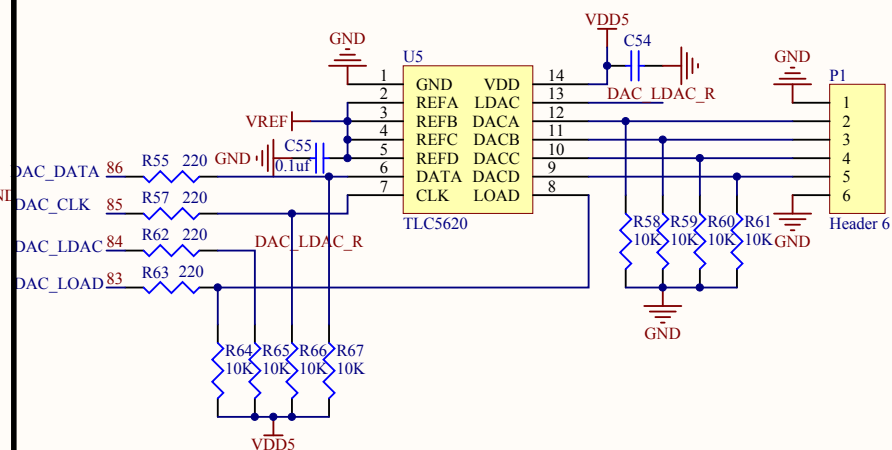
## AD



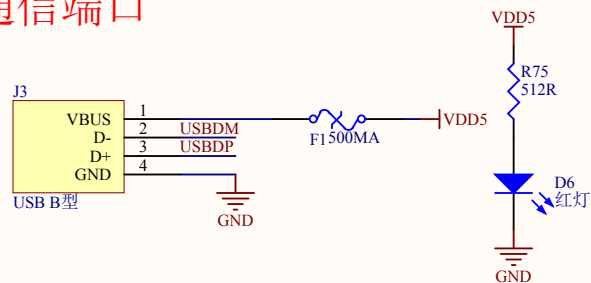
## 接口端子



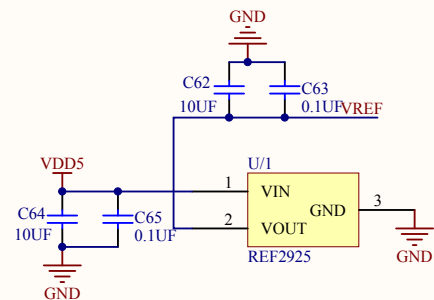
## DA



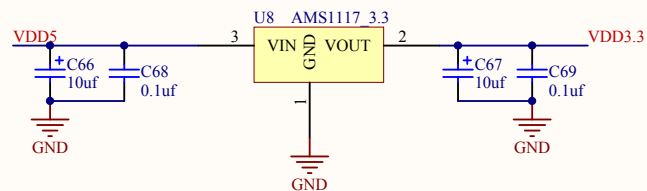
## USB通信端口



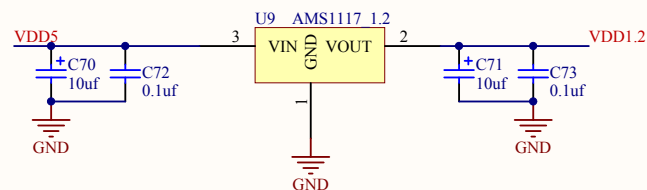
## 2.5V基准源



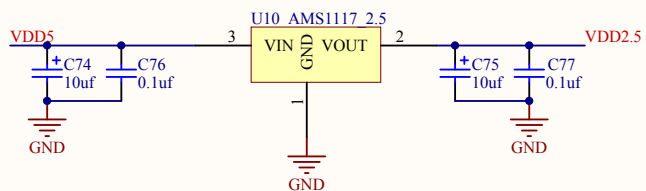
## 5V转数字3.3V电路



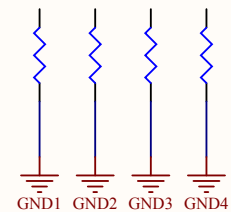
## 5V转数字1.2V电路



## 5V转2.5V电路



## 安装孔



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# 数码管电路

