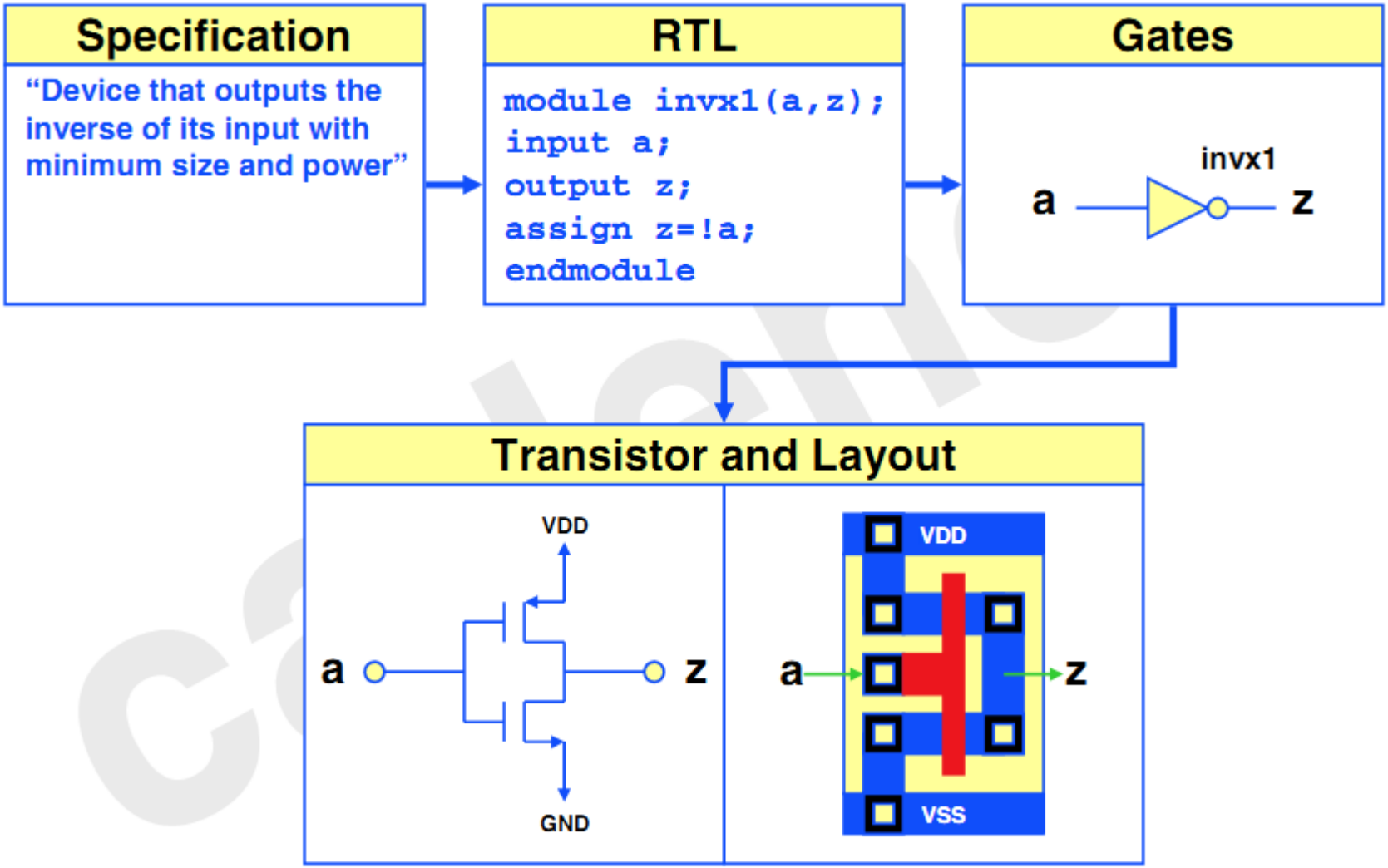
TESTBENCH PARA FPGA

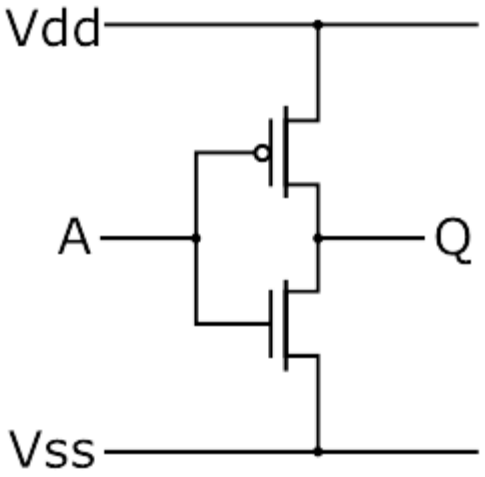
AGENDA

- Introducción sobre microelectrónica
- Niveles de abstracción
- Flujo de diseño
- Síntesis
- Simulación
- VHDL Testbench
- FPGA
- Uso de ISE

CIRCUITOS INTEGRADOS



CIRCUITOS INTEGRADOS



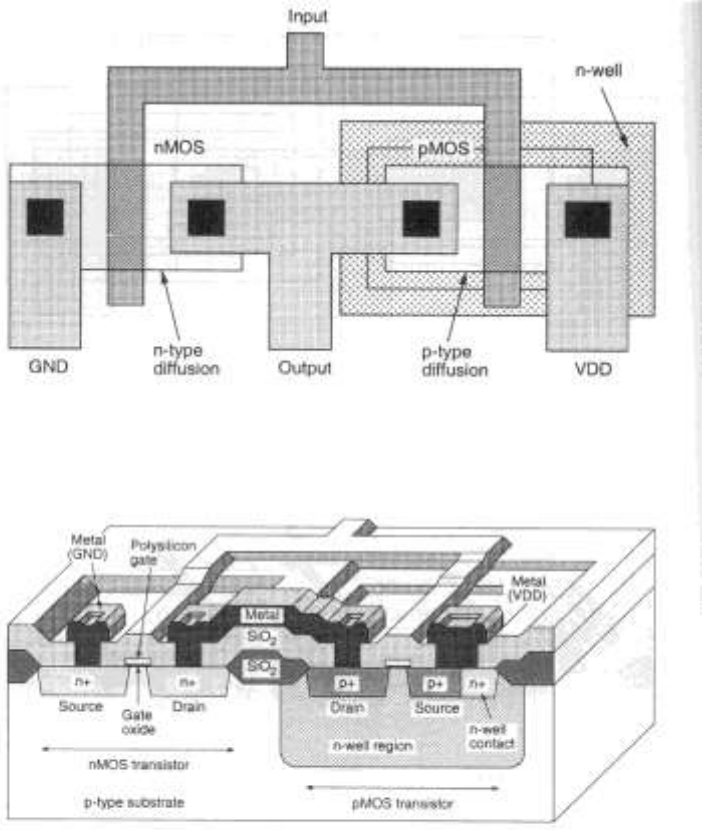
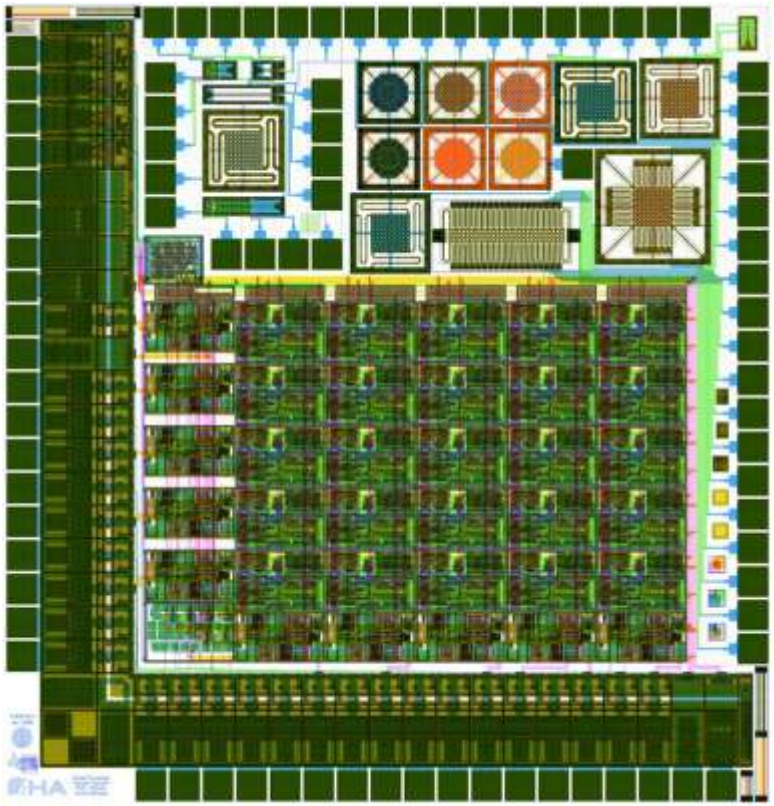


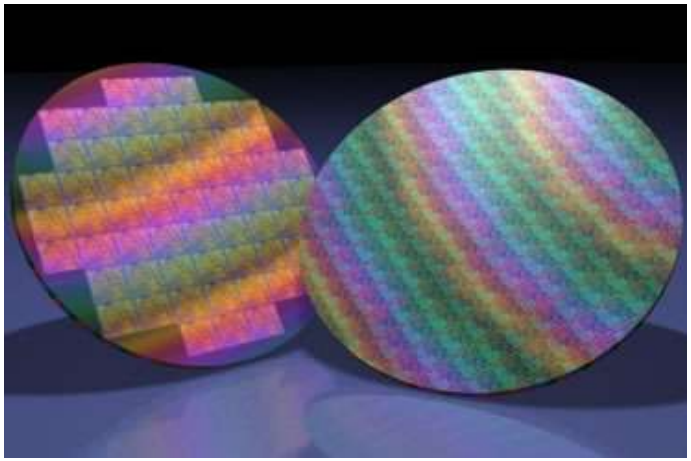
Figure 2.11. The composite layout and the resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (in the n-well), and the polysilicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except over wire-bonding pad areas. After *Atlas of IC Technologies*, by W. Maly [1].

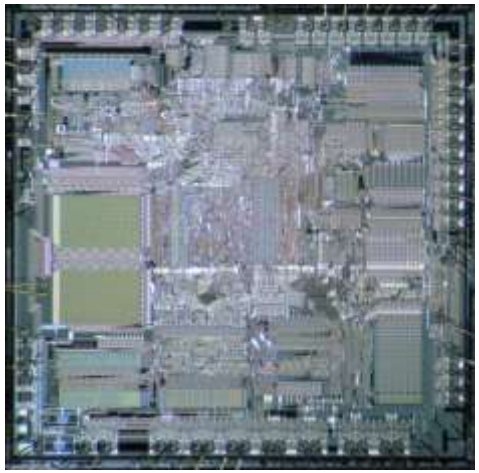
CIRCUITOS INTEGRADOS



NIVELES DE ABSTRACCIÓN

BARRERA DE ABSTRACCIÓN





NIVELES DE ABSTRACCIÓN

Diseño HDL

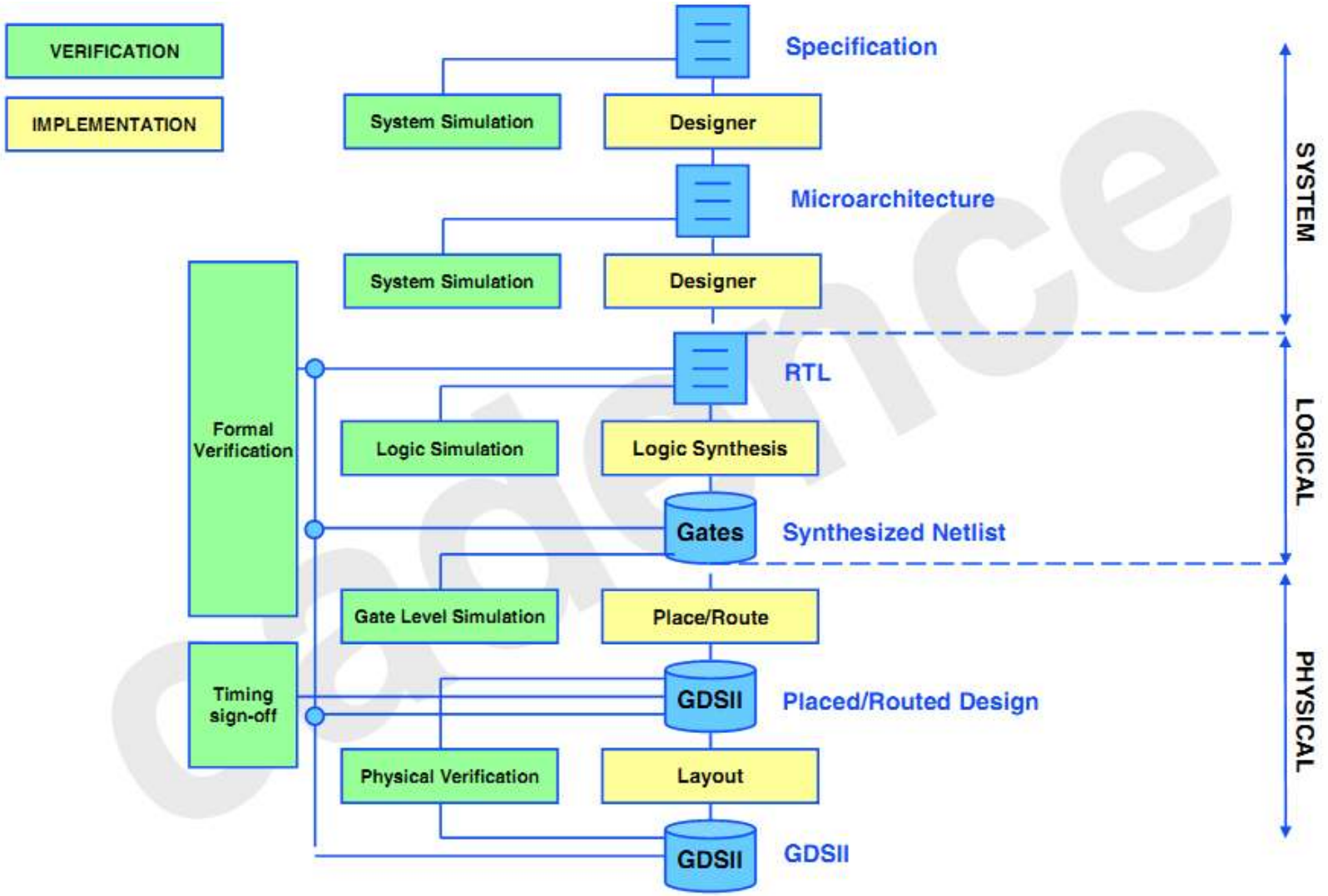
BARRERA DE ABSTRACCIÓN

IBM 65nm

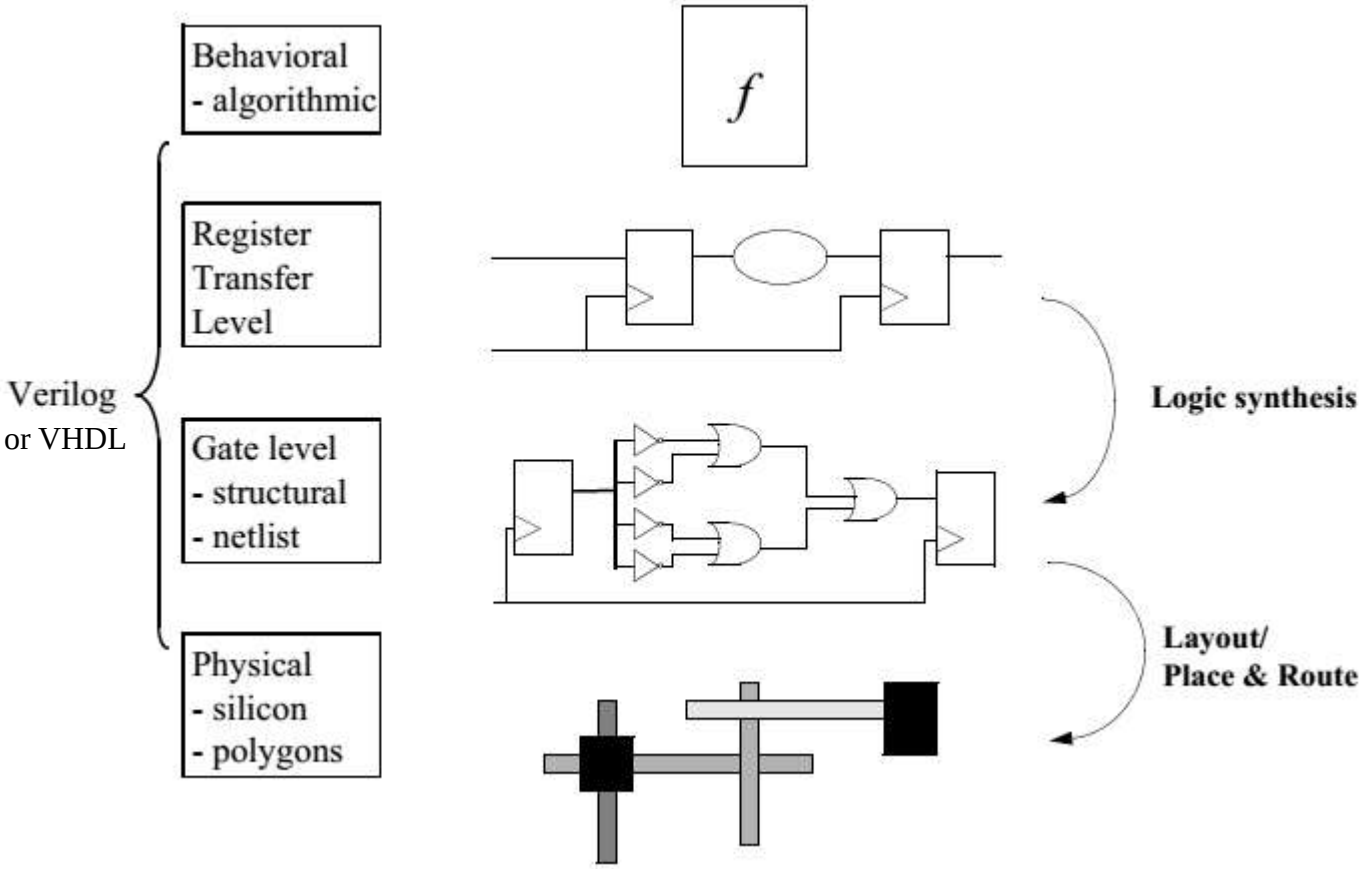
UMC 130nm

45nm

FLUJO DE DISEÑO

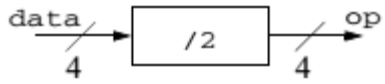


NIVELES DE ABSTRACCIÓN

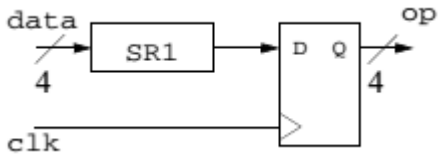


NIVELES DE ABSTRACCIÓN

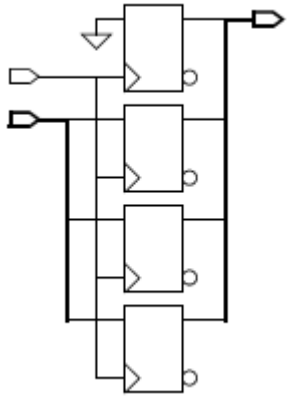
```
1  process (data)
2  begin
3     op <= data/2;
4  end process;
5
6  process (clk)
7  begin
8     if (rising_edge(clk)) then
9        op <= '0' & op(3 downto 1);
10    end if;
11 end process;
12
13 Register : FDRE
14 generic map (
15    INIT => '0')
16 port map (
17    Q => Q,
18    C => C,
19    CE => CE,
20    R => R,
21    D => D
22 );
```



Behavioral

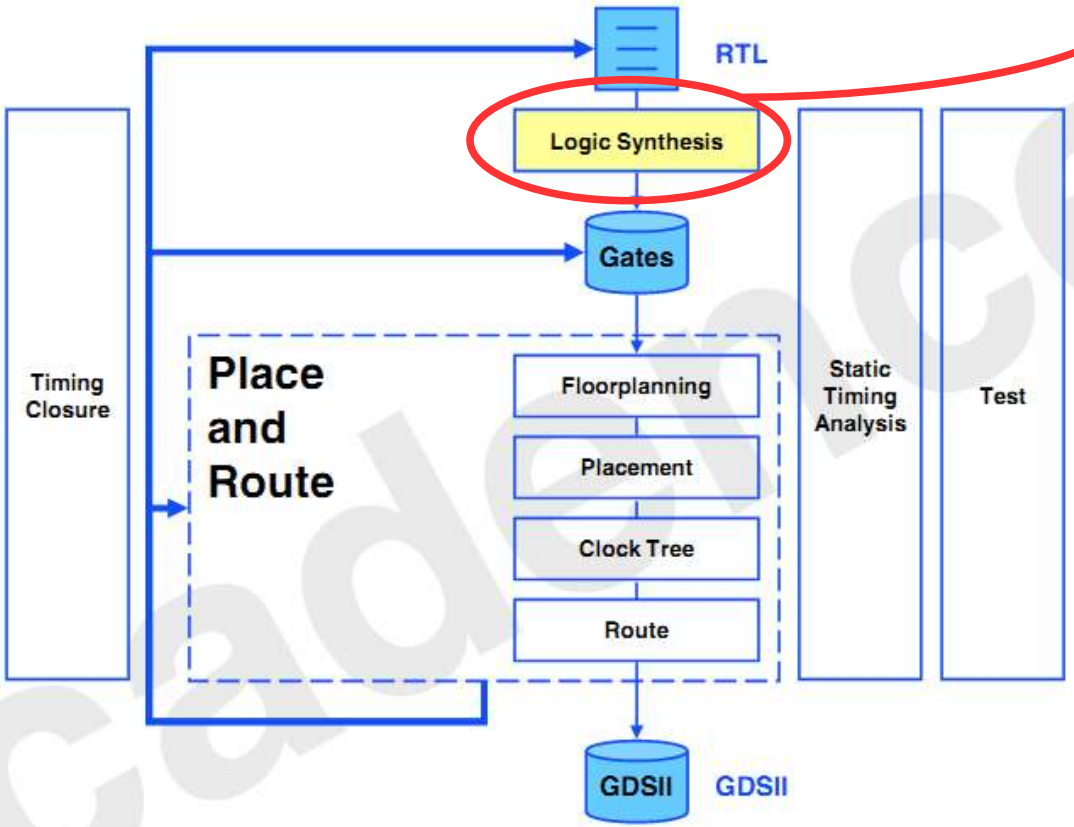


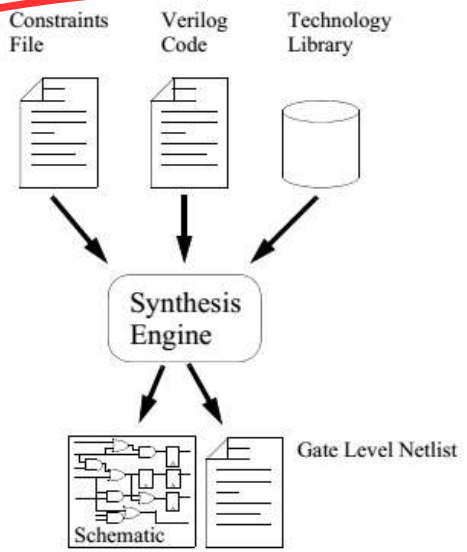
RTL

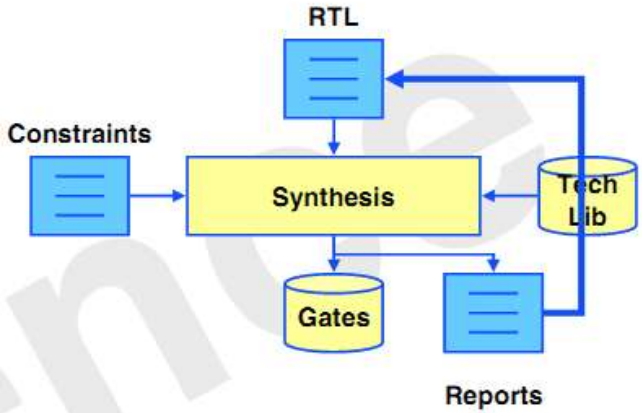


Structural

SÍNTESIS


RTL
Logic Synthesis
Gates
Timing Closure
Place and Route
Floorplanning
Placement
Clock Tree
Route
Static Timing Analysis
Test
GDSII
GDSII

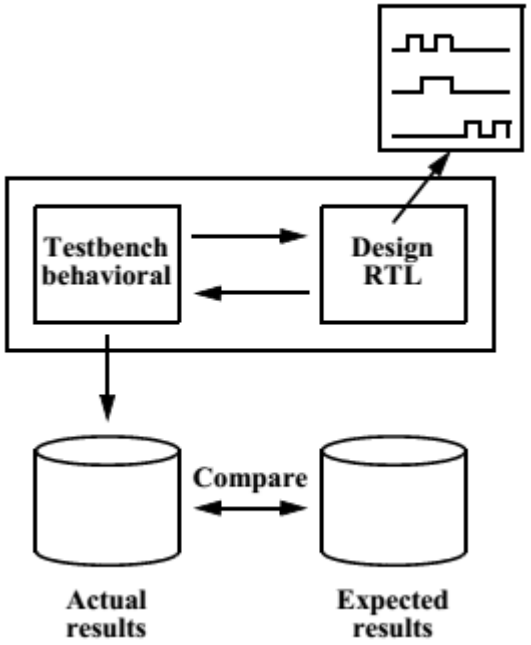

Constraints File
Verilog Code
Technology Library
Synthesis Engine
Schematic
Gate Level Netlist


RTL
Constraints
Synthesis
Tech Lib
Gates
Reports

SIMULACIÓN

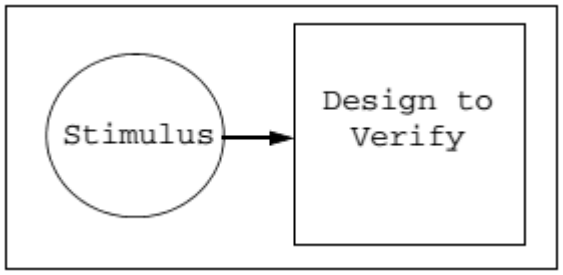
Basada en circuito esquemático

Basada en HDL



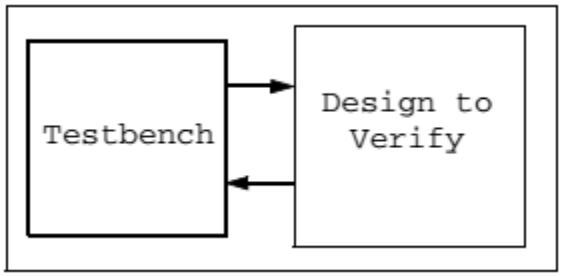
SIMULACIÓN

Testbench simple



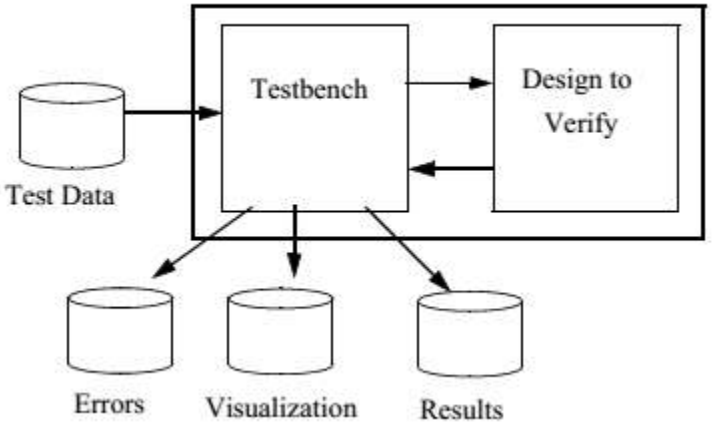
Únicamente envia datos en forma de estímulos al circuito bajo prueba, no existe interacción

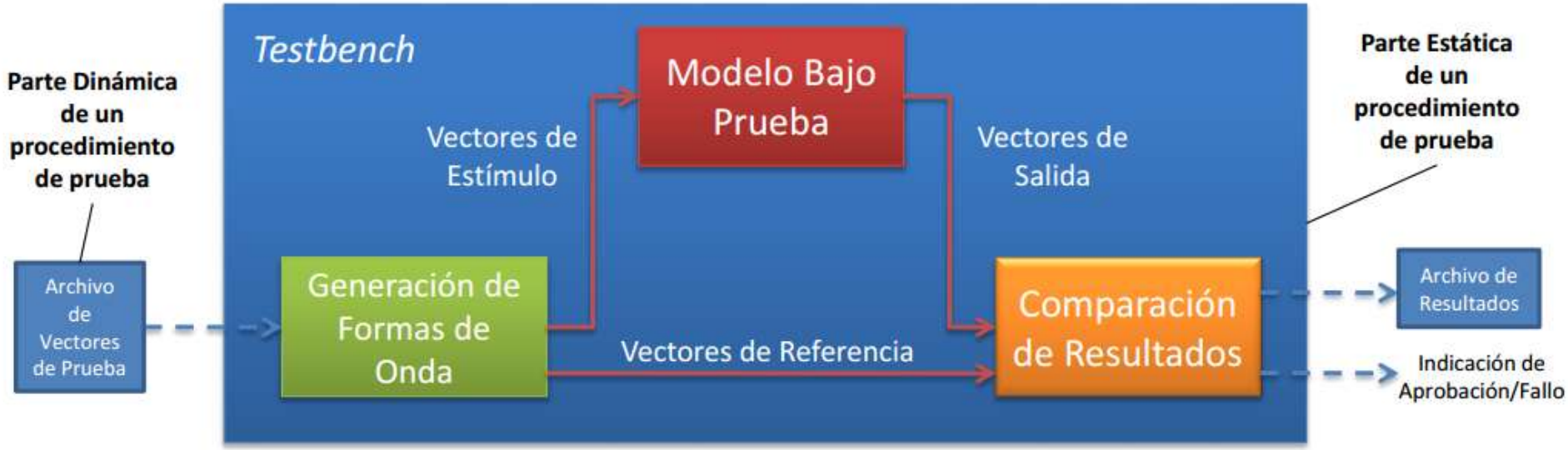
Testbench sofisticado



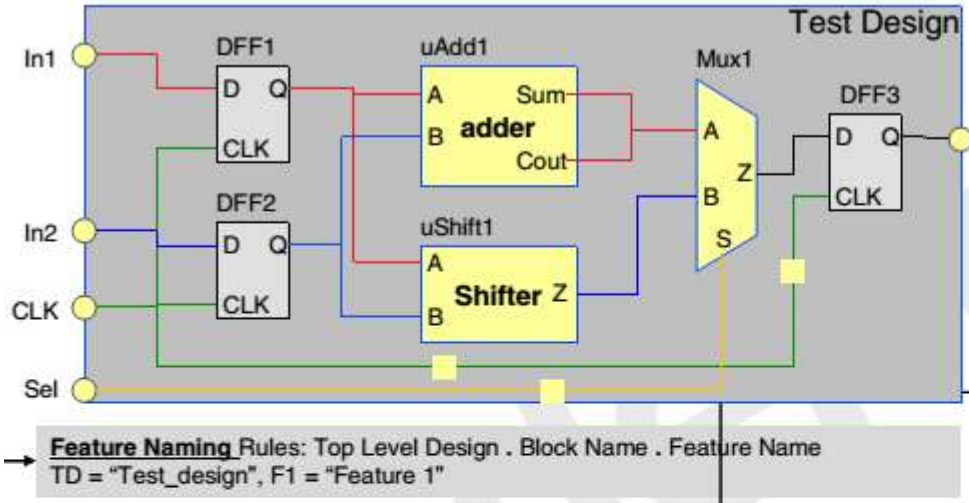
Modela el entorno que lo rodea conversando contínuamente con el circuito bajo prueba. Posibilidad de autochekeo

SIMULACIÓN


Testbench
Design to Verify
Test Data
Errors
Visualization
Results


Testbench
Parte Dinámica de un procedimiento de prueba
Archivo de Vectores de Prueba
Generación de Formas de Onda
Vectores de Estímulo
Modelo Bajo Prueba
Vectores de Salida
Vectores de Referencia
Comparación de Resultados
Parte Estática de un procedimiento de prueba
Archivo de Resultados
Indicación de Aprobación/Fallo

SIMULACIÓN



Description:
Describe each feature's function at a very high level

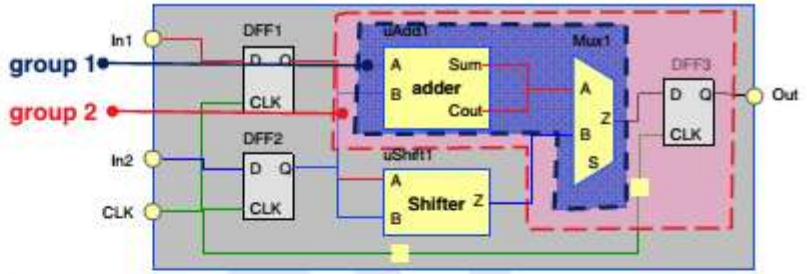
Feature Naming Rules: Top Level Design . Block Name . Feature Name
TD = "Test_design", F1 = "Feature 1"

Feature Number	Feature Description	Testing Priority
TD.uAdd1.F1	Block should correctly add numbers	10
TD.uShift1.F1	Shift operations should execute correctly	10
TD.DFF1.F1	Data should be latched correctly	5
TD.DFF2.F2	Data should be latched correctly	5
TD.Mux1.F1	Block should multiplex input data correctly	7
TD.DFF3.F1	Data should be latched correctly	5

Feature List

SIMULACIÓN

In addition to **unit** level tests, **group/transactional** tests are defined. Group tests verify more than one feature at a time.



Test Number	Description	Method	Level	Features Verified	Prio rity	Owner	Completion
TD.uAdd1.F1.T1	Keeping input B at 0, change value A from 0-9, verify result	Simu-lation	unit	TD.uAdd1.F1	10	Pak	100%
TD.uAdd1.F1.T2	Keeping input A at 0, change value B from 0-9, verify result	Simu-lation	unit	TD.uAdd1.F1		Pak	100%
TD.uShift1.F1	Shift operations should execute correctly	Formal Verif	unit		10	Flores	0%
TD.Group1.T1	Keep B=0 & SEL = 0, change A from 0 to 9; verify output Z	Simu-lation	group	TD.uAdd1.F1 TD.Mux1.F1	5	DeLaCr uz	25%
TD.Group2.T1	Same as Group1.T1; CLK @ 100 MHz, 50% duty cycle; verify output DFF3/Q	simu-lation	group	TD.uAdd1.F1 TD.Mux1.F1 TD.DFF3.F1	5	Jackson	50%

Note: This is *not* a complete list.

Test List

VHDL TESTBENCH

Sentencia 'AFTER': Inserta un retardo de tiempo finito a la sentencia anterior

```
-- Please ensure that the constant SIM_TIME is defined prior to the
-- begin statement in the architecture. Refer to the SIM_TIME Constant Template
-- for more info.

<signal_name> <= <signal_value> after SIM_TIME;
```

En este caso la asignación de signal_value a signal_name se llevará a cabo luego que pase el tiempo SIM_TIME

VHDL TESTBENCH

Sentencia 'WAIT': Espera a que ocurra un evento determinado, luego que este evento ocurre la ejecución del testbench continúa con la siguiente sentencia.

```
1  wait on <signal_name>;
2
3  wait until <signal_name> = <value>;
4
5  wait for SIM_TIME;
```

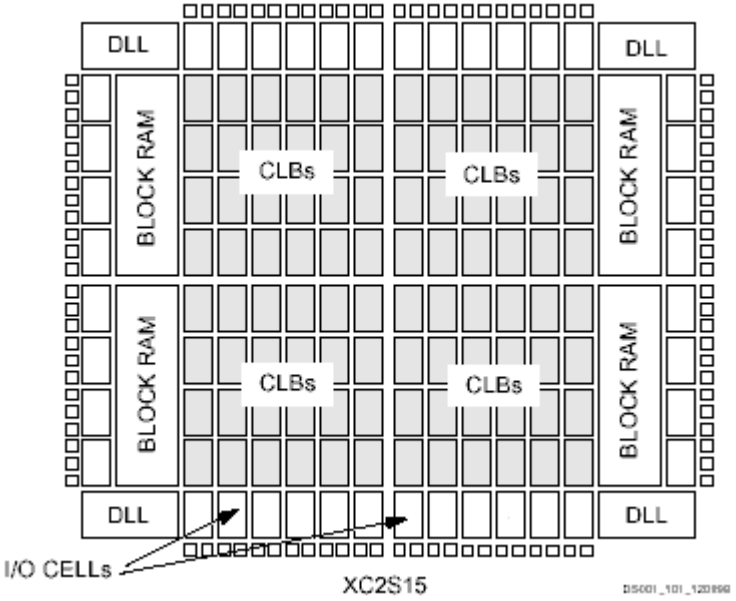
En este caso el primer wait esperará a que ocurra cualquier evento, es decir cualquier cambio de valor de la señal signal_name, luego que ocurra este evento el testbench puede proseguir con la siguiente sentencia.
El segundo wait opera de la misma manera pero en este caso esperará a que signal_name tenga el valor value.
El tercer wait simplemente espera la cantidad de tiempo indicada antes de seguir con la siguiente sentencia.

VHDL TESTBENCH

Generación de señal de clock: Existen varias formas de generar señales de clock. Aquí se muestran dos de ellas, la primera es concurrente y la segunda es secuencial.

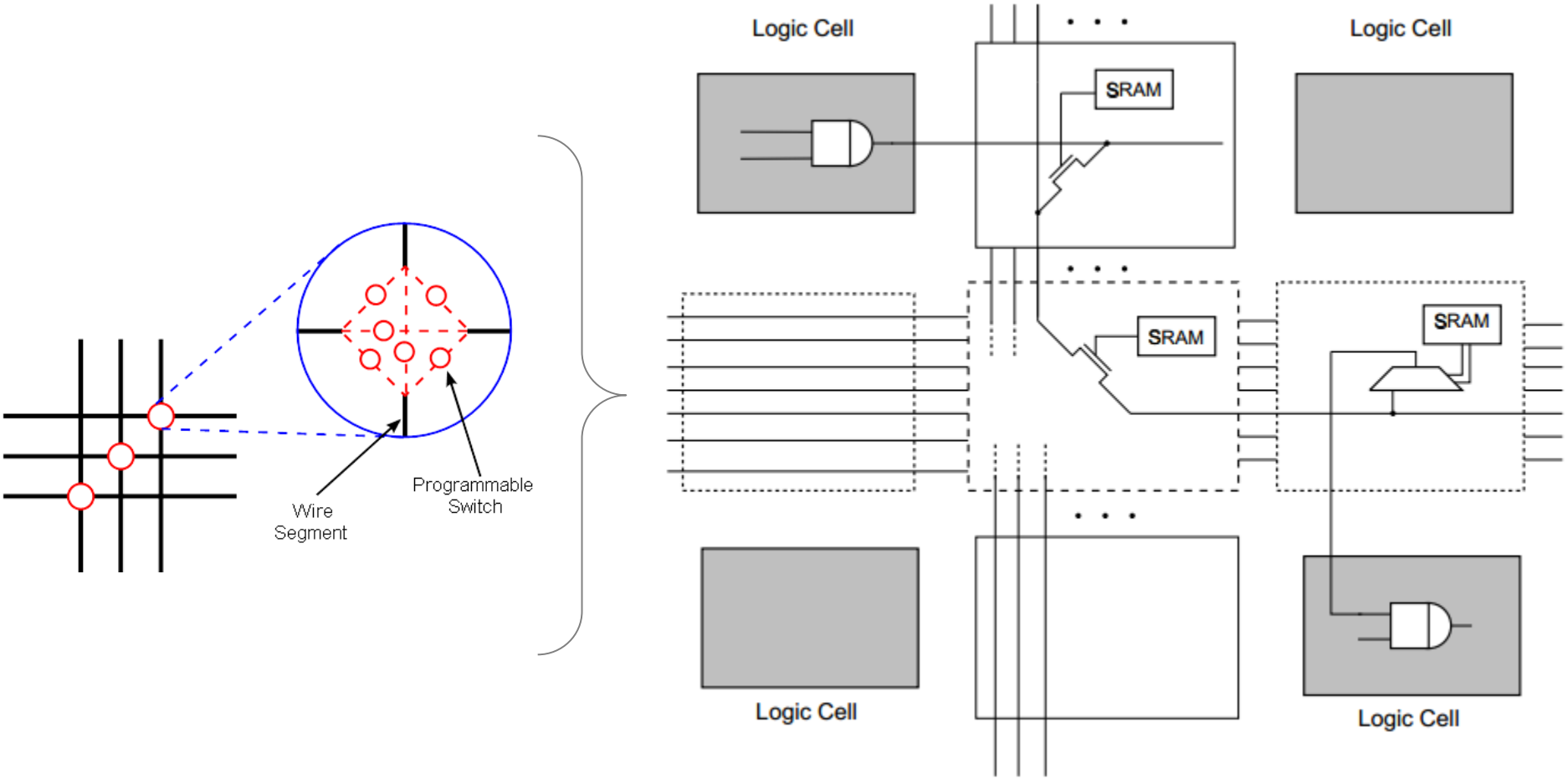
```
1  CLK <= not(CLK) after PERIOD/2;
2
3  CLK <= '0';
4  wait for PERIOD/2;
5  CLK <= '1';
6  wait for PERIOD/2;
```

FPGA


DLL
DLL
BLOCK RAM
BLOCK RAM
CLBs
CLBs
CLBs
CLBs
BLOCK RAM
BLOCK RAM
DLL
DLL
I/O CELLs
XC2S15

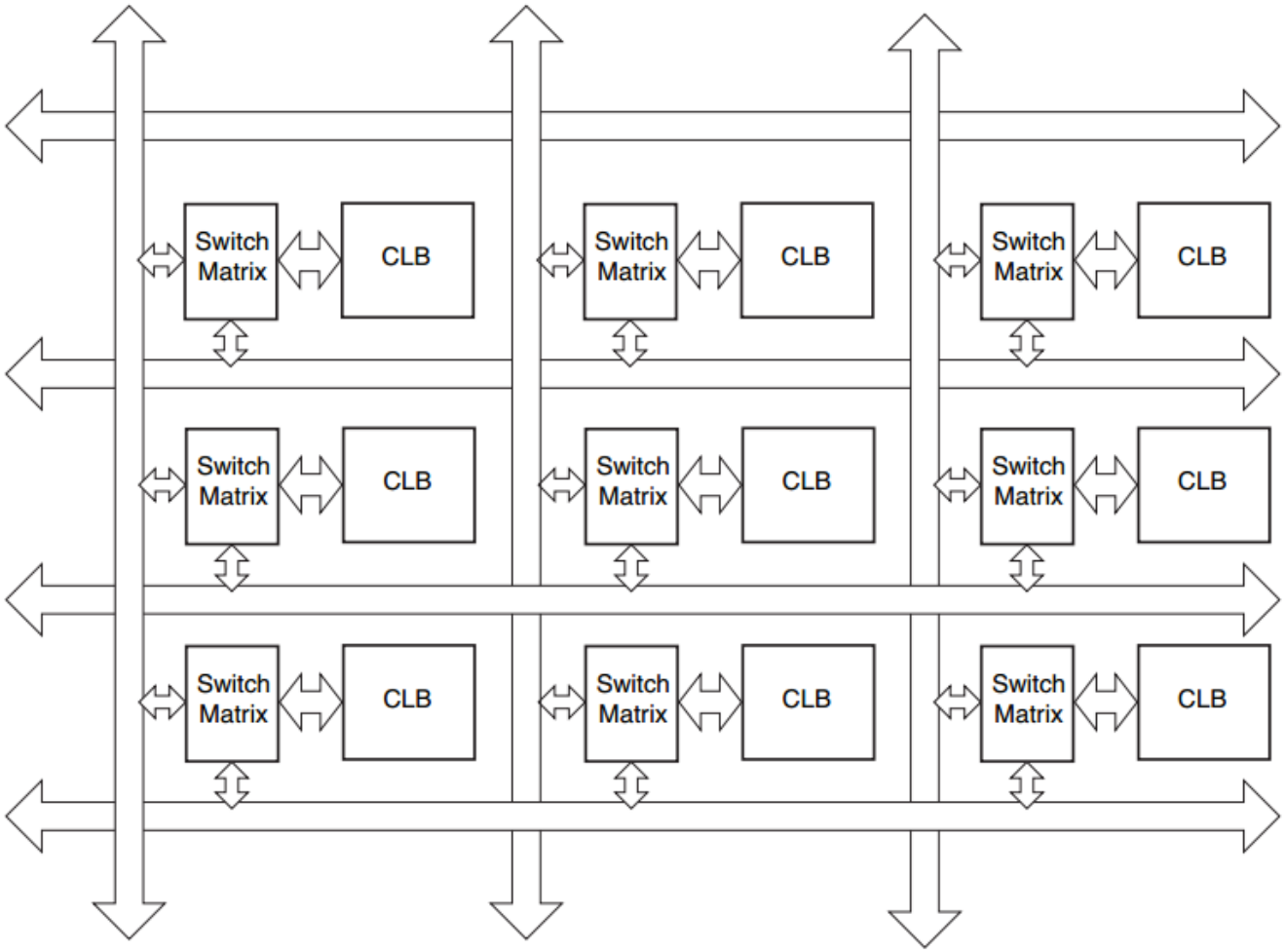

XILINX
SPARTAN

FPGA



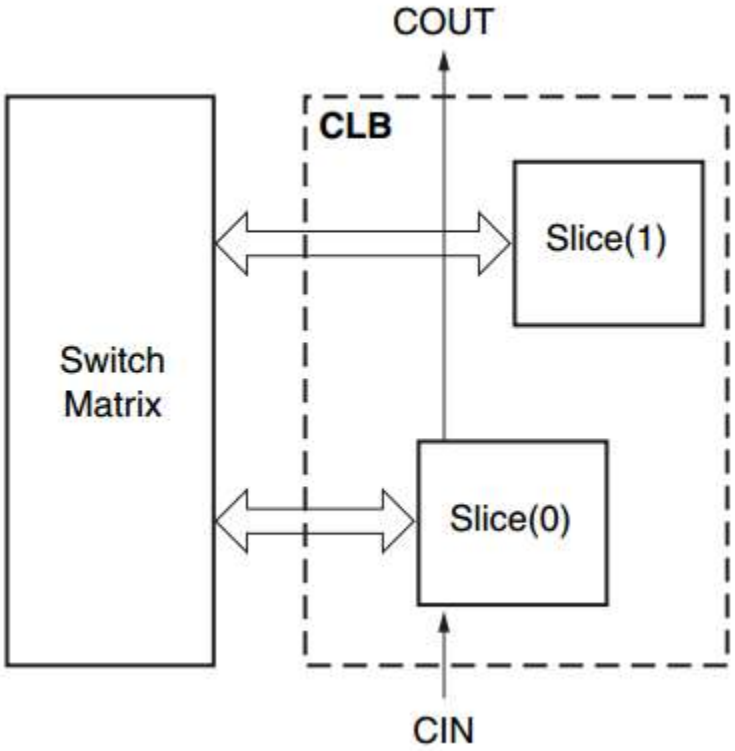
Interconección entre celdas lógicas

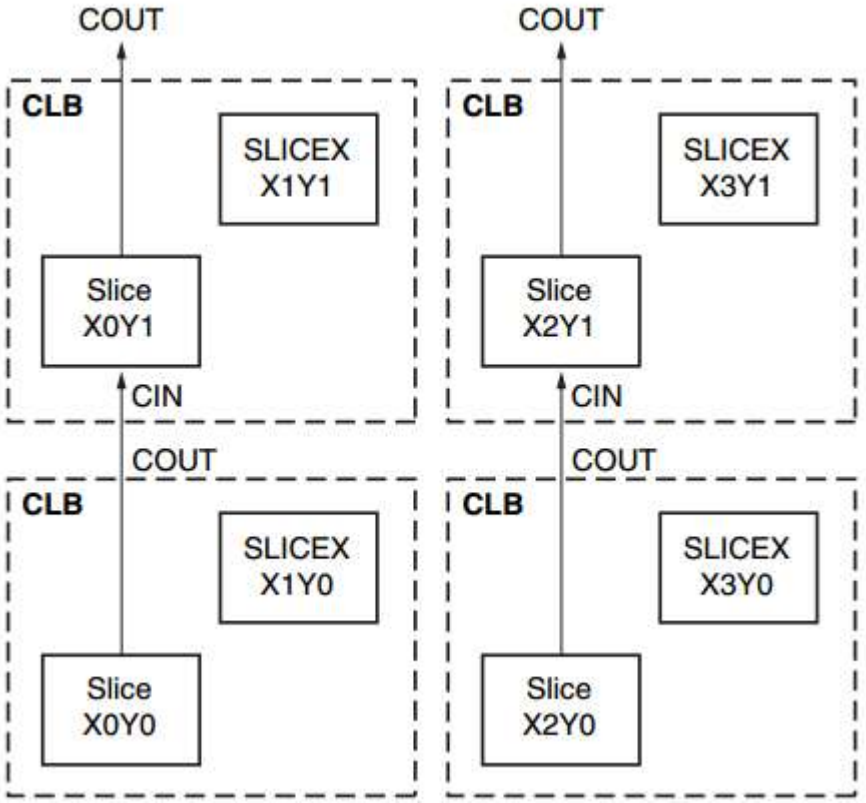
FPGA



Interconección entre celdas lógicas en el Spartan 6 de Xilinx

FPGA





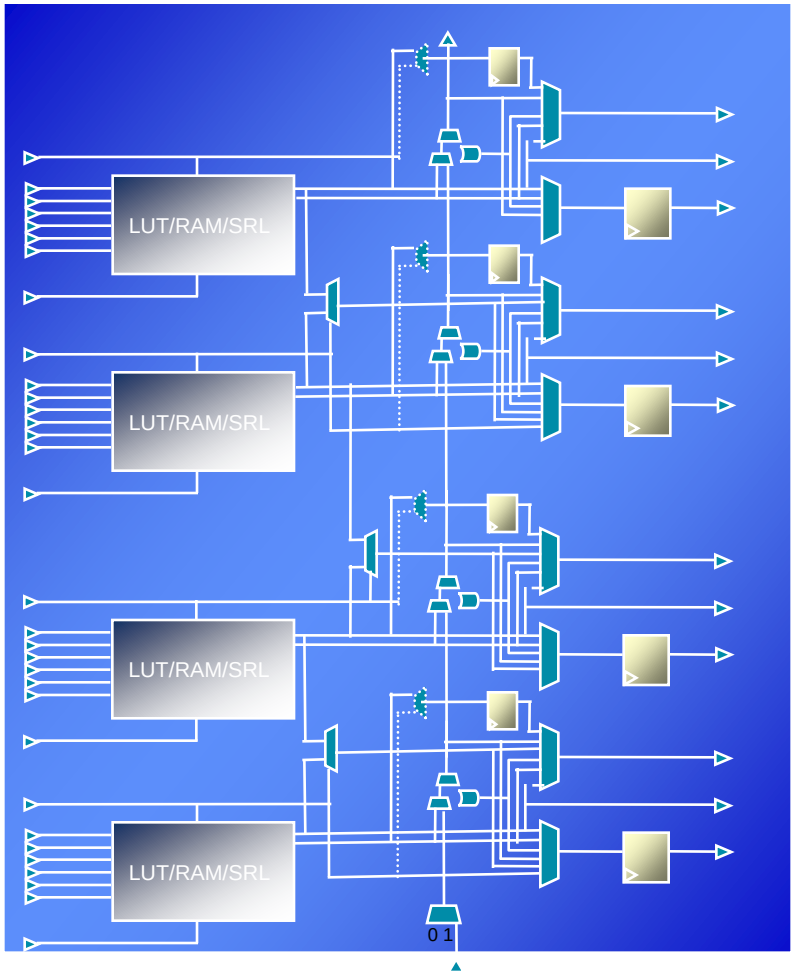
CLB: Configurable Logic Block del Spartan 6 de Xilinx

FPGA

Feature	SLICEX	SLICEL	SLICEM
6-Input LUTs	√	√	√
8 Flip-flops	√	√	√
Wide Multiplexers		√	√
Carry Logic		√	√
Distributed RAM			√
Shift Registers			√

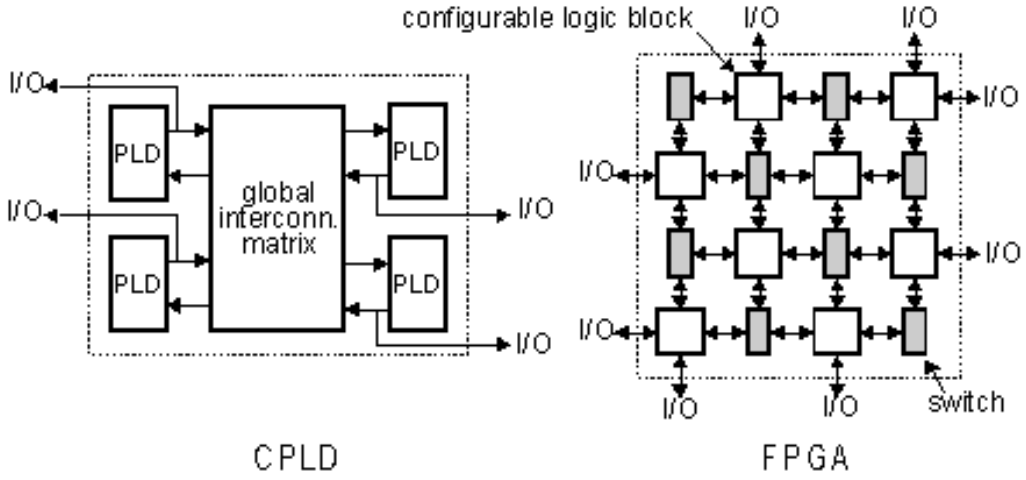
3 tipos de Slices en el Spartan 6 de Xilinx

FPGA



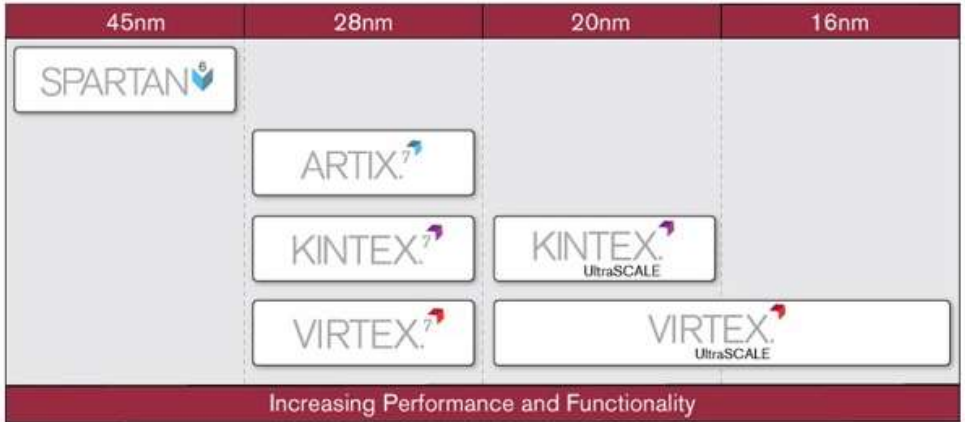
Slice del tipo SLICEX del Spartan 6 de Xilinx

FPGA



CPLD vs FPGA

FPGA



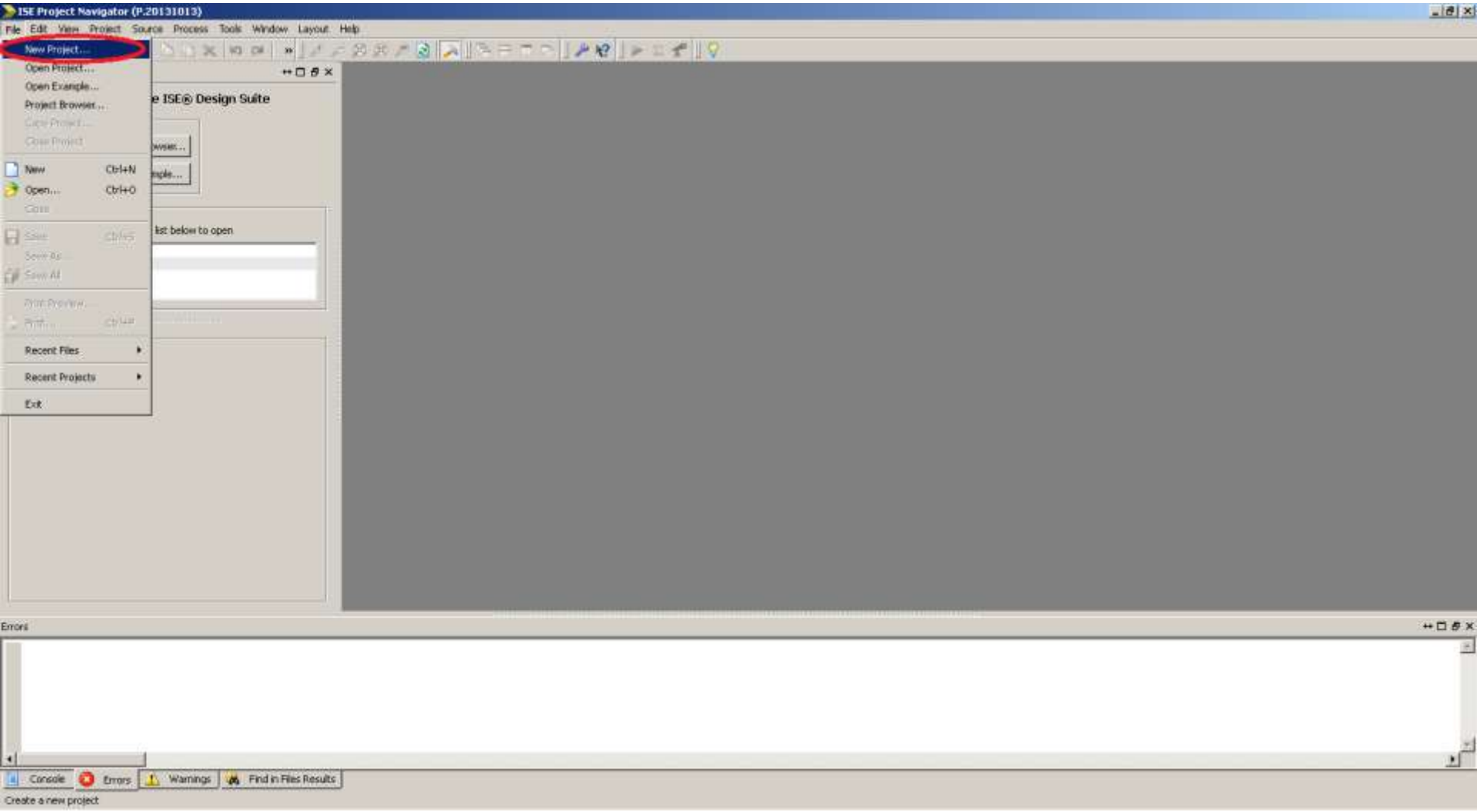
FPGA Comparison Table

	Spartan-6	Artix-7	Kintex-7	Virtex-7	Kintex UltraScale	Virtex UltraScale
Logic Cells	147,443	215,360	477, 760	1,954,560	1,160,880	4,432,680
BlockRAM	4.8Mb	13Mb	34Mb	68Mb	76Mb	132.9Mb
DSP Slices	180	740	1,920	3,600	5,520	2,880
DSP Performance (symmetric FIR)	140GMACs	930GMACs	2,845GMACs	5,335GMACs	8,180 GMACs	4,268 GMACs
Transceiver Count	8	16	32	96	64	120
Transceiver Speed	3.2 Gb/s	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s	16.3 Gb/s	32.75 Gb/s
Total Transceiver Bandwidth (full duplex)	50 Gb/s	211 Gb/s	800 Gb/s	2,784 Gb/s	2,086 Gb/s	5,886 Gb/s
Memory Interface (DDR3)	800	1,066	1,866	1,866	2,400	2,400
PCI Express® Interface	x1 Gen1	x4 Gen2	x8 Gen2	x8 Gen3	x8 Gen3	x8 Gen3
Analog Mixed Signal (AMS)/XADC	-	XADC	XADC	XADC	System Monitor	System Monitor
Configuration AES	Yes	Yes	Yes	Yes	Yes	Yes
I/O Pins	576	500	500	1,200	832	1,456
I/O Voltage	1.2V – 3.3V	1.2V – 3.3V	1.2V – 3.3V	1.2V – 3.3V	1.0 – 3.3V	1.0 – 3.3V

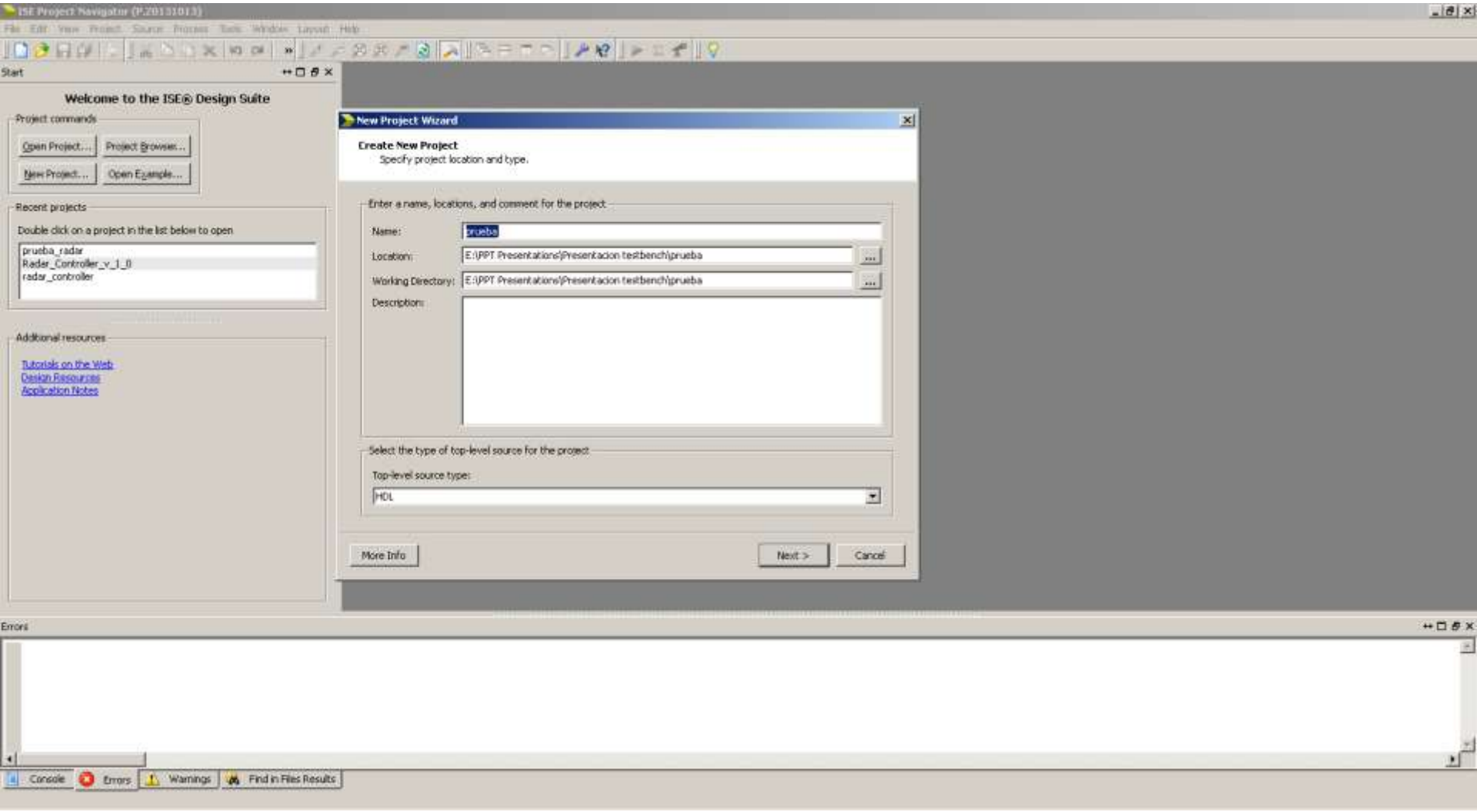
Please refer to the device data sheets for the latest product information.

Xilinx FPGAs

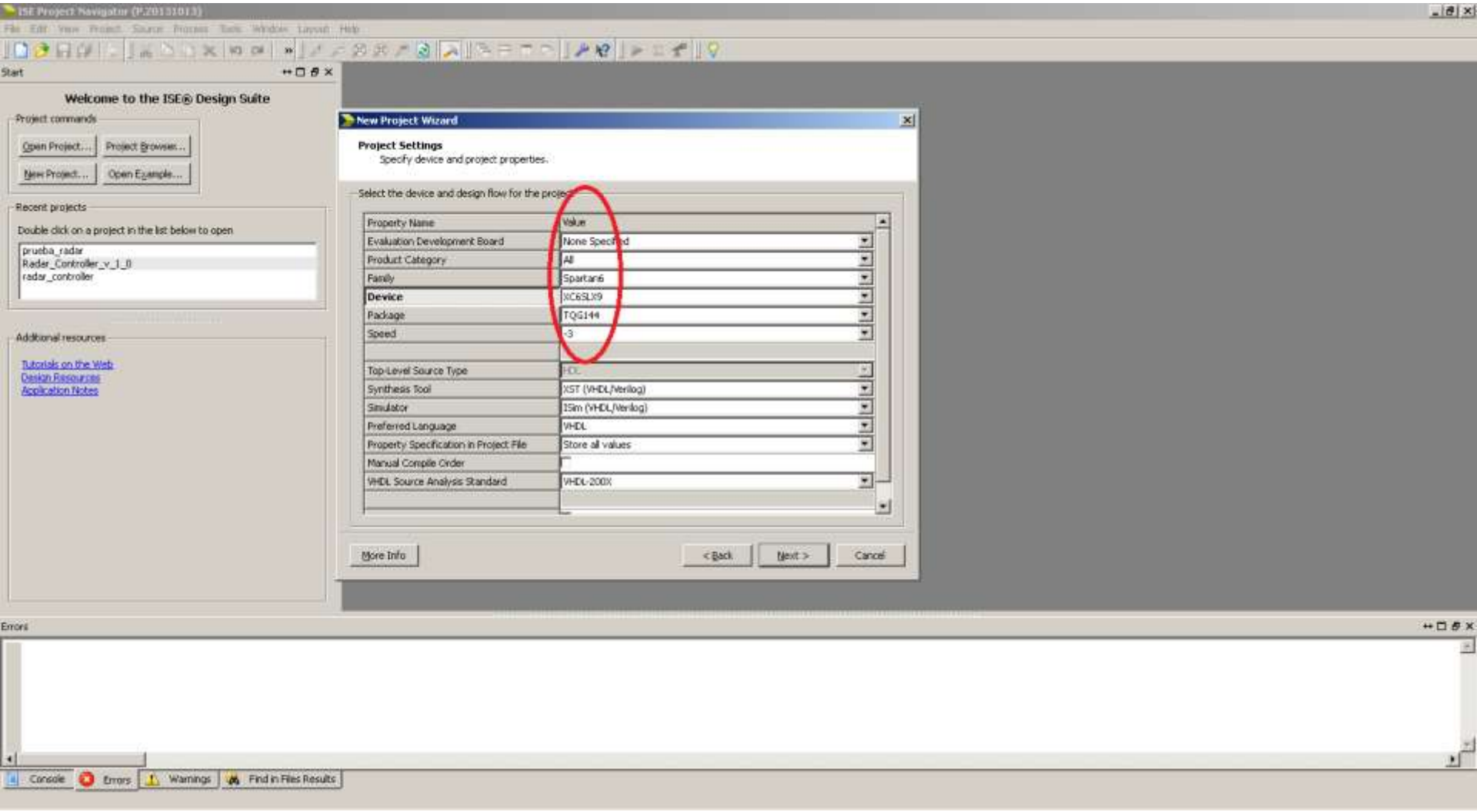
USO DE ISE


ISE Project Navigator (P.20131013)
File Edit View Project Source Process Tools Window Layout Help
New Project...
Open Project...
Open Example...
Project Browser...
New Ctrl+N
Open... Ctrl+O
Recent Files
Recent Projects
Exit
e ISE® Design Suite
list below to open
Errors
Console
Errors
Warnings
Find in Files Results
Create a new project

USO DE ISE

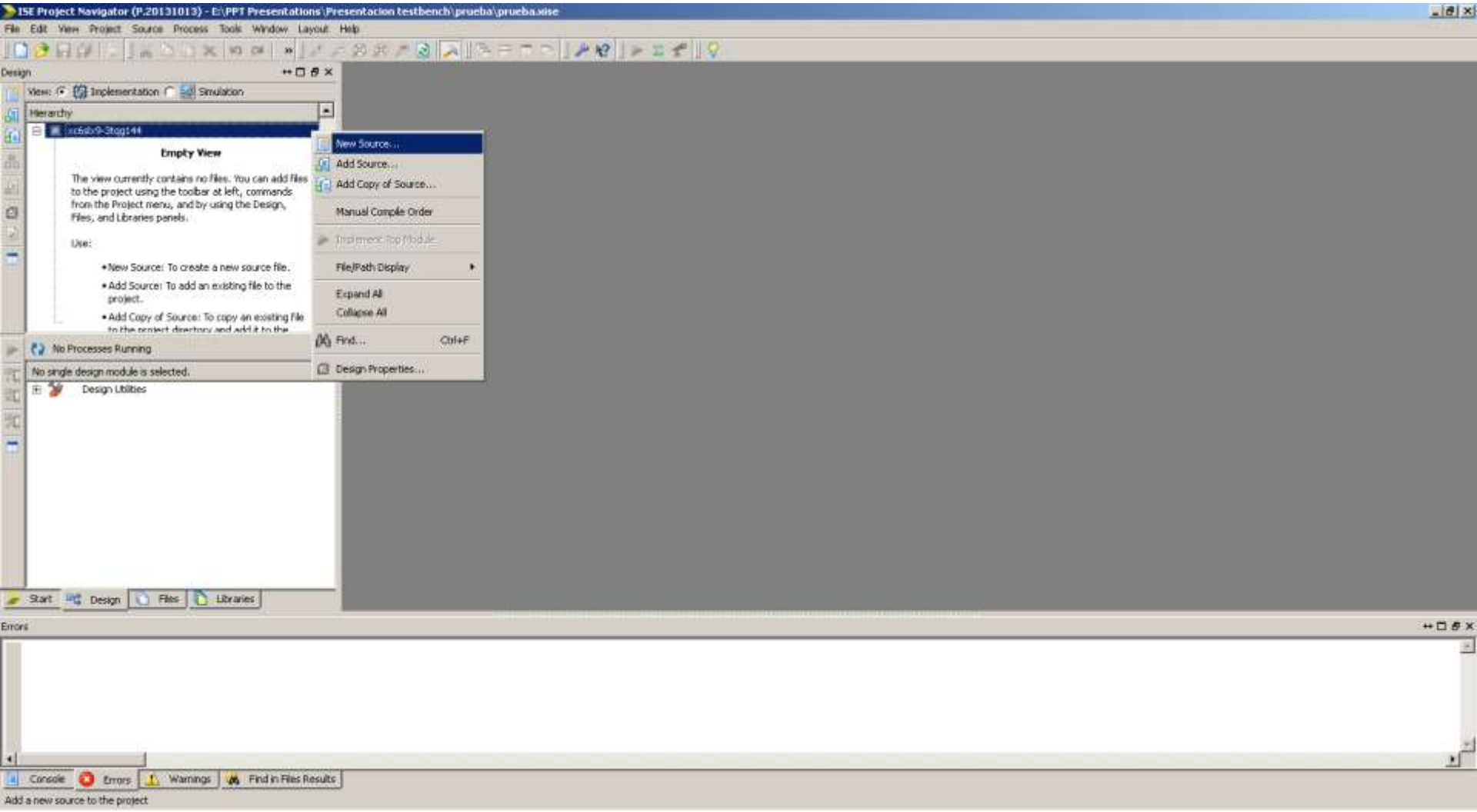

ISE Project Navigator (P.20131013)
Start
Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Double click on a project in the list below to open
prueba_radar
Radar_Controller_v_1_0
radar_controller
Additional resources
Tutorials on the Web
Design Resources
Application Notes
New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name:
prueba
Location:
E:\PPT Presentations\Presentacion testbench\prueba
Working Directory:
E:\PPT Presentations\Presentacion testbench\prueba
Description:
Select the type of top-level source for the project
Top-level source type:
HDL
More Info
Next >
Cancel
Errors
Console
Errors
Warnings
Find in Files Results

USO DE ISE

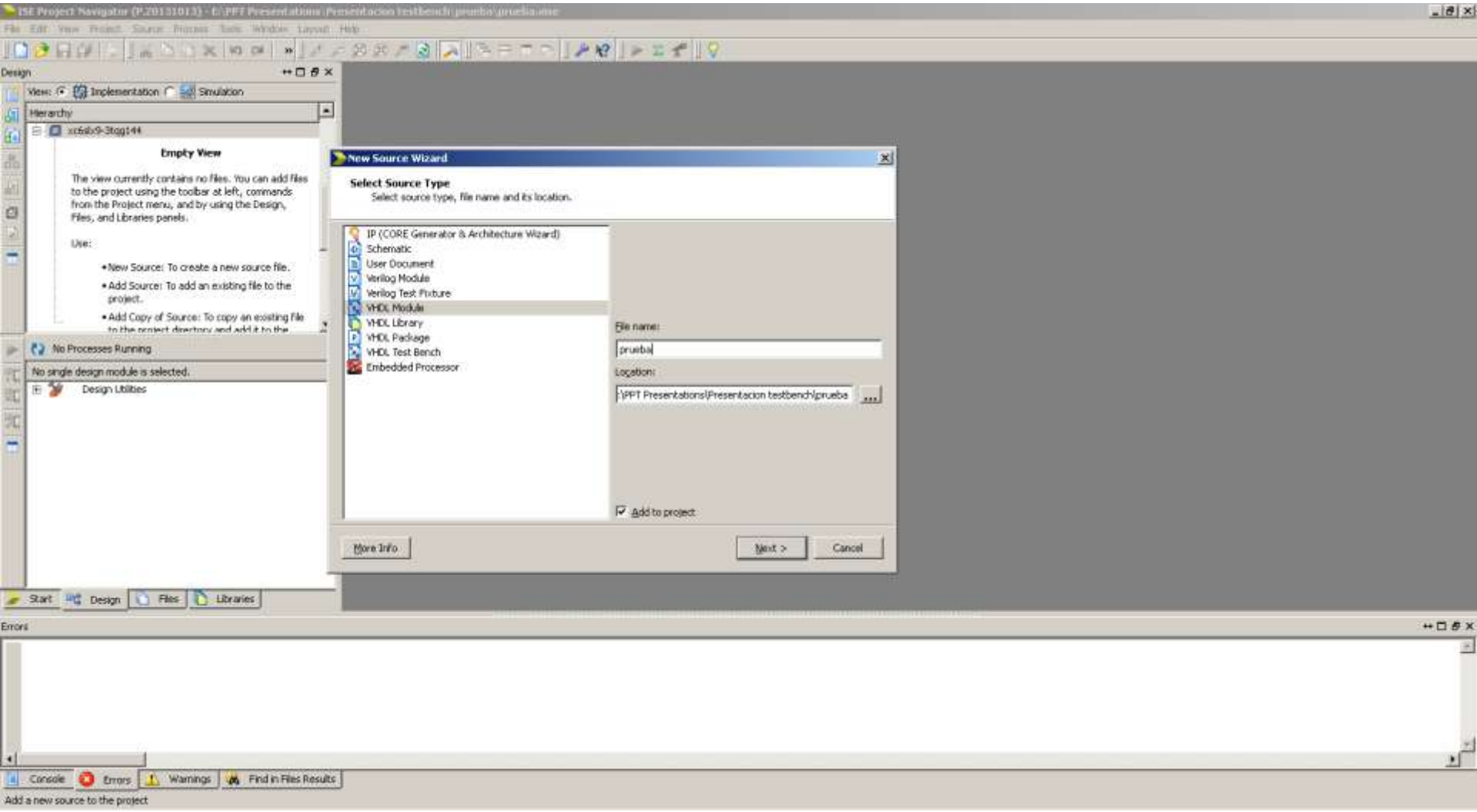

Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Double click on a project in the list below to open
prueba_radar
Radar_Controller_v_1_0
radar_controller
Additional resources
Tutorials on the Web
Design Resources
Application Notes
New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Spartan6
Device
XC6SLX9
Package
TQG144
Speed
-3
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
VHDL
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-200X
More Info
< Back
Next >
Cancel
Errors
Console
Errors
Warnings
Find in Files Results

USO DE ISE

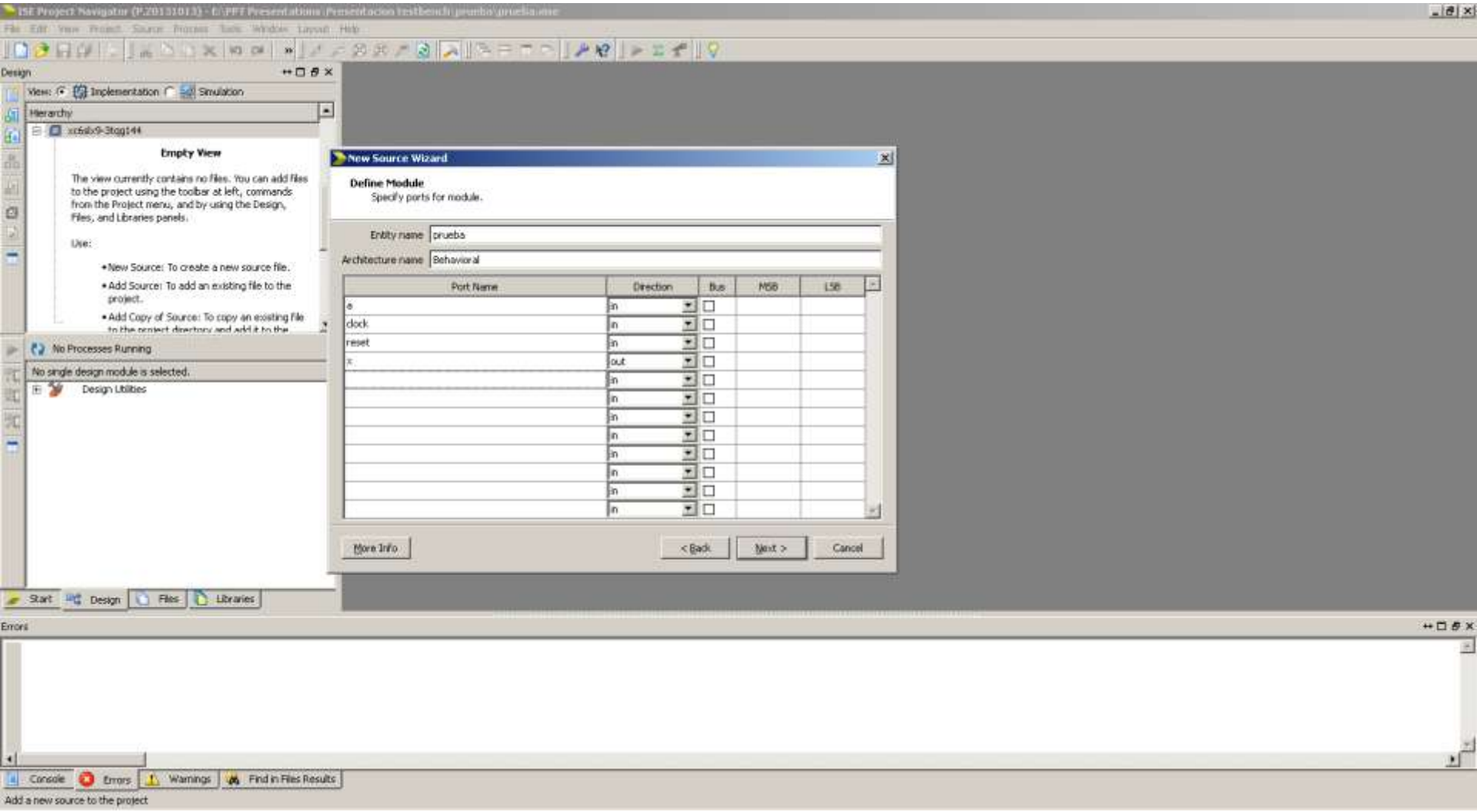
Radio Observatorio de JICAMARCA Radio Observatory



USO DE ISE

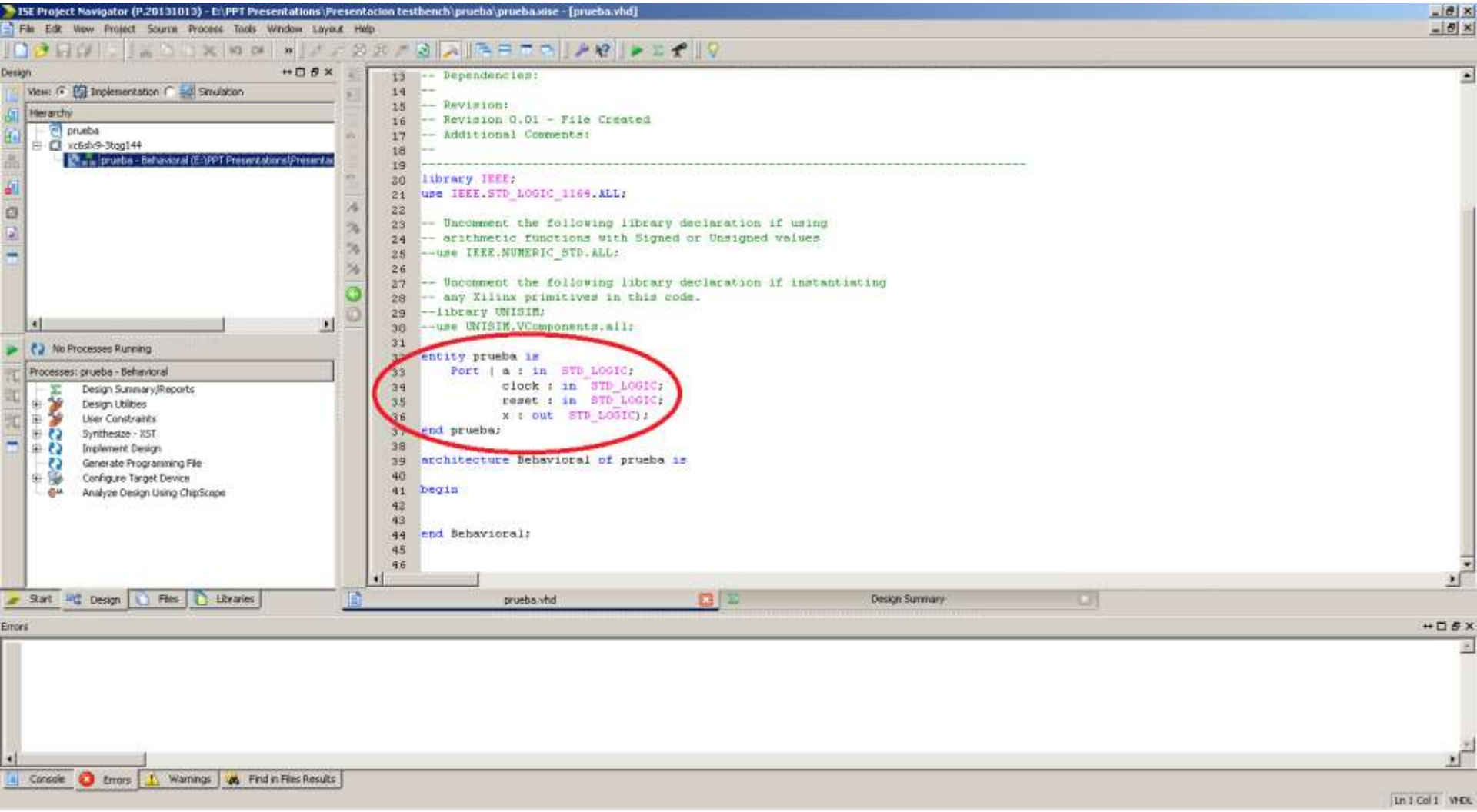

Design
View: Implementation Simulation
Hierarchy
Empty View
The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.
Use:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file
No Processes Running
No single design module is selected.
Design Utilities
Start
Design
Files
Libraries
New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
prueba
Location:
\PPT Presentations\Presentacion testbench\prueba
Add to project
More Info
Next >
Cancel
Errors
Console
Errors
Warnings
Find in Files Results
Add a new source to the project

USO DE ISE

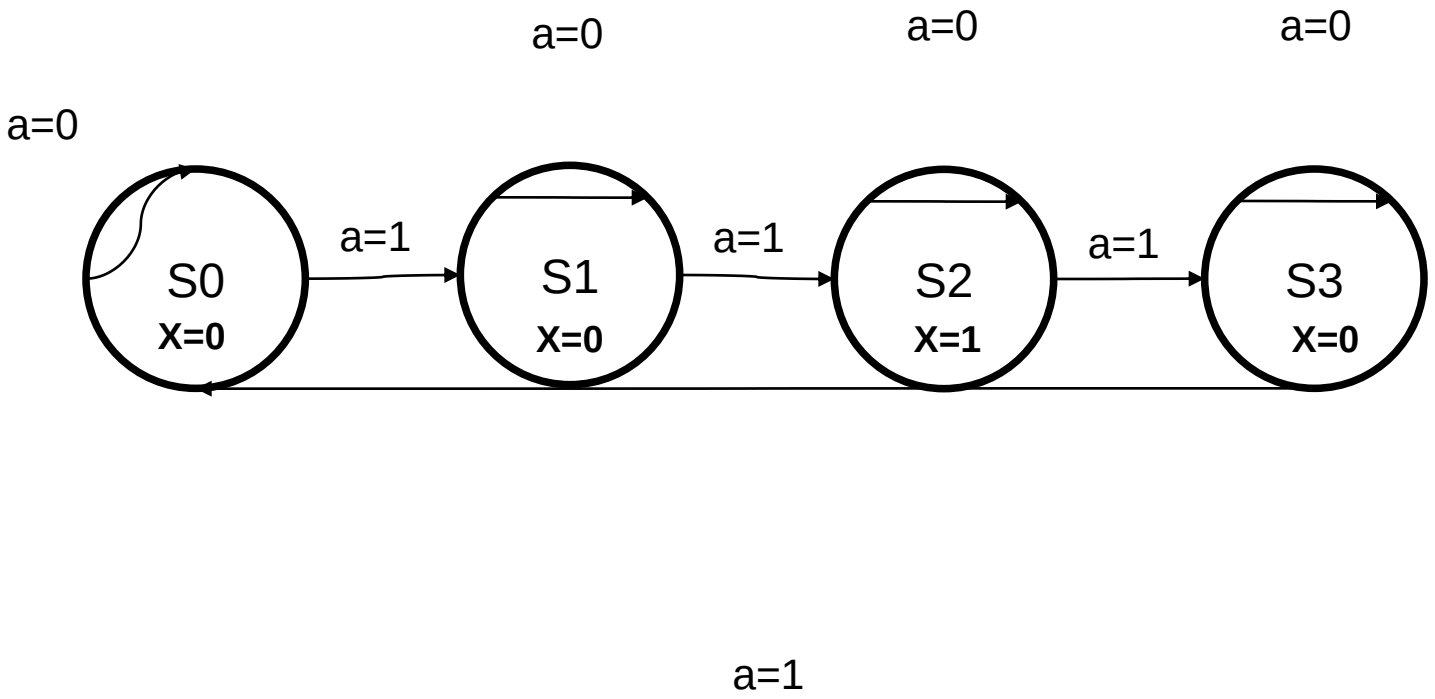

Design
View: Implementation Simulation
Hierarchy
Empty View
The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.
Use:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file
No Processes Running
No single design module is selected.
Design Utilities
Start
Design
Files
Libraries
New Source Wizard
Define Module
Specify ports for module.
Entity name: prueba
Architecture name: Behavioral
Port Name
Direction
Bus
MSB
LSB
a
clock
reset
x
in
out
More Info
< Back
Next >
Cancel
Errors
Console
Errors
Warnings
Find in Files Results
Add a new source to the project

USO DE ISE

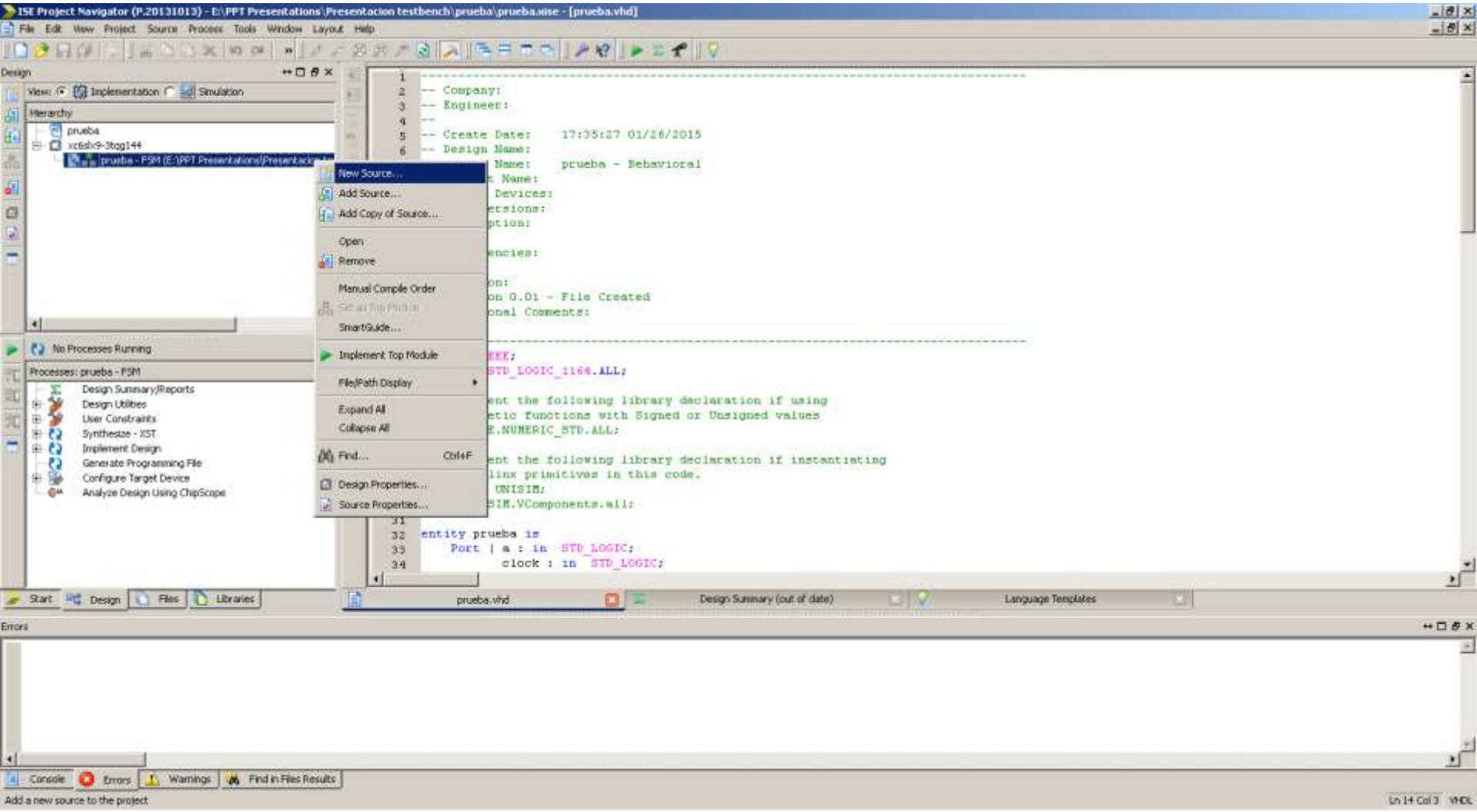
Radio Observatorio de JICAMARCA Radio Observatory



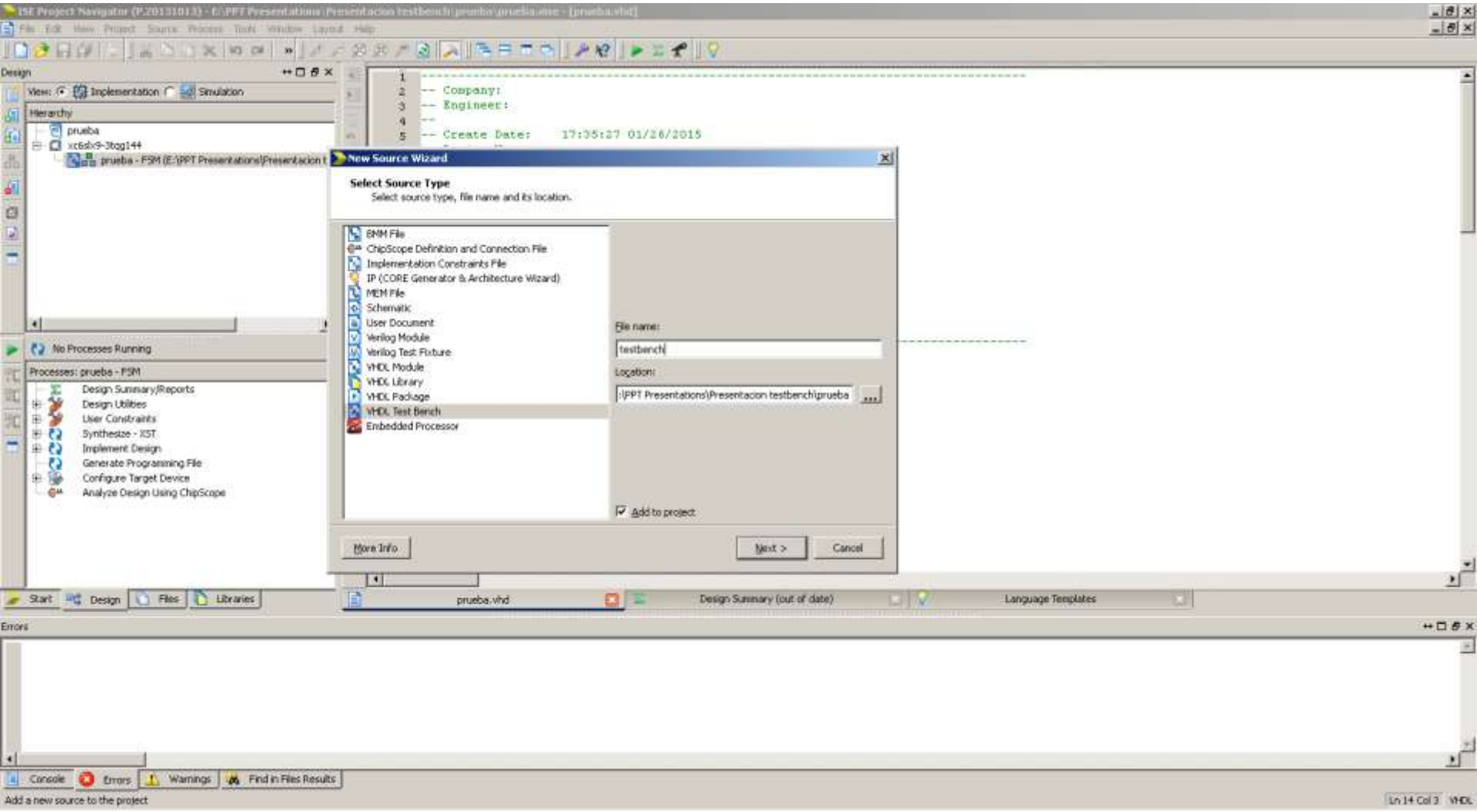
USO DE ISE



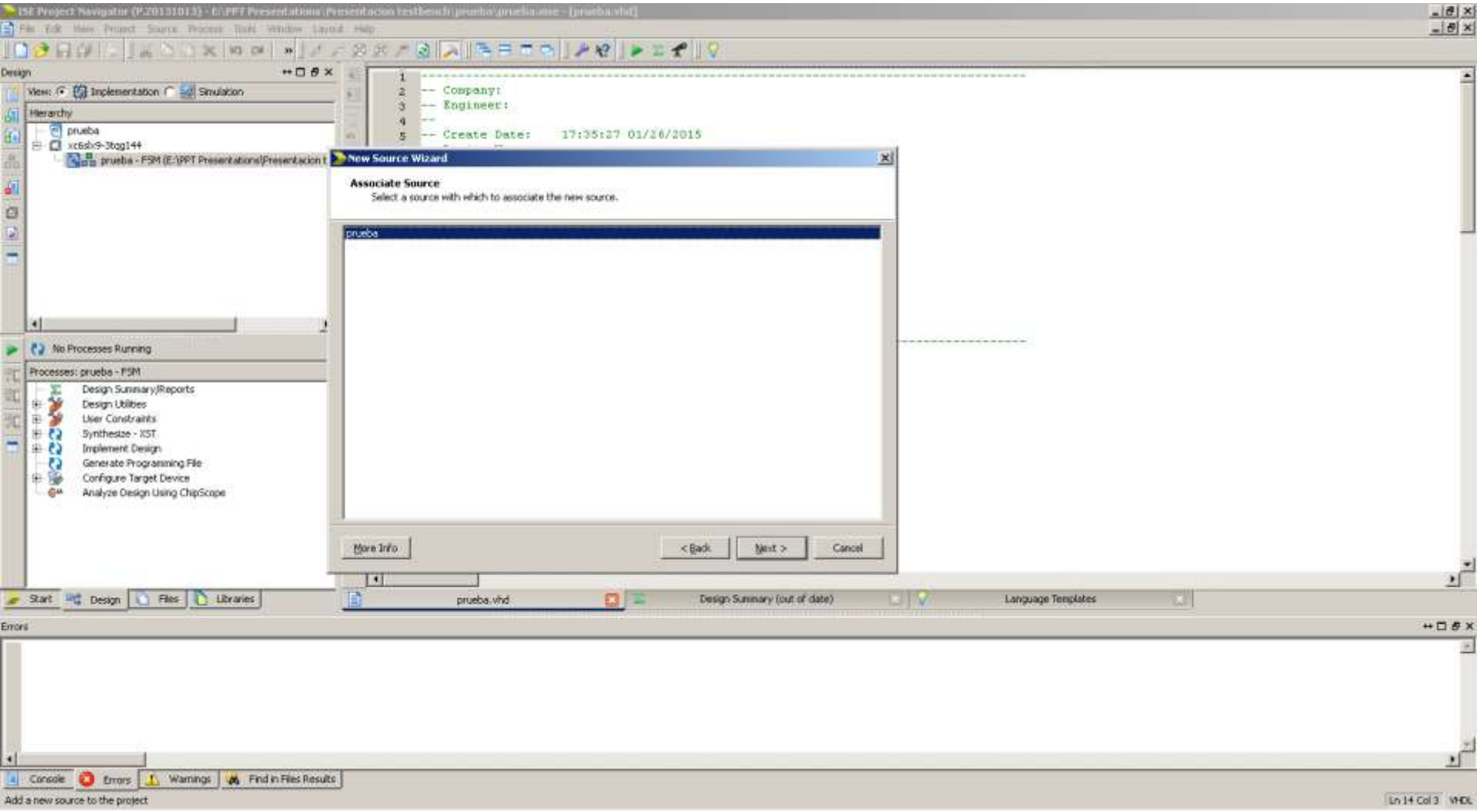
USO DE ISE


ISE Project Navigator (P.20131013) - E:\PPT Presentations\Presentacion testbench\prueba\prueba.xise - [prueba.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
prueba
xc6slx9-3tqg144
prueba - FSM (E:\PPT Presentations\Present
New Source...
Add Source...
Add Copy of Source...
Open
Remove
Manual Compile Order
SmartGuide...
Implement Top Module
File/Path Display
Expand All
Collapse All
Find... Ctrl+F
Design Properties...
Source Properties...
No Processes Running
Processes: prueba - FSM
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
-- Company:
-- Engineer:
-- Create Date: 17:35:27 01/26/2015
-- Design Name:
Name: prueba - Behavioral
Devices:
Dependencies:
Revision 0.01 - File Created
Additional Comments:
STD_LOGIC_1164.ALL;
entity prueba is
Port (a : in STD_LOGIC;
clock : in STD_LOGIC;
Start Design Files Libraries
prueba.vhd
Design Summary (out of date)
Language Templates
Errors
Console Errors Warnings Find in Files Results
Add a new source to the project
Ln 14 Col 3 VHDL

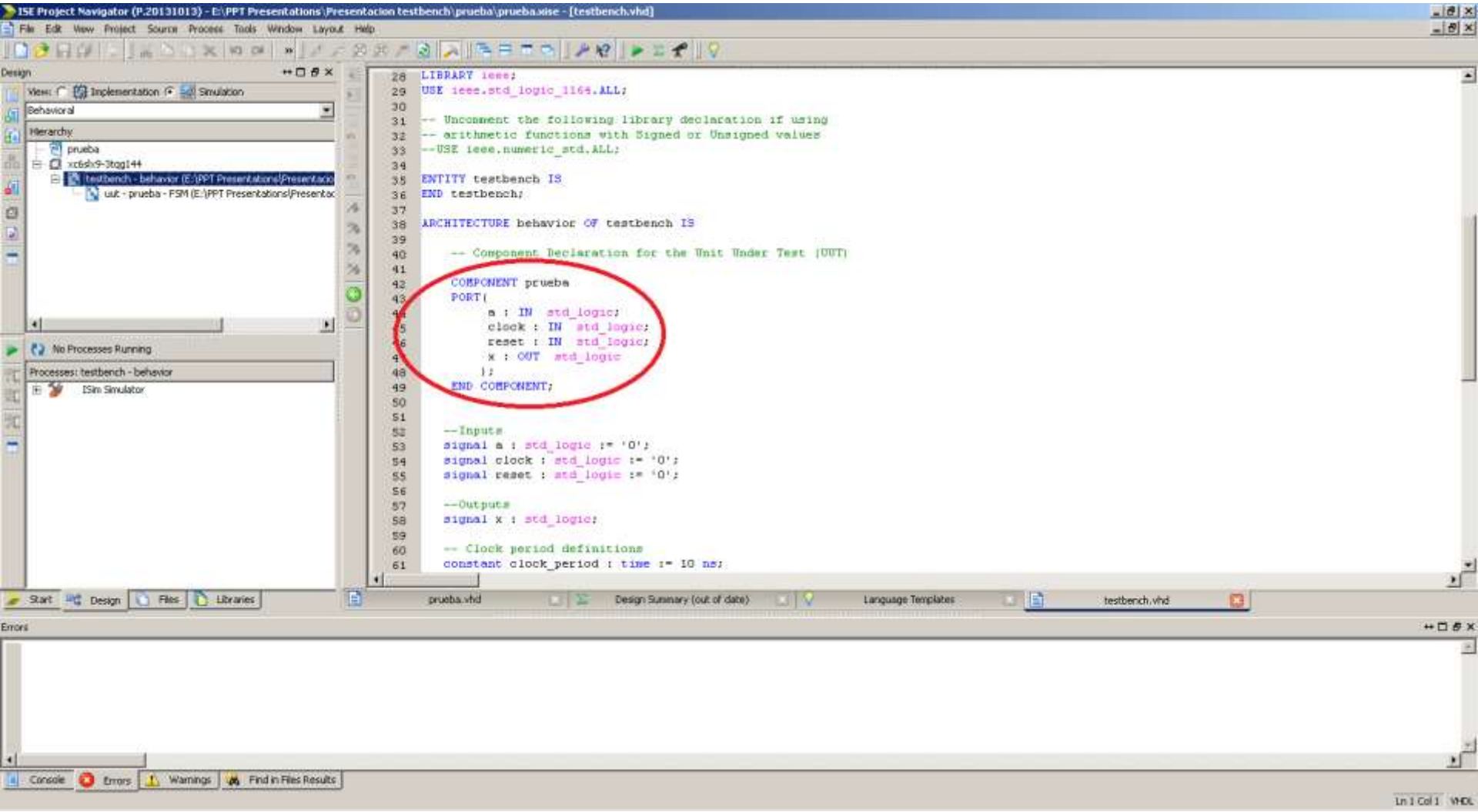
USO DE ISE


New Source Wizard
Select Source Type
Select source type, file name and its location.
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
testbench
Location:
:\PPT Presentations\Presentacion testbench\prueba
Add to project
More Info
Next >
Cancel
-- Company:
-- Engineer:
-- Create Date: 17:35:27 01/26/2015
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Errors
Console
Errors
Warnings
Find in Files Results
Add a new source to the project

USO DE ISE


Design
View: Implementation Simulation
Hierarchy
prueba
xc6slx9-3tqg144
prueba - FSM (E:\PPT Presentations\Presentacion t
No Processes Running
Processes: prueba - FSM
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
1 ----------
2 -- Company:
3 -- Engineer:
4 --
5 -- Create Date: 17:35:27 01/26/2015
New Source Wizard
Associate Source
Select a source with which to associate the new source.
prueba
More Info
< Back
Next >
Cancel
Start
Design
Files
Libraries
prueba.vhd
Design Summary (out of date)
Language Templates
Errors
Console
Errors
Warnings
Find in Files Results
Add a new source to the project
Ln 14 Col 3
VHDL

USO DE ISE


ISE Project Navigator (P.20131013) - E:\PPT Presentations\Presentacion testbench\prueba\prueba.xise - [testbench.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
prueba
xc6slx9-3tqg144
testbench - behavior (E:\PPT Presentations\Presentacio
uut - prueba - FSM (E:\PPT Presentations\Presentac
No Processes Running
Processes: testbench - behavior
ISim Simulator
Start Design Files Libraries
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;
ENTITY testbench IS
END testbench;
ARCHITECTURE behavior OF testbench IS
-- Component Declaration for the Unit Under Test (UUT)
COMPONENT prueba
PORT(
a : IN std_logic;
clock : IN std_logic;
reset : IN std_logic;
x : OUT std_logic
);
END COMPONENT;
--Inputs
signal a : std_logic := '0';
signal clock : std_logic := '0';
signal reset : std_logic := '0';
--Outputs
signal x : std_logic;
-- Clock period definitions
constant clock_period : time := 10 ns;
prueba.vhd
Design Summary (out of date)
Language Templates
testbench.vhd
Errors
Console Errors Warnings Find in Files Results
Ln 1 Col 1 VHDL

USO DE ISE

Radio Observatorio de JICAMARCA Radio Observatory