Experiment Report

Start of automated test report 2024-08-21 15:29:29
Author=UNKNOWN@yons-MS-7E06 obo Luke Vassallo

Machine Information

sysname=Linux
nodename=yons-MS-7E06
release=6.8.0-40-generic
version=#40~22.04.3-Ubuntu SMP PREEMPT_DYNAMIC Tue Jul 30 17:30:19 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i9-14900KF
CPU cores : 32
CPU base clock : 5.7000 GHz
CPU boost clock : 5.7000 GHz
System Memory : 94.13GB
Nvidia driver version : 550.90.07
Device 0 : NVIDIA GeForce RTX 4090
Device 0 : 23.99GB

Library Information

python : 3.8.19
torch : 1.13.1+cu117
optuna : 3.2.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

parameter_experiment_622:1724204021_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204021_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	70.74	70.74	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	38.16	38.16	37.08	12.81
voltage_datalogger_adc2	trial_1	25.38	24.38	24.38	12.18
voltage_datalogger_adc2	trial_2	28.02	28.02	28.02	13.9
voltage_datalogger_adc2	trial_3	25.0	25.0	25.0	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	84.26	84.26	45.1
voltage_datalogger_afe	trial_3	-	97.39	97.39	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204021_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204021_0	nan ± nan (0)	70.74 ± 0.0 (1)	70.74 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204021_0	29.14 ± 5.34 (4)	28.89 ± 5.53 (4)	28.62 ± 5.07 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204021_0	nan ± nan (0)	90.82 ± 6.56 (2)	90.82 ± 6.56 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204021_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	74.32	74.32	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	29.4	29.4	29.35	12.02
voltage_datalogger_adc2	trial_1	21.55	21.14	21.14	12.07
voltage_datalogger_adc2	trial_2	23.64	23.64	23.64	13.34
voltage_datalogger_adc2	trial_3	27.97	27.97	27.97	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	97.0	97.0	76.72
voltage_datalogger_afe	trial_3	-	126.42	126.42	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204021_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204021_0	nan ± nan (0)	74.32 ± 0.0 (1)	74.32 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204021_0	25.64 ± 3.17 (4)	25.54 ± 3.31 (4)	25.52 ± 3.29 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204021_0	nan ± nan (0)	111.71 ± 14.71 (2)	111.71 ± 14.71 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204023_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204023_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	27.68	27.68	27.68	12.81
voltage_datalogger_adc2	trial_1	31.85	31.85	31.85	12.18
voltage_datalogger_adc2	trial_2	26.99	25.45	24.74	13.9
voltage_datalogger_adc2	trial_3	28.99	23.01	22.98	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204023_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204023_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204023_0	28.88 ± 1.86 (4)	27.0 ± 3.25 (4)	26.81 ± 3.36 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204023_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204023_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	25.45	25.45	25.45	12.02
voltage_datalogger_adc2	trial_1	34.71	34.71	34.71	12.07
voltage_datalogger_adc2	trial_2	25.49	23.13	22.23	13.34
voltage_datalogger_adc2	trial_3	26.47	35.34	24.21	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204023_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204023_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204023_0	28.03 ± 3.88 (4)	29.66 ± 5.43 (4)	26.65 ± 4.79 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204023_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204025_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204025_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	70.4	70.4	36.03
voltage_datalogger_adc0	trial_3	-	95.83	95.83	28.57
voltage_datalogger_adc2	trial_0	43.52	43.52	37.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.11	12.18
voltage_datalogger_adc2	trial_2	28.02	28.02	28.02	13.9
voltage_datalogger_adc2	trial_3	25.0	25.0	25.0	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	83.1	83.1	45.1
voltage_datalogger_afe	trial_3	-	-	109.11	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204025_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204025_0	nan ± nan (0)	83.12 ± 12.71 (2)	83.12 ± 12.71 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204025_0	32.18 ± 8.11 (3)	32.18 ± 8.11 (3)	29.55 ± 4.52 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204025_0	nan ± nan (0)	83.1 ± 0.0 (1)	96.1 ± 13.01 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204025_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	72.95	72.95	41.48
voltage_datalogger_adc0	trial_3	-	103.45	103.45	29.14
voltage_datalogger_adc2	trial_0	34.7	34.7	29.35	12.02
voltage_datalogger_adc2	trial_1	-	-	34.35	12.07
voltage_datalogger_adc2	trial_2	23.64	23.64	23.64	13.34
voltage_datalogger_adc2	trial_3	28.74	28.74	28.74	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	101.09	101.09	76.72
voltage_datalogger_afe	trial_3	-	-	137.26	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204025_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204025_0	nan ± nan (0)	88.2 ± 15.25 (2)	88.2 ± 15.25 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204025_0	29.03 ± 4.52 (3)	29.03 ± 4.52 (3)	29.02 ± 3.79 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204025_0	nan ± nan (0)	101.09 ± 0.0 (1)	119.18 ± 18.08 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204027_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204027_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204027_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204027_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204027_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204027_0	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204027_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204027_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204027_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204027_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204027_0	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204411_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	28.87	26.68	30.87
voltage_datalogger_adc0	trial_1	-	-	24.48	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	25.9	28.57
voltage_datalogger_adc2	trial_0	15.98	13.79	13.7	12.81
voltage_datalogger_adc2	trial_1	-	15.11	14.5	12.18
voltage_datalogger_adc2	trial_2	16.78	13.03	12.59	13.9
voltage_datalogger_adc2	trial_3	15.66	14.99	13.48	12.85
voltage_datalogger_afe	trial_0	-	-	49.98	49.34
voltage_datalogger_afe	trial_1	-	-	46.34	49.26
voltage_datalogger_afe	trial_2	-	-	44.02	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204411_0	nan ± nan (0)	28.87 ± 0.0 (1)	25.69 ± 0.91 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204411_0	16.14 ± 0.47 (3)	14.23 ± 0.86 (4)	13.57 ± 0.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204411_0	nan ± nan (0)	nan ± nan (0)	46.78 ± 2.45 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.05	29.08	58.96
voltage_datalogger_adc0	trial_1	-	-	27.7	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	33.69	29.14
voltage_datalogger_adc2	trial_0	14.29	11.18	12.33	12.02
voltage_datalogger_adc2	trial_1	-	14.09	13.33	12.07
voltage_datalogger_adc2	trial_2	17.81	14.31	13.89	13.34
voltage_datalogger_adc2	trial_3	22.05	18.4	17.0	15.88
voltage_datalogger_afe	trial_0	-	-	60.75	77.93
voltage_datalogger_afe	trial_1	-	-	65.99	78.01
voltage_datalogger_afe	trial_2	-	-	51.84	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204411_0	nan ± nan (0)	29.05 ± 0.0 (1)	30.16 ± 2.56 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204411_0	18.05 ± 3.17 (3)	14.5 ± 2.57 (4)	14.14 ± 1.74 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204411_0	nan ± nan (0)	nan ± nan (0)	59.53 ± 5.84 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204411_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.33	30.87
voltage_datalogger_adc0	trial_1	-	-	31.41	25.52
voltage_datalogger_adc0	trial_2	-	-	23.55	36.03
voltage_datalogger_adc0	trial_3	-	70.72	28.36	28.57
voltage_datalogger_adc2	trial_0	11.76	11.26	10.66	12.81
voltage_datalogger_adc2	trial_1	15.9	12.65	11.49	12.18
voltage_datalogger_adc2	trial_2	13.98	11.27	10.71	13.9
voltage_datalogger_adc2	trial_3	15.55	15.06	14.17	12.85
voltage_datalogger_afe	trial_0	-	44.7	44.7	49.34
voltage_datalogger_afe	trial_1	-	-	47.31	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204411_1	nan ± nan (0)	70.72 ± 0.0 (1)	27.66 ± 2.81 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204411_1	14.3 ± 1.63 (4)	12.56 ± 1.55 (4)	11.76 ± 1.43 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204411_1	nan ± nan (0)	44.7 ± 0.0 (1)	46.0 ± 1.3 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.87	58.96
voltage_datalogger_adc0	trial_1	-	-	32.95	25.98
voltage_datalogger_adc0	trial_2	-	-	26.86	41.48
voltage_datalogger_adc0	trial_3	-	86.76	27.54	29.14
voltage_datalogger_adc2	trial_0	10.6	10.46	9.91	12.02
voltage_datalogger_adc2	trial_1	13.42	11.72	10.59	12.07
voltage_datalogger_adc2	trial_2	15.45	10.11	9.67	13.34
voltage_datalogger_adc2	trial_3	22.09	22.07	21.03	15.88
voltage_datalogger_afe	trial_0	-	48.53	48.53	77.93
voltage_datalogger_afe	trial_1	-	-	57.54	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204411_1	nan ± nan (0)	86.76 ± 0.0 (1)	28.8 ± 2.42 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204411_1	15.39 ± 4.23 (4)	13.59 ± 4.93 (4)	12.8 ± 4.76 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204411_1	nan ± nan (0)	48.53 ± 0.0 (1)	53.04 ± 4.5 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204413_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	33.08	25.52
voltage_datalogger_adc0	trial_2	27.55	27.55	26.46	36.03
voltage_datalogger_adc0	trial_3	-	-	30.51	28.57
voltage_datalogger_adc2	trial_0	19.88	19.88	11.99	12.81
voltage_datalogger_adc2	trial_1	17.36	11.94	11.11	12.18
voltage_datalogger_adc2	trial_2	13.77	13.07	10.81	13.9
voltage_datalogger_adc2	trial_3	18.24	11.83	11.1	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	54.57	54.57	49.26
voltage_datalogger_afe	trial_2	-	-	55.31	45.1
voltage_datalogger_afe	trial_3	-	52.35	52.35	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204413_0	27.55 ± 0.0 (1)	27.55 ± 0.0 (1)	30.02 ± 2.73 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204413_0	17.31 ± 2.24 (4)	14.18 ± 3.33 (4)	11.25 ± 0.44 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204413_0	nan ± nan (0)	53.46 ± 1.11 (2)	54.08 ± 1.26 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	39.02	25.98
voltage_datalogger_adc0	trial_2	28.08	28.08	28.94	41.48
voltage_datalogger_adc0	trial_3	-	-	32.44	29.14
voltage_datalogger_adc2	trial_0	16.15	16.15	14.46	12.02
voltage_datalogger_adc2	trial_1	13.73	10.29	9.55	12.07
voltage_datalogger_adc2	trial_2	14.83	14.19	12.54	13.34
voltage_datalogger_adc2	trial_3	15.06	10.29	9.65	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	60.13	60.13	78.01
voltage_datalogger_afe	trial_2	-	-	67.81	76.72
voltage_datalogger_afe	trial_3	-	66.61	66.61	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204413_0	28.08 ± 0.0 (1)	28.08 ± 0.0 (1)	33.47 ± 4.18 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204413_0	14.94 ± 0.86 (4)	12.73 ± 2.54 (4)	11.55 ± 2.07 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204413_0	nan ± nan (0)	63.37 ± 3.24 (2)	64.85 ± 3.37 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204413_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	34.29	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	17.27	12.31	11.98	12.81
voltage_datalogger_adc2	trial_1	-	19.69	13.75	12.18
voltage_datalogger_adc2	trial_2	15.78	12.11	10.98	13.9
voltage_datalogger_adc2	trial_3	16.67	15.6	14.72	12.85
voltage_datalogger_afe	trial_0	-	-	47.98	49.34
voltage_datalogger_afe	trial_1	49.74	49.74	44.79	49.26
voltage_datalogger_afe	trial_2	-	51.75	50.82	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204413_1	nan ± nan (0)	nan ± nan (0)	34.29 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204413_1	16.57 ± 0.61 (3)	14.93 ± 3.08 (4)	12.86 ± 1.46 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204413_1	49.74 ± 0.0 (1)	50.74 ± 1.0 (2)	47.86 ± 2.46 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	39.19	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	18.2	11.09	10.52	12.02
voltage_datalogger_adc2	trial_1	-	21.03	13.02	12.07
voltage_datalogger_adc2	trial_2	16.42	10.15	9.77	13.34
voltage_datalogger_adc2	trial_3	18.29	16.08	16.87	15.88
voltage_datalogger_afe	trial_0	-	-	51.5	77.93
voltage_datalogger_afe	trial_1	55.09	55.09	55.37	78.01
voltage_datalogger_afe	trial_2	-	52.55	57.36	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204413_1	nan ± nan (0)	nan ± nan (0)	39.19 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204413_1	17.64 ± 0.86 (3)	14.59 ± 4.35 (4)	12.55 ± 2.77 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204413_1	55.09 ± 0.0 (1)	53.82 ± 1.27 (2)	54.74 ± 2.43 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204415_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204415_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204415_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204415_0	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204415_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204415_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204415_0	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204415_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	18.78	18.78	18.78	12.81
voltage_datalogger_adc2	trial_1	30.27	30.27	30.27	12.18
voltage_datalogger_adc2	trial_2	25.49	24.91	24.91	13.9
voltage_datalogger_adc2	trial_3	-	23.22	23.22	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204415_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204415_1	24.85 ± 4.71 (3)	24.3 ± 4.11 (4)	24.3 ± 4.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204415_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	17.55	17.55	17.55	12.02
voltage_datalogger_adc2	trial_1	33.3	33.3	33.3	12.07
voltage_datalogger_adc2	trial_2	24.17	24.09	24.09	13.34
voltage_datalogger_adc2	trial_3	-	36.14	36.14	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204415_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204415_1	25.01 ± 6.46 (3)	27.77 ± 7.39 (4)	27.77 ± 7.39 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204415_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204417_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204417_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204417_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204417_0	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204417_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204417_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204417_0	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204417_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	18.78	18.78	18.78	12.81
voltage_datalogger_adc2	trial_1	30.27	30.27	30.27	12.18
voltage_datalogger_adc2	trial_2	25.49	24.91	24.91	13.9
voltage_datalogger_adc2	trial_3	-	23.22	23.22	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204417_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204417_1	24.85 ± 4.71 (3)	24.3 ± 4.11 (4)	24.3 ± 4.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204417_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	17.55	17.55	17.55	12.02
voltage_datalogger_adc2	trial_1	33.3	33.3	33.3	12.07
voltage_datalogger_adc2	trial_2	24.17	24.09	24.09	13.34
voltage_datalogger_adc2	trial_3	-	36.14	36.14	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204417_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204417_1	25.01 ± 6.46 (3)	27.77 ± 7.39 (4)	27.77 ± 7.39 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204417_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed