Experiment Report

Start of automated test report 2024-08-21 15:29:31
Author=UNKNOWN@yons-MS-7E06 obo Luke Vassallo

Machine Information

sysname=Linux
nodename=yons-MS-7E06
release=6.8.0-40-generic
version=#40~22.04.3-Ubuntu SMP PREEMPT_DYNAMIC Tue Jul 30 17:30:19 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i9-14900KF
CPU cores : 32
CPU base clock : 2.5699 GHz
CPU boost clock : 2.5699 GHz
System Memory : 94.13GB
Nvidia driver version : 550.90.07
Device 0 : NVIDIA GeForce RTX 4090
Device 0 : 23.99GB

Library Information

python : 3.8.19
torch : 1.13.1+cu117
optuna : 3.2.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

parameter_experiment_622:1724204021_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204021_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204021_0	nan ± nan (0)	70.74 ± 0.0 (1)	70.74 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204021_0	29.14 ± 5.34 (4)	28.89 ± 5.53 (4)	28.62 ± 5.07 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204021_0	nan ± nan (0)	90.82 ± 6.56 (2)	90.82 ± 6.56 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204021_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204021_0	nan ± nan (0)	74.32 ± 0.0 (1)	74.32 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204021_0	25.64 ± 3.17 (4)	25.54 ± 3.31 (4)	25.52 ± 3.29 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204021_0	nan ± nan (0)	111.71 ± 14.71 (2)	111.71 ± 14.71 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204023_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204023_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204023_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204023_0	28.88 ± 1.86 (4)	27.0 ± 3.25 (4)	26.81 ± 3.36 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204023_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204023_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204023_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204023_0	28.03 ± 3.88 (4)	29.66 ± 5.43 (4)	26.65 ± 4.79 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204023_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204025_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204025_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204025_0	nan ± nan (0)	83.12 ± 12.71 (2)	83.12 ± 12.71 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204025_0	32.18 ± 8.11 (3)	32.18 ± 8.11 (3)	29.55 ± 4.52 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204025_0	nan ± nan (0)	83.1 ± 0.0 (1)	96.1 ± 13.01 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204025_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204025_0	nan ± nan (0)	88.2 ± 15.25 (2)	88.2 ± 15.25 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204025_0	29.03 ± 4.52 (3)	29.03 ± 4.52 (3)	29.02 ± 3.79 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204025_0	nan ± nan (0)	101.09 ± 0.0 (1)	119.18 ± 18.08 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204027_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204027_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204027_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204027_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204027_0	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204027_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204027_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204027_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204027_0	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204411_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204411_0	nan ± nan (0)	28.87 ± 0.0 (1)	25.69 ± 0.91 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204411_0	16.14 ± 0.47 (3)	14.23 ± 0.86 (4)	13.57 ± 0.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204411_0	nan ± nan (0)	nan ± nan (0)	46.78 ± 2.45 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204411_0	nan ± nan (0)	29.05 ± 0.0 (1)	30.16 ± 2.56 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204411_0	18.05 ± 3.17 (3)	14.5 ± 2.57 (4)	14.14 ± 1.74 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204411_0	nan ± nan (0)	nan ± nan (0)	59.53 ± 5.84 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204411_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204411_1	nan ± nan (0)	70.72 ± 0.0 (1)	27.66 ± 2.81 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204411_1	14.3 ± 1.63 (4)	12.56 ± 1.55 (4)	11.76 ± 1.43 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204411_1	nan ± nan (0)	44.7 ± 0.0 (1)	46.0 ± 1.3 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204411_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204411_1	nan ± nan (0)	86.76 ± 0.0 (1)	28.8 ± 2.42 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204411_1	15.39 ± 4.23 (4)	13.59 ± 4.93 (4)	12.8 ± 4.76 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204411_1	nan ± nan (0)	48.53 ± 0.0 (1)	53.04 ± 4.5 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204413_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204413_0	27.55 ± 0.0 (1)	27.55 ± 0.0 (1)	30.02 ± 2.73 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204413_0	17.31 ± 2.24 (4)	14.18 ± 3.33 (4)	11.25 ± 0.44 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204413_0	nan ± nan (0)	53.46 ± 1.11 (2)	54.08 ± 1.26 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204413_0	28.08 ± 0.0 (1)	28.08 ± 0.0 (1)	33.47 ± 4.18 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204413_0	14.94 ± 0.86 (4)	12.73 ± 2.54 (4)	11.55 ± 2.07 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204413_0	nan ± nan (0)	63.37 ± 3.24 (2)	64.85 ± 3.37 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204413_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204413_1	nan ± nan (0)	nan ± nan (0)	34.29 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204413_1	16.57 ± 0.61 (3)	14.93 ± 3.08 (4)	12.86 ± 1.46 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204413_1	49.74 ± 0.0 (1)	50.74 ± 1.0 (2)	47.86 ± 2.46 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204413_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204413_1	nan ± nan (0)	nan ± nan (0)	39.19 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204413_1	17.64 ± 0.86 (3)	14.59 ± 4.35 (4)	12.55 ± 2.77 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204413_1	55.09 ± 0.0 (1)	53.82 ± 1.27 (2)	54.74 ± 2.43 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204415_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204415_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204415_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204415_0	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204415_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204415_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204415_0	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204415_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204415_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204415_1	24.85 ± 4.71 (3)	24.3 ± 4.11 (4)	24.3 ± 4.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204415_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204415_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204415_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204415_1	25.01 ± 6.46 (3)	27.77 ± 7.39 (4)	27.77 ± 7.39 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204415_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204417_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204417_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204417_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204417_0	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204417_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204417_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204417_0	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1724204417_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204417_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1724204417_1	24.85 ± 4.71 (3)	24.3 ± 4.11 (4)	24.3 ± 4.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1724204417_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/yons/work/RL_PCB-main/experiments/10_parameter_exeperiments/work/eval_testing_set/1724204417_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1724204417_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1724204417_1	25.01 ± 6.46 (3)	27.77 ± 7.39 (4)	27.77 ± 7.39 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1724204417_1	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed