High Performance Computer Architecture (CS60003)

Class Test 1

Model Answers

1. Estimate the speedup (in percentage) that would be obtained by replacing a CPU having an average CPI (clock cycles per instruction) of 5 and clock period of 100ns with another CPU having an average CPI of 3.5 and clock period of 120ns. [**3]**

   Ans: S=((5X100-3.5X120)/(3.5X120))X100=19%

2. Assume that you have a 16-core processor and that the number of cores to be used for executing a program can be set as a compiler parameter. Assume that 1% code of a certain program is purely sequential and the rest of the code is ideally parallel. For this program, you need a speed up of 10 over a single core performance. How many cores would you configure the compiler to use? **[3]**

   Ans: 10 = 1/(0.01+0.99/x); 1=10*x/(x+99); x = 11 processors

3. Consider a 1GHz unpipelined processor. This processor takes 4 cycles for ALU operations, 5 cycles for branches, and 4 cycles for memory operations. Assume that the relative frequencies of these operations are 50%, 30% and 15% respectively for a certain benchmark program being executed on this processor. Later, this processor was pipelined with stages similar to the simple MIPS processor. Assume a pipeline overhead of 0.15 ns. Ignoring various hazards, how much speed up will be observed while executing the given benchmark program? **[5]**

   Ans: The average instruction execution time on the unpipelined processor = Clock cycle time∗ Avg. CPI =1ns ∗ ((0.5 ∗ 4) + (0.35 ∗ 5) + (0.15 ∗ 4)) = 4.35ns ---2 Mark

   The avg. instruction execution time on pipelined processor is = 1ns +0.15ns =1.15ns ---2 Mark

   So speed up =4.35/1.15 = 3.78 ---- 1 Mark

4. For a 1 GHz processor designed based on the simple 5-stage pipelined MIPS processor, the stages were observed to be perfectly balanced. We are now required to design a new more complicated instruction for this processor. Two design options (indicated as a) and b) below) are being explored. Determine which design option would be superior for executing large programs and how much faster is it expected to run as compared to the other option? You may ignore the effect of hazards. Clearly show your work out. **[5]**

   a) Adding extra logic circuits to the execute stage of the pipeline. This would increase the latency of the EXE stage by 20%.

   Answer:

The cycle time of the processor would have to be increased by 20%. Therefore, the time to execute the program would be $(10^6+4) * 1.2 * 1nsec = 1.2 * 10^{-3}$ Sec (2Marks)

b) Adding a new stage after the EXE stage altogether, making it a 6-stage pipeline. This arrangement would leave the cycle time unaffected.

Answer:

The total number of cycles in this case would be: $(10^6+5) * 1nsec = 10^{-3}$ Sec (2Marks)

c) What will be the speedup of having an extra stage over the case of having extra logic circuitry?

Speedup = 1.2 **(1 Mark)**

5. The frequencies of two processors A and B are 2.5GHz and 2.0GHz respectively. The CPIs of these two computers are 2.5 and 2 respectively. Which computer has better MIPS rating for a given program? **[5]**

MIPS= Clock rate / $(CPI*10^6)$

Processor A: $2.5*10^9/ (2.5*10^6)=1000$ --- (2)

Processor B: $2.0*10^9/ (2*10^6)= 1000$ ---(2)

Both have equal MIPS rating ---(1)

6. Consider the following code to be run on a simple 5 stage MIPS processor.
   a) Identify the various types of dependencies in the code and label them as either true, anti, or output. The instructions have been labeled (a)-(d), to help you in identifying the dependencies in your answer. To indicate a true dependency between instructions 1 and 2 on account of t0, please write **1 --- true t0→ 2. [6]**
   b) Which of the dependencies would result in hazards? Consider the cases when there is no forwarding and when there is full forwarding? **[2]**
   c) Compute the stall cycles that would be necessary due to hazards. Consider the cases when there is no forwarding and when there is full forwarding? **[2]**
   d) Determine number of comparators that should be deployed in a simple MIPS processor for detection of data hazard. Assume that there is no data forwarding circuitry.

```
1:    lw     $t0,   0($R1)
2:    srl    $t1,   $t0,    1
3:    addi   $t2,   $t1,    1
4:    add    $t1,   $t2,    $R1
5:    sw     $t1,   28($t2)
6:    add    $t1,   $t2,    $t3
```

Ans:

a)

i. 1—true t0→2 **(1 Mark penalty for each incorrect)**
ii. 2—true t1→3
iii. 2—output t1→4
iv. 3 —true t2→4
v. 3—anti t1→4
vi. 4—true t1→5
vii. 3—true t2→5
viii. 2 — output t1→6
ix. 4 —output t1 →6
x. 6 —anti t1 → 5
xi. 6 —anti t1→ 3
xii. 3 —true t2 →6

b) No forwarding: i) ii) iv) vi) vii)
With forwarding: Only i)

c) No forwarding: 8 Cycles
With forwarding: 1 Cycle

d) 4

7. Three enhancements with the following speed-ups are proposed for a new version of a processor: Enhancement A: Speed-up = 10; Enhancement B: Speed-up = 4; Enhancement C: Speed-up = 2. Enhancement A is usable for the entire execution time of a program irrespective of the usage of Enhancements B and C. However, enhancements B and C are such that they are usable 20% time each, but are usable only one at a time. Compute the speed up that would be achieved the new processor. **[6]**

Ans: Speed up due to enhancement A= 1/[(1/10) = 10 --- Award 2 marks

Speedup due to enhancements B and C = 10/(0.6+0.2/4+0.2/2)] =10/0.75 = 40/3=13.33 ------- Award 4 marks

8. Assume that the cost of a processor using a simple 5 stage MIPS pipeline is 25% of the total cost of a computer system. The disks, main memory, power supply and enclosure make up the other 75% of the total cost. It is now proposed to increase the speed of the processor by a factor of 10 using a superscalar design approach. But this will increase the cost of the processor by a factor of 10. However, simulation studies show that the superscalar processor would have to wait on the average 30% of time for I/O. On the other hand, the original pipelined processor stalled only 10% time for I/O. From a cost/performance viewpoint, is increasing the speed by a factor of 10 desirable? Assume that both the processors do not

stall on account of data or control hazards. Justify your answer with a quantitative analysis of the two computers. **[6]**

Ans Let us normalize cost to simple 5-stage MIPS pipelined computer:
Computer 1 = processor 0.25 + Other 0.75 = 1.00
Computer 2 = processor 2.50 + Other 0.75 = 3.25 …….. Award 2 marks
Therefore 3.25× increase in cost

Original Computer stalls 10% of the time. Therefore does useful work 90% of time.
Useful non pipelined cycles = 0.9. …….. award 1 mark

Pipelined CPU 10x faster, but stalls 30% of the time, and therefore does useful work 70% of the time. Useful CPU pipelined cycles = 10 x 1 x 0.7 = 7 …….award 2 marks

3.25 x cost increase produces 7x performance improvement. … award 1 mark
Therefore the enhancement is worthwhile.

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