top_level Project Status			
Project File:	newRadixBooth.xise	**Parser Errors:**	No Errors
Module Name:	top_level	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3ftg256	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	157 Warnings (157 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	63	18,224	1%	
Number used as Flip Flops	63			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	196	9,112	2%	
Number used as logic	192	9,112	2%	
Number using O6 output only	173			
Number using O5 output only	13			
Number using O5 and O6	6			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	4			
Number with same-slice register load	1			
Number with same-slice carry load	3			
Number with other load	0			
Number of occupied Slices	69	2,278	3%	
Number of MUXCYs used	60	4,556	1%	
Number of LUT Flip Flop pairs used	196			
Number with an unused Flip Flop	135	196	68%	
Number with an unused LUT	0	196	0%	
Number of fully used LUT-FF pairs	61	196	31%	
Number of unique control sets	7			
Number of slice register sites lost to control set restrictions	33	18,224	1%	
Number of bonded IOBs	19	186	10%	
Number of LOCed IOBs	18	19	94%	
Number of RAMB16BWERs	0	32	0%	

Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	3.72			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Mar 13 14:41:23 2020	0	156 Warnings (156 new)	10 Infos (10 new)
Translation Report	Current	Fri Mar 13 14:41:29 2020	0	0	0
Map Report	Current	Fri Mar 13 14:41:42 2020	0	1 Warning (1 new)	7 Infos (7 new)
Place and Route Report	Current	Fri Mar 13 14:41:51 2020	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Fri Mar 13 14:41:56 2020	0	0	4 Infos (4 new)
Bitgen Report	Current	Fri Mar 13 14:42:04	0	0	0

		2020			

Secondary Reports		[-]
Report Name	**Status**	**Generated**
WebTalk Report	Current	Fri Mar 13 14:42:05 2020
WebTalk Log File	Current	Fri Mar 13 14:42:05 2020

Date Generated: 03/13/2020 - 14:44:16