

TRANSISTOR.  $\rightarrow$   $0.7\text{V}(\text{Si}) / 0.3\text{V}(\text{Ge})$  at anode.

BJT (Bipolar Junction Transistor) =  $I_{\text{base}} \propto I_{\text{emitter}}$  (currents).

FET (Field Effect Transistor) =  $V_{\text{GS}} \propto I_{\text{drain}}$ .

JFET.  $\curvearrowleft$  (MOSFET). metal oxide.

Depletion.

Depletion.

Enhancement.

N-channel P-channel.

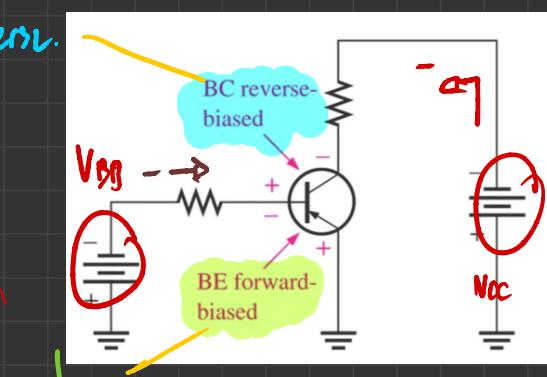
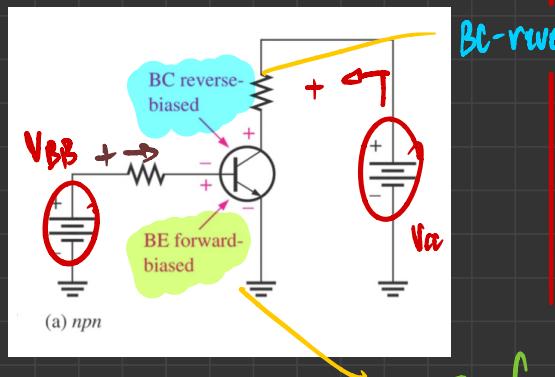
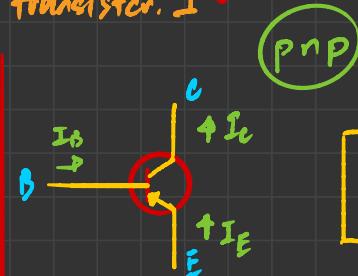
N-channel  
P-channel.

N-channel  
P-channel.

Application for transistor.  $\rightarrow$  1. Amplifier / 2. Switch.

\* three terminal device which output current, voltage or power in input.

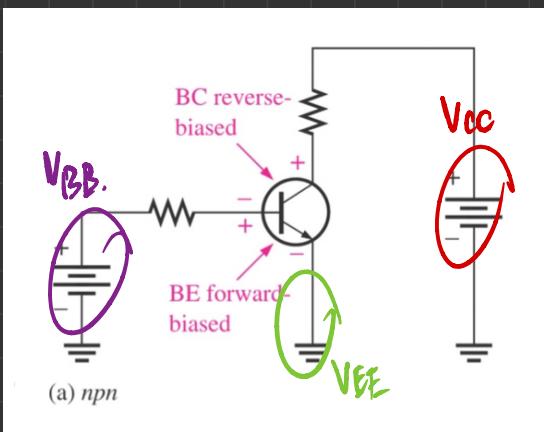
• [types of transistor.] •



\*  $V_{CC} > V_{BB}$  !

BE - forward.

## [transistor voltages]



$V_{CC}$  → The power supply voltage.

$V_{BB}$  → dc voltage used to bias T.

$V_{EE}$  → connect to ground easily.

$V_C$  → collector to ground.

$V_B$  → base to ground.

$V_E$  → emitter to ground.

$V_{CE}$  → V measured from collector to emitter.

$V_{BE}$  → V measured from base to emitter.

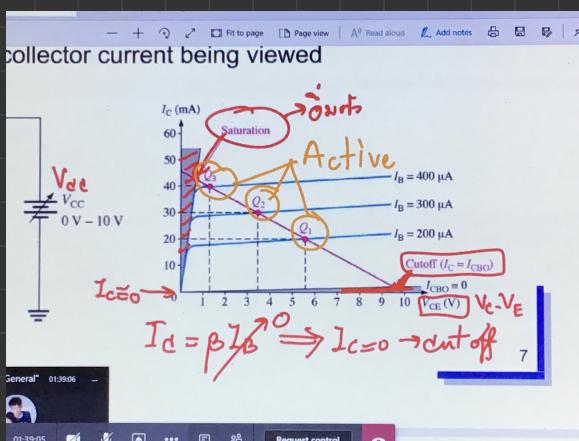
$V_{CB}$  → V measured from collector to base.

## [current in transistor]

$$I_E = I_B + I_C$$

$$I_O = \beta_{DC} I_B$$

$$I_E = I_B + \beta I_B$$



## [Operating Region]

1. Active

2. Cutoff.

3. Saturation.

Cutoff.  $\rightarrow$  Both transistor junctions are reverse bias.

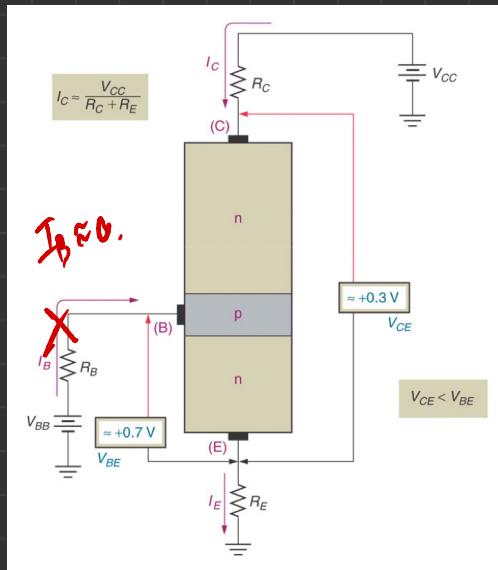
$$V_{CE} = V_{CC}$$

$$I_B = 0 \rightarrow I_C = 0$$

Saturation.  $\rightarrow$  Both transistor junctions are forward bias.

$\rightarrow I_C$  reaches maximum value.

$$V_{CE} = 0$$



Proof. Eq. (KVL)

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0.$$

$$\therefore V_{OC} - V_{CE} = I_C (R_C + R_E)$$

$$\therefore I_C = \frac{V_{CC}}{R_C + R_E}$$

as when  $I_{Cmax}$  of.

$$V_{BE} \approx 0.7 \text{ V.}$$

Active  $\rightarrow$  BE forward bias, CE reverse bias.

$\rightarrow I_C$  depends on  $\beta$  and  $I_B$ .

$$\rightarrow V_{CE} \approx 0.7 \text{ V } (V_{BE} < V_{CE} < V_{CC})$$

Note!  $\propto$  (Alpha) ratio of  $I_C$  to  $I_E$ :

$$\alpha_{DC} = \frac{I_C}{I_E} \rightarrow \alpha_{DC} \approx 1.$$

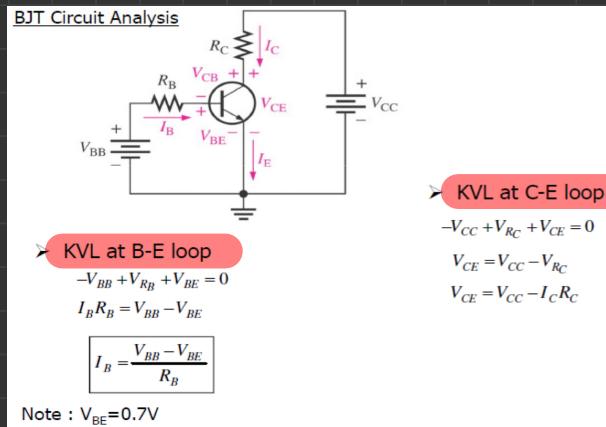
## [ Current and Voltage analysis ] .

- $V_{BE} \approx 0.7 \text{ V}$  (forward bias)
- if  $V_E = 0$ , by KVL.  $V_{RB} = V_{BB} - V_{BE} = 0$  ,  $V_{RB} = I_B R_B = 0$
- $-V_{CC} + V_{RC} + V_{CE} = 0$  (KVL)

$\therefore$

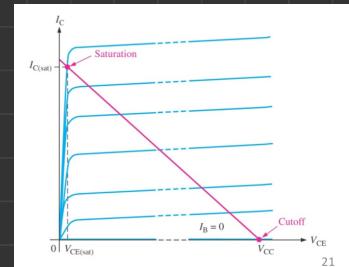
$$V_{CE} = V_{CC} - V_{RC}$$

$$V_{RC} = I_C R_C$$



## [ Dc load line ] .

- Dc load line = line between cutoff, saturation
- Ideal of cutoff.  $I_C = 0$ ,  $V_{CE} = V_{CC}$
- Ideal of saturation.  $I_C = I_{C(sat)}$ ,  $V_{CE} \approx 0$
- A line between cutoff, saturation is active region.



[BJT as a switch].

1. cutoff.  $\rightarrow$  switch off.
2. saturation.  $\rightarrow$  switch on.

\*Active - விசைப்புவாறு கொள்ளுத்  
கொடுக்குவது.

