



Transistor bias circuits

Objectives



- Discuss the concept of dc biasing of a transistor for linear operation
- Analyze voltage-divider bias, base bias, emitter bias and collector-feedback bias circuits.
↳ configuration -

Biasing

(බයිසින්ඩි)



Biasing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

Operating Point

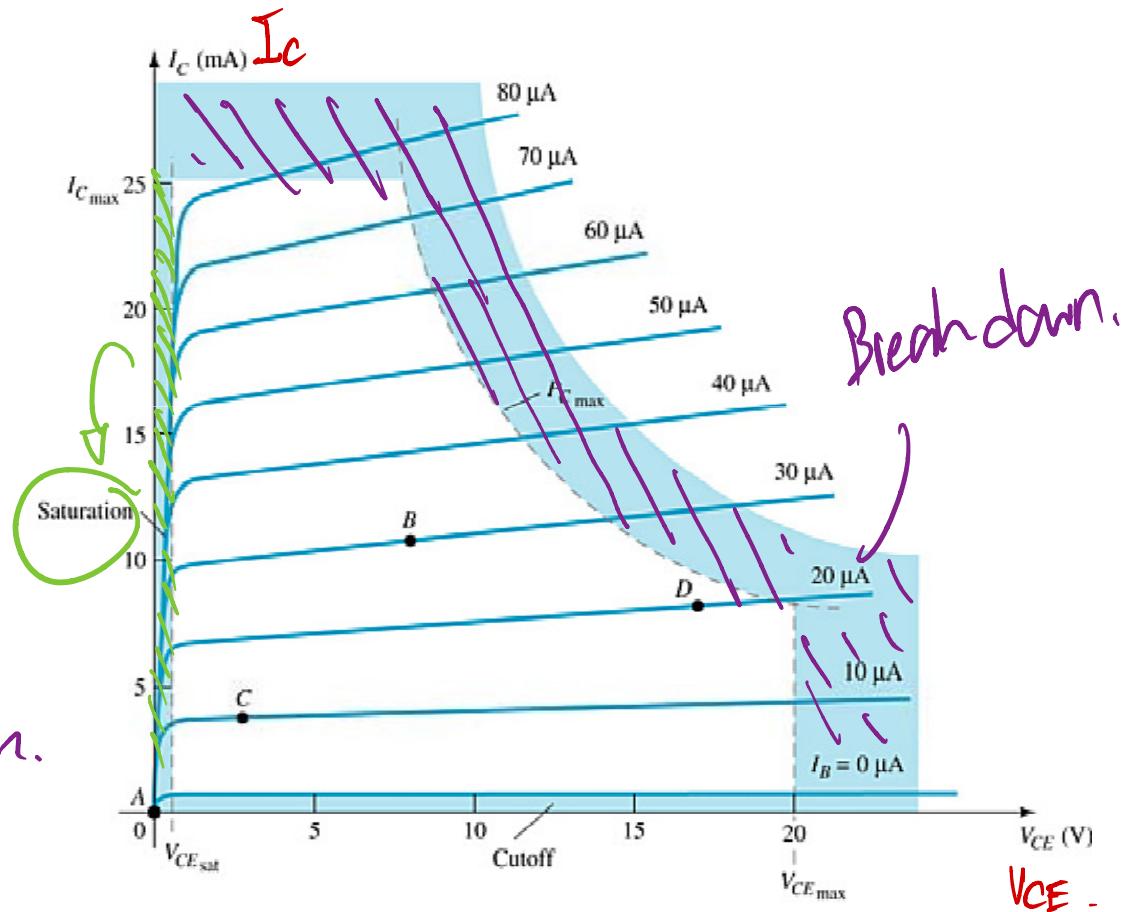


The DC input establishes an operating or *quiescent point* called the *Q-point*.

$I_C, V_{CE} \rightarrow$ minimum power.

① β or load line
② Q point.

③ I_{CQ} } dimension regulation.
④ V_{CEOQ}



The Three States of Operation



- **Active or Linear Region Operation**
 - Base–Emitter junction is forward biased Base–Collector junction is reverse biased
- **Cutoff Region Operation**
 - Base–Emitter junction is reverse biased
- **Saturation Region Operation**
 - Base–Emitter junction is forward biased Base–Collector junction is forward biased

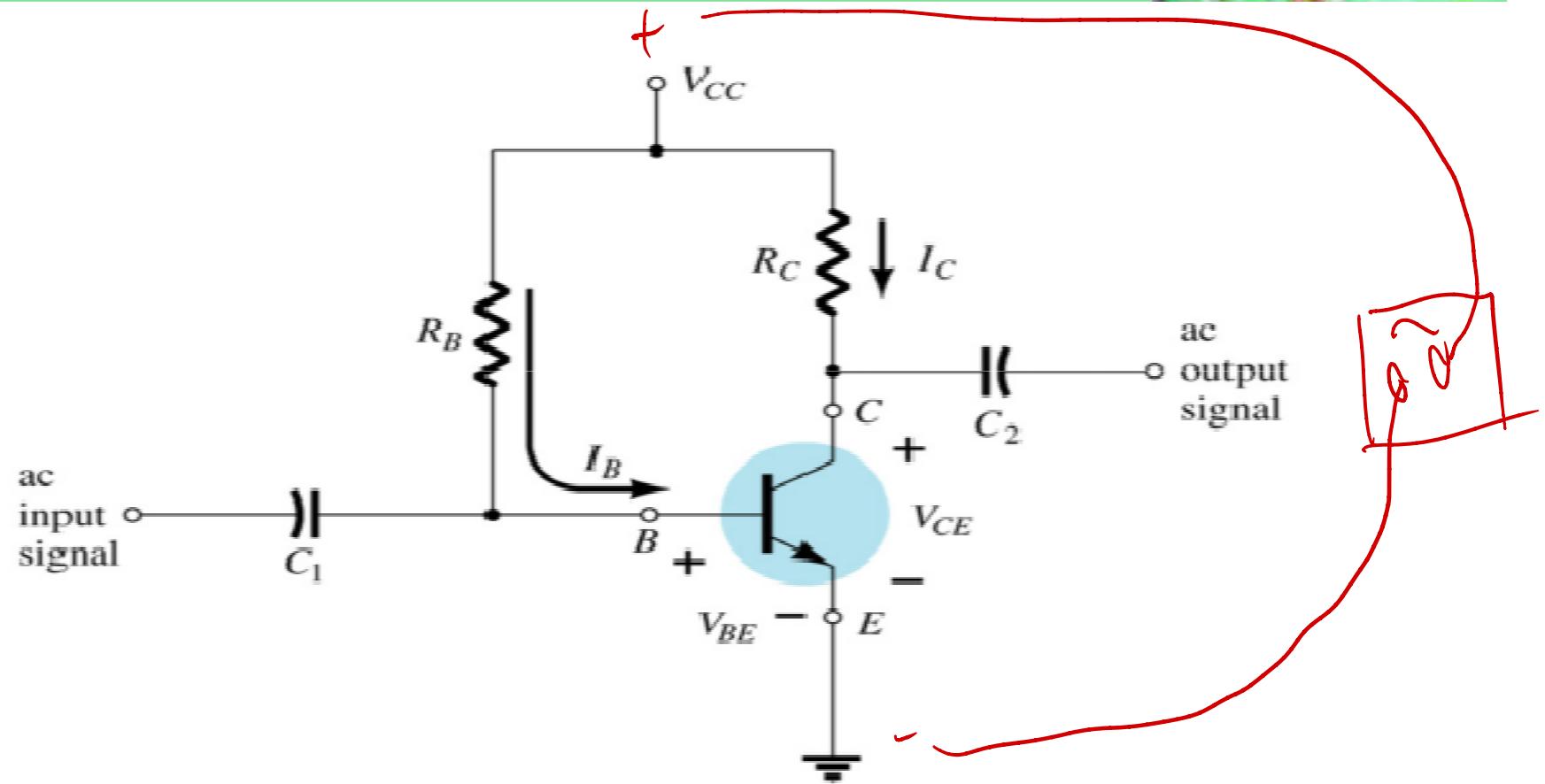
DC Biasing Circuits



5 IDEAS:
Next shown -

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback

Fixed Bias



The Base - Emitter Loop

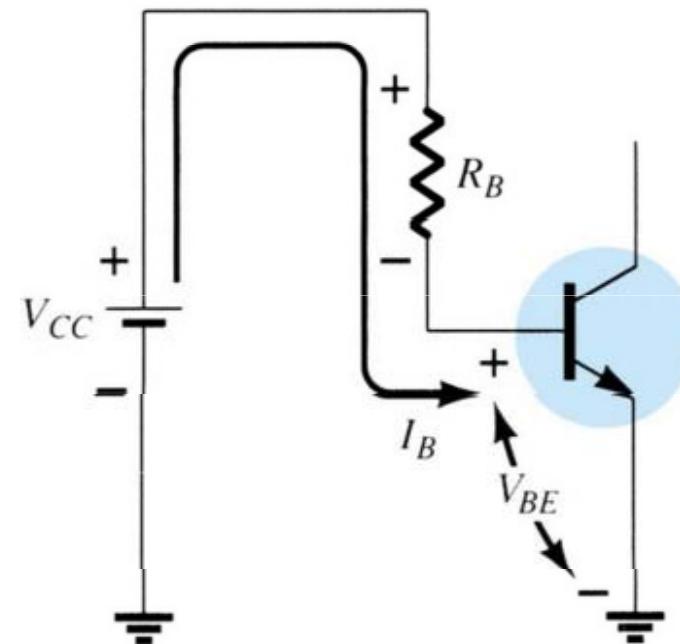


From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



Collector-Emitter Loop

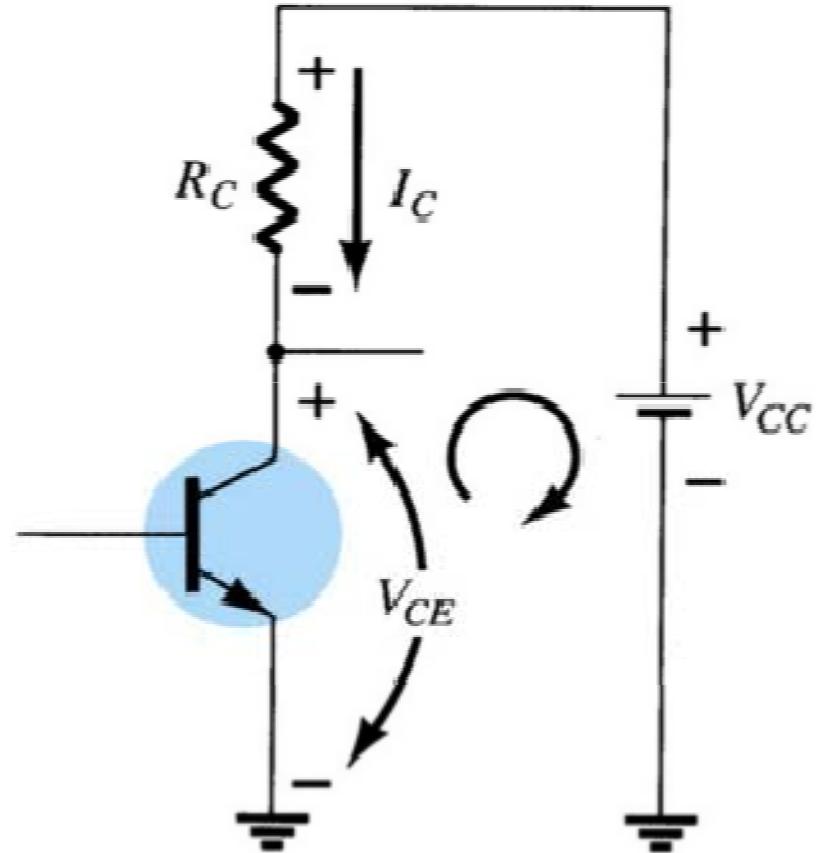


Collector current:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$



Saturation



When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

$$I_{C\text{sat}} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \approx 0 \text{ V}$$

Load Line Analysis



The end points of the load line

are: $I_{C\text{sat}}$

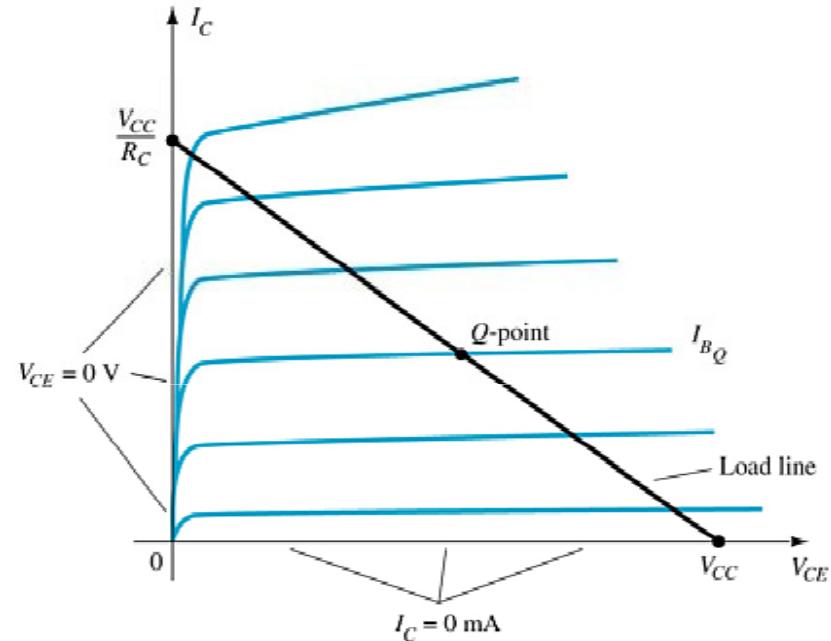
$$I_C = V_{CC} / R_C$$

$$V_{CE} = 0 \text{ V}$$

$V_{CE\text{cutoff}}$

$$V_{CE} = V_{CC}$$

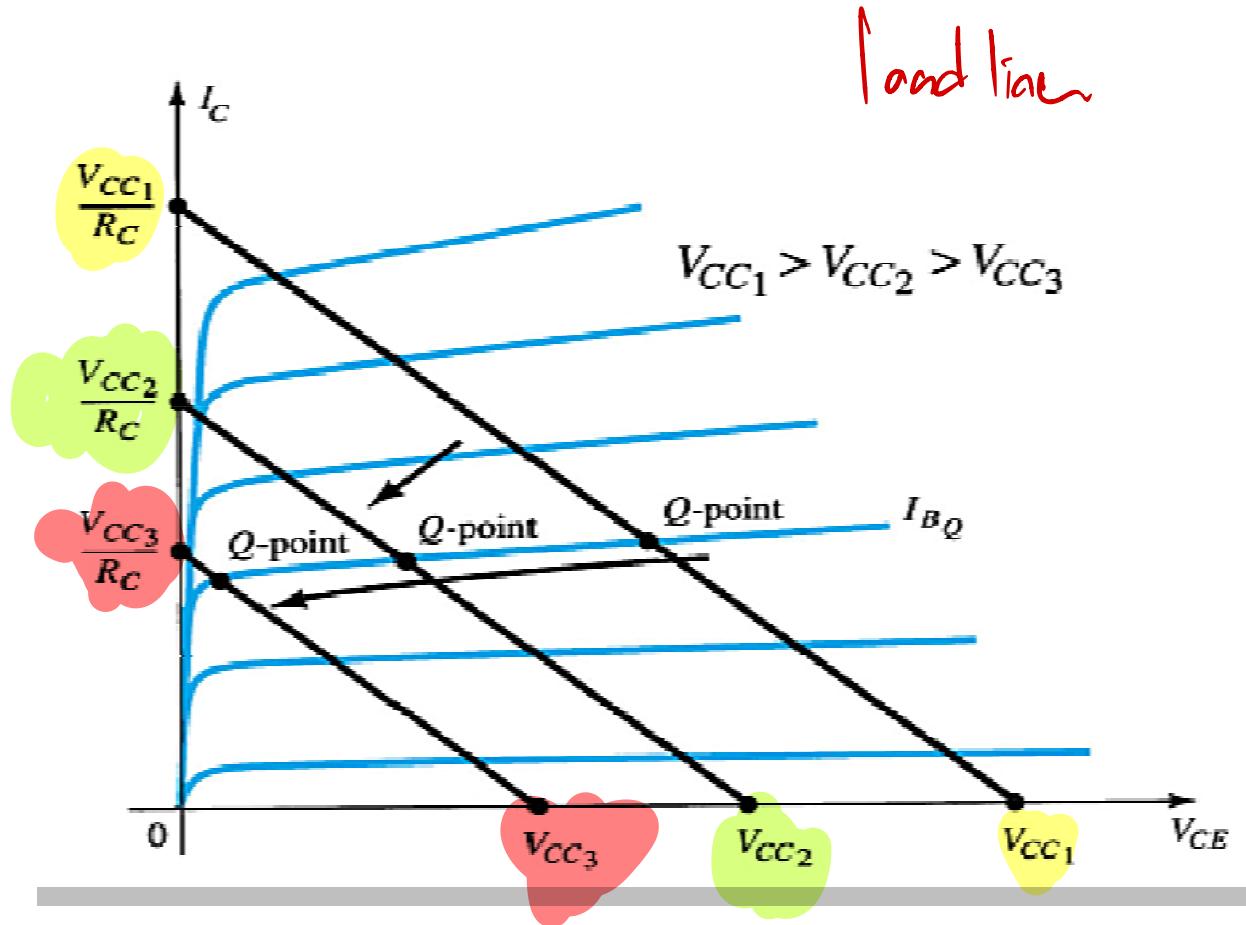
$$I_C = 0 \text{ mA}$$



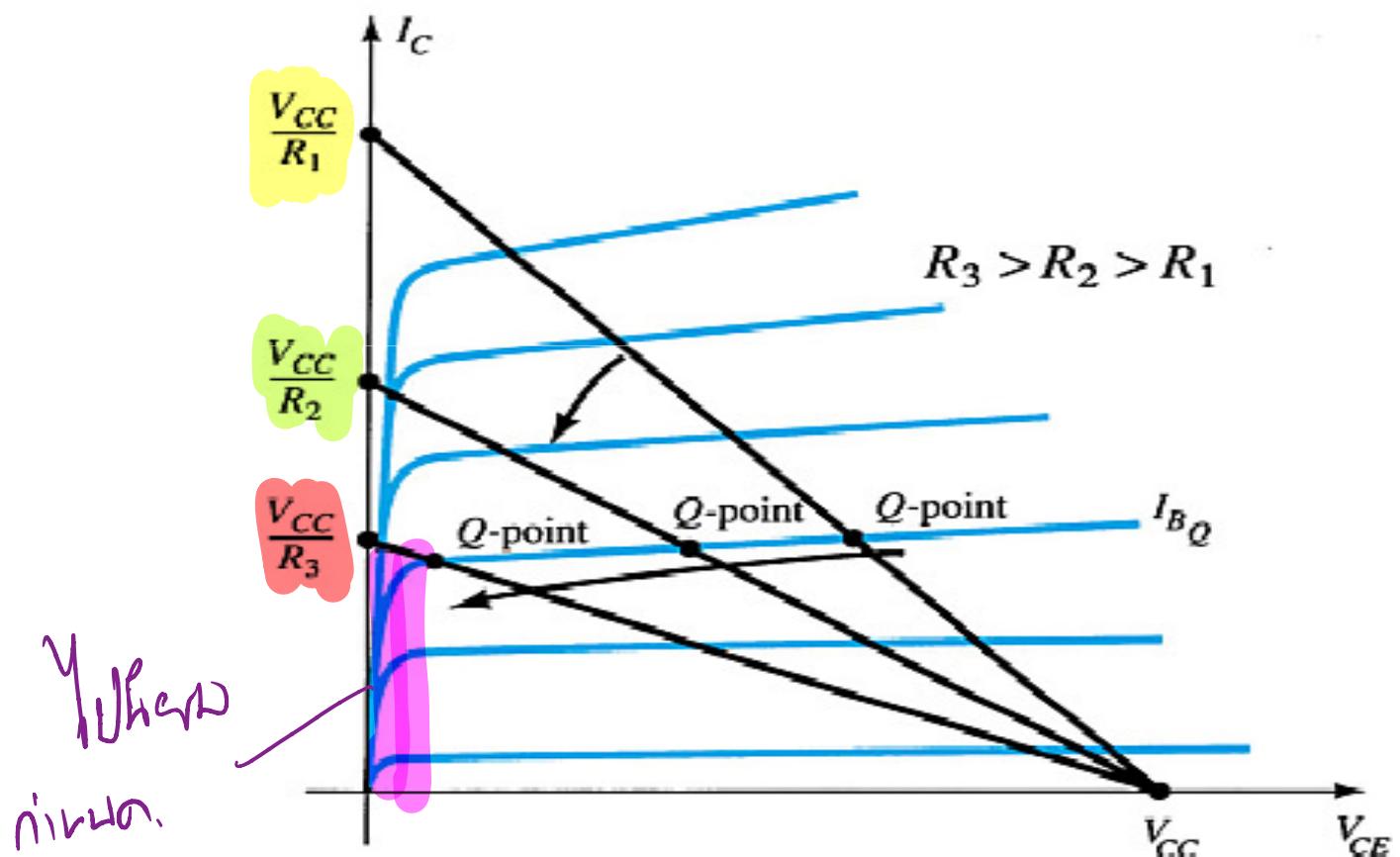
The *Q*-point is the operating point:

- where the value of R_B sets the value of I_B
- that sets the values of V_{CE} and I_C

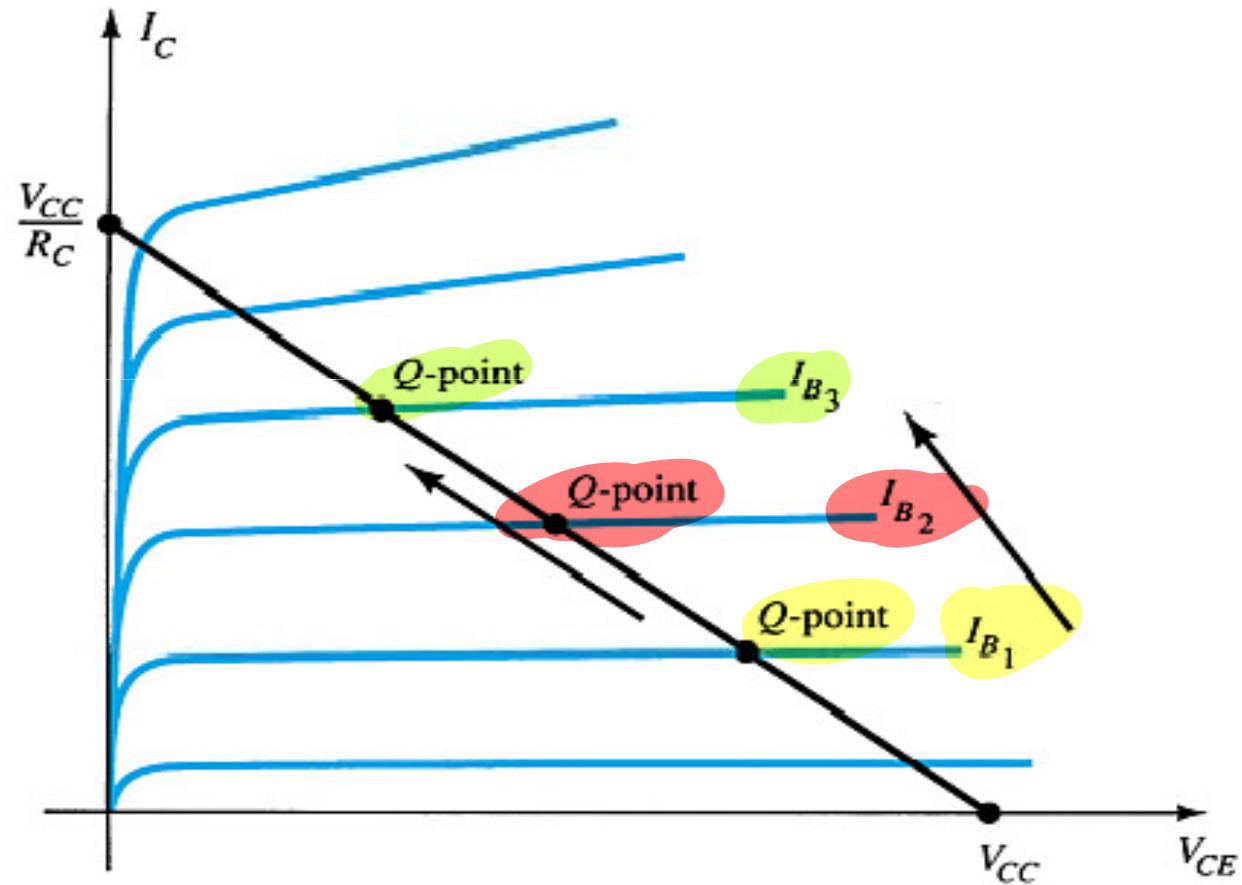
Circuit Values Affect the Q-Point



Circuit Values Affect the Q-Point



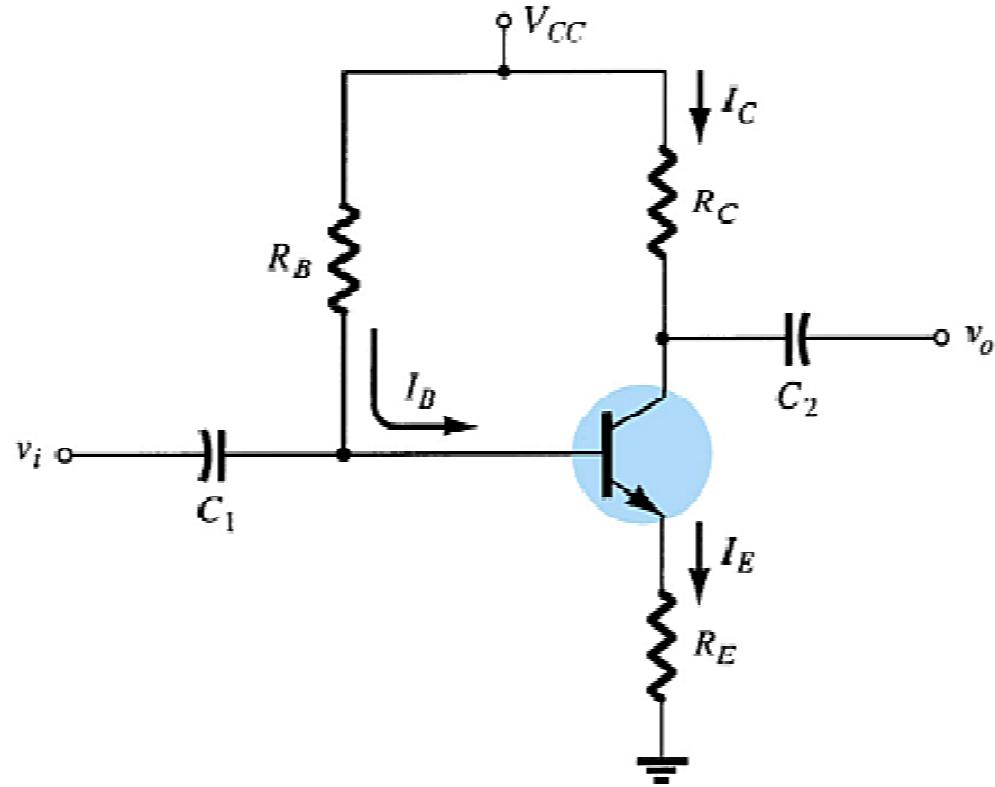
Circuit Values Affect the Q-Point



Emitter-Stabilized Bias Circuit



Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



Base-Emitter Loop



From Kirchhoff's voltage law:

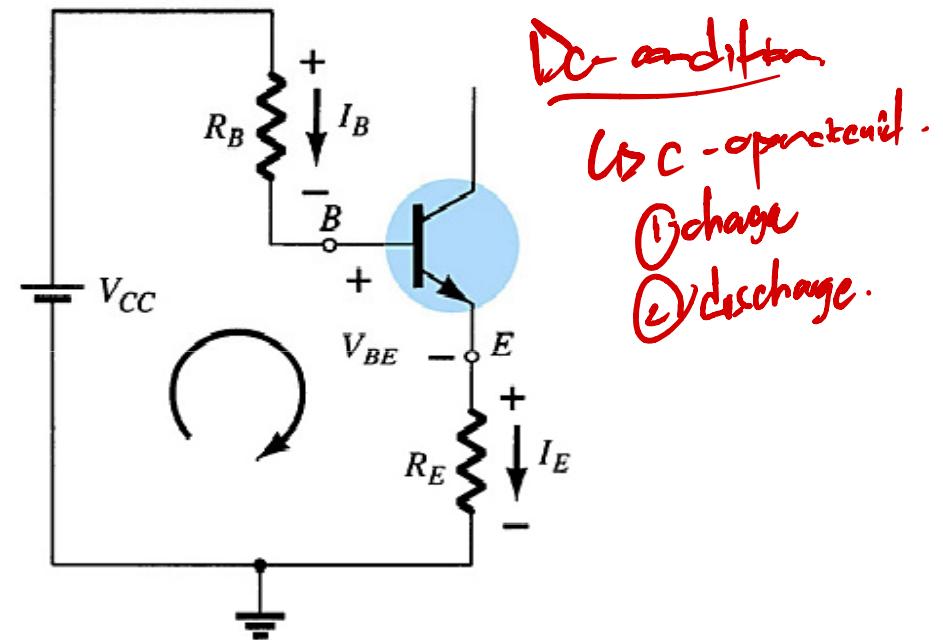
$$+ V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - (\beta + 1)I_B R_E - V_{BE} = 0$$

Solving for I_B :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$



Collector-Emitter Loop



From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \approx I_C$:

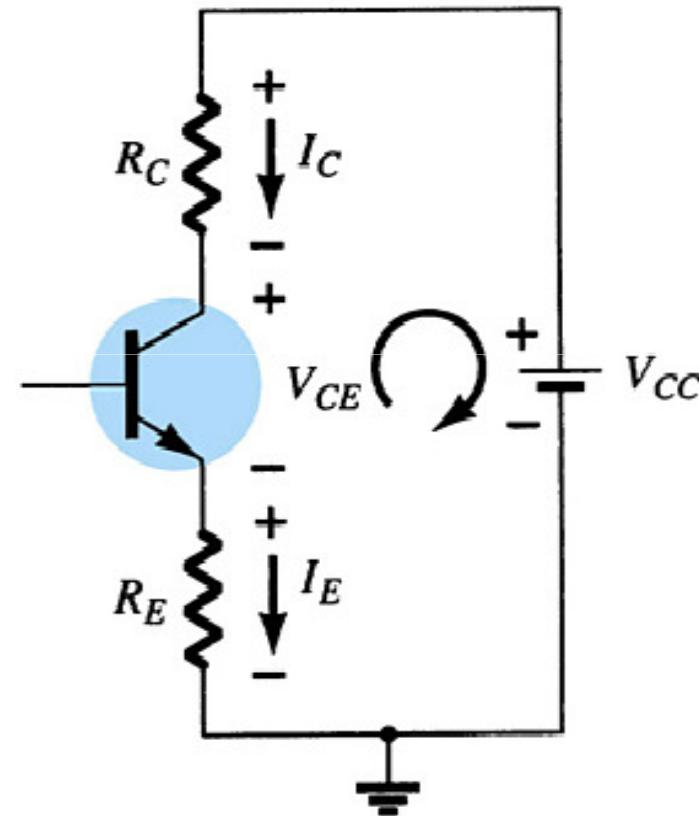
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$



b'g news.

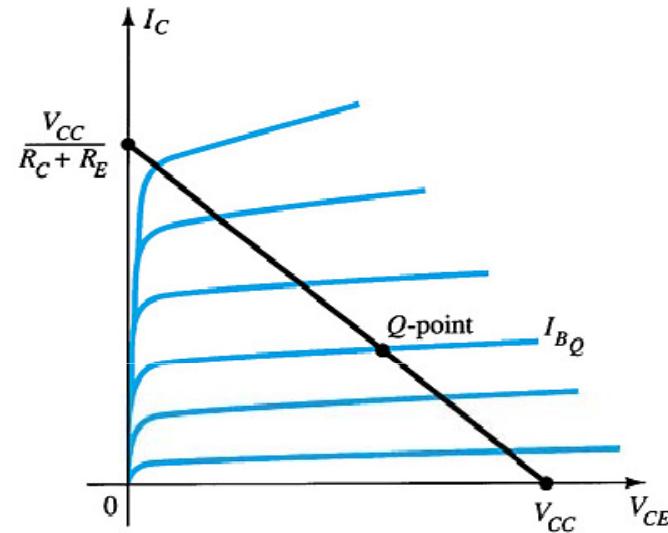
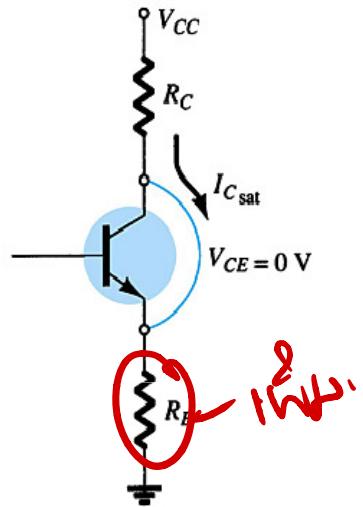
Improved Biased Stability



Stability refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.

Adding RE to the emitter improves the stability of a transistor.

Saturation Level



The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$$V_{CE} = V_{CC}$$

$$I_C = 0 \text{ mA}$$

I_{Csat} :

$$V_{CE} = 0 \text{ V}$$

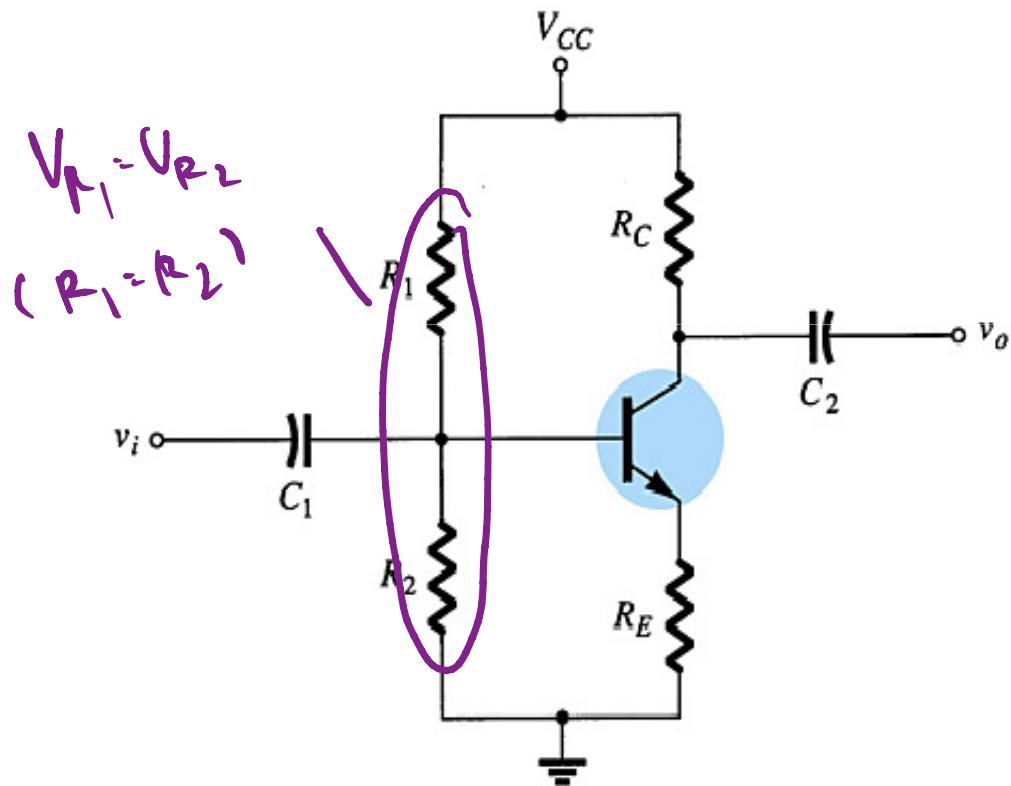
$$I_C = \frac{V_{CC}}{R_C + R_E}$$

Voltage Divider Bias



This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in β .



Approximate Analysis



Where $I_B \ll I_1$ and $I_1 \approx I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

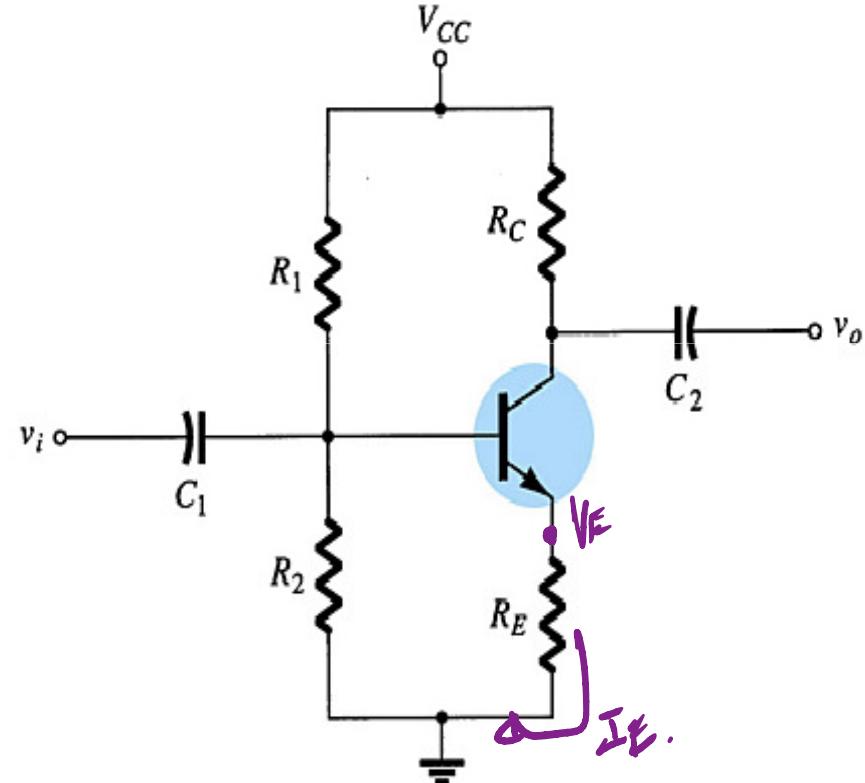
$$V_E = V_B - V_{BE}$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \approx I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$



Voltage Divider Bias Analysis



Transistor Saturation Level

$$I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0\text{mA}$$

Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

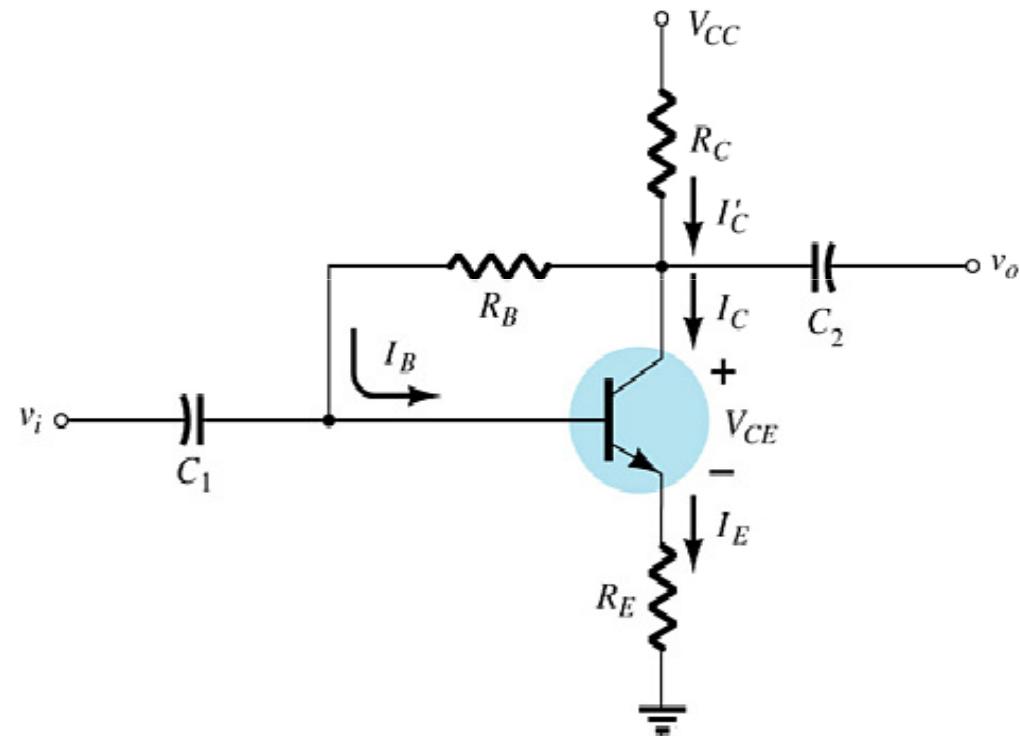
$$V_{CE} = 0\text{V}$$

DC Bias with Voltage Feedback



Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, β .



Base-Emitter Loop



From Kirchhoff's voltage law:

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Where $I_B \ll I_C$:

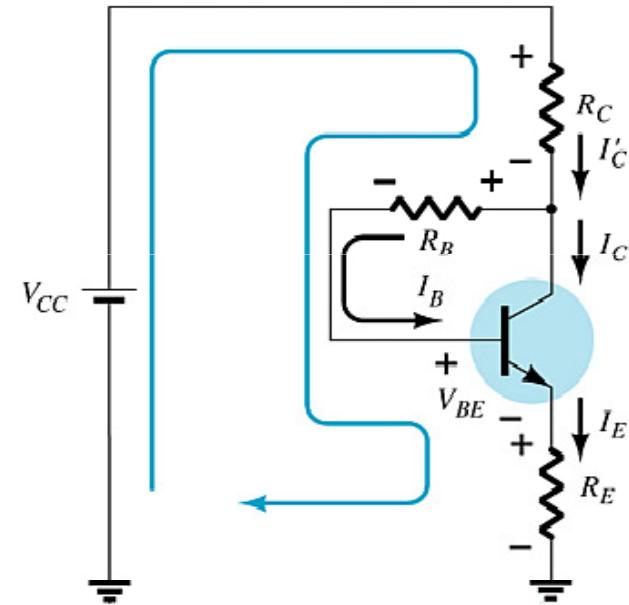
$$I'_C = I_C + I_B \approx I_C$$

Knowing $I_C = \beta I_B$ and $I_E \approx I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Solving for I_B :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$



Collector-Emitter Loop



Applying Kirchoff's voltage law:

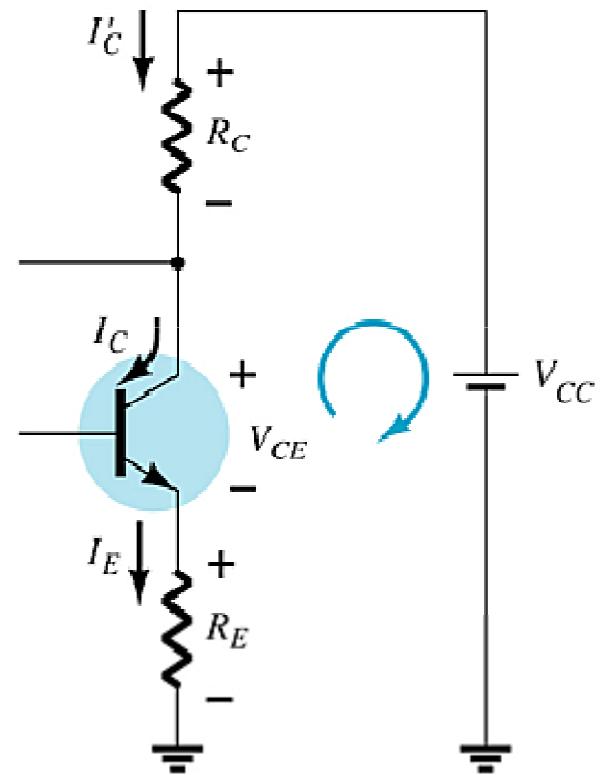
$$I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I''_C \approx I_C$ and $I_C = \beta I_B$:

$$I_C (R_C + R_E) + V_{CE} - V_{CC} = 0$$

Solving for V_{CE} :

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$



Base-Emitter Bias Analysis



Transistor Saturation Level

$$I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$\begin{aligned} V_{CE} &= V_{CC} \\ I_C &= 0 \text{ mA} \end{aligned}$$

Saturation:

$$\begin{aligned} I_C &= \frac{V_{CC}}{R_C + R_E} \\ V_{CE} &= 0 \text{ V} \end{aligned}$$

PNP Transistors



The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.

Analysis of Voltage Bias for PNP Transistor



- Base voltage

$$V_B = \left(\frac{R_1}{R_1 + R_2 \parallel \beta_{DC} R_E} \right) V_{EE}$$

- Emitter voltage

$$V_E = V_B + V_{BE}$$

- By Ohm's Law,

$$V_{EE} = V_B + I_B R_B + I_E R_E + V_{BE}$$

- And,

$$V_C = I_C R_C$$

$$V_{EC} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E = \frac{V_{EE} - V_B - V_{BE}}{R_E + \frac{R_B}{\beta_{DC}}}$$

Example 1



- Evaluate IC and VEC for pnp transistor circuit in Figure below.
Given $V_{EE} = +15V$, $R_1 = 63k\Omega$, $R_2 = 27k\Omega$, $R_C = 1.8k\Omega$, $R_E = 2.6k\Omega$, $\beta_{DC} = 120$.

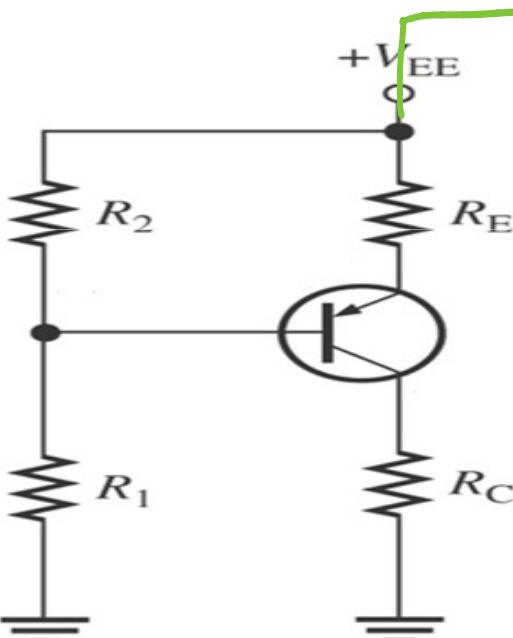
$$\therefore -V_{EE} + \beta I_B R_E + V_{CE} = 0$$

$$+ \beta I_B R_C = 0$$

$$I_B = \frac{V_{EE} - V_{CE}}{\beta (R_C + R_E)}$$

$$I_B = \frac{15 - 0}{120 (4.4k)} = \frac{15}{528k}$$

$$\therefore I_C = \beta I_B = \frac{15}{4400} A.$$



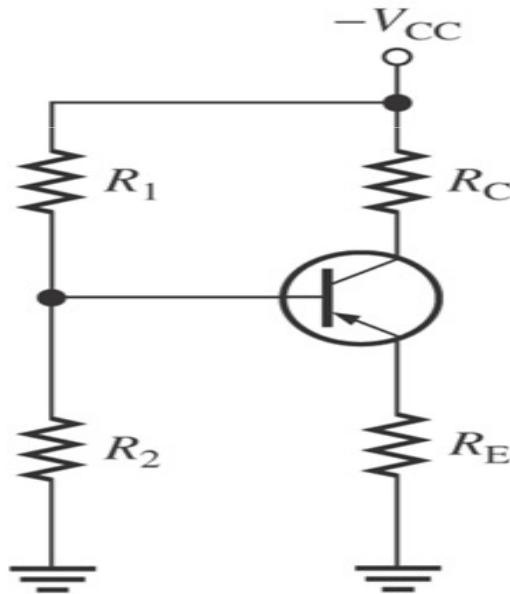
$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C = 0$$

V_{EE} is 15V.

Example 2



- Figure below shows the schematic with a negative supply voltage, determine IC and VCE for a pnp transistor circuit with given values: $R_1 = 25\text{k}\Omega$, $R_2 = 60\text{k}\Omega$, $R_C = 6\text{k}\Omega$, $R_E = 9\text{k}\Omega$, $V_{CC} = -12\text{V}$, and $\beta_{DC} = 90$



Example 3



- Construct a complete circuit required to replace the transistor in Figure below with a pnp transistor. Given $V_{CC} = 10V$, $R_1 = 78k\Omega$, $R_2 = 100k\Omega$, $R_C = 18k\Omega$, $R_E = 8k\Omega$.

