

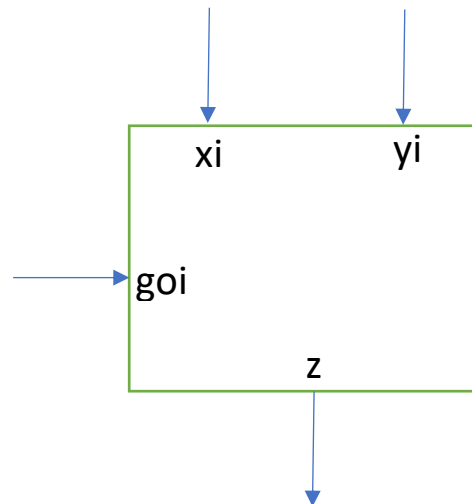
CSE 234 Logic Circuits and Digital Design

Lab 6 – FSM with Datapath

Lab Session (Exact Duration: 90min):

C code:

```
while (goi==0) ;  
x = xi;  
y = yi;  
z = 1;  
diff = x - y;  
diff2 = diff;  
while(diff > 0) {  
    z = z * diff2;  
    diff = diff - 1;}  
}
```



- First draw ASM.
- Design datapath on Logisim and update ASM accordingly.
- Design your FSM controller using Logisim and combine datapath and controller in Logisim.
- Simulate your resultant circuit to be sure it works flawless.

Rules:

DO NOT USE ANALYZE CIRCUIT PROPERTY OF LOGISIM. You can use multiplier subtractor or adder in Logisim. Using less components makes a better score. X, y, z, diff and diff2 are registers in datapath. Assume 8 bit numbers.

Demo Session:

During demo, explain and simulate each step of your design. Do not forget you only have at most 4 minutes for that. Also you will answer any questions asked by the TA.