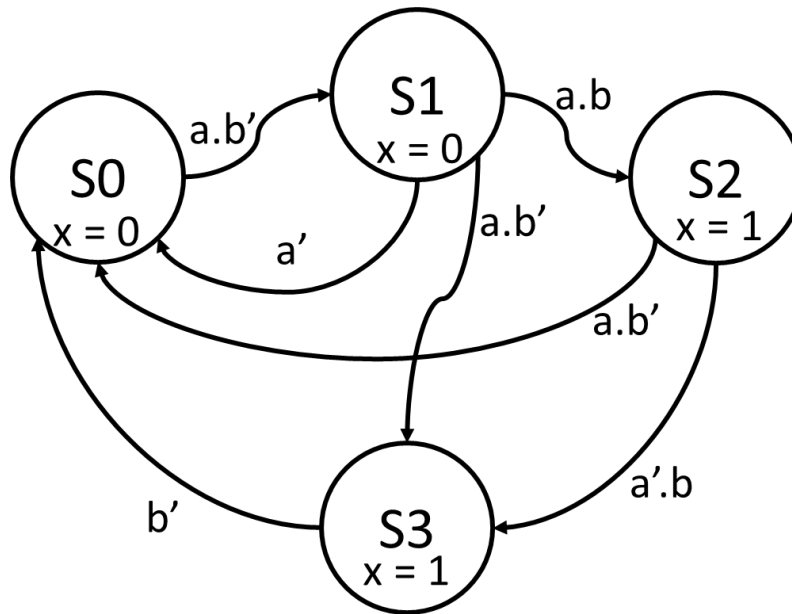# CSE 234 Logic Circuits and Digital Design

Lab 3 – Basic FSM Controller Design

Lab Session (Exact Duration: 60min):

You will design the following FSM in this lab session:

Assume if any one of the transition conditions is not satisfied, then the FSM stays at its current state.

a and b are input signals and x is the output signal for that FSM. Connect x signal to a red led. a and b will be the input pins for your FSM.

a. Draw the state table for this FSM.
b. Extract and simplify Boolean equations for next state logic us.ng your table.
c. Design and simulate your FSM in Logisim. Do not forget to observe the state when different inputs come to the FSM.

Demo Session:

Show and prove that you have accurately designed the above FSM and answer the questions of the TA. Show that you make right transitions and go to the right state. Remind that you have 4 minutes to express yourself so be prepared for the demo.