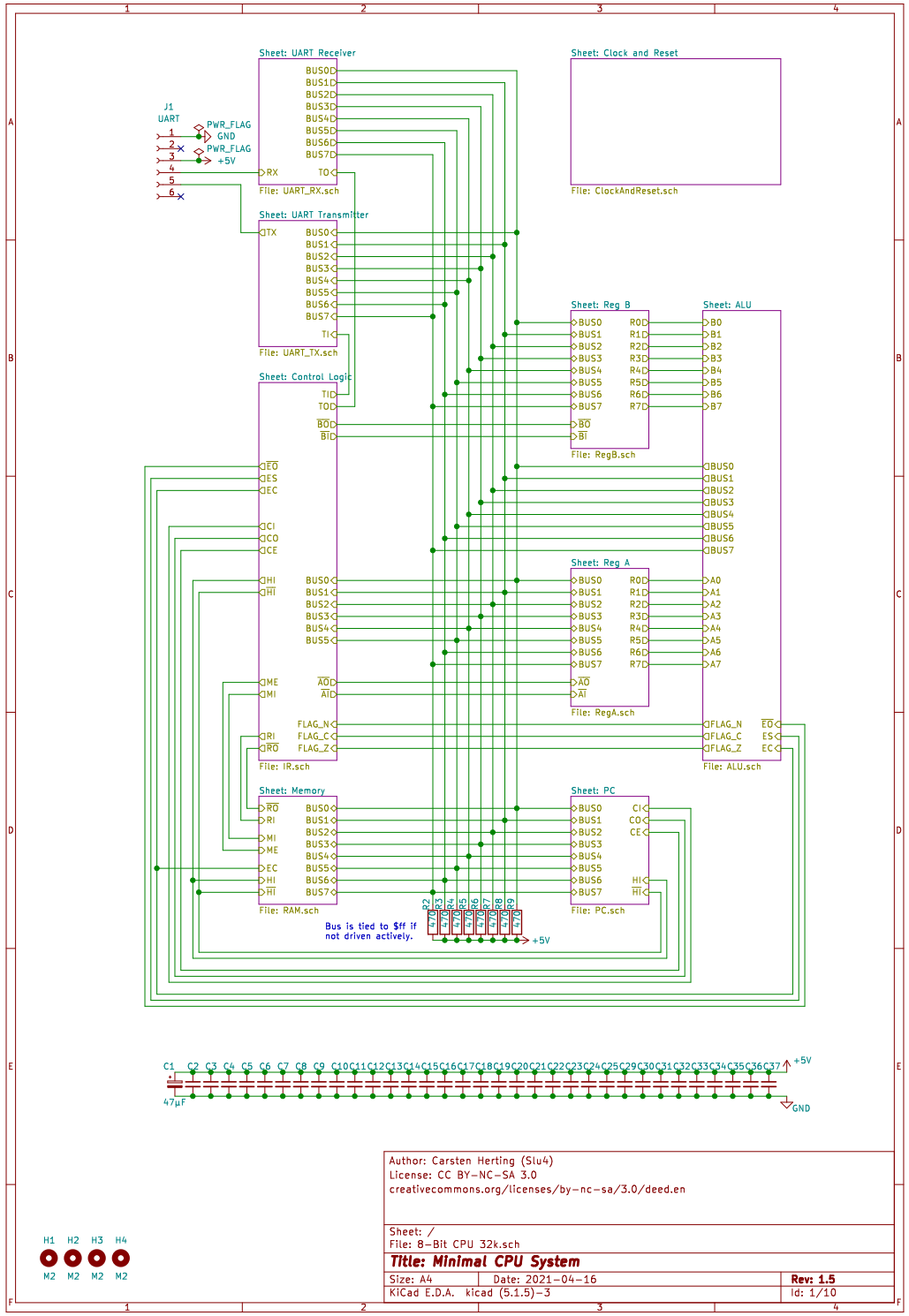

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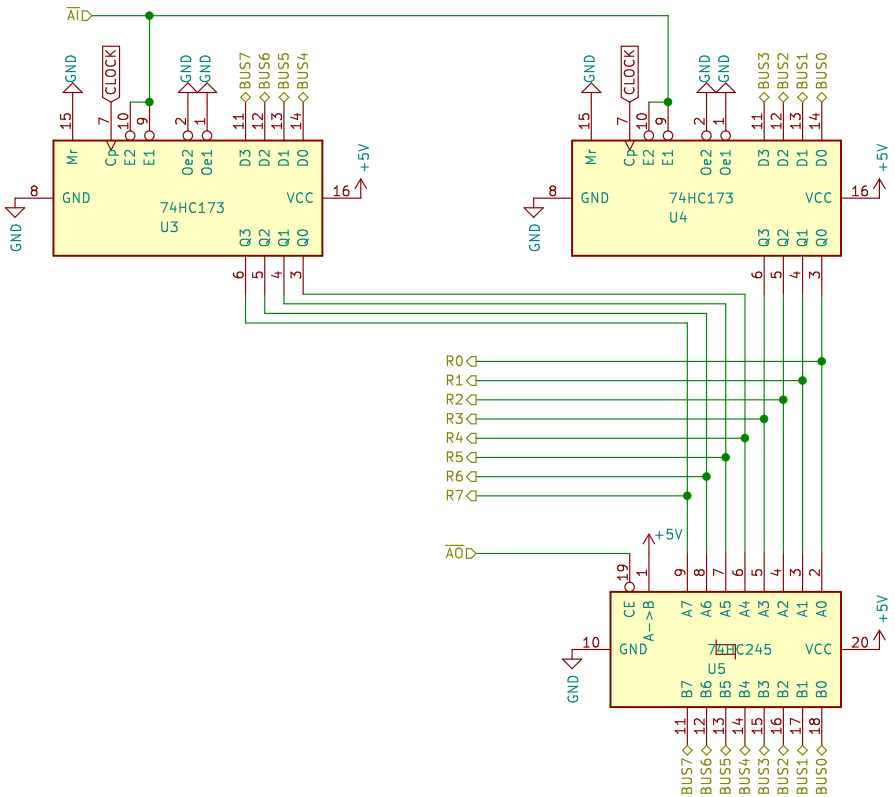
Sheet: /
File: 8-Bit CPU 32k.sch

Title: Minimal CPU System

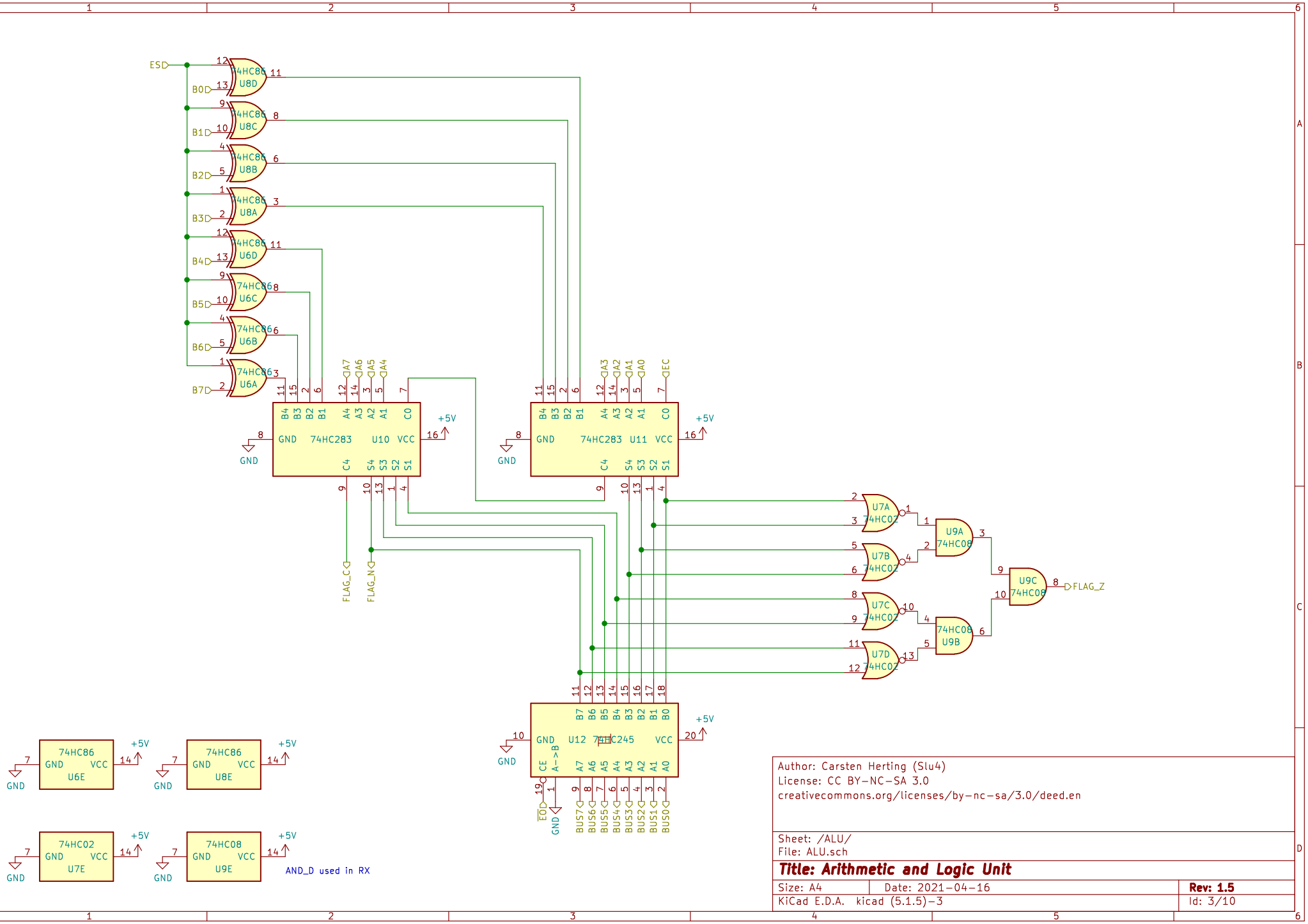
Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/10



Sheet: /Reg A/
File: RegA.sch

Title: A Register

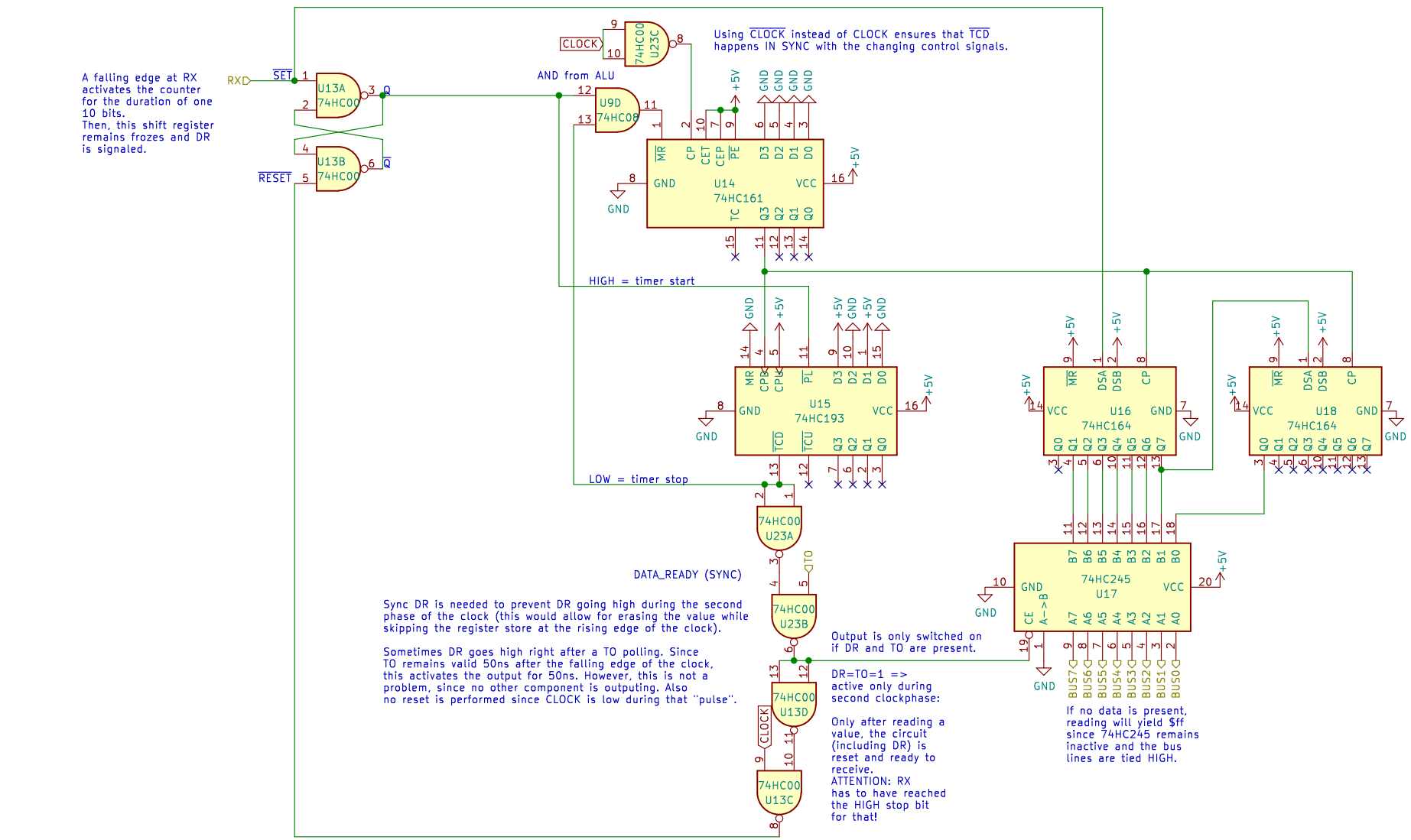
Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/10



Sheet: /ALU/
File: ALU.sch

Title: Arithmetic and Logic Unit

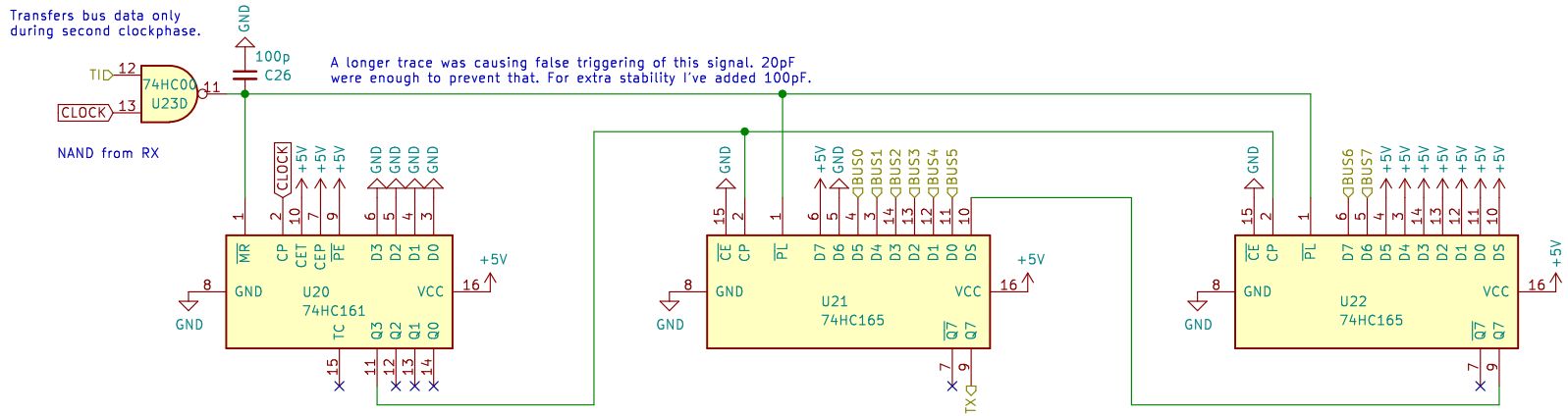
Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 3/10



Sheet: /UART Receiver/
File: UART_RX.sch

Title: UART Receiver

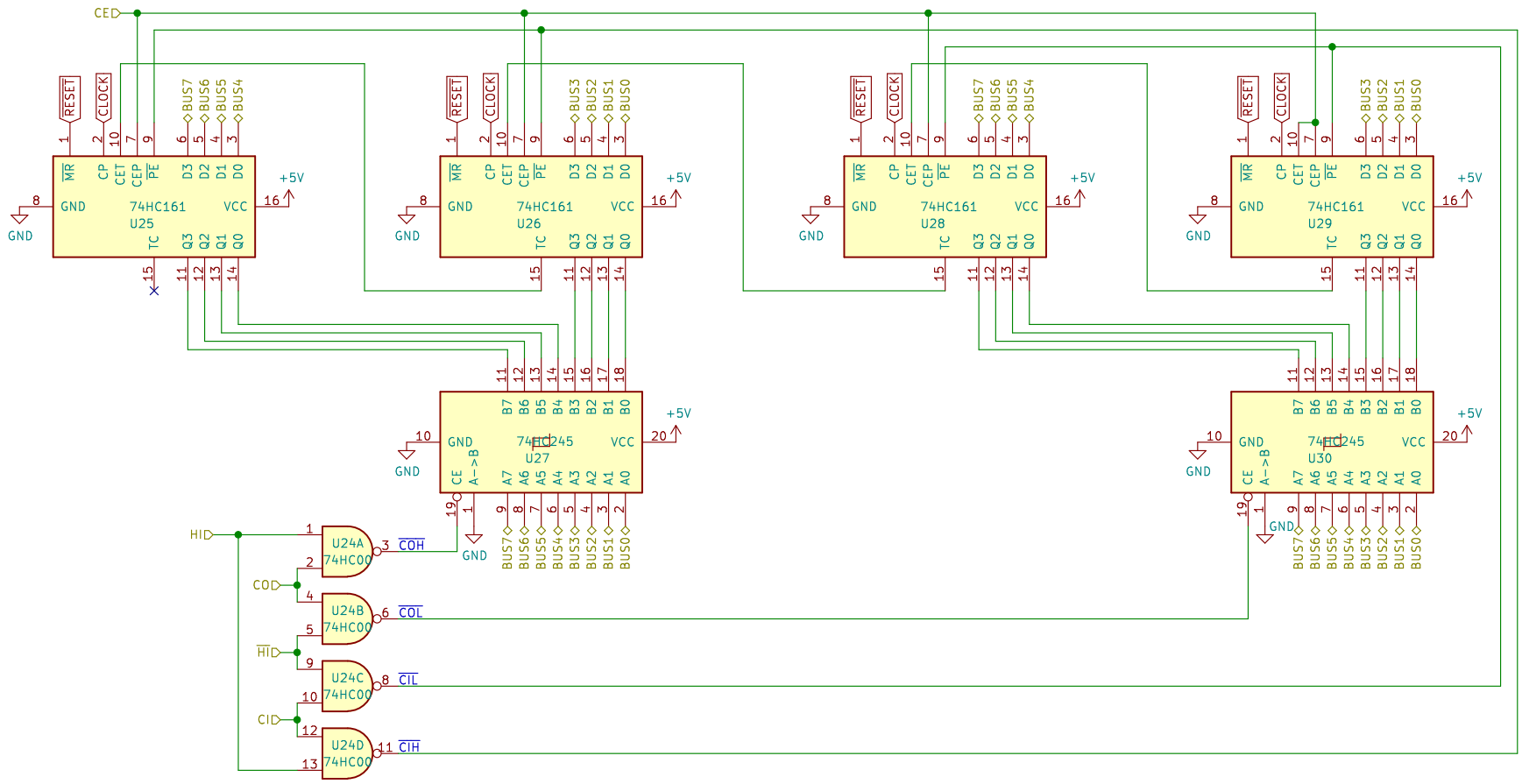
Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/10

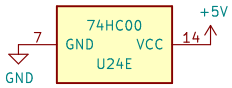


Sheet: /UART Transmitter/
File: UART_TX.sch

Title: UART Transmitter

Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/10





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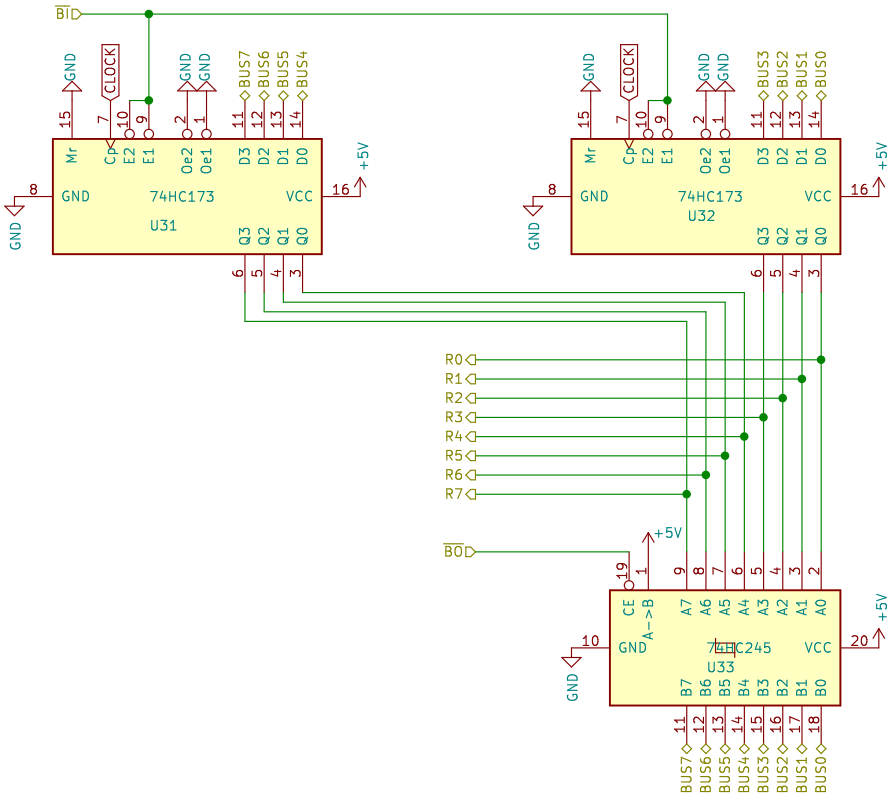
Sheet: /PC/
File: PC.sch

Title: Program Counter

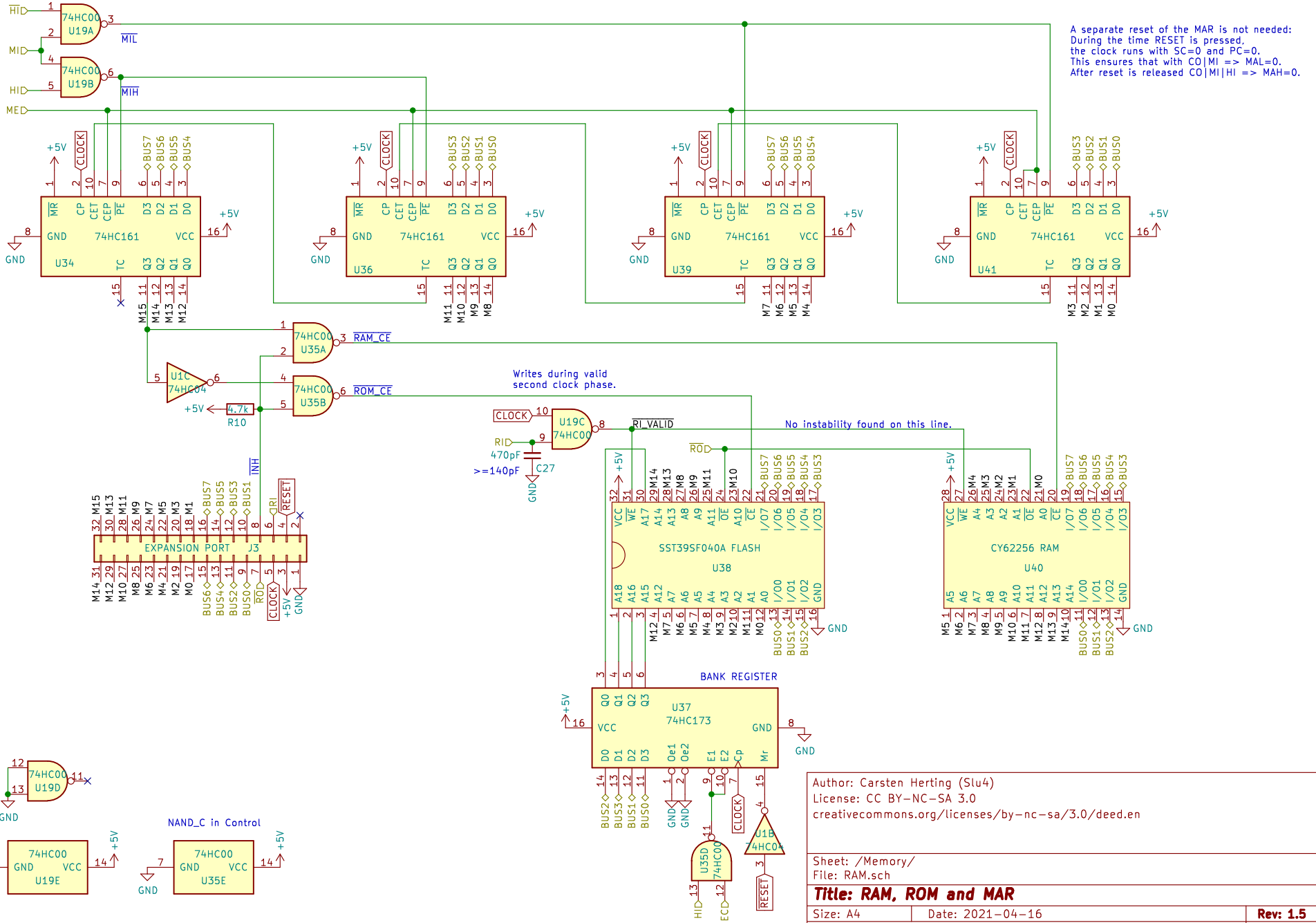
Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 6/10



Sheet: /Reg B/
File: RegB.sch

Title: B Register

Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 7/10


A separate reset of the MAR is not needed:
During the time RESET is pressed,
the clock runs with SC=0 and PC=0.
This ensures that with CO|MI => MAL=0.
After reset is released CO|MI|HI => MAH=0.
Writes during valid
second clock phase.
No instability found on this line.
BANK REGISTER
NAND_C in Control
EXPANSION PORT J3
SST39SF040A FLASH
U38
CY62256 RAM
U40
74HC161
74HC00
74HC04
74HC173
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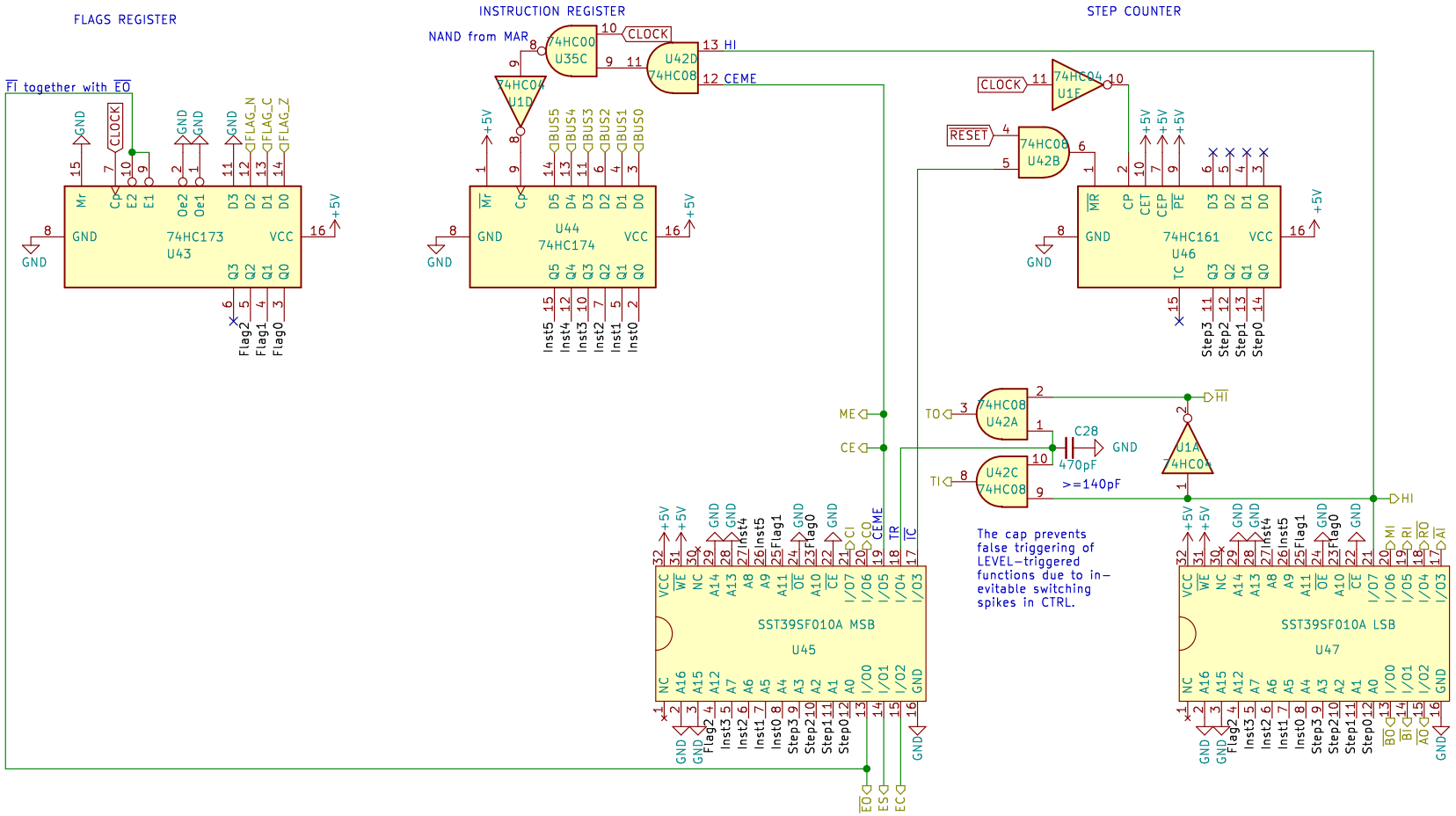
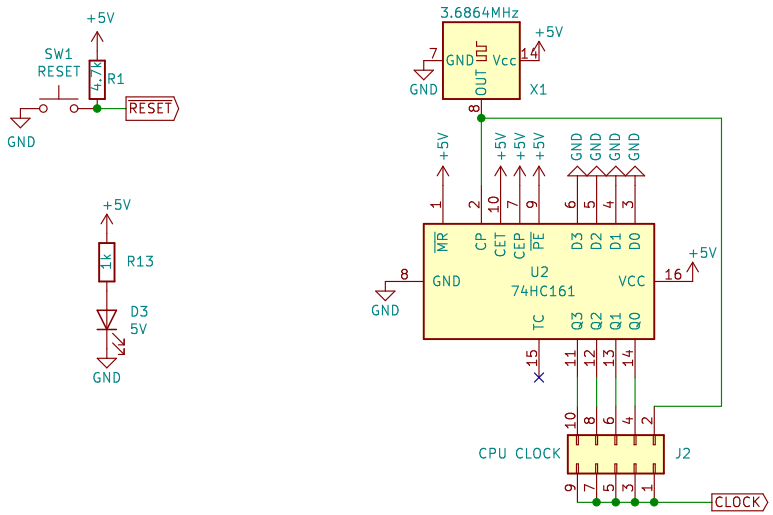
Sheet: /Memory/
File: RAM.sch
Title: RAM, ROM and MAR
Size: A4
Date: 2021-04-16
Rev: 1.5
KiCad E.D.A. kicad (5.1.5)-3
Id: 8/10



Sheet: /Control Logic/
File: IR.sch

Title: Control Logic

Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/10



Sheet: /Clock and Reset/
File: ClockAndReset.sch

Title: Clock and Reset

Size: A4	Date: 2021-04-16	**Rev: 1.5**
KiCad E.D.A. kicad (5.1.5)-3		Id: 10/10