ERIES HD46505 (CRTC)
IT CONTROLLER
CHI

● FEATURES

The HD46505 (CRTC) is a peripheral chip of HMCS6800 Microcomputer LSI families. It is designed in order to provide a simple and effective means of interfacing the raster scan CRT display to MPU bus. Its primary function is to generate the proper refresh address and video timings according to display format.

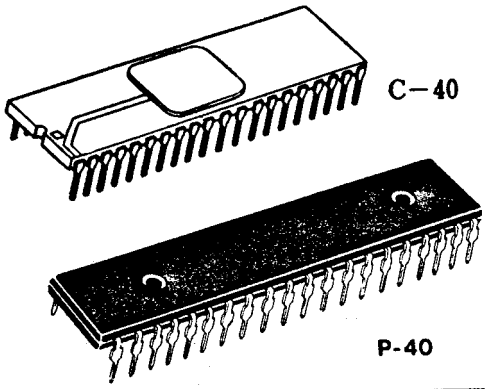
HD46505 is applicable to wide range of raster scan displays.

It is optimized for hardware/software balance in order to achieve integration of complex CRT interface functions and to maintain flexibility.

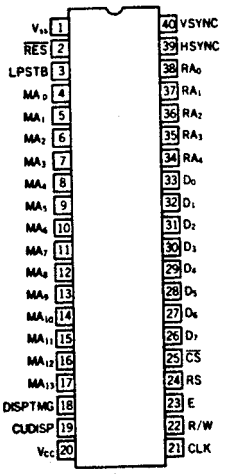
Applications include intelligent CRT terminals, information display systems and video games.

- Programmable Screen and Character Format.
- Line Buffer-less Refreshing
- 14 Bits Refresh Memory Address
- Programmable Interface or Non-Interface Scan
- Cursor Control Function
- Programmable Cursor Format and its Blink
- Light Pen Detection Function
- Limited or Full Graphic Display Capability
- Character by Character Video Control (Color, Blink, Inverse, etc.)
- Hardware Scrolling and Paging Functions
- No DMA Required, Refresh Memory is Time-multiplexed Between CRTC and MPU
- Directly Interfaceable to MPU Bus
- Single +5V Power Supply
- Directly TTL Compatible—All Inputs and Outputs
- N Channel E/D MOS Technology
- 40 Pin DIL Package

● PACKAGE

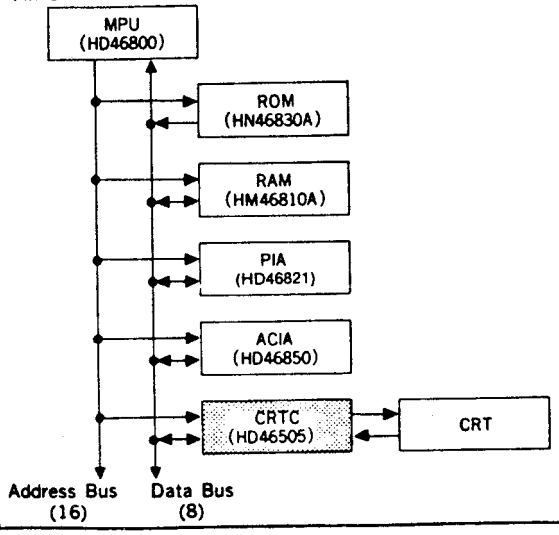


● PIN ARRANGEMENT

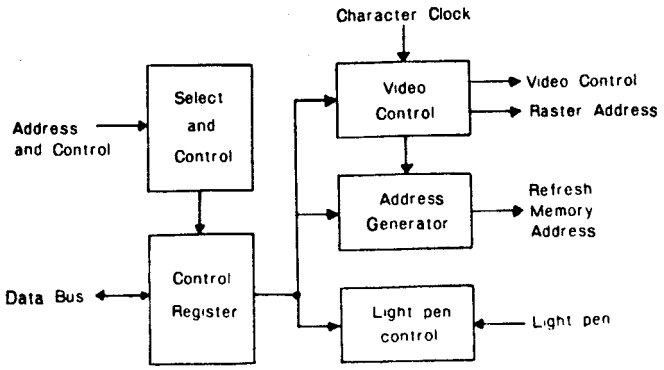


● BLOCK DIAGRAM

HMCS 6800 SYSTEM BLOCK DIAGRAM



CRTC (HD46505) BLOCK DIAGRAM



HD46505R(CRTC) is an exclusive LSI controller to interface the microcomputer HD46800D and CRT display of raster scan type.

HD46505R(CRTC) is one of HMC6800 LSI family and has a perfect compatibility about the data line and control line with MPU (HD46800D).

The main function of CRTC is to generate necesary timing signals for a CRT dispaly of raster scan type according to the specification programmed by MPU. Therefore CRTC is applicable to very wide CRT displays such as a small size and low level character display, a large size and high level limited graphic display and raster type full graphic display by the designed feature, that is, programmable controller.

• FUNCTIONS OF HD46505R (CRTC)

Item		Function of HD46505R (CRTC)	Remark
Function of CRTC	Programmable structure of a picture	Horizontal scanning interval	Programmable by one character interval unit
		Vertical scanning interval (Row unit)	Programmable by one row interval unit.
		Vertical scanning interval (Fine control)	Programmable by one raster unit.
		Displayed character number of one row	
		Displayed character number of one picture	
		Raster number of one row	Vertical dot number of one character + row space
		Horizontal displayed position on CRT	Possible by programming the output timing of synchronous signals.
		Vertical displayed position on CRT	
		Pulse width of the horizontal synchronous signal	
	Programmable Cursor Display	Displayed position of cursor on a picture	Internal cursor register of 14 bit.
		Cursor format	
		Cursor blink and its cycle	Blink cycle is selectable one of 16 or 32 frame cycle.
	Scan mode	Non interlace mode	Selectable one of these three modes.
		Interlace sink mode	
		Interlace sink and video mode	
	Light Pen	Internal light pen register of 14 bit	
	Addressing of refresh memory	Put out the refresh memory address of 14 bit	Accessable refresh memory of 16K words max.
	Programmable start address	Internal start address register of 14 bit (Able to determine the display start address on the refresh memory by program.)	Operations such as paging, scrolling etc. are usable.
LSI Structure of CRTC	Power supply	Single +5V	
	Bus function	Directly connectable with HMCS6800 HMCS6800 family.	
	Process	N channel Si gate E/D MOS	
	Operation	Perfect static circuit	
	Package	40 pin Dual In Line type	
CRTC Expandability		Character display	Alpha numeric character and other character
		Limited (simple type) graphic display	Graphic display (Raster scan type)
		Full graphic display	
		Color display, Blink of displayed character	
		Cluster control	

• FUNCTIONS OF SIGNAL LINE

Internal signals of HD46505R (CRTC) are composed of 13 interface signals with MPU and 25 interface signals with CRT display.

- **INTERFACE SIGNAL WITH MPU**
  Bidirectional Data Bus (D_0 ~ D_7)
  Bidirectional data bus (D_0 ~ D_7) are used for the data transfer between CRTC and MPU. Data bus output is a three state buffer and is in high impedance state except that MPU reads the data of CRTC.

- **READ/WRITE (R/W)**
  Read/Write Signal (R/W) controls the direction of data transfer between MPU and CRTC, that is, the data of CRTC is transferred to MPU while R/W is in "High" level and the data of MPU is transferred to CRTC while R/W is in "Low" level.

- **CHIP SELECT ($\overline{CS}$)**
  Chip select signal ($\overline{CS}$) is a signal to address CRTC chip and MPU can execute the operation of read/write to the internal registers of CRTC only when $\overline{CS}$ is in "Low" level. Normally this signal is obtained by decoding the address signals of MPU under the condition that VMA signal of MPU is in "High" level.

- **REGISTER SELECT (RS)**
  Register select signal (RS) is used for separating internal registers into one address register and 18 control registers, that is, the address register is selected while RS is in "Low" level and control register are selected while RS is in "High" level.
  Normally the LSB of MPU's address bus (A_0) is used for this signal.

- **ENABLE (E)**
  Enable signal (E) is used for a strobe signal when MPU read or writes internal registers of CRTC. Normally ϕ_2 clock of MPU is used for this signal.

- **Reset ($\overline{RES}$)**
  Reset signal ($\overline{RES}$) is an input signal to reset CRTC externally. Internal states of CRTC become as follows when $\overline{RES}$ becomes "Low" level.
  1) Internal counters of CRTC are all cleared and stopped their operations.
  2) All output signals of CRTC become "Low" level.
  3) Internal address register and control registers of CRTC keep former states regardless of $\overline{RES}$.

  This signal has difference functions from that of HMCS6800 family LSIs and its remarks are as follows.
  1) $\overline{RES}$ signal is usable as reset signal only when LPSTB signal is in "Low" level.
  2) Output signals of MA_0 ~ MA_{13}, RA_0 ~ RA_4 become "Low" level synchronizing with the "Low" level of CLK signal after $\overline{RES}$ becomes a "Low" level.

  (CLK signal is necessary at least one cycle in order to make those output signals "Low" level.)
  3) CRTC starts display operation immediately after $\overline{RES}$ becomes from "Low" level to "High" level and reset is canceled.

■ INTERFACE SIGNAL WITH CRT DISPLAY EQUIPMENT

- **CHARACTER CLOCK (CLK)**
  Character clock signal (CLK) is used for a standard clock of CRTC's internal operation. This signal is given by the external high speed dot timing logic.

- **HORIZONTAL SYNCHRONIZATION (HSYNC)**
  Horizontal synchronization signal (HSYNC) is used as a driving signal of horizontal deflection circuit of CRT display equipment.
  Pulse width of vertical synchronization signal is fixed to 16 rasters cycle.

- **DISPLAY TIMING (DISPTMG)**
  This signal is a signal which shows picture display interval of horizontal and vertical deflection. Video signal has to be sent to CRT display equipment only while this signal is in "High" level.

- **REFRESH MEMORY ADDRESS (MA_0 ~ MA_{13})**
  Refresh memory address (MA_0 ~ MA_{13}) is used for memory address to refresh the displayed picture on CRT display equipment at a constant cycle. Address of 16K words (0 ~ 16383) max. can be designated by this address signal. Therefore paging to 8 pages is possible, for instance, in case of the display equipment of 2000 characters.

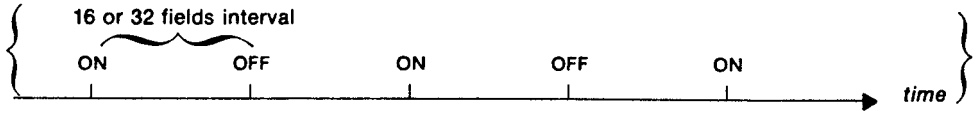
- **RASTER ADDRESS (RA_0 ~ RA_4)**
  Raster address (RA_0 ~ RA_4) is used for a raster select signal of character generator and pattern generator.

- **CURSOR DISPLAY (CUDISP)**
  Cursor display signal (CUDISP) is a video signal to display the cursor on CRT display equipment. This signal is inhibited while DISPTMG is in "Low" level. Normally this signal is mixed with character video signal and sent to CRT display equipment.
- **LIGHT PEN STROBE (LPSTB)**
  Light pen strobe signal (LPSTB) is the detected pulse of character from the light pen. The content of refresh memory address ($MA_0 \sim MA_{13}$) shown in Fig. 5 is set in the light pen register of 14 bit when this signal is put in. Memory address being set should be compensated by software for a delay time between display equipment and light pen and its control circuit.

Internal Registers of HD46505R (CRTC)

$\overline{CS}$	RS	Address Reg. 4 3 2 1 0	Register No.	Register Name	Program Unit	READ	WRITE	Data Bit 7	6	5	4	3	2	1	0	Notes
1	X	X X X X X		Invalid	—	—	—	\	\	\	\	\	\	\	\	
0	0	X X X X X	AR	Address Req.	—	X		\	\	\						
0	1	0 0 0 0 0	R0	Horizontal total character number	Character	X	O									1, 7
0	1	0 0 0 0 1	R1	Horizontal displayed character number	ditto	X	O									
0	1	0 0 0 1 0	R2	Position of horizontal sync. pulse	ditto	X	O									7
0	1	0 0 0 1 1	R3	Pulse width of horizontal sync. pulse	ditto	X	O	\	\	\	\					
0	1	0 0 1 0 0	R4	Vertical total character number	Line	X	O	\								7
0	1	0 0 1 0 1	R5	Total raster adjust	Raster	X	O	\	\	\						
0	1	0 0 1 1 0	R6	Vertical displayed character number	Line	X	O	\								2
0	1	0 0 1 1 1	R7	Position of vertical sync. pulse	ditto	X	O	\								7
0	1	0 1 0 0 0	R8	Interlaced mode	—	X	O	\	\	\	\	\	\	V	S	3
0	1	0 1 0 0 1	R9	Maximum raster raster	Raster	X	O	\	\	\						4, 7
0	1	0 1 0 1 0	R10	Cursor start raster	ditto	X	O	\	B	P						5, 6
0	1	0 1 0 1 1	R11	Cursor end raster	ditto	X	O	\	\	\						6
0	1	0 1 1 0 0	R12	Start address (H)	—	X	O	\	\							
0	1	0 1 1 0 1	R13	Start address (L)	—	X	O									
0	1	0 1 1 1 0	R14	Cursor (H)	—	O	O	\	\							
0	1	0 1 1 1 1	R15	Cursor (L)	—	O	O									
0	1	1 0 0 0 0	R16	Light Pen (H)	—	O	X	\	\							
0		1 0 0 0 1	R17	Light Pen (L)	—	O	X									

Notes:
1. Set data should be odd in case of interlaced mode (R8 = 1 or 3).
2. Set data should be N/2 (N is a real displayed row number) when R8 = 3.
3. V designates video mode when S = 1. S designates interlaced mode.
4. Set data should be odd in case of R8 = 3.
5. B designates cursor blink and P designates blink cycle.



6. Combination of start raster and end raster should be (odd-odd) or (even-even) when R8 = 3.
7. (Set data) = (Designated data) − 1.

*: 0 ..... "Low" level, 1 ..... "High" level

• **INTERLACE MODE**

V	S	Mode
0	0	Non interlace mode
1	0	
0	1	Interlace sink mode
1	1	Interlace sink and video mode

• **CURSOR DISPLAY**

B	P	Cursor Display Mode
0	0	Cursor doesn't blink.
0	1	Cursor isn't displayed.
1	0	Cursor blinks by the cycle of 16 fields interval.
1	1	Cursor blinks by the cycle of 32 fields interval.

• **RESTRICTIONS ON PROGRAMMING OF HD46505R (CRTC)**

1) $0 < Nhd < Nht + 1 \leqslant 256$
2) Nht: Odd number (When interlace sink or interlace sink and video mode)
3) $0 < Nvd < Nvt + 1 \leqslant 128$
4) $Nhsp + Nhsw < Nht + 1$
5) $Nvsp \leqslant Nvt$
6) $0 \leqslant N_{CSTART} \leqslant N_{CEND} \leqslant Nr$
7) One of next two cases should be selected in case of interlace sink and video mode
   i. N_{CSTART}, N_{CEND} are both even.
   ii. N_{CSTART}, N_{CEND} are both odd.

Meanings of symbols mentioned above.

Set data of Register

Nht	:	(Horizontal total character number)-1
Nhd	:	Horizontal displayed character number
Nvt	:	(Vertical total character number)-1
Nvd	:	Vertical displayed character number
Nhsp	:	(Position of horizontal sync.)-1
Nvsp	:	(Position of vertical sync.)-1
Nr	:	Maximum raster address
N_{CSTART}	:	Cursor start raster address
N_{CEND}	:	Cursor end raster address

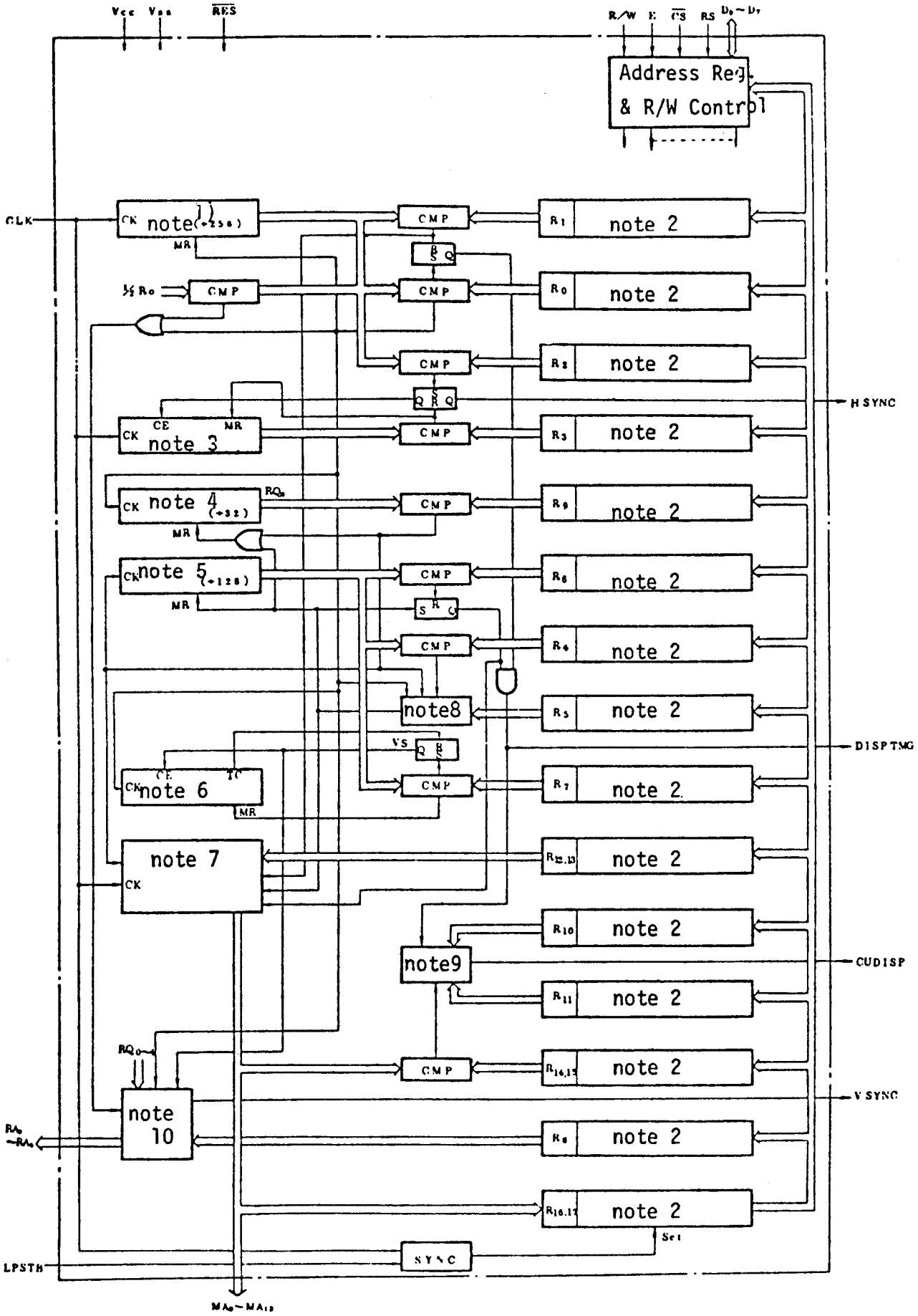


FIGURE 1. INTERNAL BLOCK DIAGRAM OF HD46505R (CRTC)

Notes: 1. Character Counter
2. Register names are as follows:

Register Number	Register Name
R0	Horizontal Total Character Number Reg.
R1	Horizontal Displayed Character Number Reg.
R2	Horizontal Synchronizing Position Reg.
R3	H. Synchronous Pulse Width Reg.
R4	Vertical Total Character Number Reg.
R5	Total Raster Adjust Reg.
R6	Vertical Displayed Character Number Reg.
R7	V. Synchronous Position Reg.
R8	Interlace Mode Reg.
R9	Maximum Raster Address Reg.
R10	Cursor Start Raster Reg.
R11	Cursor End Raster Reg.
R12	Start Address (H) Reg.
R13	Start Address (L) Reg.
R14	Cursor (H) Reg.
R15	Cursor (L) Reg.
R16	Light Pen (H) Reg.
R17	Light Pen (L) Reg.

3. H. Synchronous Pulse Width Counter
4. Raster Counter
5. Line Counter
6. V. Synchronous Pulse Width Counter
7. Linear Address Generator
8. V. total Controller
9. Cursor Controller
10. Interlace Controller

■ MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 ~ 7.0	V
Input Voltage*	V_{IN}	-0.3 ~ 7.0	V
Operating Temperature	T_{opr}	-20 ~ 75	°C
Storage Temperature	T_{stg}	-55 ~ 150	°C

*In respect to *Vss (GND).*

NOTE)
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.75	5	5.25	V
Input Voltage*	V_{IL} V_{IH}	-0.3 2.0	— —	0.8 V_{CC}	V V
Operating Temperature	T_{opr}	-20	25	75	°C

*In respect to *Vss (GND).*

• ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = -20 ~ 75°C)

Item		Symbol	Test Condition	min.	typ.*	max.	Unit
Input "High" Level Voltage	All Inputs	V_{IH}		2.0	—	V_{CC}	V
Input "Low" Level Voltage	All Inputs	V_{IL}		-0.3	—	0.8	V
Input Leak Current	Inputs without D_0 ~ D_7	I_{IN}	V_{IN} = 0 ~ 5.25V	—	1.0	2.5	μA
Input Current at Three state (OFF)	D_0 ~ D_7	I_{TSI}	V_{IN} = 0.4 ~ 2.4V	—	2.0	10	μA
Output "High" Level Voltage	D_0 ~ D_7	V_{OH}	I_{LOAD} = -205μA	2.4	—	—	V
	Other outputs		I_{LOAD} = -100μA				
Output "Low" Level Voltage	All Outputs	V_{OL}	I_{LOAD} = 1.6mA	—	—	0.4	V
Input Capacitance	D_0 ~ D_7	C_{IN}	V_{IN} = 0V, T_a = 25°C, f = 1MHz	—	—	12.5	pF
	Other Inputs			—	—	10.0	pF
Output Capacitance		C_{out}	V_{IN} = 0V, T_a = 25°C, f = 1MHz	—	—	10.0	pF
Power Dissipation		P_D		—	600	1000	mW

*Value at T_a = 25°C, V_{CC} = 5V.

• TIMING CHARACTERISTICS

Control Signal Timing of CRTC

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Clock Frequency		f_c	Fig. 4	—	—	3.0	MHz
Clock Pulse Width	"Low" Level	PW_{CL}	Fig. 4	150	—	—	ns
	"High" Level	PW_{CH}	Fig. 4	150	—	—	ns
Rise/Fall Time of Clock Input		t_{cr} t_{cf}	Fig. 4	—	—	15	ns
Memory-Address Delay Time		t_{MAD}	Fig. 4	—	—	160	ns
Raster-Address Delay Time		t_{RAD}	Fig. 4	—	—	160	ns
Display-Timing Delay Time		t_{DTD}	Fig. 4	—	—	250	ns
H. Sync. Delay Time		t_{HSD}	Fig. 4	—	—	250	ns
V. Sync. Delay Time		t_{VSD}	Fig. 4	—	—	250	ns
Cursor Display Delay Time		t_{CDD}	Fig. 4	—	—	250	ns
Pulse Width of Light Pen Strobe		PW_{LPH}	Fig. 4	80	—	—	ns
Uncertain Time of Light Pen Strobe Receiving		t_{LPD1}	Fig. 5	—	—	80	ns
		t_{LPD2}	Fig. 5	—	—	10	ns

• BUS TIMING CHARACTERISTICS

• READ SEQUENCE

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Enable Cycle Time		t_{CYCE}	Fig. 2	1.0	—	—	μs
Enable Pulse Width	"High" Level	PW_{EH}	Fig. 2	0.45	—	—	μs
	"Low" Level	PW_{EL}	Fig. 2	0.40	—	—	μs
Setup Time of ADDRESS-ENABLE		t_{AS}	Fig. 2	140	—	—	ns
Data Delay Time		t_{DDR}	Fig. 2	—	—	320	ns
Data Hold Time		t_H	Fig. 2	10	—	—	ns
Rise/Fall Time of Enable Input		t_{Er} t_{Ef}	Fig. 2	—	—	25	ns
Address Hold Time		t_{AH}	Fig. 2	10	—	—	ns
Data Access Time		t_{ACC}	Fig. 2	—	—	460	ns

• WRITE SEQUENCE

Item		Symbol	Test Condition	min.	typ.	max.	Unit
Enable Cycle Time		t_{CYCE}	Fig. 3	1.0	—	—	μs
Enable Pulse Width	"High" Level	PW_{EH}	Fig. 3	0.45	—	—	μs
	"Low" Level	PW_{EL}	Fig. 3	0.40	—	—	μs
Setup Time of ADDRESS-ENABLE		t_{AS}	Fig. 3	140	—	—	ns
Data Setup Time		t_{DSW}	Fig. 3	195	—	—	ns
Data Hold Time		t_H	Fig. 3	10	—	—	ns
Rise/Fall Time of Enable Input		t_{Er} t_{Ef}	Fig. 3	—	—	25	ns
Address Hold Time		t_{AH}	Fig. 3	10	—	—	ns

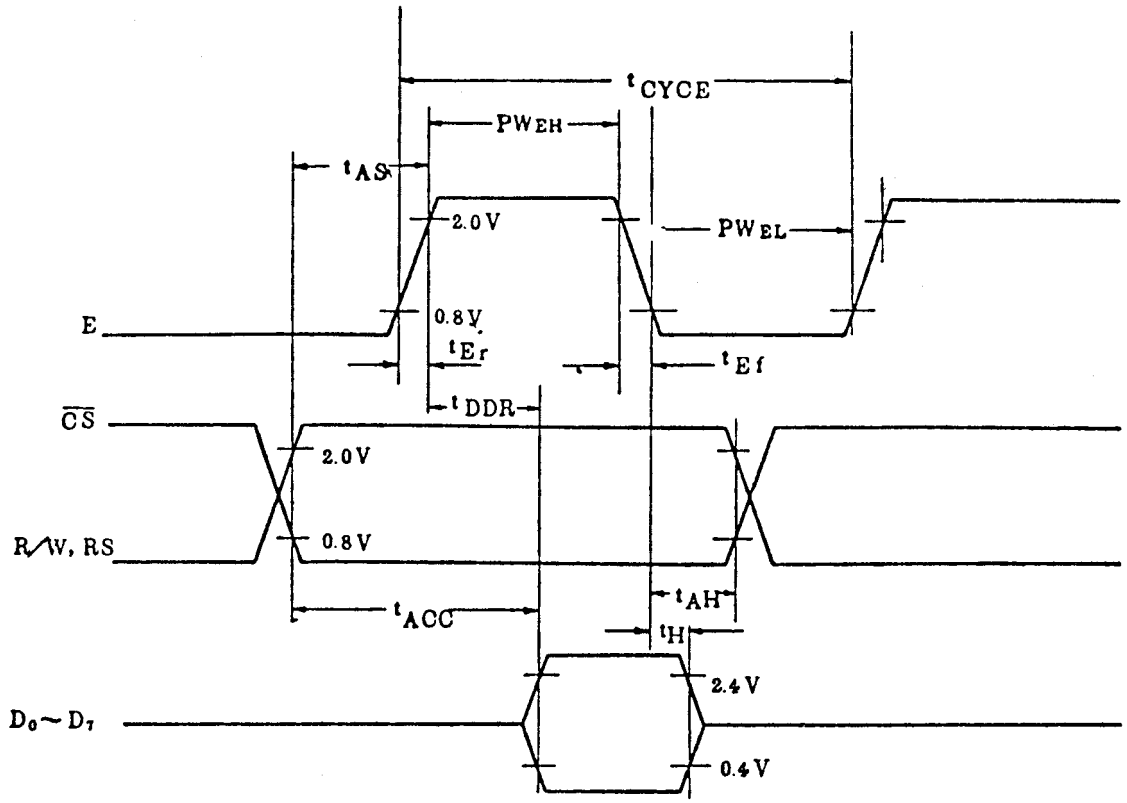


FIGURE 2. READ SEQUENCE

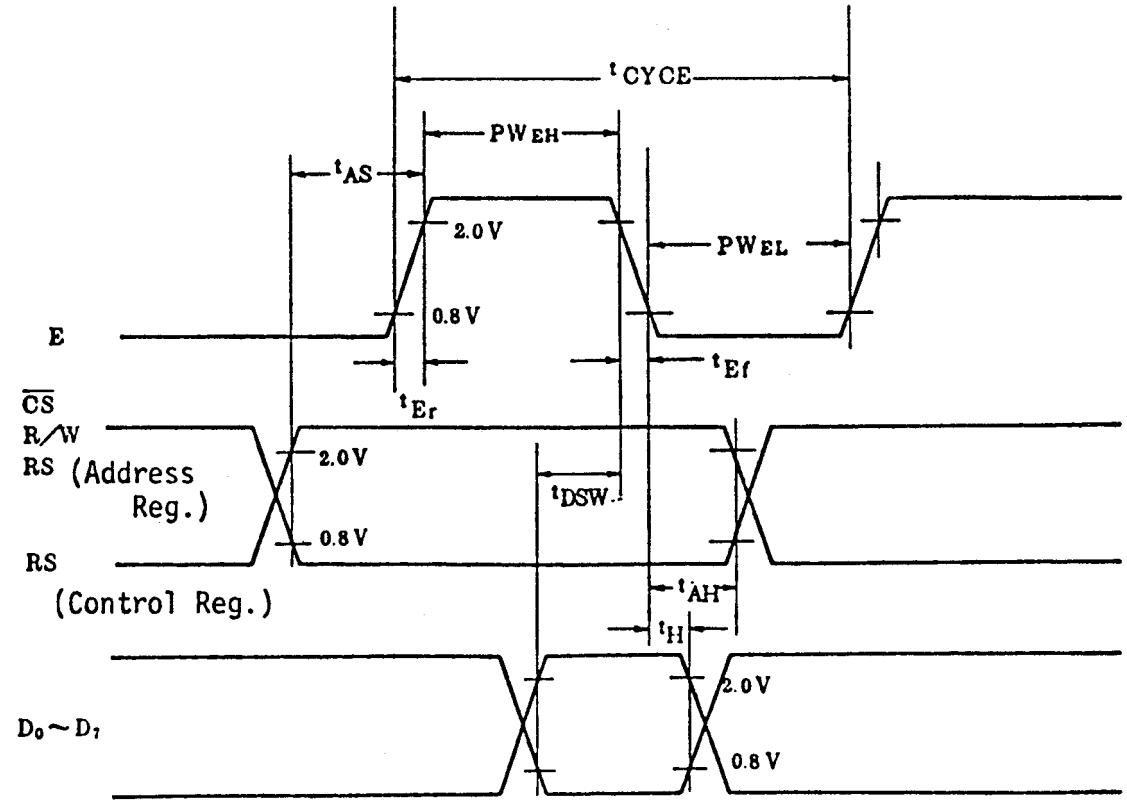
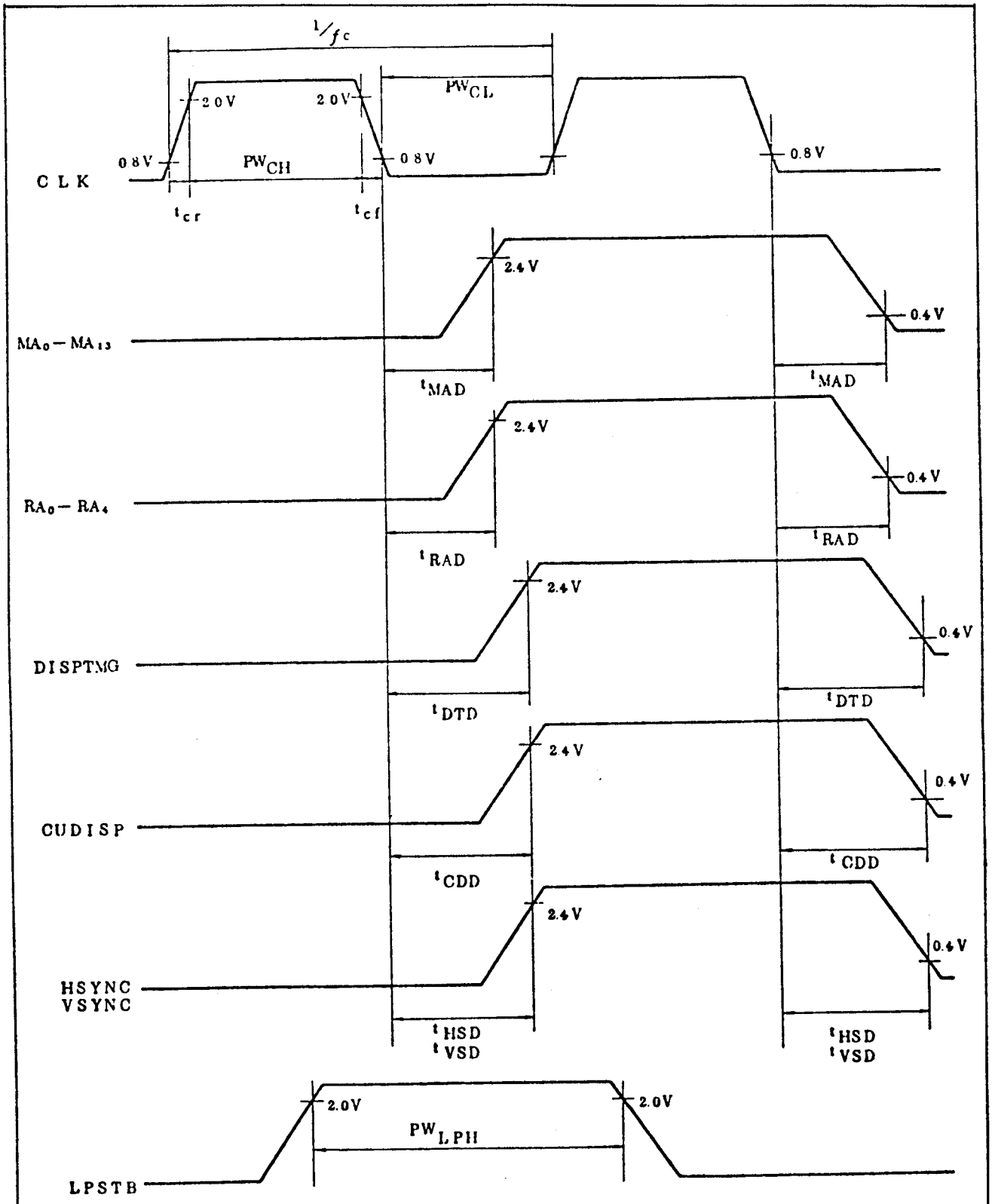


FIGURE 3. WRITE SEQUENCE



This figure shows the timing relationship of CLK signal and output signals.

FIGURE 4. CRTC TIME CHART

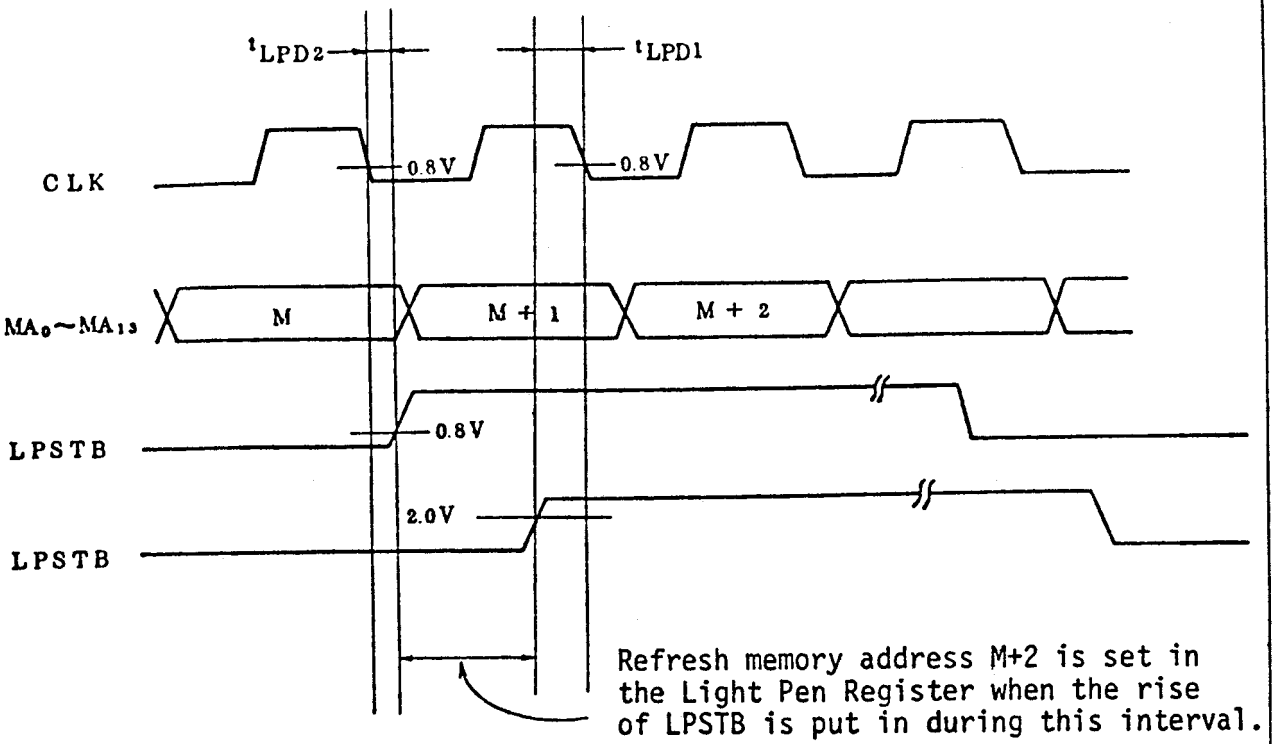


FIGURE 5. INPUT TIMING OF LPSTB AND SET MEMORY ADDRESS

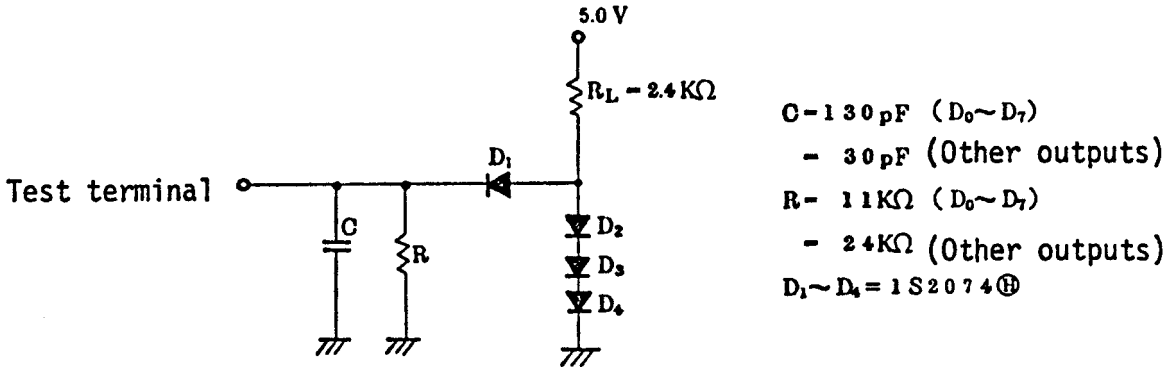


FIGURE 6. LOAD CIRCUIT

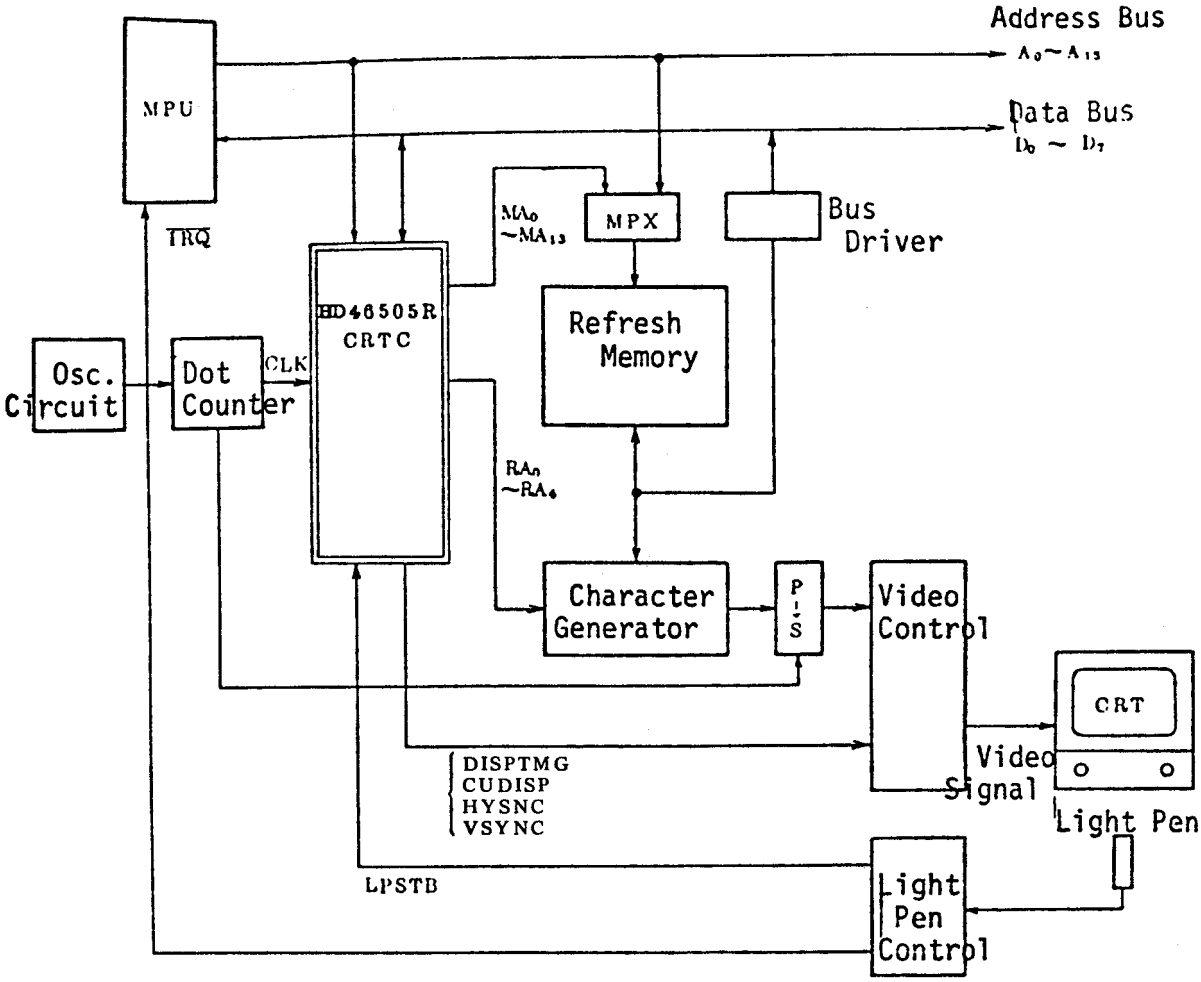


FIGURE 7. CHARACTER DISPLAY SYSTEM EXAMPLE USING HD46505R (CRTC)