NC State University

Department of Electrical and Computer Engineering

ECE 463/563: Fall 2021 (Rotenberg)

Project #3: Dynamic Instruction Scheduling

by

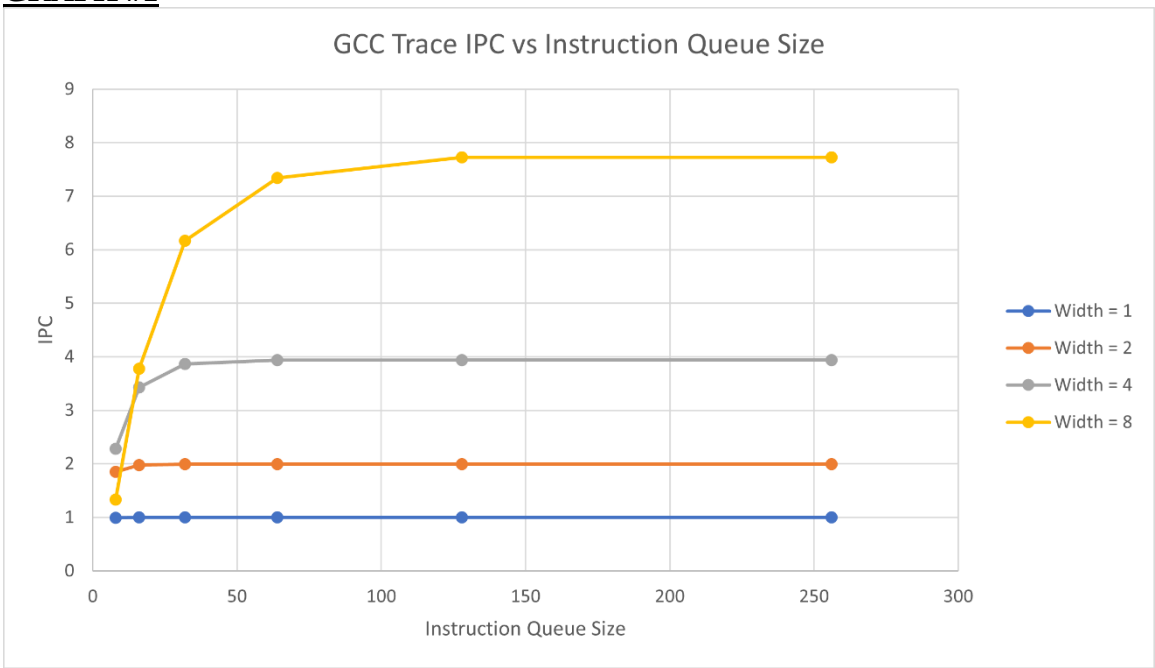
Cristian Hellmer

NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this project."

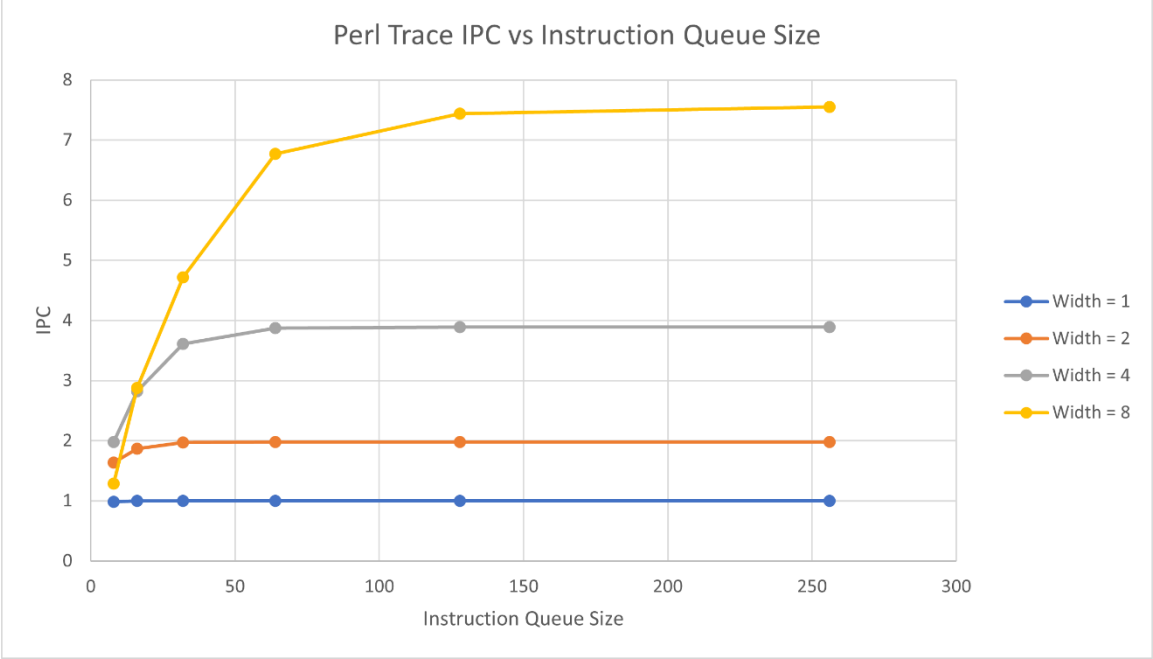
Student's electronic signature: _____Cristian Hellmer_____
(sign by typing your name)

Course number: _____ECE 563_____

GRAPH #1



GRAPH #2



	Optimized IQ_SIZE per WIDTH	
	Benchmark 1 (gcc)	**Benchmark 2 (perl)**
WIDTH = 1	8	8
WIDTH = 2	16	32
WIDTH = 4	32	64
WIDTH = 8	64	128

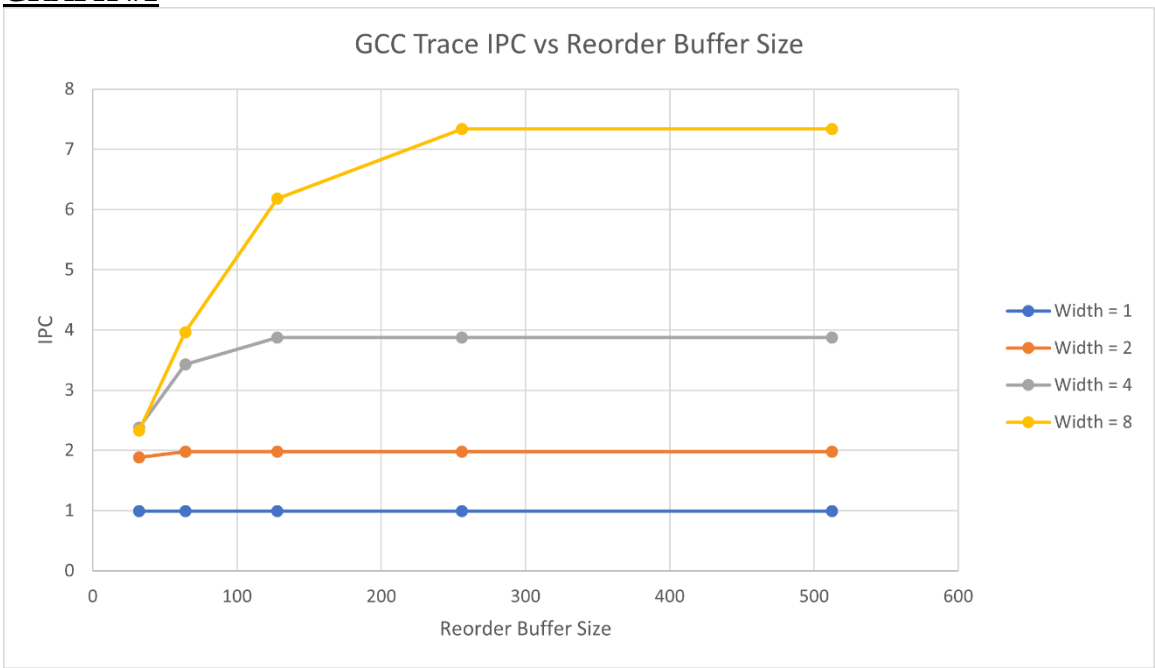
1. **The goal of a superscalar processor is to achieve an IPC that is close to WIDTH. As we increase WIDTH, what trend do you notice regarding the IQ_SIZE needed to achieve this goal? Why is there this trend?**

As we increase the WIDTH, the IQ_SIZE needs to increase as well to achieve close to ideal performance. This is because the larger number of instructions which are taken into the pipeline each cycle requires more space in the instruction queue to optimally store all the instructions necessary to avoid pipeline stalls due to no instruction queue space.

2. **Do some benchmarks show higher or lower IPC than other benchmarks, for the same microarchitecture configuration? Why might this be the case?**

Benchmark 2 (perl) has a lower IPC for each microarchitecture configuration in comparison to benchmark 1 (gcc). This could be because benchmark 2 has more true dependencies. True dependencies have the potential to cause pipeline stalls due to full hardware components as some instructions wait for other instructions to complete. This could also be because benchmark 2 has more instructions which take more cycles to complete. Since each instruction can take 1, 2, or 5 cycles to complete, there could be a wide range of cycles needed to finish any given benchmark based on the opcodes.

GRAPH #1



GRAPH #2