**vlsimaster@JAI-SHRI-RAM:~$** cd PI\_RISCV\_Chip\_Tapeout\_2025/

**vlsimaster@JAI-SHRI-RAM:~/PI\_RISCV\_Chip\_Tapeout\_2025$** ls

Week0 Week1

**vlsimaster@JAI-SHRI-RAM:~/PI\_RISCV\_Chip\_Tapeout\_2025$** cd Week1

**vlsimaster@JAI-SHRI-RAM:~/PI\_RISCV\_Chip\_Tapeout\_2025/Week1$** ls

good\_mux good\_mux\_synth.v log1.txt sky130\_fd\_sc\_hd\_\_tt\_025C\_1v80.lib tb\_multiple\_modules.v

good\_mux.v good\_mux\_synth\_.v multiple\_modules.v tb\_good\_mux.v

**vlsimaster@JAI-SHRI-RAM:~/PI\_RISCV\_Chip\_Tapeout\_2025/Week1$** iverilog good\_mux.v tb\_good\_mux.v -o good\_mux

**vlsimaster@JAI-SHRI-RAM:~/PI\_RISCV\_Chip\_Tapeout\_2025/Week1$** ./good\_mux

VCD info: dumpfile tb\_good\_mux.vcd opened for output.

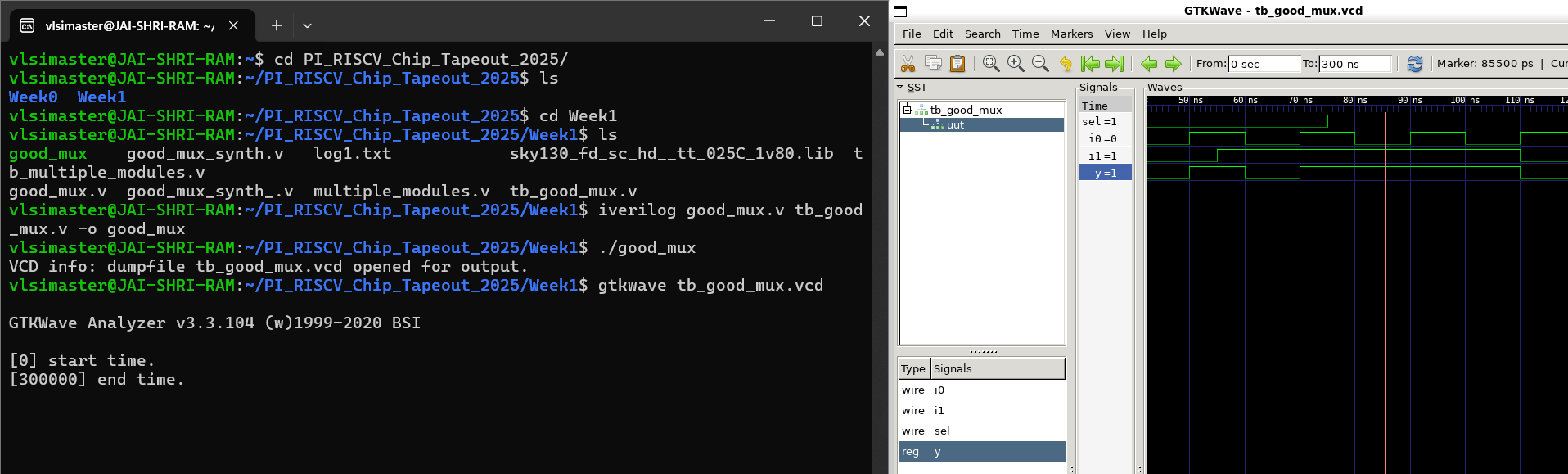
**vlsimaster@JAI-SHRI-RAM:~/PI\_RISCV\_Chip\_Tapeout\_2025/Week1$** gtkwave tb\_good\_mux.vcd

GTKWave Analyzer v3.3.104 (w)1999-2020 BSI

[0] start time.

[300000] end time.

WM Destroy



**vlsimaster@JAI-SHRI-RAM:~/PI\_RISCV\_Chip\_Tapeout\_2025/Week1$ yosys**

/----------------------------------------------------------------------------\

| yosys -- Yosys Open SYnthesis Suite |

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Yosys 0.55+46 (git sha1 5b8b5292e, g++ 11.4.0-1ubuntu1~22.04 -fPIC -O3)

**yosys> read\_liberty -lib sky130\_fd\_sc\_hd\_\_tt\_025C\_1v80.lib**

1. Executing Liberty frontend: sky130\_fd\_sc\_hd\_\_tt\_025C\_1v80.lib

Imported 418 cell types from liberty file.

**yosys> read\_verilog good\_mux.v**

2. Executing Verilog-2005 frontend: good\_mux.v

Parsing Verilog input from `good\_mux.v' to AST representation.

Generating RTLIL representation for module `\good\_mux'.

Successfully finished Verilog frontend.

**yosys> synth -top good\_mux**

3.22.1.1. Executing ABC.

Running ABC command: "<yosys-exe-dir>/yosys-abc" -s -f <abc-temp-dir>/abc.script 2>&1

ABC: ABC command line: "source <abc-temp-dir>/abc.script".

ABC:

ABC: + read\_blif <abc-temp-dir>/input.blif

ABC: + read\_library <abc-temp-dir>/stdcells.genlib

ABC: + strash

ABC: + dretime

ABC: + map

ABC: + write\_blif <abc-temp-dir>/output.blif

3.22.1.2. Re-integrating ABC results.

ABC RESULTS: MUX cells: 1

ABC RESULTS: internal signals: 0

ABC RESULTS: input signals: 3

ABC RESULTS: output signals: 1

Removing temp directory.

3.24. Executing HIERARCHY pass (managing design hierarchy).

Attribute `top' found on module `good\_mux'. Setting top module to good\_mux.

3.24.1. Analyzing design hierarchy..

Top module: \good\_mux

3.24.2. Analyzing design hierarchy..

Top module: \good\_mux

Removed 0 unused modules.

3.25. Printing statistics.

=== good\_mux ===

Number of wires: 4

Number of wire bits: 4

Number of public wires: 4

Number of public wire bits: 4

Number of ports: 4

Number of port bits: 4

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 1

$\_MUX\_ 1

3.26. Executing CHECK pass (checking for obvious problems).

Checking module good\_mux...

Found and reported 0 problems.

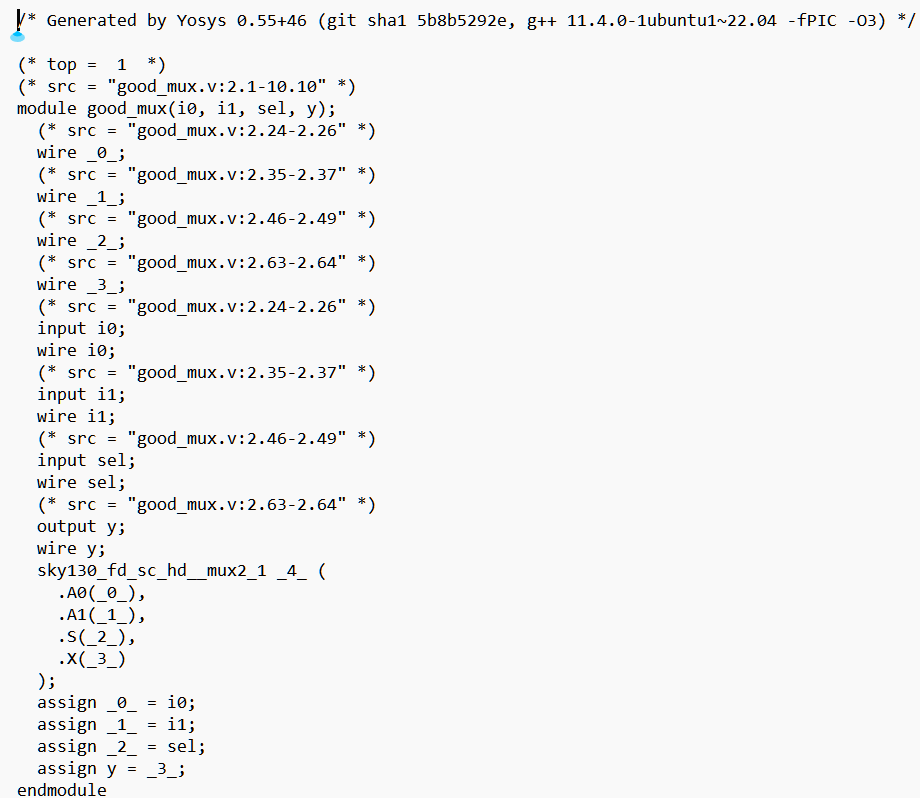
**yosys> abc -liberty sky130\_fd\_sc\_hd\_\_tt\_025C\_1v80.lib**

**yosys> show**

****

**yosys> write\_verilog good\_mux\_synth1.v**

*(without -noattr)*



**yosys> write\_verilog -noattr good\_mux\_synth2.v**

*(with -noattr)*

A screenshot of a computer

AI-generated content may be incorrect.

vlsimaster@JAI-SHRI-RAM:~/PI\_RISCV\_Chip\_Tapeout\_2025/Week1$ yosys

/----------------------------------------------------------------------------\

| yosys -- Yosys Open SYnthesis Suite |

| Copyright (C) 2012 - 2025 Claire Xenia Wolf <claire@yosyshq.com> |

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Yosys 0.55+46 (git sha1 5b8b5292e, g++ 11.4.0-1ubuntu1~22.04 -fPIC -O3)

yosys> read\_liberty -lib sky130\_fd\_sc\_hd\_\_tt\_025C\_1v80.lib

1. Executing Liberty frontend: sky130\_fd\_sc\_hd\_\_tt\_025C\_1v80.lib

Imported 418 cell types from liberty file.

yosys> read\_verilog multiple\_modules.v

2. Executing Verilog-2005 frontend: multiple\_modules.v

Parsing Verilog input from `multiple\_modules.v' to AST representation.

Generating RTLIL representation for module `\sub\_module2'.

Generating RTLIL representation for module `\sub\_module1'.

Generating RTLIL representation for module `\multiple\_modules'.

Successfully finished Verilog frontend.

yosys> synth -top multiple\_modules

3.25. Printing statistics.

=== multiple\_modules ===

Number of wires: 5

Number of wire bits: 5

Number of public wires: 5

Number of public wire bits: 5

Number of ports: 4

Number of port bits: 4

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 2

sub\_module1 1

sub\_module2 1

=== sub\_module1 ===

Number of wires: 3

Number of wire bits: 3

Number of public wires: 3

Number of public wire bits: 3

Number of ports: 3

Number of port bits: 3

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 1

$\_AND\_ 1

=== sub\_module2 ===

Number of wires: 3

Number of wire bits: 3

Number of public wires: 3

Number of public wire bits: 3

Number of ports: 3

Number of port bits: 3

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 1

$\_OR\_ 1

=== design hierarchy ===

multiple\_modules 1

sub\_module1 1

sub\_module2 1

Number of wires: 11

Number of wire bits: 11

Number of public wires: 11

Number of public wire bits: 11

Number of ports: 10

Number of port bits: 10

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 2

$\_AND\_ 1

$\_OR\_ 1

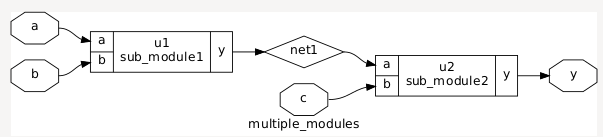
yosys> abc -liberty sky130\_fd\_sc\_hd\_\_tt\_025C\_1v80.lib

yosys> show

5. Generating Graphviz representation of design.

ERROR: For formats different than 'ps' or 'dot' only one module must be selected.

yosys> show multiple\_modules



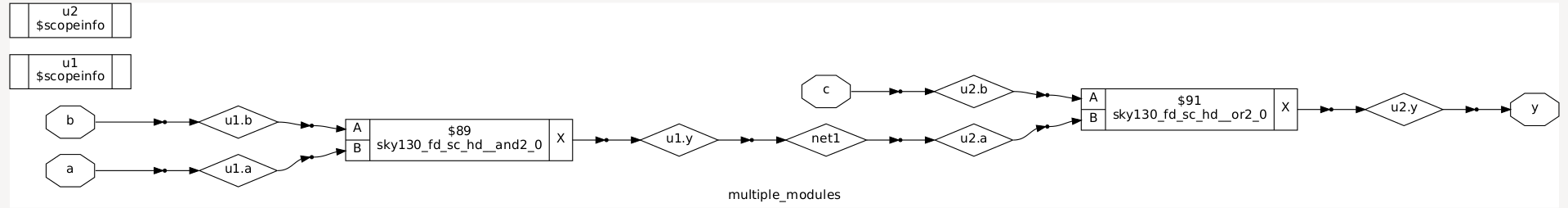
yosys> flatten

7. Executing FLATTEN pass (flatten design).

Deleting now unused module sub\_module1.

Deleting now unused module sub\_module2.

yosys> show multiple\_modules



yosys> synth -top sub\_module2d

yosys> show sub\_module2

