YOUNG Optics

ENGINE SPECIFICATION

Customer Acceptance Specification

To:

Model: FLE2-T

P/N: 95.LE420G004

Approved by

R/D : _____

_____ Sales : _____

(Customer) (Young Optics)

Customer	**Young Optics Inc.** No. 7, Hsin-Ann Rd., Hsinchu Science Park, Hsinchu, Taiwan 30076, R.O.C. Tel: + 886-3-6206789 Fax: + 886-3-6231122	Issued Date:	10/12/2015
		Version:	2.1
Telstar		Page No.:	Page 1, Total 29 pages

REVISION HISTORY

Date	Revision	Changes and Additions	Page	By
02/29/2012	1.0	First Draft	1	Toby/Snake
04/12/2012	1.1	Update Engine Dimension / Package and Handling	14,16-23	Snake/Toby
04/24/2012	1.2	Update brightness & test condition	16	iain
07/06/2012	1.3	Update Thermal shock test & focus force & drawing	16,18,24	iain
07/16/2012	1.4	Add LED characteristics Update Optical Parameter & Image Quality on projected screen	15,17,18	Toby
07/20/2012	1.5	Update Engine Tray Add Engine Label	24,26,27	Snake
12/18/2013	1.6	Update brightness & thermistor & LED FPC Pin Descriptions	14,15,19	Iain/Arthur
05/05/2015	1.7	Update brightness & current & color band spec	19,20	iain
08/04/2015	2.0	Update brightness & current & engine 2d for 95.LE420G004	19-21	iain
10/12/2015	2.1	Add Projection offest	6	Snake

Table of Content

1 STANDARD TEST CONDITIONS

Warm up period	< 1 minute
Ambient Light	Optical data measurement at <=0.01 lux dark room, Image quality checking at <=0.5 lux dark room
Ambient Temperature	25 Celsius degree
Image Size	20” at 974±48mm (From 1st surface of the p-lens to Screen)
Input Signal	640X360 at 60Hz
Instruments	Color & Uniformity: CL-200A / Contrast: T-10

2 CONFIGURATION OF ENGINE

Parts Detail:

(1) Engine unit. (From LED module to projection lens)
(2) LED module: Red/Blue 2 chips in 1 package. Converter Green package (including flex cable)
(3) DMD Chip set
(4) Projection lens
(5) Flash Board

3 KEY PARTS SPECIFICATION

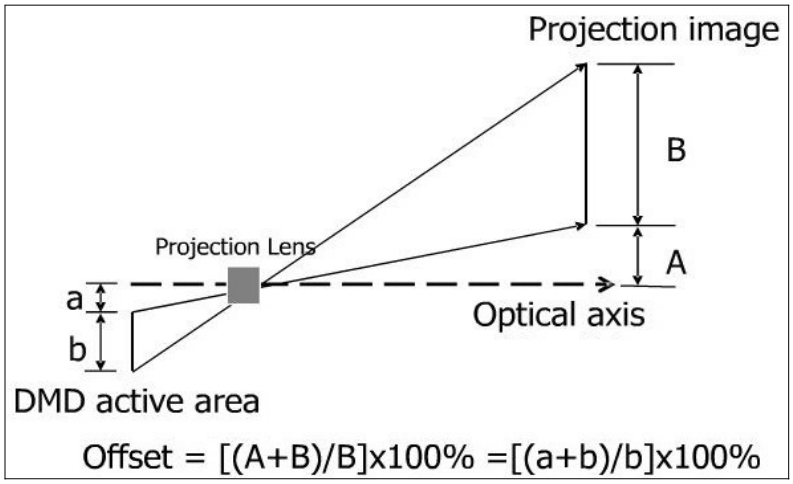
3.1 Panel

Manufacturer:	Texas Instruments
Type:	DLP® 0.2 nHD DMD
Size:	0.22 inches<diagonal>
Active pixels:	640(H) x 360(V) pixels.

3.2 Projection Lens

Engine model	FLE2 DLP OPTICS ENGINE
Lens manufacturer	Young Optics, Inc
Projection distance	974±48mm at 20” Diagonal
Throw ratio	(Projection Distance/Width of Image) 2.2
TV distortion	+/- 1.0 % maximum
Throw Distance	488mm ~ 2922mm
Projection Image Size	10”~60”
Projection offset	104%

Definition of TV-Distortion



Definition of Projection offset

4 *Electrical Portion*

4.1 Flash Board Block Diagram:

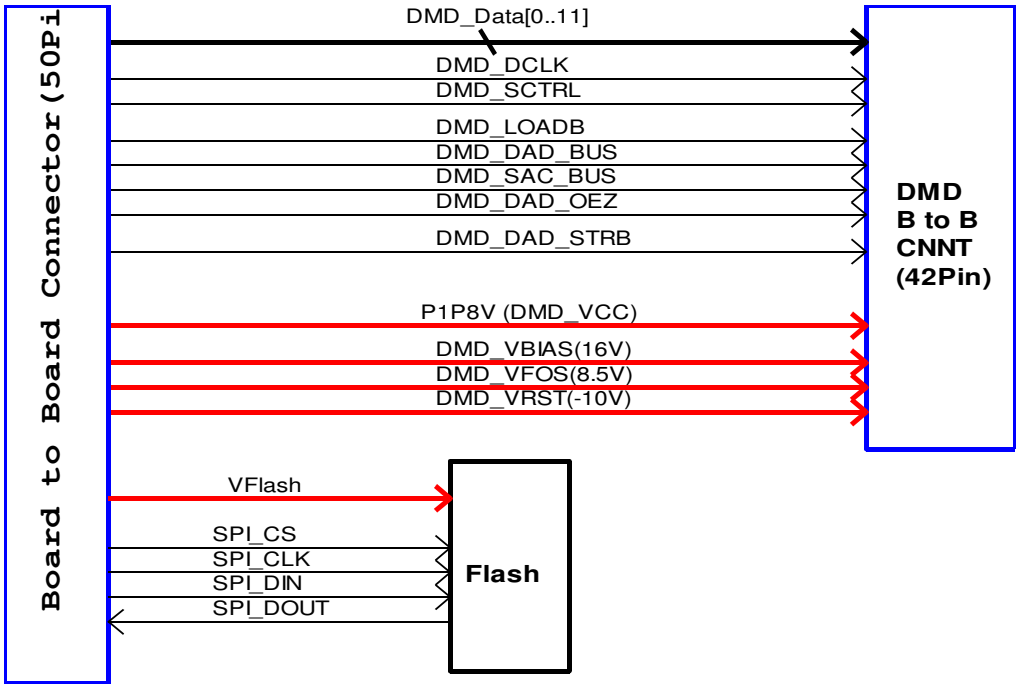


Figure 4.1- Block Diagram

4.2 Flash Board PCB:

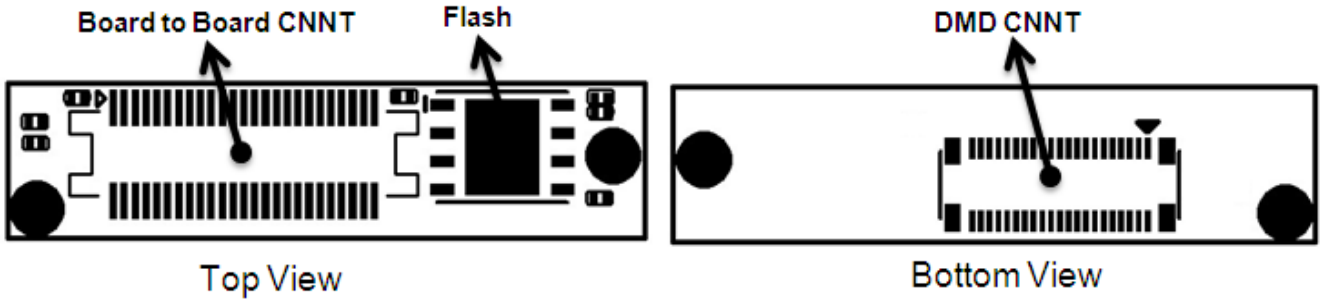


Figure 4.2-Flash Board PCB

4.3 Board to Board Connector and Pin Assignment:

User can connect the flash board via 50pin board to board connector; the connector type is ACES 88389-50. There are DMD power、DMD control and serial flash signals built in board to board connector. The connector pin assignment is shown as table 4.1.

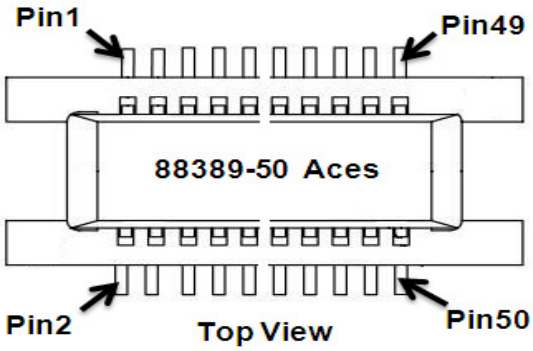


Figure 4.3- Board to Board Connector

Table 4.1- Board to Board Connector Pin Assignment

Pin#	Signal Name	I/O Type	Description
1	DMD_VCC	PWR	DMD VCC (1.8V)
2	DMD_VCC	PWR	DMD VCC (1.8V)
3	DMD_D1	I	DMD Data_1
4	DMD_D9	I	DMD Data_9
5	GND	GND	Ground
6	GND	GND	Ground
7	DMD_D2	I	DMD Data_2
8	DMD_D8	I	DMD Data_8
9	GND	GND	Ground
10	GND	GND	Ground
11	DMD_D3	I	DMD Data_3
12	DMD_D11	I	DMD Data_11
13	DMD_D4	I	DMD Data_4
14	DMD_D10	I	DMD Data_10
15	DMD_D5	I	DMD Data_5
16	GND	GND	Ground
17	GND	GND	Ground
18	DMD_DCLK	I	DMD Data Clock
19	DMD_D7	I	DMD Data_7

20	DMD_LOADB	I	DMD Parallel Latch Load Enable
21	DMD_VCC	PWR	DMD VCC (1.8V)
22	DMD_VCC	PWR	DMD VCC (1.8V)
23	DMD_D6	I	DMD Data_6
24	DMD_SCTRL	I	DMD Serial Control Signal
25	DMD_D0	I	DMD Data_0
26	GND	GND	Ground
27	GND	GND	Ground
28	DMD_BUS	I	DMD Reset Control Serial Bus
29	DMD_STRB	I	DMD Bus Strobe
30	DMD_VOFS	PWR	DMD OFFSET Power (8.5V)
31	DMD_VBIAS	PWR	DMD BIAS Power (16V)
32	DMD_SAC_BUS	I	DMD SAC Bus Data
33	GND	GND	Ground
34	GND	GND	Ground
35	GND	GND	Ground
36	DMD_OEZ	I	DMD Output Enable
37	GND	GND	Ground
38	GND	GND	Ground
39	DMD_VRST	PWR	DMD RESET Power (-10V)
40	N.C	-	Not Connected
41	DMD_VCC	PWR	DMD VCC (1.8V)
42	DMD_VCC	PWR	DMD VCC (1.8V)
43	FLASH_DOUT	O	Serial Flash Data Output
44	FLASH_CLK	I	Serial Flash Clock Input
45	FLASH_CSZ	I	Serial Flash Chip Select Input
46	GND	GND	Ground
47	VFLASH	PWR	Serial Flash Power Supply
48	FLASH_DIN	I	Serial Flash Data Input
49	GND	GND	Ground
50	GND	GND	Ground

I: Input ; O:Output ; PWR:Power ; GND:Ground

4.4 Electrical Characteristics:

4.4.1 Absolute Maximum Ratings:

The flash board absolute maximum ratings are shown as table 4.2.

Table 4.2 Absolute maximum ratings (Note)					
PARAMETER		MIN	NOM	MAX	UNIT
DMD_VCC	LVCMOS Logic power supply voltage	-0.5	-	4	V
DMD_VBIAS	Mirror Electrode Voltage	-0.5	-	17	V
DMD_VRST	Mirror Electrode Voltage	-11	-	0.5	V
DMD_VOFS	Mirror Electrode and HVCMOS voltage	-0.5	-	8.75	V
VFLASH	SPI Flash Power	-0.6	-	4	V

Note:
This flash board has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

4.4.2 Recommended Operating Conditions:

The flash board recommended operating condition is shown as table 4.3

Table 4.3 Recommended Operating Conditions					
PARAMETER		MIN	NOM	MAX	UNIT
DMD_VCC	LVCMOS Logic power supply voltage	1.65	1.8	1.95	V
DMD_VBIAS	Mirror Electrode Voltage	15.5	16	16.5	V
DMD_VRST	Mirror Electrode Voltage	-9.5	-10	-10.5	V
DMD_VOFS	Mirror Electrode and HVCMOS voltage	8.25	8.5	8.75	V
VFLASH	Flash supply voltage	2.3	3.3	3.6	V

4.4.3 Power Dissipation:

Table 4.4-Recommended Operating Conditions						
PARAMETER		Test Condition	MIN	NOM	MAX	UNIT
DMD_VCC	LVCMOS Logic power supply voltage	DMD_VCC=1.8V	-	21	26	mA
DMD_VBIAS	Mirror Electrode Voltage	DMD_VBIAS=16V	-	0.7	1.3	mA
DMD_VRST	Mirror Electrode Voltage	DMD_VRST=-10V	-	0.4	1.2	mA
DMD_VOFS	Mirror Electrode and HVCMOS voltage	DMD_VOFS=8.5V	-	0.7	1.5	mA
VFLASH	SPI Flash Power	VFLASH=3.3V	-	6	10	mA

4.5 DMD Interface:

The flash board can connect with DPP2601/7 ASIC to drive 0.2" nHD DMD. The DMD data bus and control signals are shown as table 4.5, these signals are built in the 50pin board to board connector interface.

Table 4.5- DMD Pin Descriptions

Pin Name	Description
DATA(11:0)	· Data Bus0~11
DMD_DCLK	· Data Clock
DMD_LOADB	· Parallel Latch Load Enable
DMD_SCTRL	· Serial Control
DMD_BUS	· Reset Control Serial Bus
DMD_OEZ	· Output Enable signal for internal Reset Driver circuitry
DMD_STRB	· Rising Edge on DAD_STROBE latches in the Control Signals
DMD_SAC_BUS	· Stepped Address Control Serial Bus
DMD_VCC	· Power Supply for Low Voltage CMOS logic
DMD_ VBIAS	· Power supply for Positive Bias level of Mirror Reset signal
DMD_ VOFFSET	· Power Supply for High Voltage CMOS logic
DMD_ VRESET	· Power supply for Negative Reset level of Mirror Reset signal

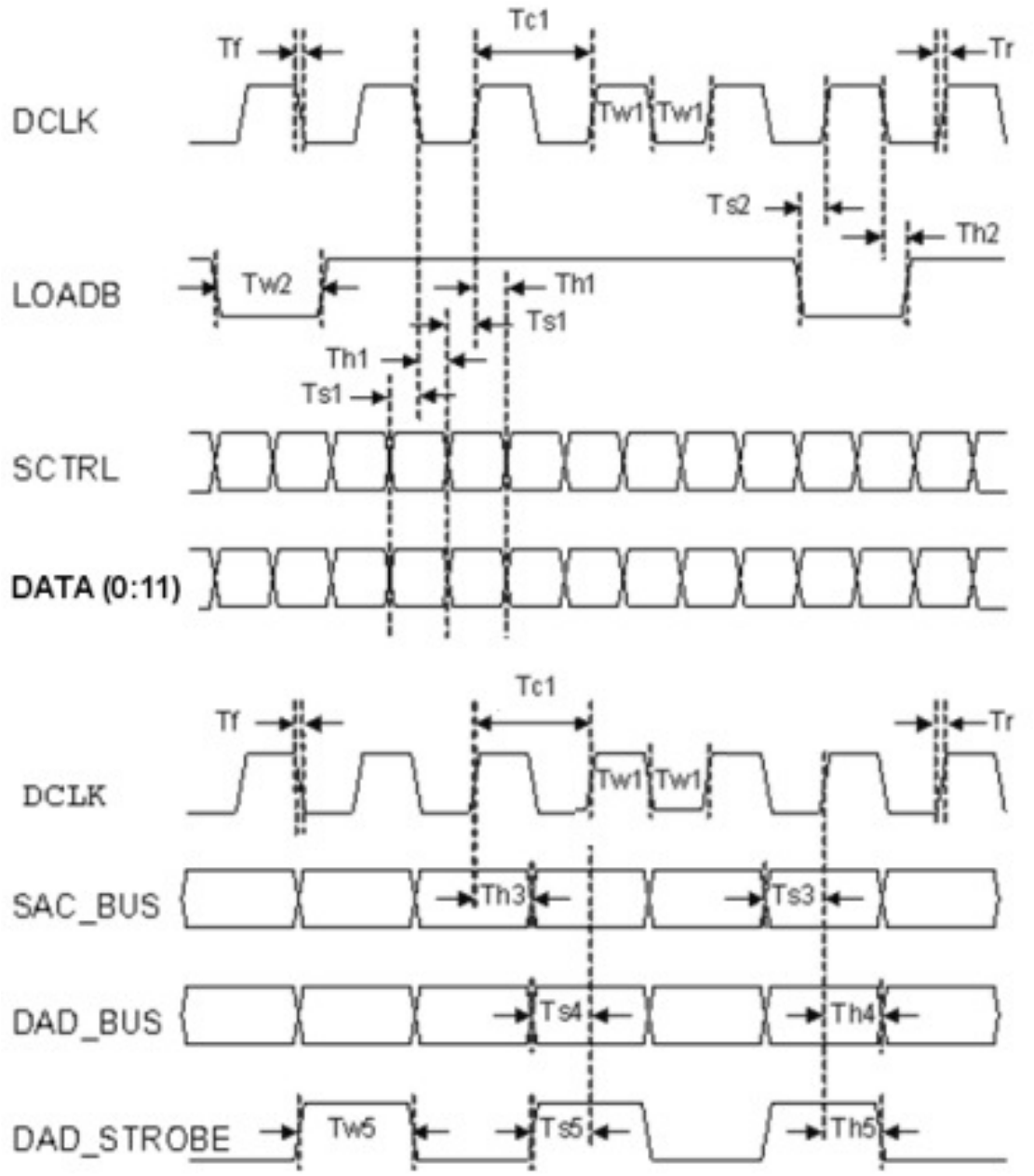


Figure 4.4- DMD Timing Waveforms

Table 4.6- DMD Timing AC Characteristics					
Parameter		MIN	NOM	MAX	UNIT
Ts1	Setup time: DATA before rising or falling edge of DCLK	1			ns
Ts1	Setup time: SCTRL before rising or falling edge of DCLK	1			ns
Ts2	Setup time: LOADB low before rising edge of DCLK	1			ns
Ts3	Setup time: SAC_BUS low before rising edge of DCLK	2			ns
Ts4	Setup time: DAD_BUS high before rising edge of DCLK	2			ns
Ts5	Setup time: DAD_STROBE high before rising edge of DCLK	2			ns
Th1	Hold time: DATA after rising or falling edge of DCLK	1			ns
Th1	Hold time: SCTRL after rising or falling edge of DCLK	1			ns
Th2	Hold time: LOADB low after falling edge of DCLK	1			ns
Th3	Hold time: SAC_BUS low after rising edge of DCLK	2			ns

Th4	Hold time: DAD_BUS after rising edge of DCLK	2			ns
Th5	Hold time: DAD_STROBE after rising edge of DCLK	2			ns
Tc1	Clock Cycle: DCLK	12.5		16.67	ns
Tw1	Pulse Width high or low: DCLK	5			ns
Tw2	Pulse Width low: LOADB	7			ns
Tw5	Pulse Width high: DAD_STROBE	7			ns
tr	Rise time (20% – 80%): DCLK			2.5	ns
tr	Rise time (20% – 80%): DATA / SCTRL / LOADB			2.5	ns
tf	Fall time (80% – 20%): DCLK			2.5	ns
tf	Fall time (80% – 20%): DATA // SCTRL / LOADB			2.5	ns

4.6 Flash Interface:

The flash board built in 4M-Bits W25X40BLZP Winbond serial flash for initial data and LED duty storage. The serial flash signals are shown as table 4.7, these signals are built in the 50pin B-TO-B connector interface.

Table 4.7- Serial Flash Pin Descriptions

Name	Description
FLASH_CSZ	Chip Select Input
FLASH_DOUT	Data Output
FLASH_DIN	Data Input
FLASH_CLK	Serial Clock Input
VFLASH	Power Supply

4.7 LED FPC Golden Finger pin Assignment:

The LED FPC golden finger pin assignment is shown as table 4.8

Table 4.8- LED Golden Finger Pin Descriptions

Pin #	Name	Description
1	COMMON_ANODE	Common Anode of Red、Green and Blue LED
2	COMMON_ANODE	Common Anode of Red、Green and Blue LED
3	RED_CATHODE	Cathode of Red LED
4	RED_CATHODE	Cathode of Red LED

5	THERMISTOR	Thermistor2
6	THERMISTOR	Thermistor1
7	GREEN_CATHODE	Cathode of Green LED
8	GREEN_CATHODE	Cathode of Green LED
9	BLUE_CATHODE	Cathode of Blue LED
10	BLUE_CATHODE	Cathode of Blue LED

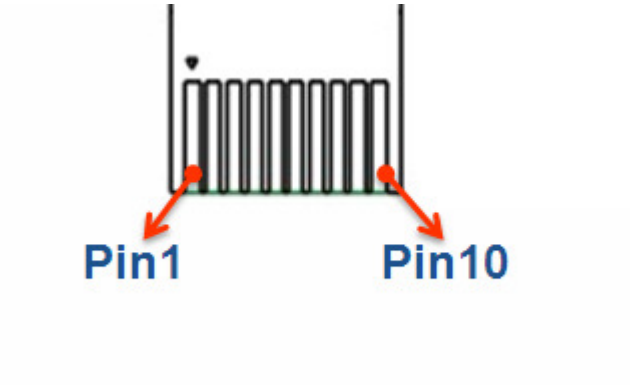
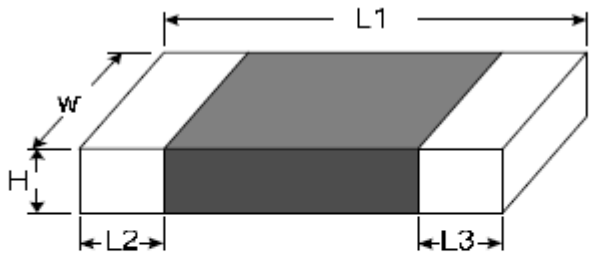


Figure 4.5- LED FPC Golden Finger

4.7.1 Thermistor Specification and LUT Table

4.7.1.1 Structure and Dimensions



(unit : mm)

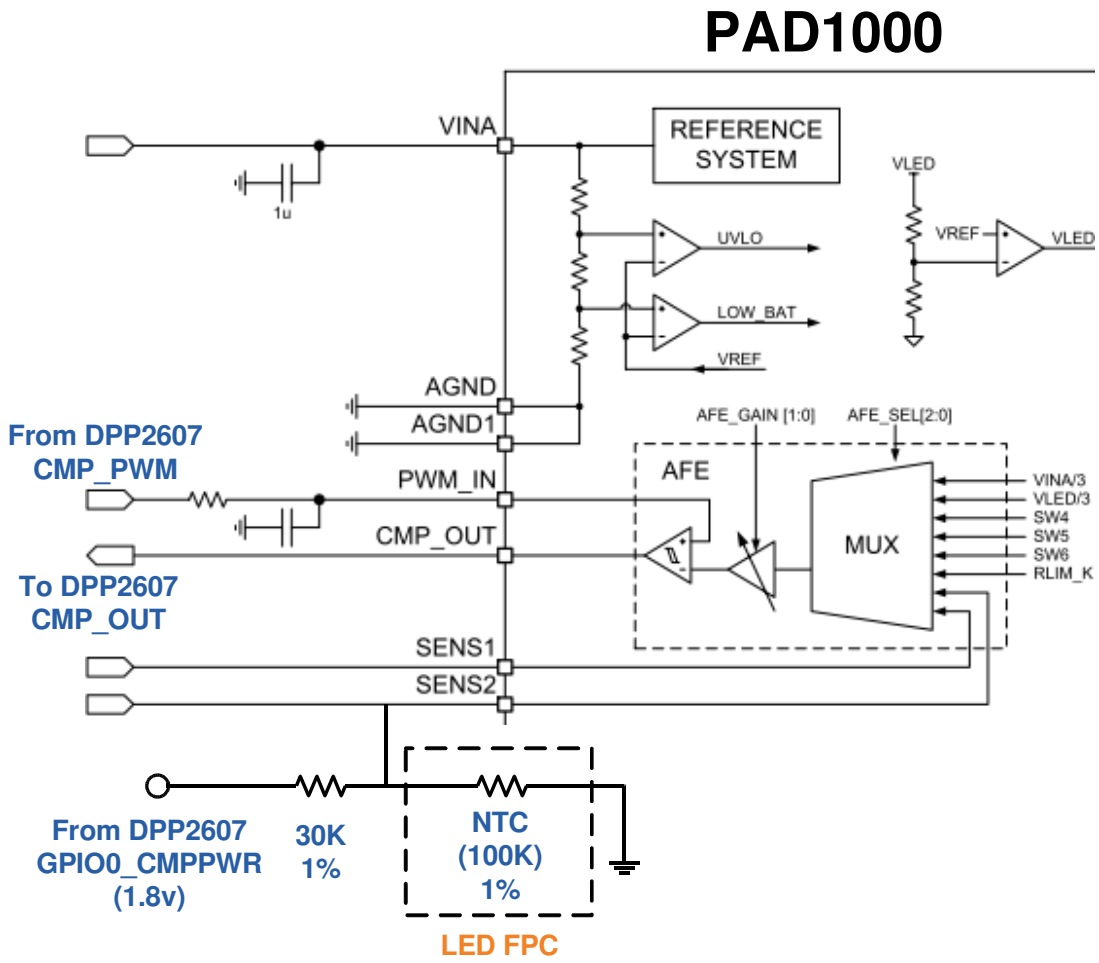
L1	W	H max.	L2 and L3
1.00±0.15	0.50±0.10	0.60	0.20±0.10

4.7.1.2 Electrical Characteristics

Part No.	Zero Power Resistance at 25℃	Tolerance of R_{25}	$B_{25/85}$ Value	Tolerance of B Value	Max. Power Dissipation at 25℃	Dissipation Factor	Thermal Time Constant	Operating Temperature Range
	R_{25}(KΩ)	(± %)	(K)	(± %)	P_{max}(mW)	δ (mW/℃)	τ (sec.)	T_L~T_U(℃)
TSM0A104F39H1RZ	100	1	3975	1	170	Approx. 1.7	Approx. 2.0	-40 ~ +125

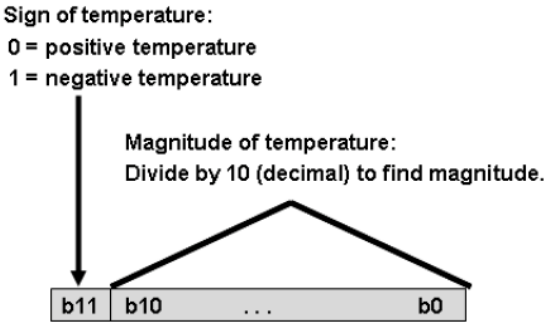
4.7.1.3 Hardware requirement:

The DPP2607 can support Temperature measurement using an external Thermistor. A typical Thermistor circuit used to interface to the DPP2607 and PAD1000 as shown below. GPIO0_CMPPWR is power supply for Thermistor. Thermistor is used in a voltage divider with resistor 30K. Depend on a voltage divider resistor 30K, a Thermistor LUT is generated by the software and stored in Flash. The Thermistor LUT contains look-up data that maps comparator voltages to 12-bit temperature outputs in signed format. Please note that if host want to use DPP2607 to read temperature, the voltage divider resistor must be 30K.



4.7.1.4 Read Temperature value:

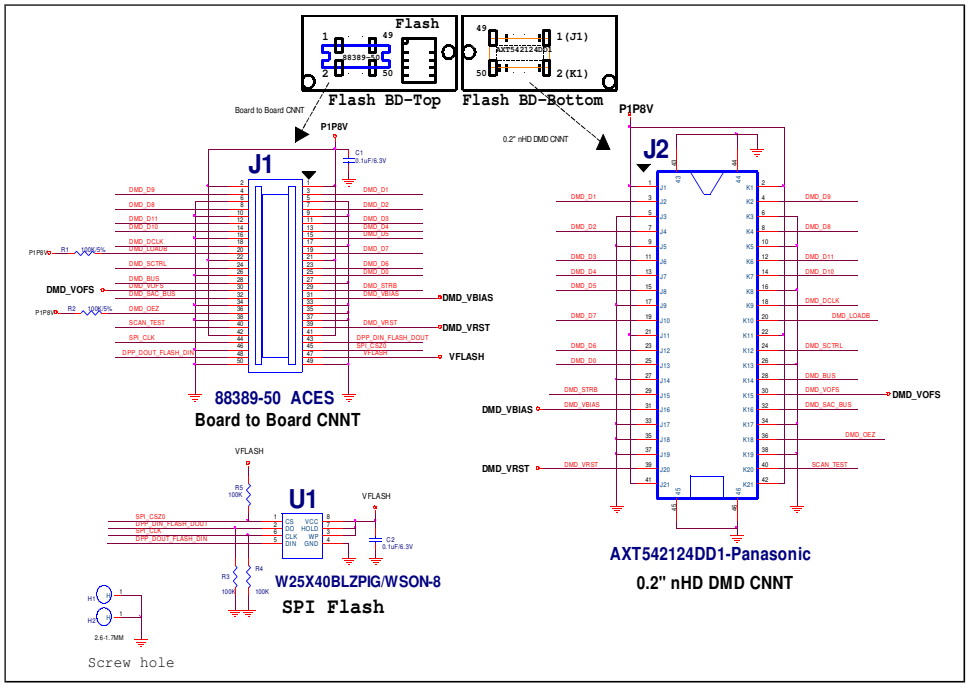
This command is used to read the temperature in degree C as derived from the thermistor. The temperature is a 12-bit value in sign-magnitude format as shown below.



Example #1: b(11:0) = 000110101010
426d / 10d = +42.6degC

Example #2: b(11:0) = 100110101010
426d / 10d = -42.6degC

4.8 Flash Board Circuit:



4.9 LED Characteristics

4.9.1 LED Amber And Blue Colors:

Maximum Ratings

			Values		
Parameter					
Junction temperature			125		
Forward current per chip DC (Ts=25°C)	(r (n		100 500		
Surge current per chip t≤10 µs, D = 0.1; TA=25°C			1500		
			1000		
Reverse voltage per chip DC(T_S=25°C)		V_R	Not designed for reverse operation		V
Forward voltage per chip IF=350mA	(min.) (typ.) (max.)	V_F V_F V_F	2.0 2.2 2.7	2.7 3.4 3.8	V

* Condensation on the module has to be avoided.

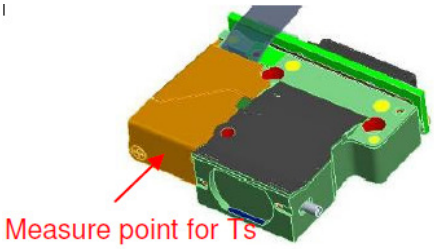
4.9.2 LED Green Color:

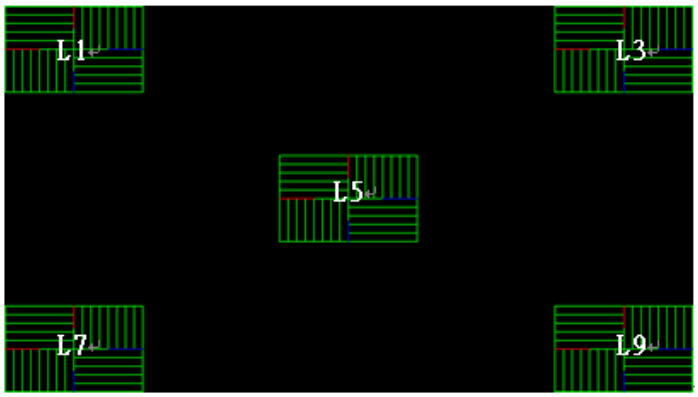
Maximum Ratings

			Values		
Parameter			Green		
Junction temperature			125		
Forward current per chip DC (Ts=25°C)	((		100 500		
Surge current per chip t≤10 µs, D = 0.1; TA=25°C			1500		
			1000		
Reverse voltage per chip DC(T_S=25°C)		V_R	Not designed for reverse operation		V
Forward Voltage IF=350mA	(min.) (typ.) (max.)	V_F V_F V_F	2.7 3.4 3.9		V

5 OPTICAL PERFORMANCE

5.1 Optical Parameter

Item	Formula / Measurement Location	Specification
Brightness	((Ave {P1...P9})*Screen Area)	19.0lm(typical) and 15.0lm(min) at 400mA & Ts= 42±5°C  Note: 1. Ts=LED copper plate temperature. 2. Suggest Ts<65deg.C at RT to keep LED safe.
Luminance Uniformity	(Ave.(P1, P3,P7,P9)/P5)	80% (Typ.) 70% (Min.)
Contrast Ratio	Full White/ Full Black	1300:1 (Typ.) 900:1 (Min.)
Color Coordinate	Full white x, y coordinate in P5	X = 0.30±0.01 Y = 0.32±0.01 @400mA LED Current and Ts:42±5°C
Flare	Use pattern, and measured by ruler. Please refer to the Picture-B / Flare pattern	≦7 pixel
Focus force	Use force gauge and test jig to measure focus force	0~65g



Picture-B /Flare pattern

5.2 Image Quality on projected screen

5.2.1 Particle imaging on the screen

SCREEN	ACCEPTANCE CRITERIA
Gray 10	1. No Bright Pixels in Active Area 2. ≤ 1 Bright Pixels in the POM
White	1. ≤ 4 Dark Pixels in the Active Area
Any screen	1. No Adjacent Pixels/Clusters 2. No Unstable Pixels in Active Area 3. No DMD window aperture shadowing on the Active Area 4. No Row or Column defects 5. Blemishes are allowed 6. Eyecatcher and Border Artifacts are allowed

5.2.2 Definition of Ghost

The intensity of ghost on the screen of full dark shall be less than 4 times of the intensity of projected image center.

5.2.3 Definition of Color band

Follow limited sample defined by YOI & customer.

5.3 Dimension and weight

Width	29.85 mm
Depth	28.50 mm
Height	7.70 mm
Weight	~8g

5.4 Engine Dimension

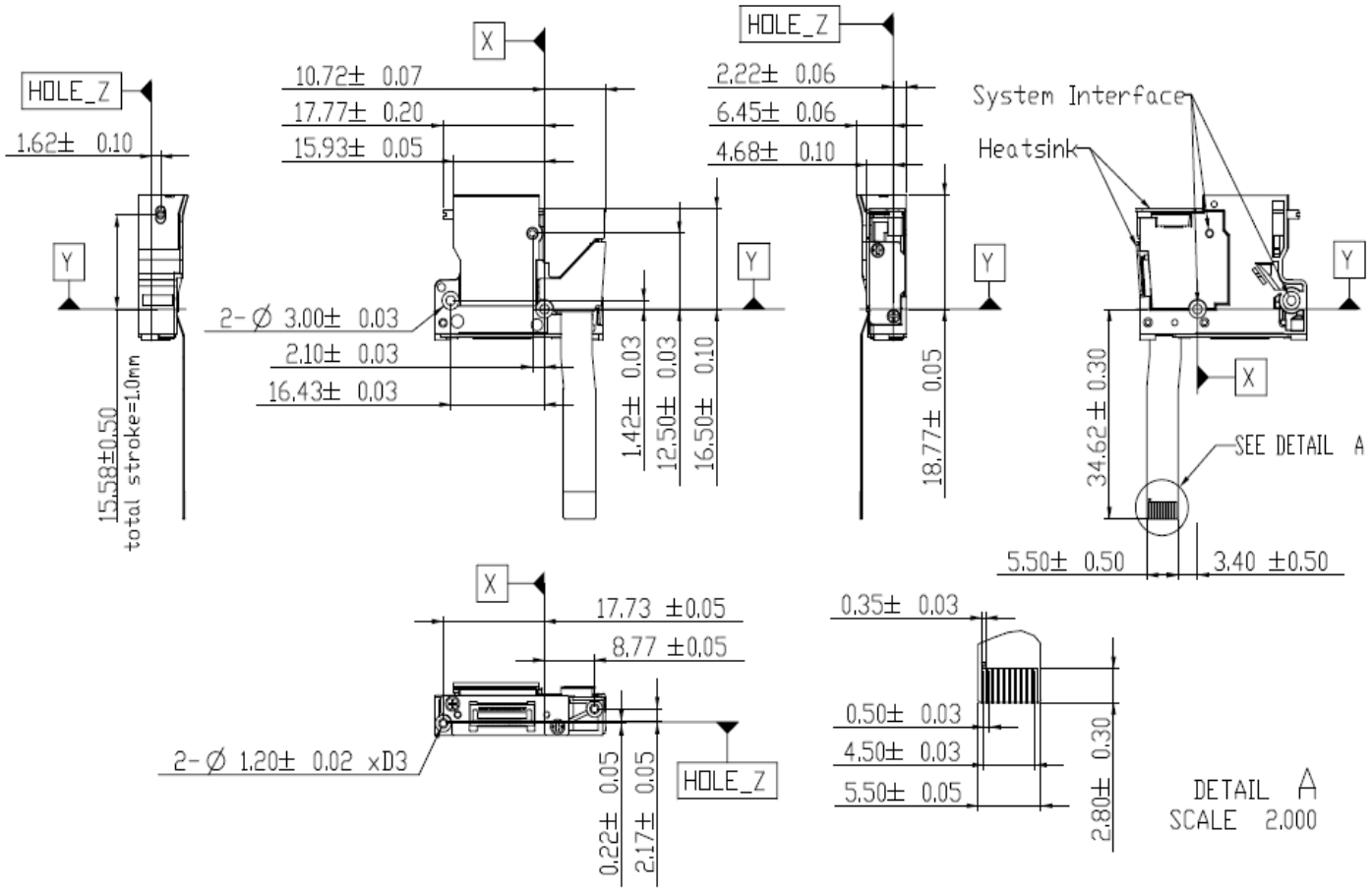
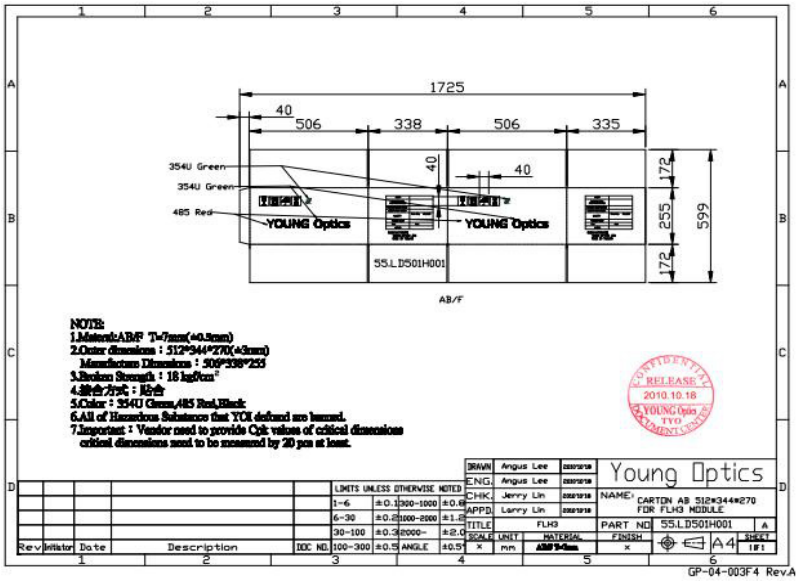


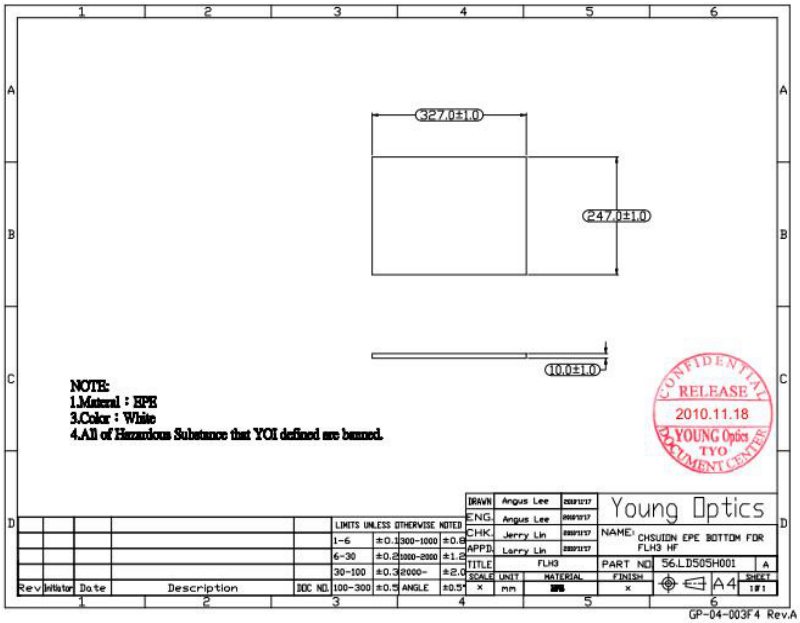
Figure 6-1 **FLE2-F** Engine Outline dimension

6 Package and Handling

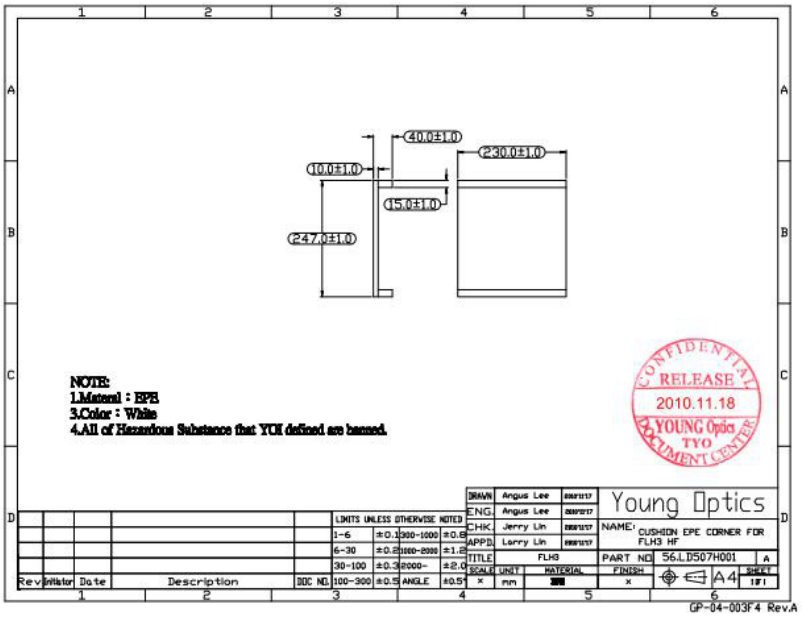
6.1 Package Illustration



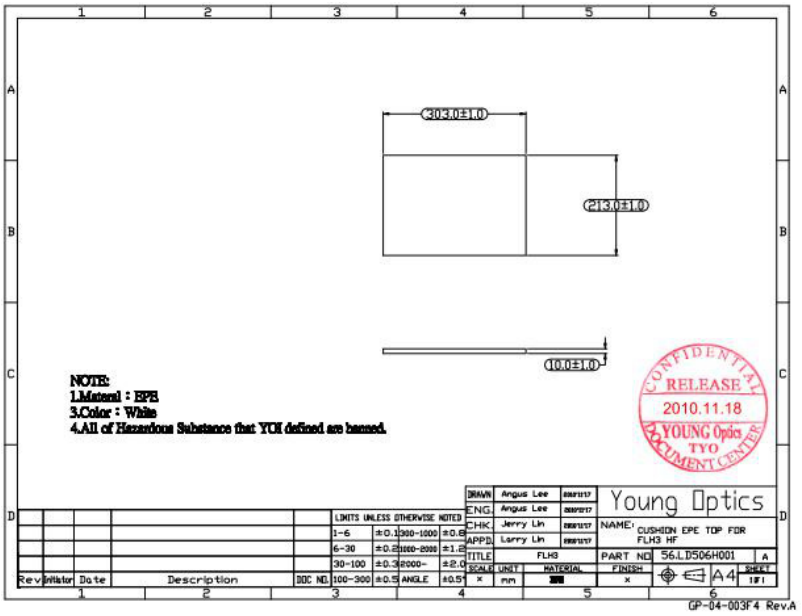
6.2 Cushion EPE Bottom



6.3 Cushion EPE Corner

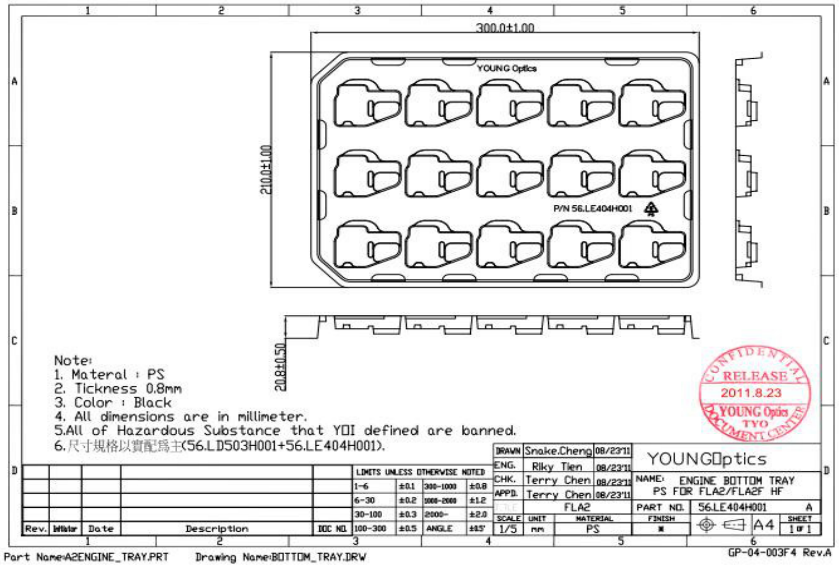


6.4 Cushion EPE Top

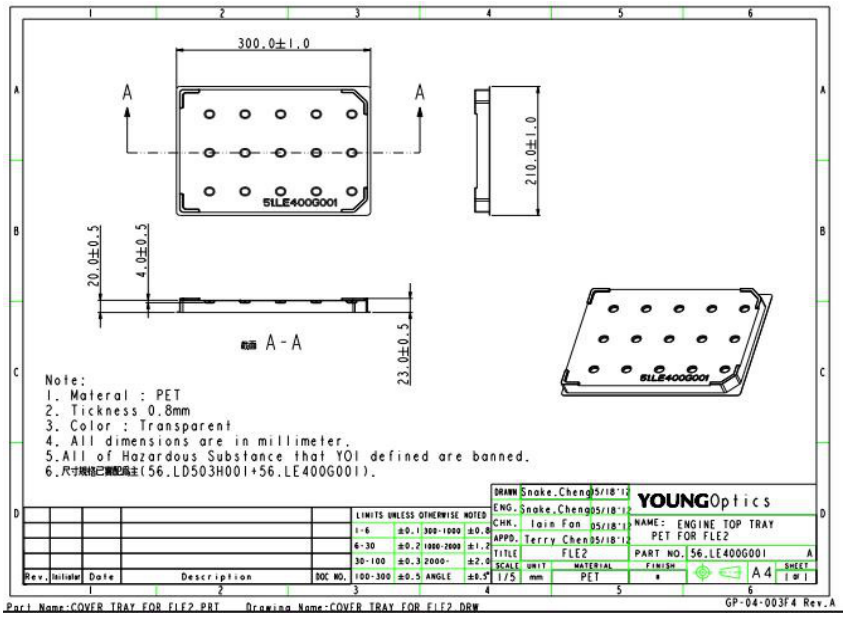


7 Handling Illustration

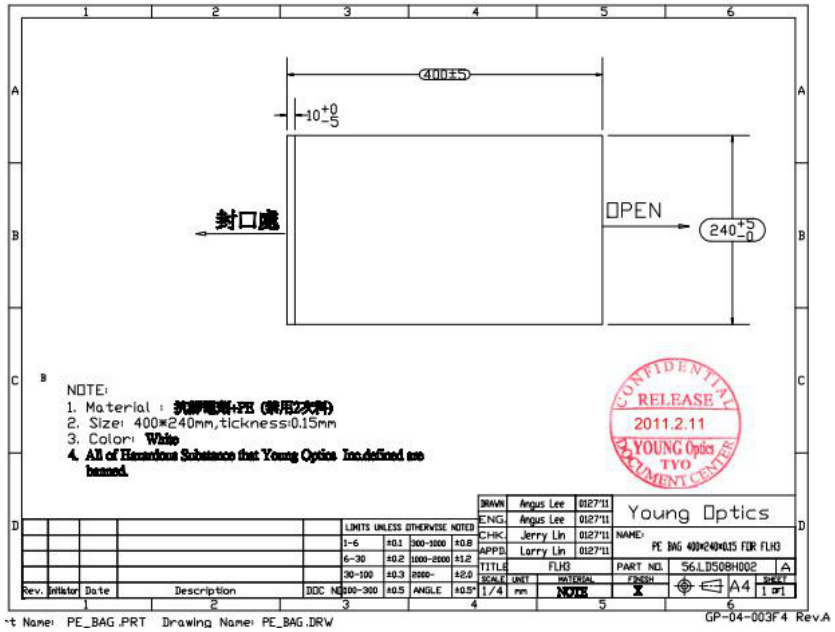
7.1 Tray Base



7.2 Tray Cover



7.3 PE Bag for Tray



7.3.1 Marking on shipping box

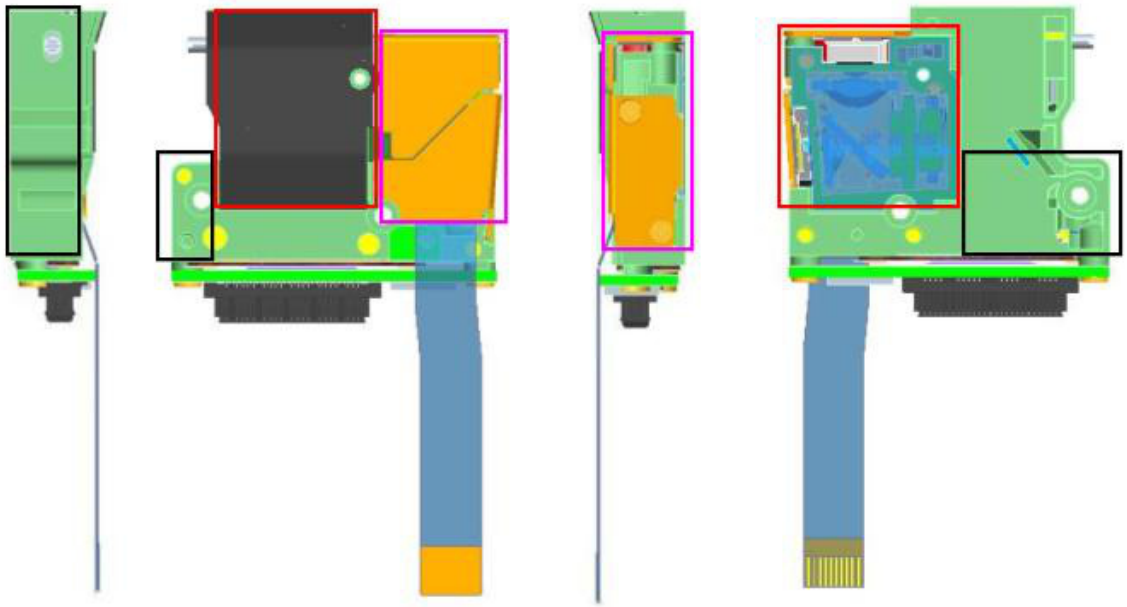
Customer :	
Information:	
Q'ty :	PCS
P/O :	
Remark :	

MANUFACTURER:
YOUNGOPTICS(KUNSHAN)Co. ,LTD
MADE IN CHINA
P/N : 55.L9504G001.A

7.4 Handing Illustration

7.4.1 Handling Attention

- Each tray plate contains 15 Engines.
- Each carton box contains 20 tray plates.
- Do not let the product soak in (contact with) any liquids.
- Do not clean the P-Lens with flammable liquids.
- Keep the P-Lens away from sharp objects.
- Do not apply any physical destruction or disassembly to the product.
- Use the ESD antistatic gloves to pick the Engine up.



The red frame is " can't touch area", include SOMA , Mylar.
The black frame is handle area that YOI suggest.
The pink frame is heatsink, Strongly suggest to wear finger cot if you maybe touch hetsink.

7.5 Engine Label

7.5.1 Marking /Barcode Label on engine

Label size 7.0 x 10.0mm

Code Define

LE42 4
1 2
A 12 07
3 4 5
10 A T
6 7 8
00087
9

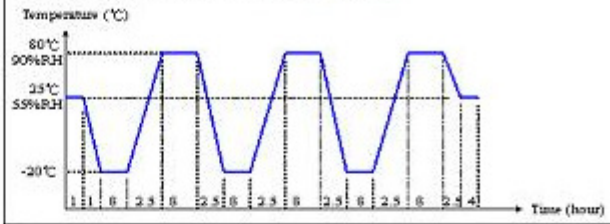
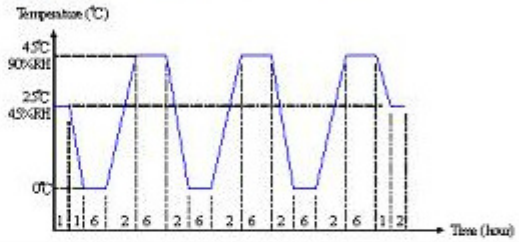
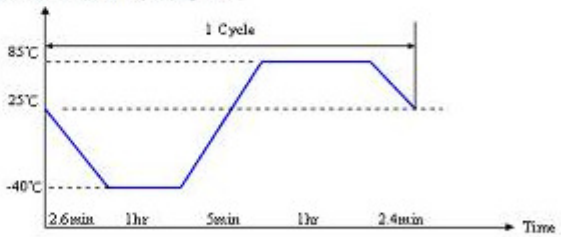
Item	Definite description
1	YOI Project Code (LE42)
2	Extension Code (1,2,3...)
3	Engine version (A,B,C...)
4	Year of production (12→2012, 13→2013...)
5	Month of production (01→January, 02→February...)
6	Day of production (01→01 ,02→02...)
7	Assembly Line (A,B,C...)
8	Production Location (T→TYO)
9	Serial Number (00001,00002,...,99999)

8 Green Product requirement

(1) All of hazardous substances that YOI defined are banned.

(2) Component and Engine module: Conformity with DIRECTIVE 2002/95/EC (RoHS) of the European Union.

9 Reliability test

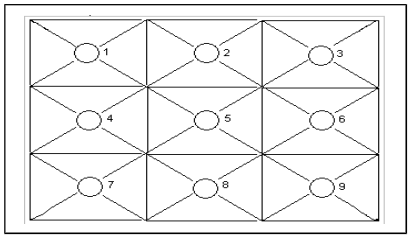
No.	Test Item	Test Condition / Specification
1	Temperature / Humidity Cycle Test (Without Package)	Non-Operating: -20℃~ 80℃, 0%~90%RH, 3 Cycles, 69 hrs 
		Operating : 0℃~ 45℃, 0%~90%RH, 3 Cycles, 51 hrs 
2	Low Temp Test (Without Package)	Non-Operating: -40℃, 168 Hr
		Operating: 0C, 168Hr
3	High Temp (Without Package)	Operating: 45C, 168Hr
4	Thermal Shock	Non-Operating: -40℃~85℃, ramp rate:5 min Dwell time :1hrs, 30Cycles 
5	Vibration	Non-Operating: Sine wave,20~2000Hz,4G , 4min/cycle , 4cycle/axis Projection Module placed in a Dummy Phone Case。
6	Drop Test	120cm, 1 time/Face, 6Faces, 2cycle
7	Mechanical Shock	Non-Operating: Half-sine, 1500g , 0.5ms, ±X, ±Y,±Z 1times for each direction . Projection Module placed in a Dummy Phone Case .

10 Appendix

10.1 Appendix-I: inspection method

- ***Brightness (A1)***

Luminance is the average luminance (lux) of each of the 9 points (position 1~9) multiplied by the screen area in square meters on the FULL WHITE pattern as Picture-B.



Picture-D

- ***Luminance Uniformity (A2)***

Luminance uniformity is the Japan standard,
Average luminance (lux) of position (1, 3, 7, 9) divided by the luminance (lux) of position P5 on FULL WHITE pattern as Picture-D

- ***Full White/ Full black Contrast (A3)***

The luminance ratio of a FULL WHITE to a FULL BLACK pattern in the position 5 of picture-A .

- ***Color Coordinate (A4)***

Cartesian coordinates used to define a color in CIE color space. The 1931 chromaticity values are designated x, y. The Color coordinate value is the x,y value in each of the position 5 on the FULL WHITE pattern as Picture-D respectively