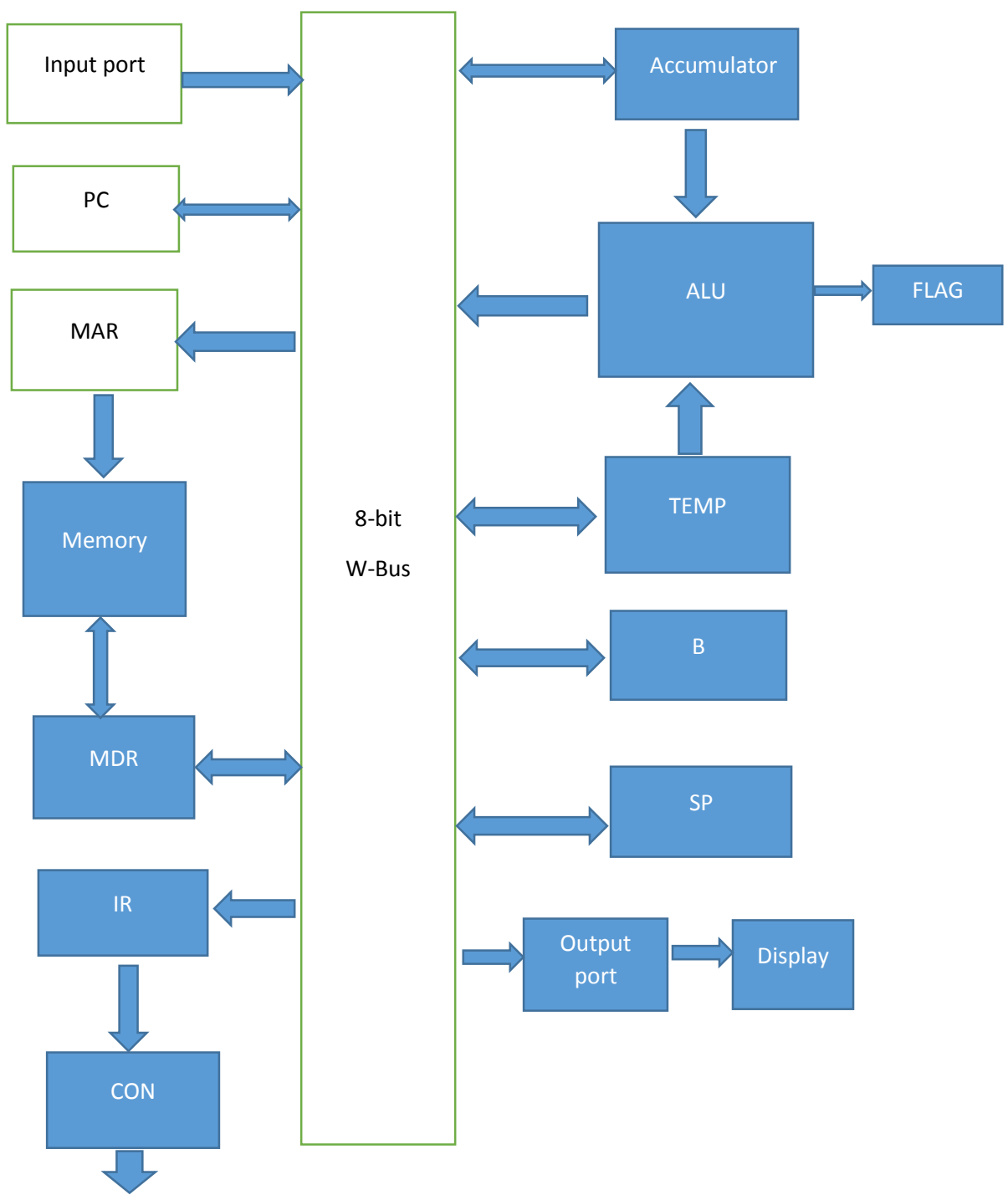
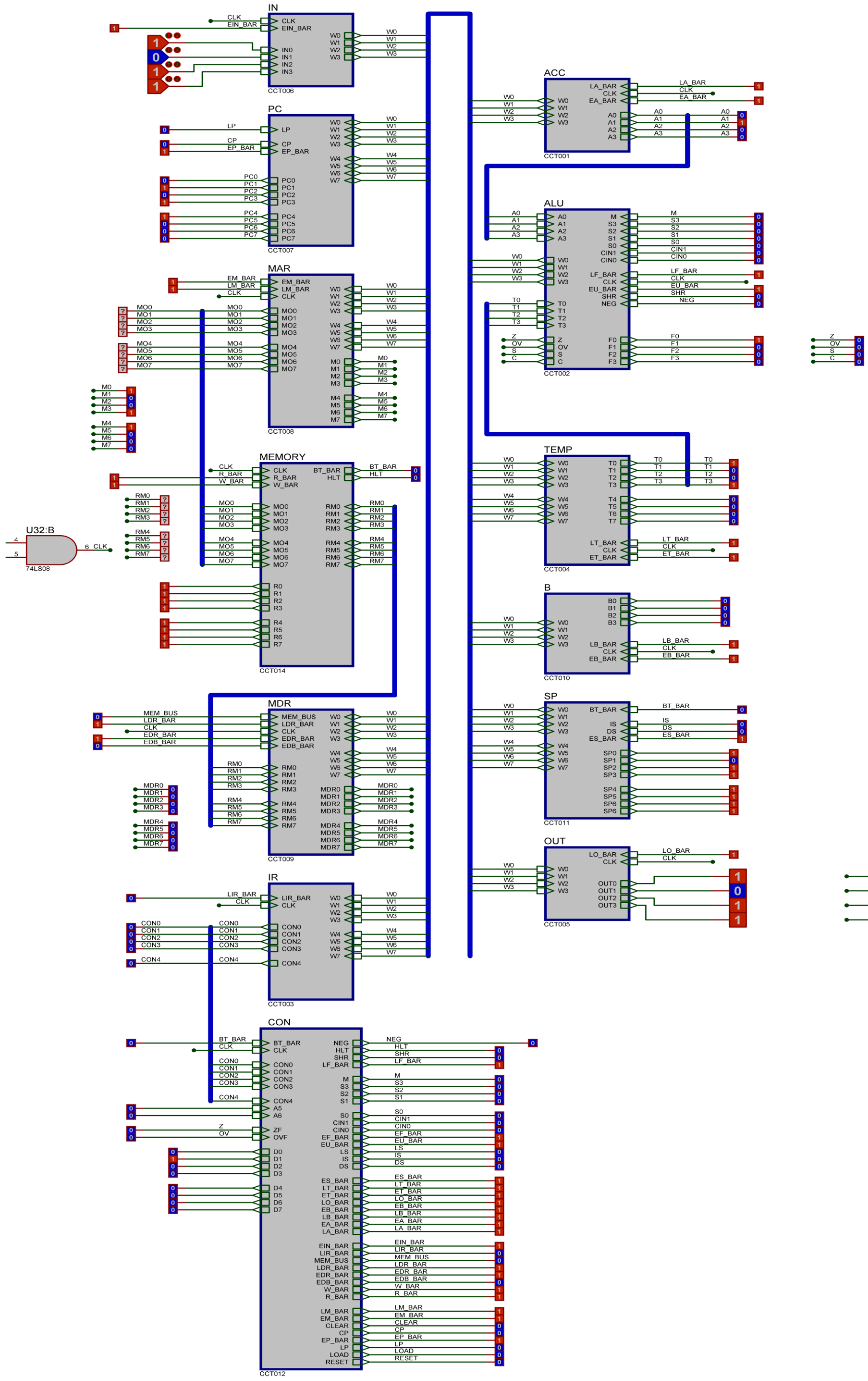
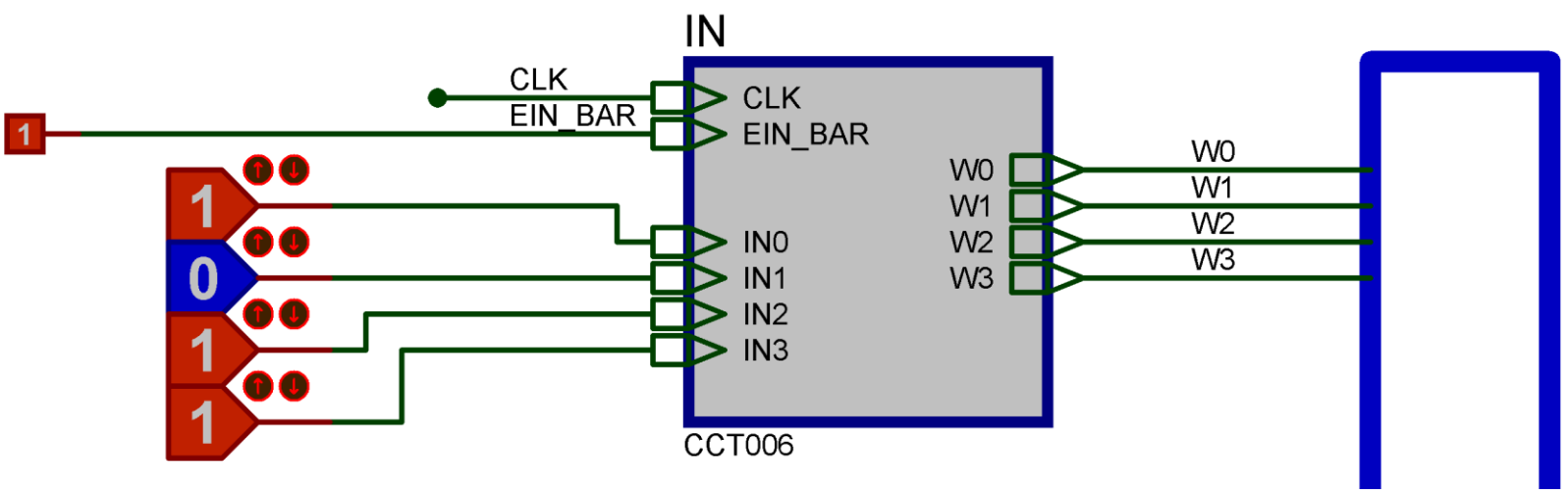
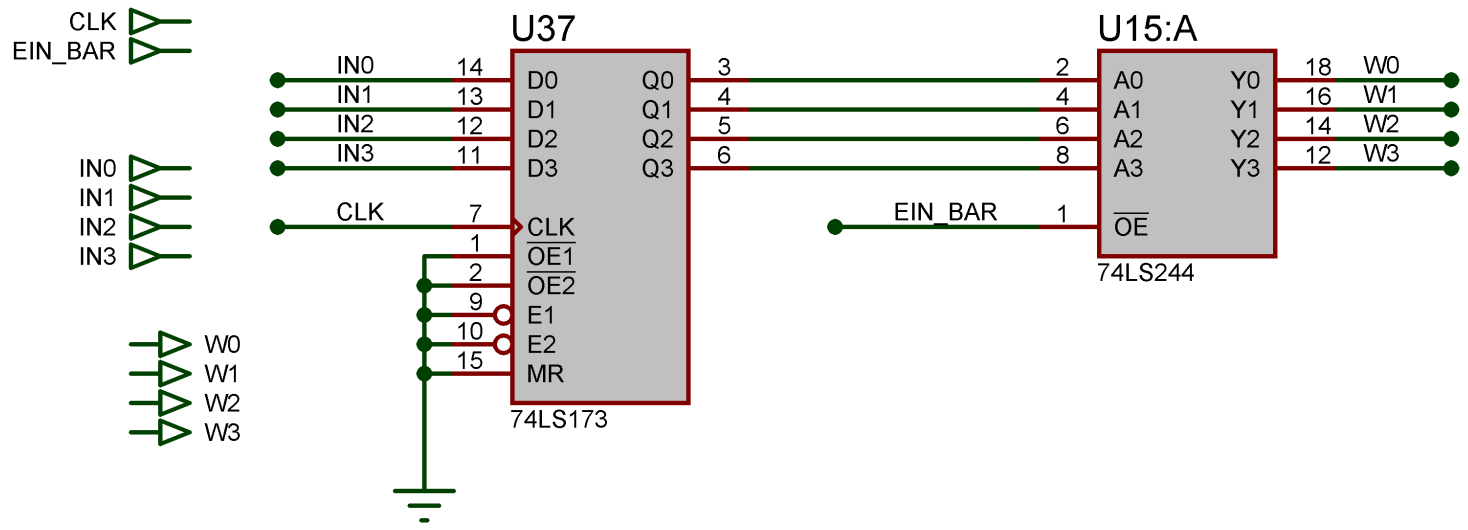
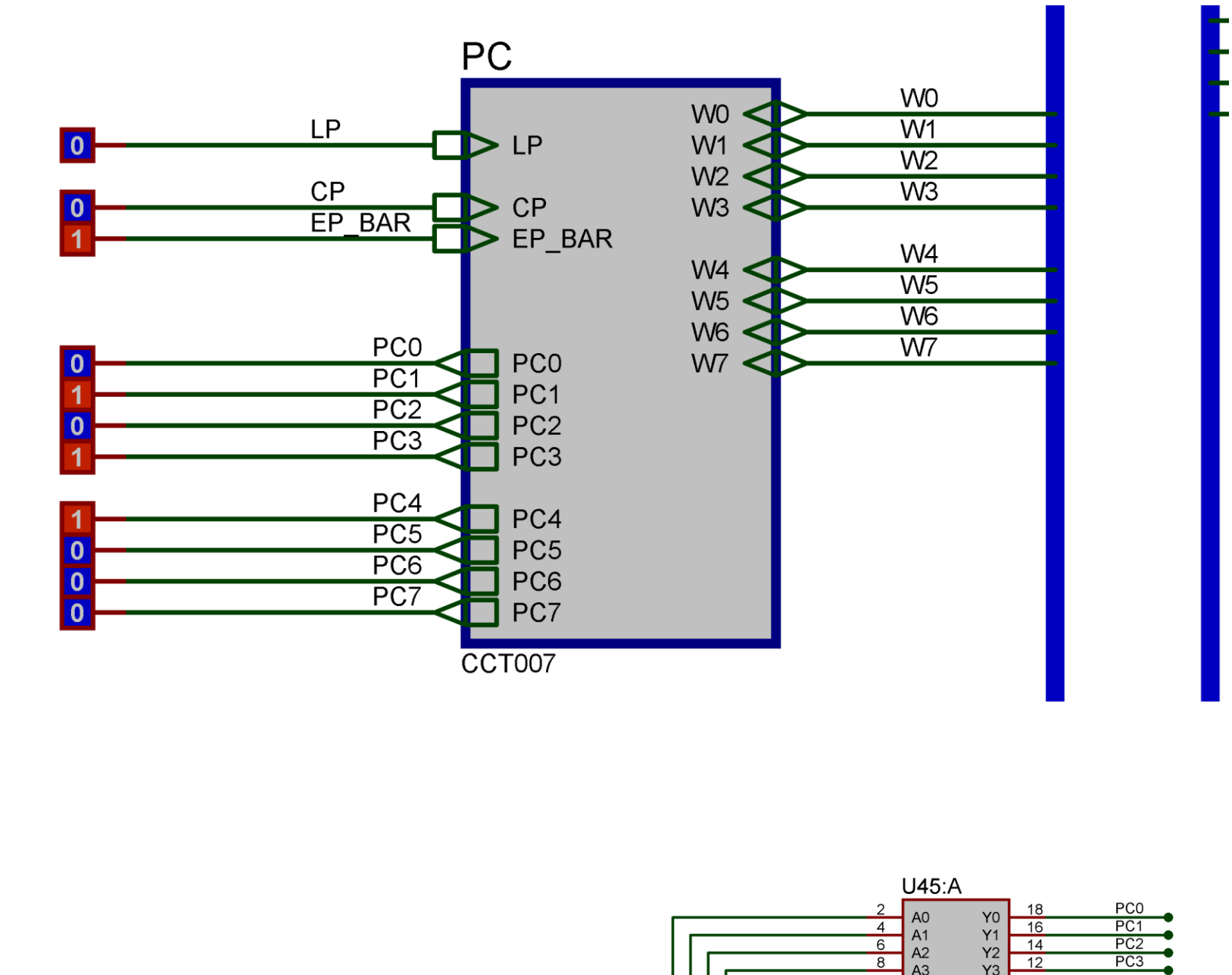
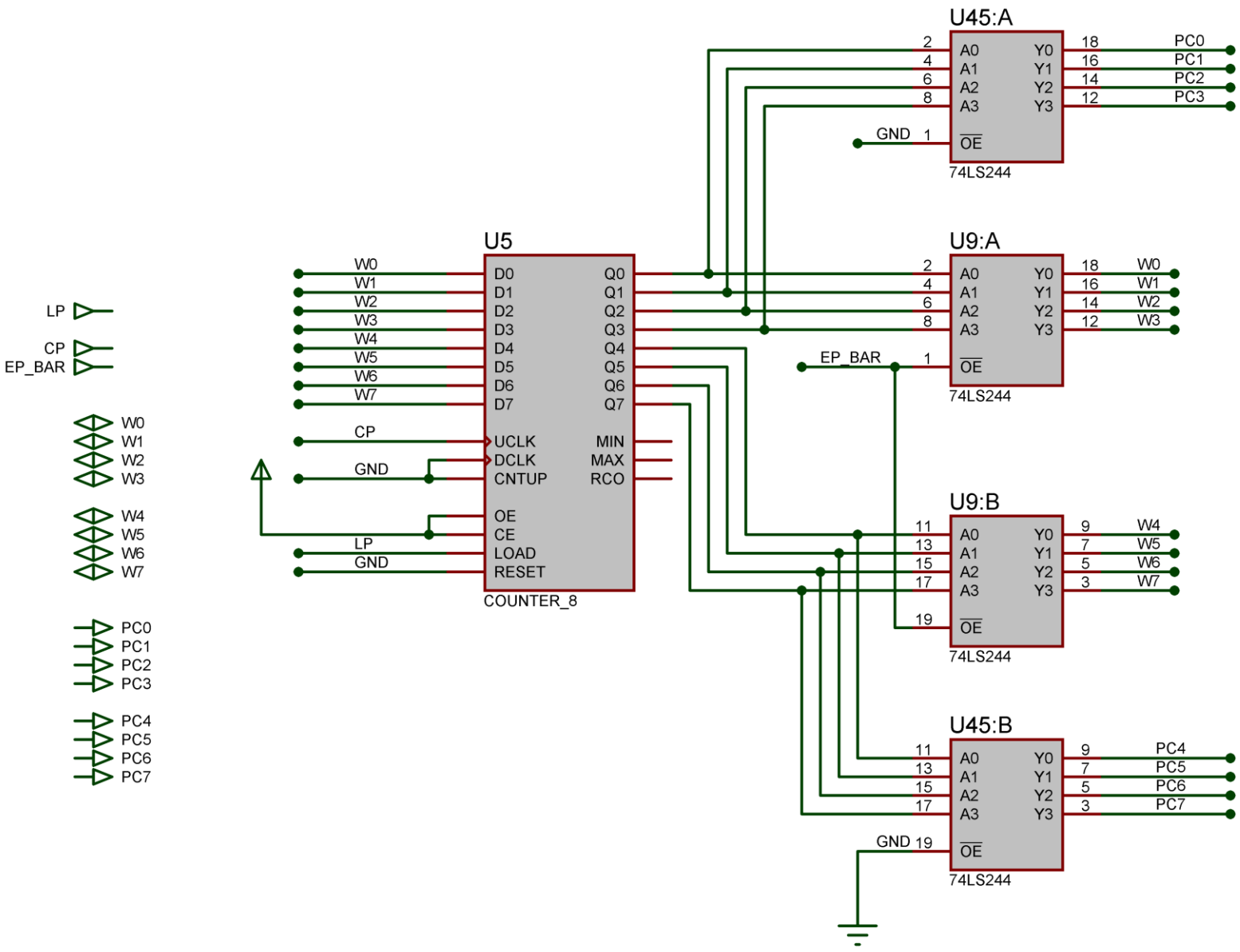

Input port
PC
MAR
Memory
MDR
IR
CON
8-bit
W-Bus
Accumulator
ALU
FLAG
TEMP
B
SP
Output port
Display

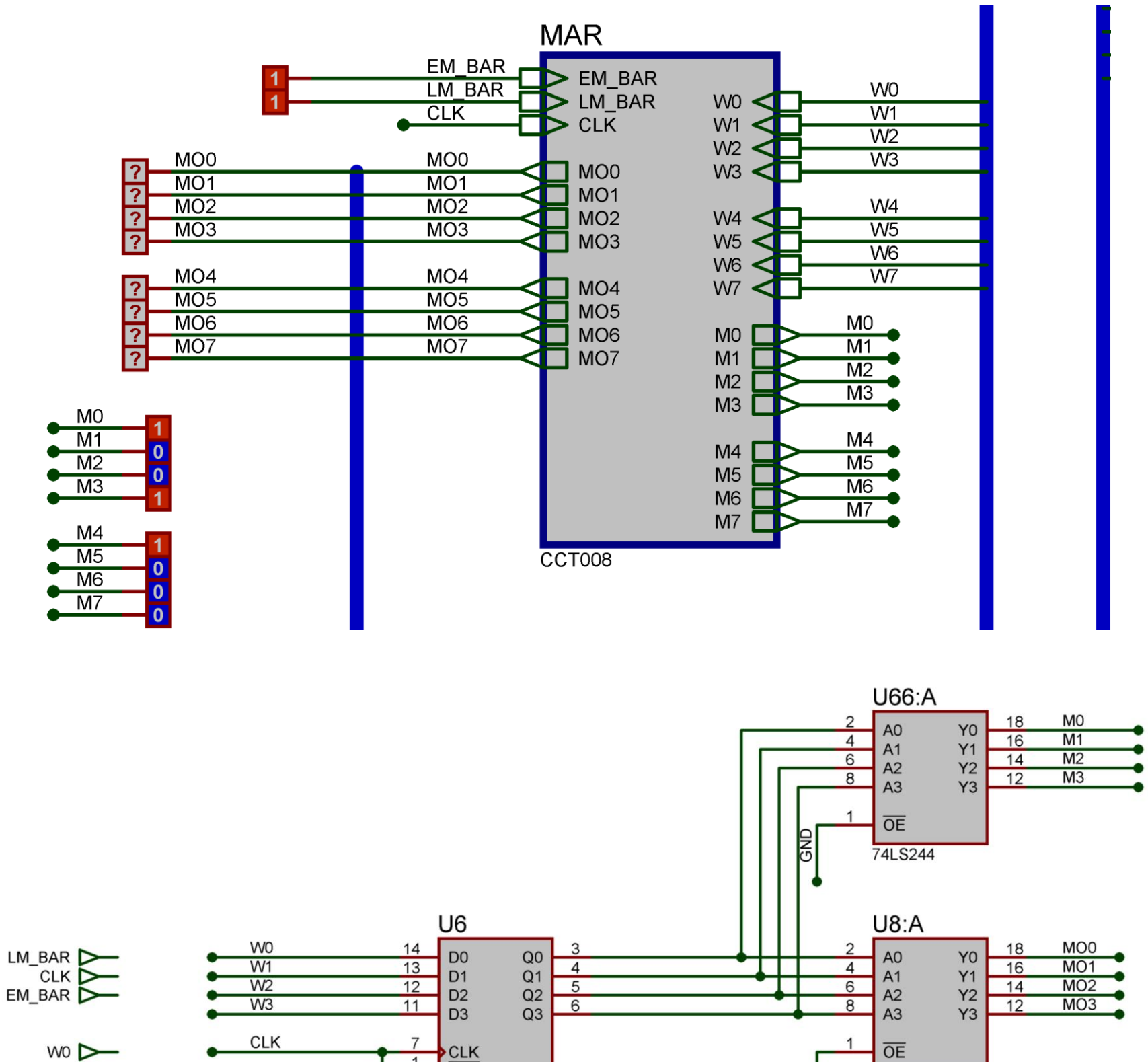

IN
CCT006
PC
CCT007
MAR
CCT008
MEMORY
CCT014
U32:B
74LS08
MDR
CCT009
IR
CCT003
CON
CCT012
ACC
CCT001
ALU
CCT002
TEMP
CCT004
B
CCT010
SP
CCT011
OUT
CCT005

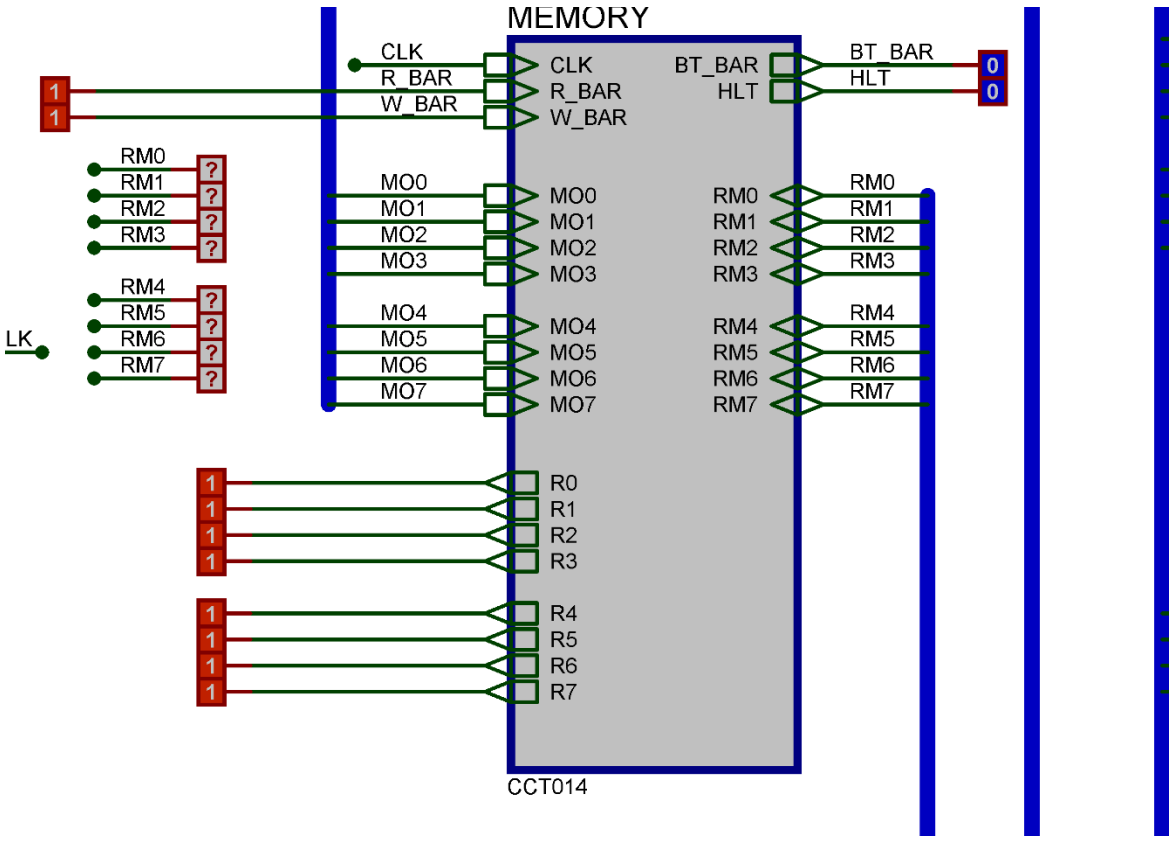

IN
CLK
EIN_BAR
CLK
EIN_BAR
W0
W1
W2
W3
IN0
IN1
IN2
IN3
CCT006
1
1
0
1
1
W0
W1
W2
W3


CLK
EIN_BAR
IN0
IN1
IN2
IN3
W0
W1
W2
W3
U37
IN0
IN1
IN2
IN3
CLK
14
13
12
11
7
1
2
9
10
15
D0
D1
D2
D3
CLK
OE1
OE2
E1
E2
MR
Q0
Q1
Q2
Q3
3
4
5
6
74LS173
U15:A
2
4
6
8
1
A0
A1
A2
A3
OE
Y0
Y1
Y2
Y3
18
16
14
12
W0
W1
W2
W3
EIN_BAR
74LS244

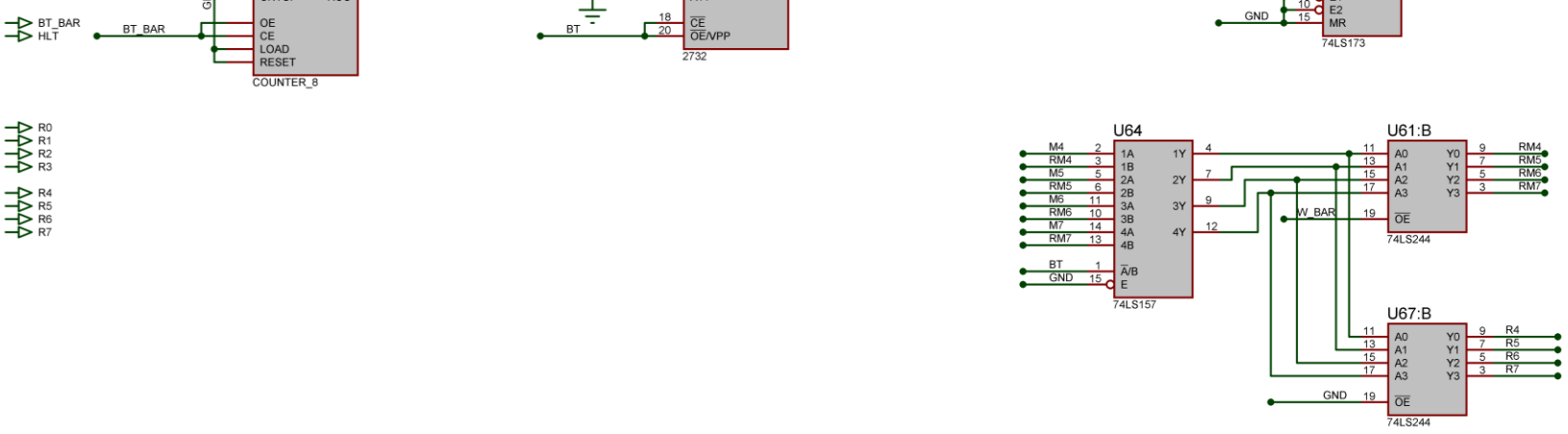

PC
LP
CP
EP_BAR
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
W0
W1
W2
W3
W4
W5
W6
W7
CCT007

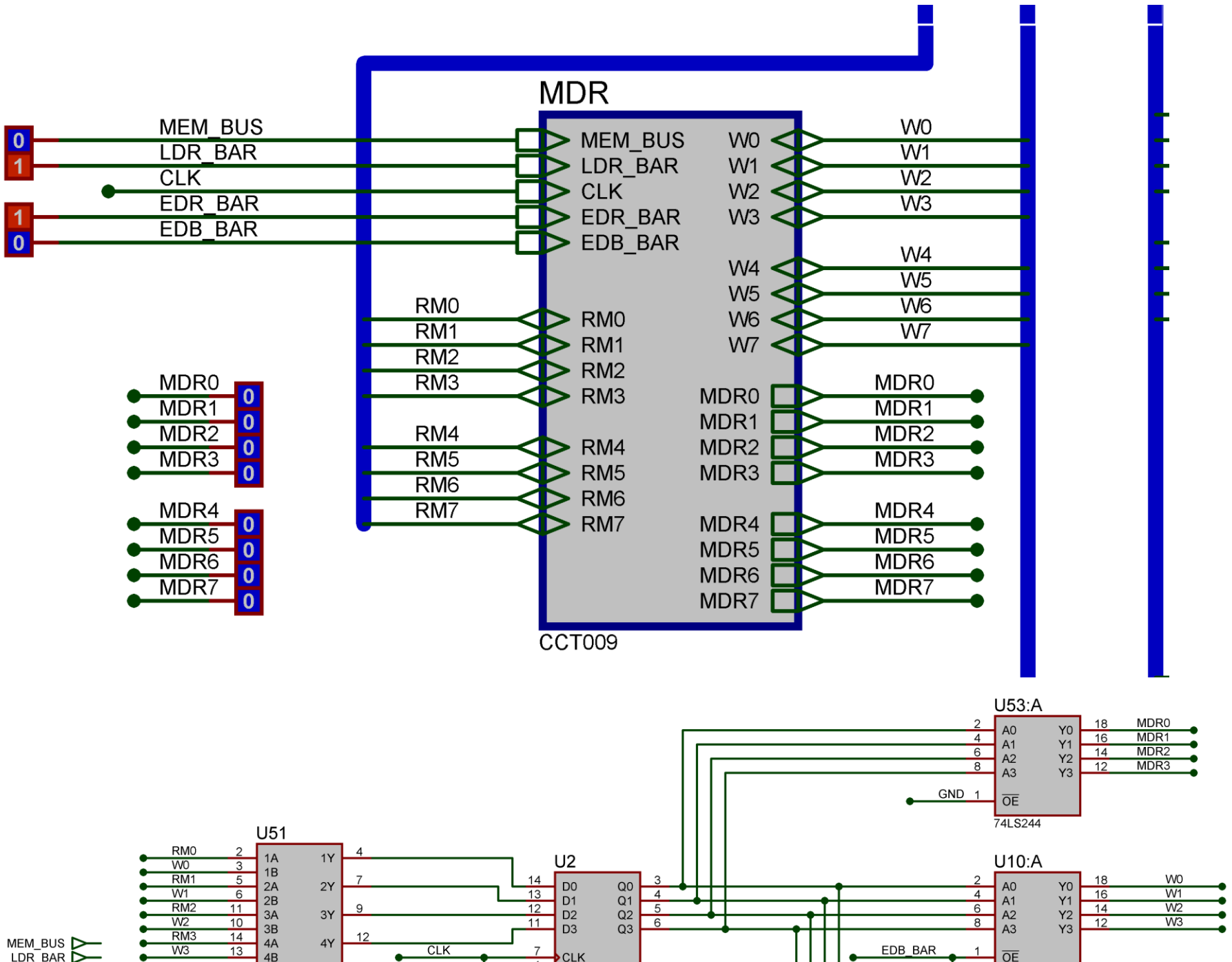

U45:A
U5
U9:A
U9:B
U45:B
74LS244
COUNTER_8
GND
EP_BAR
CP
LP
W0
W1
W2
W3
W4
W5
W6
W7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7

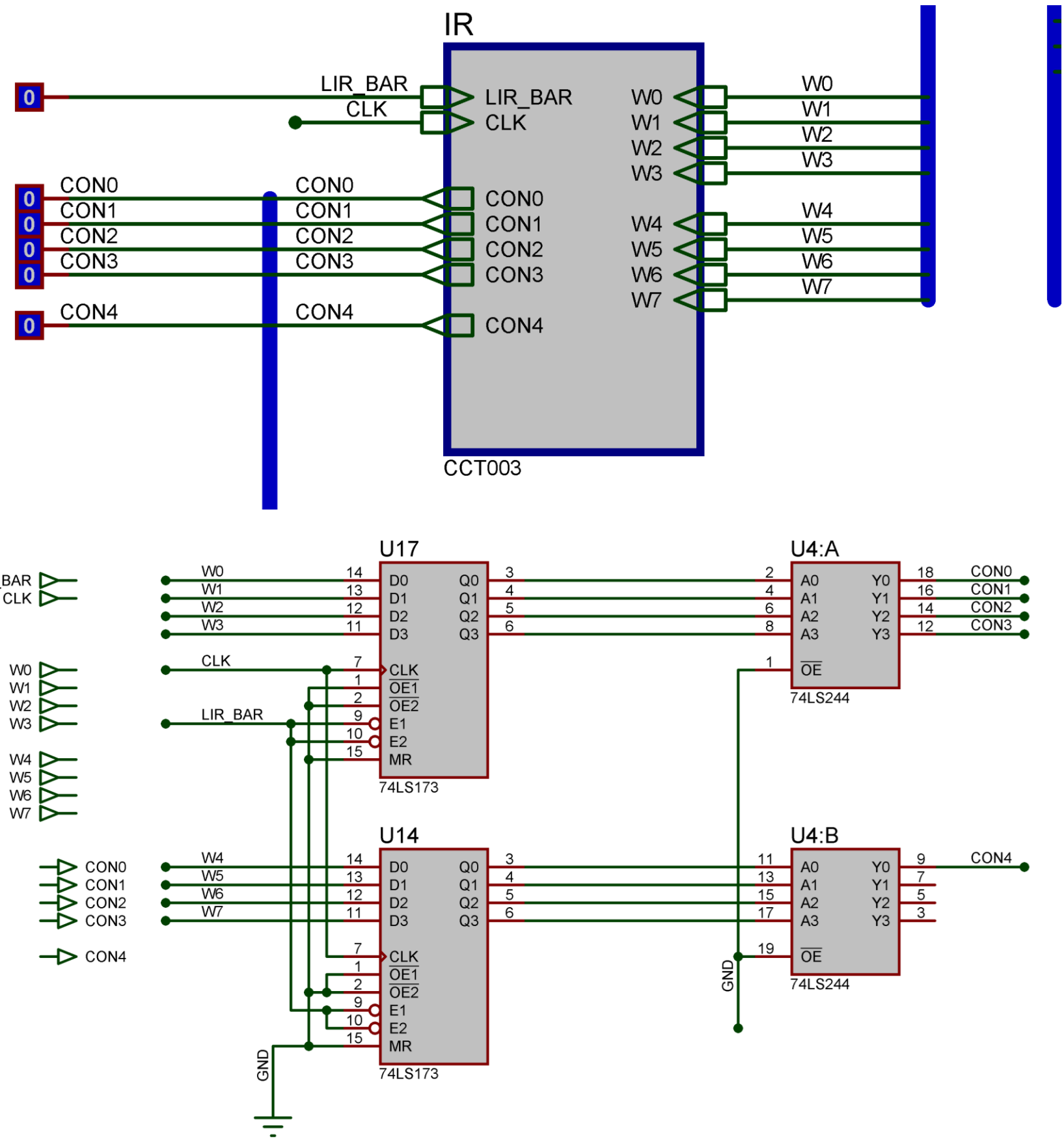

MAR
EM_BAR
LM_BAR
CLK
MO0
MO1
MO2
MO3
MO4
MO5
MO6
MO7
W0
W1
W2
W3
W4
W5
W6
W7
M0
M1
M2
M3
M4
M5
M6
M7
CCT008
U66:A
74LS244
GND
U6
74LS173
U8:A
U7
U8:B
U66:B

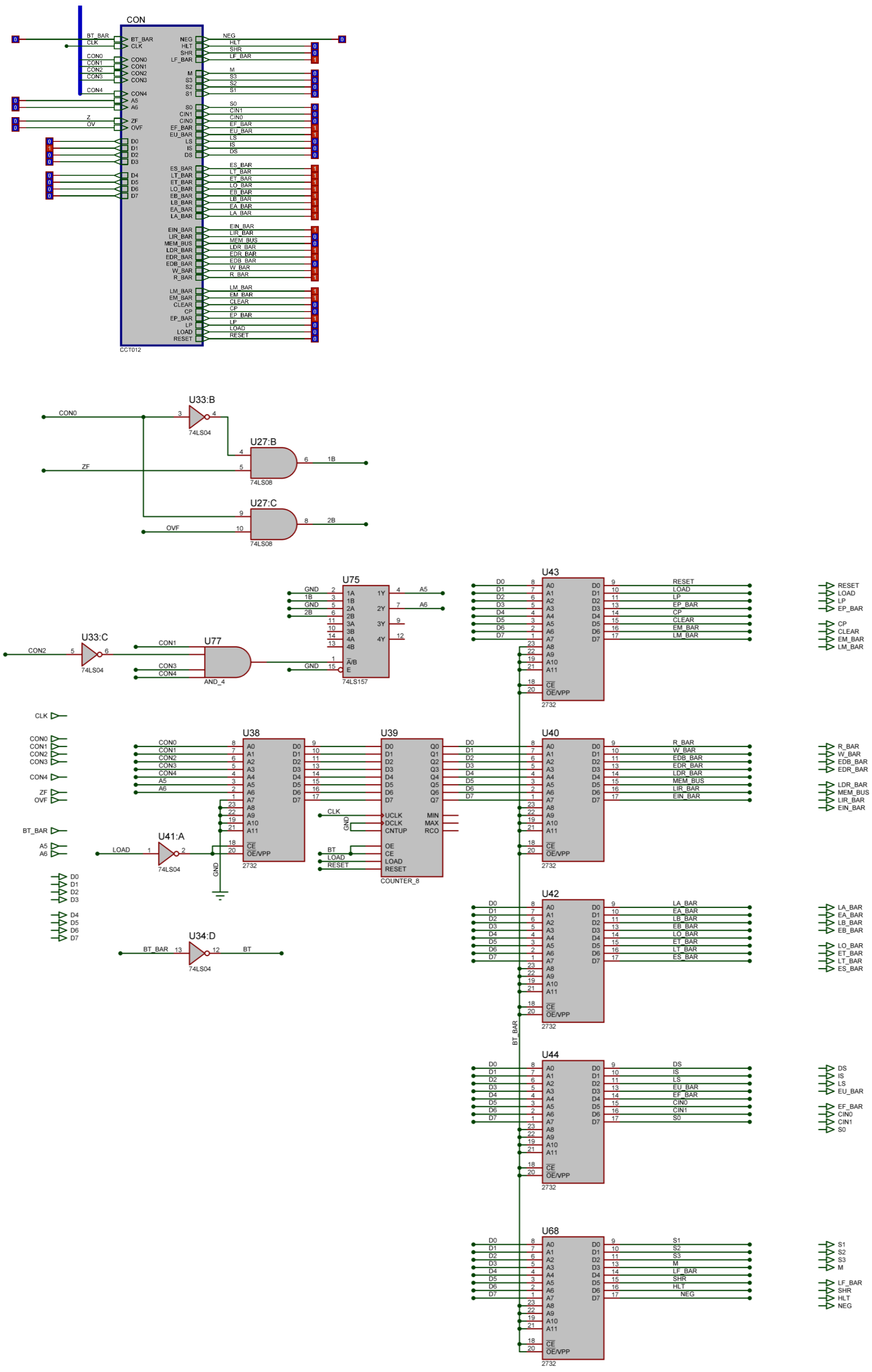

MEMORY
CLK
R_BAR
W_BAR
MO0
MO1
MO2
MO3
MO4
MO5
MO6
MO7
BT_BAR
HLT
RM0
RM1
RM2
RM3
RM4
RM5
RM6
RM7
LK
R0
R1
R2
R3
R4
R5
R6
R7
CCT014

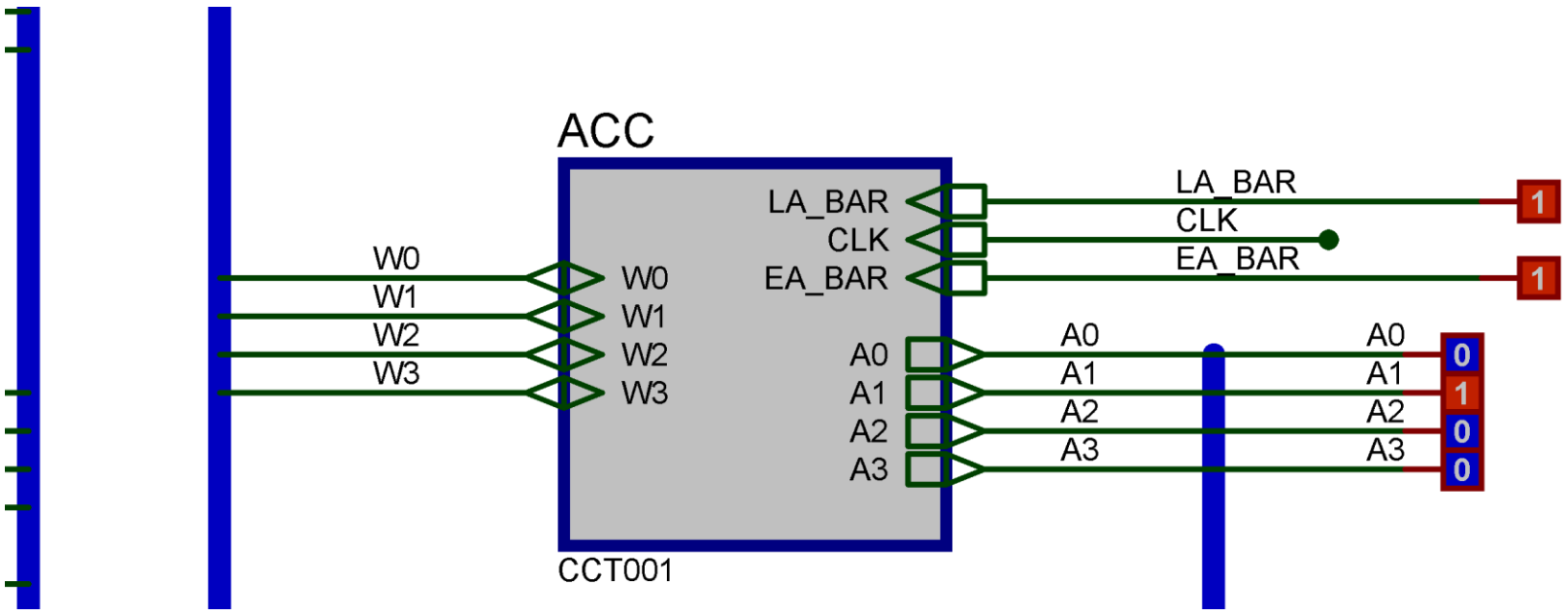
U55
COUNTER_4
U54
2732
U58
6116
U56:A
74LS08
U1
74LS157
U67:A
U61:A
74LS244
U13
COUNTER_8
U60
U62:A
U62:B
74HC21
U63:A
U65
74LS173
U57:C
74LS04
COMB_CLK
CP_ROM
CLR_ROM
BT_BAR
BT
GND

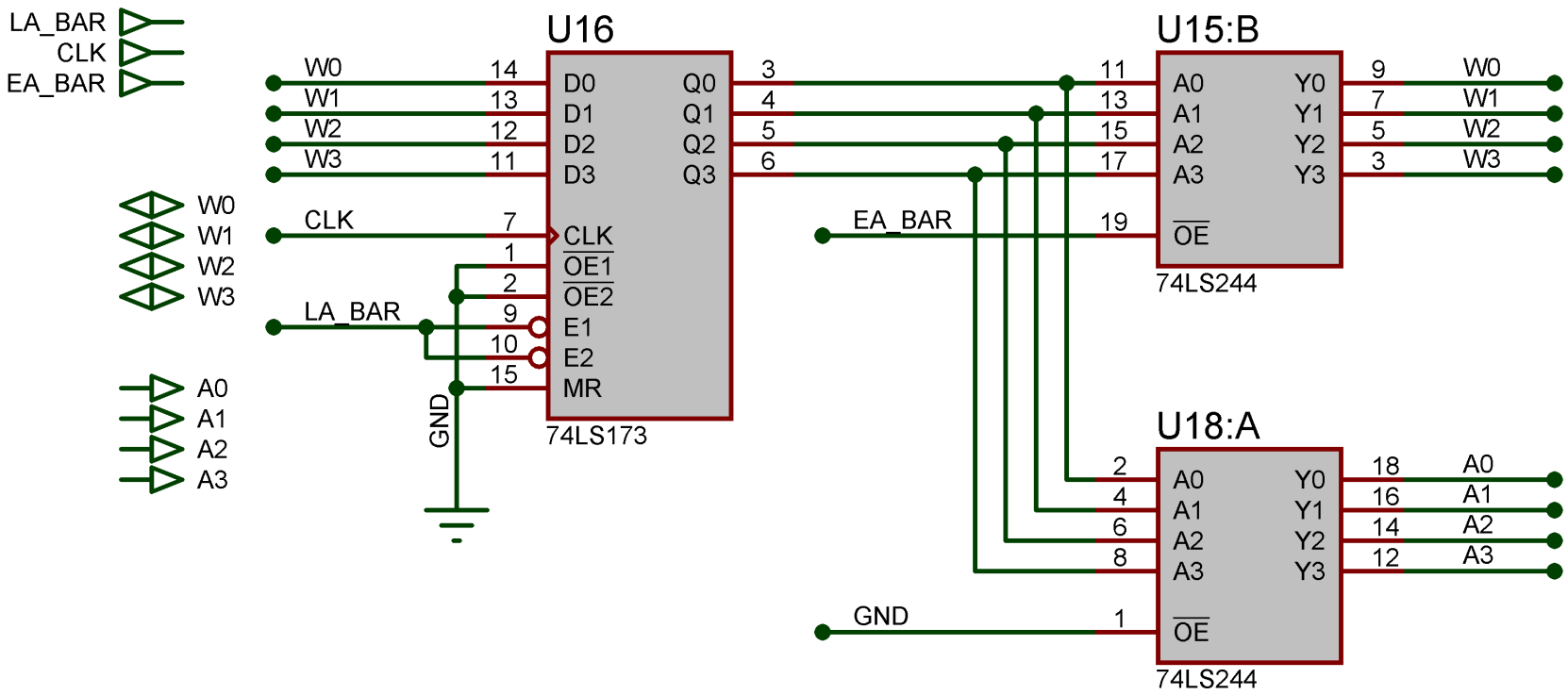

U64
74LS157
U61:B
U67:B
74LS244
W_BAR
GND

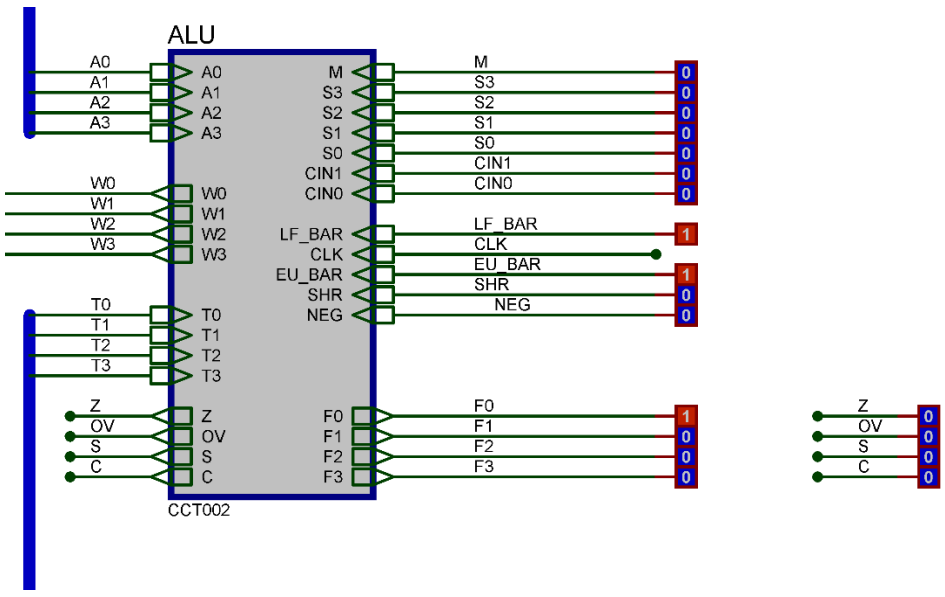

MDR
MEM_BUS
LDR_BAR
CLK
EDR_BAR
EDB_BAR
RM0
RM1
RM2
RM3
RM4
RM5
RM6
RM7
W0
W1
W2
W3
W4
W5
W6
W7
MDR0
MDR1
MDR2
MDR3
MDR4
MDR5
MDR6
MDR7
CCT009
U51
74LS157
U2
74LS173
U3
74LS173
U52
74LS157
U53:A
U53:B
U10:A
U10:B
U11:A
U11:B
74LS244
GND

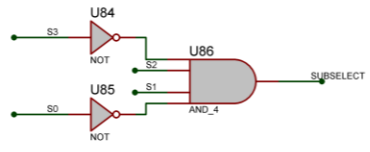

IR
LIR_BAR
CLK
CON0
CON1
CON2
CON3
CON4
W0
W1
W2
W3
W4
W5
W6
W7
CCT003
U17
U4:A
74LS173
74LS244
U14
U4:B
GND

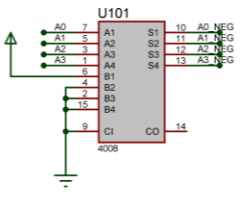

CON
BT_BAR
CLK
CON0
CON1
CON2
CON3
CON4
Z
OV
D0
D1
D2
D3
D4
D5
D6
D7
NEG
HLT
SHR
LF_BAR
M
S3
S2
S1
S0
CIN1
CIN0
EF_BAR
EU_BAR
LS
IS
DS
ES_BAR
LT_BAR
ET_BAR
LO_BAR
EB_BAR
LB_BAR
EA_BAR
LA_BAR
EIN_BAR
LIR_BAR
MEM_BUS
LDR_BAR
EDR_BAR
EDB_BAR
W_BAR
R_BAR
LM_BAR
EM_BAR
CLEAR
CP
EP_BAR
LP
LOAD
RESET
A5
A6
ZF
OVF
CCT012
U33:B
U27:B
U27:C
74LS04
74LS08
U75
74LS157
U33:C
U77
AND_4
U43
U38
U39
U40
U41:A
U42
U44
U68
U34:D
2732
COUNTER_8
CLK
LOAD
BT
GND
BT_BAR


ACC
W0
W1
W2
W3
W0
W1
W2
W3
LA_BAR
CLK
EA_BAR
A0
A1
A2
A3
LA_BAR
CLK
EA_BAR
1
1
A0
A1
A2
A3
A0
A1
A2
A3
0
1
0
0
CCT001

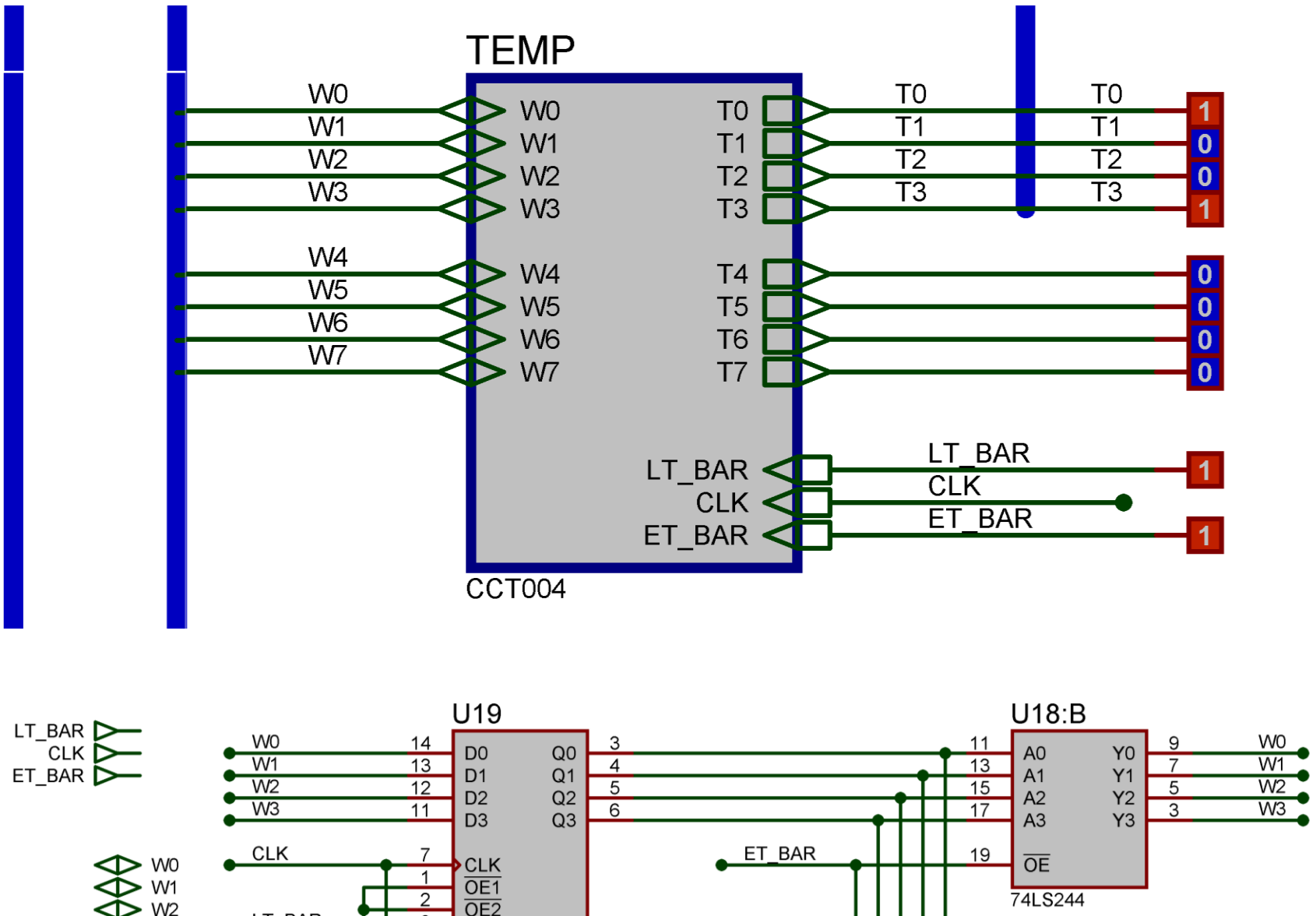

LA_BAR
CLK
EA_BAR
W0
W1
W2
W3
A0
A1
A2
A3
U16
W0
W1
W2
W3
CLK
LA_BAR
GND
14
13
12
11
7
1
2
9
10
15
D0
D1
D2
D3
CLK
OE1
OE2
E1
E2
MR
Q0
Q1
Q2
Q3
3
4
5
6
74LS173
U15:B
EA_BAR
11
13
15
17
19
A0
A1
A2
A3
OE
Y0
Y1
Y2
Y3
9
7
5
3
W0
W1
W2
W3
74LS244
U18:A
GND
2
4
6
8
1
A0
A1
A2
A3
OE
Y0
Y1
Y2
Y3
18
16
14
12
A0
A1
A2
A3
74LS244

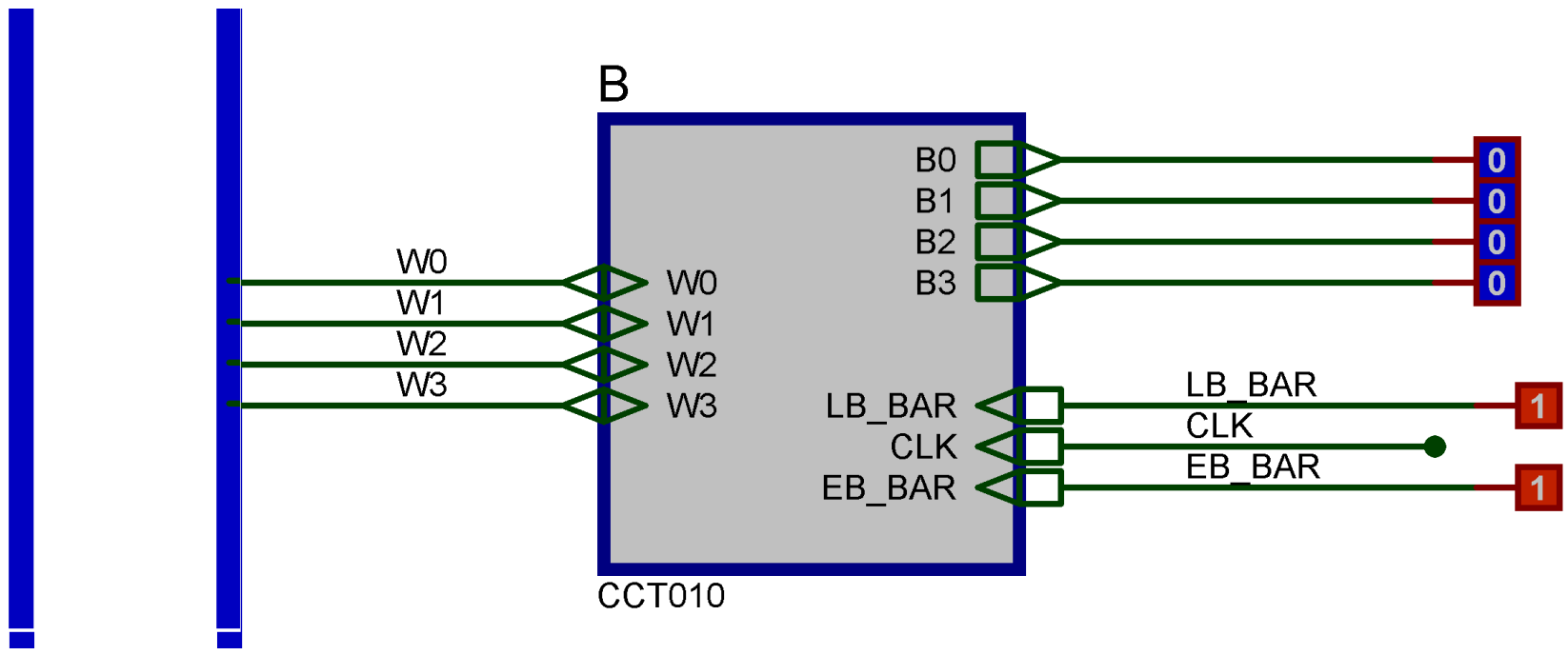

ALU
A0
A1
A2
A3
W0
W1
W2
W3
T0
T1
T2
T3
Z
OV
S
C
M
S3
S2
S1
S0
CIN1
CIN0
LF_BAR
CLK
EU_BAR
SHR
NEG
F0
F1
F2
F3
CCT002

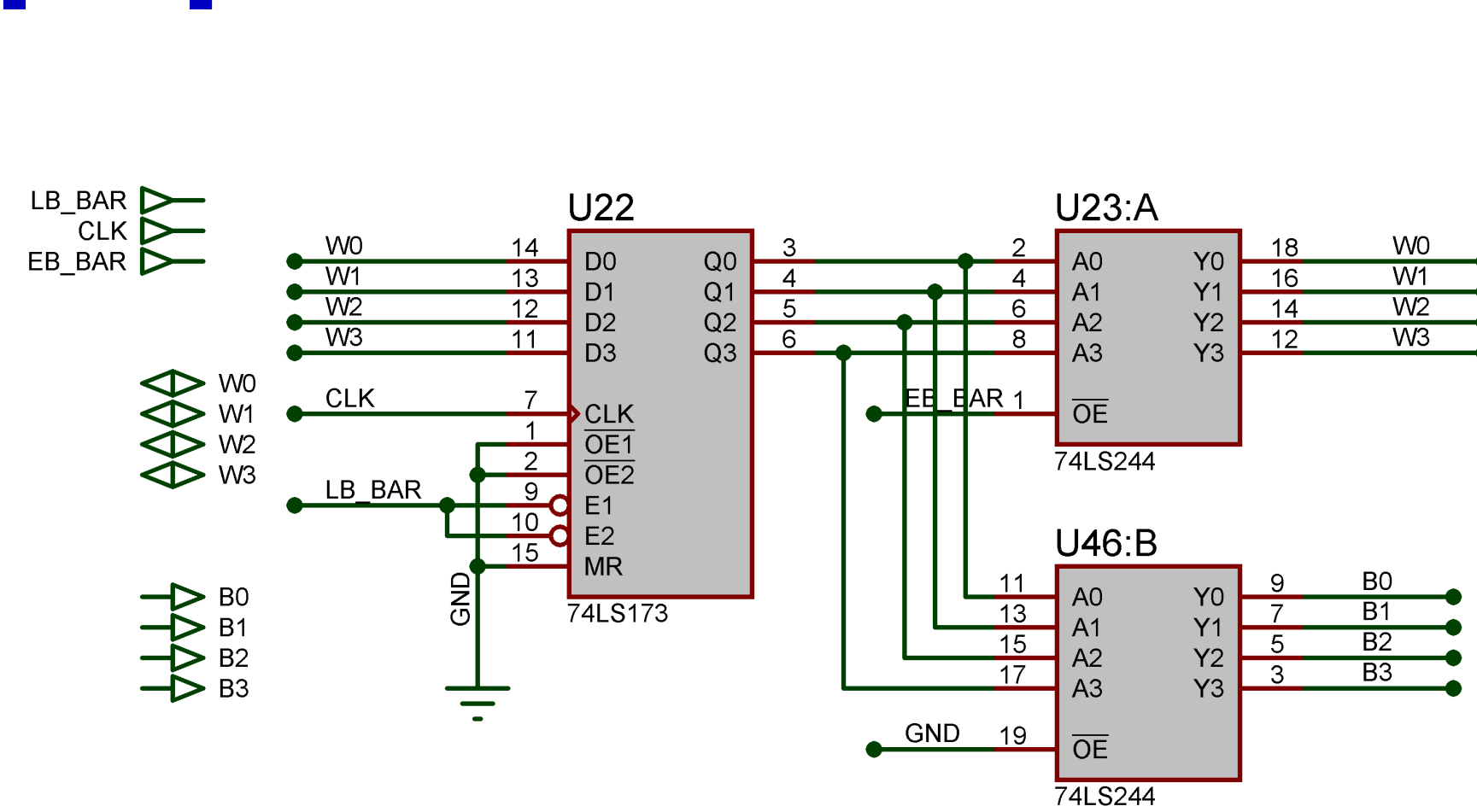

U84
NOT
U85
NOT
U86
AND_4
SUBSELECT

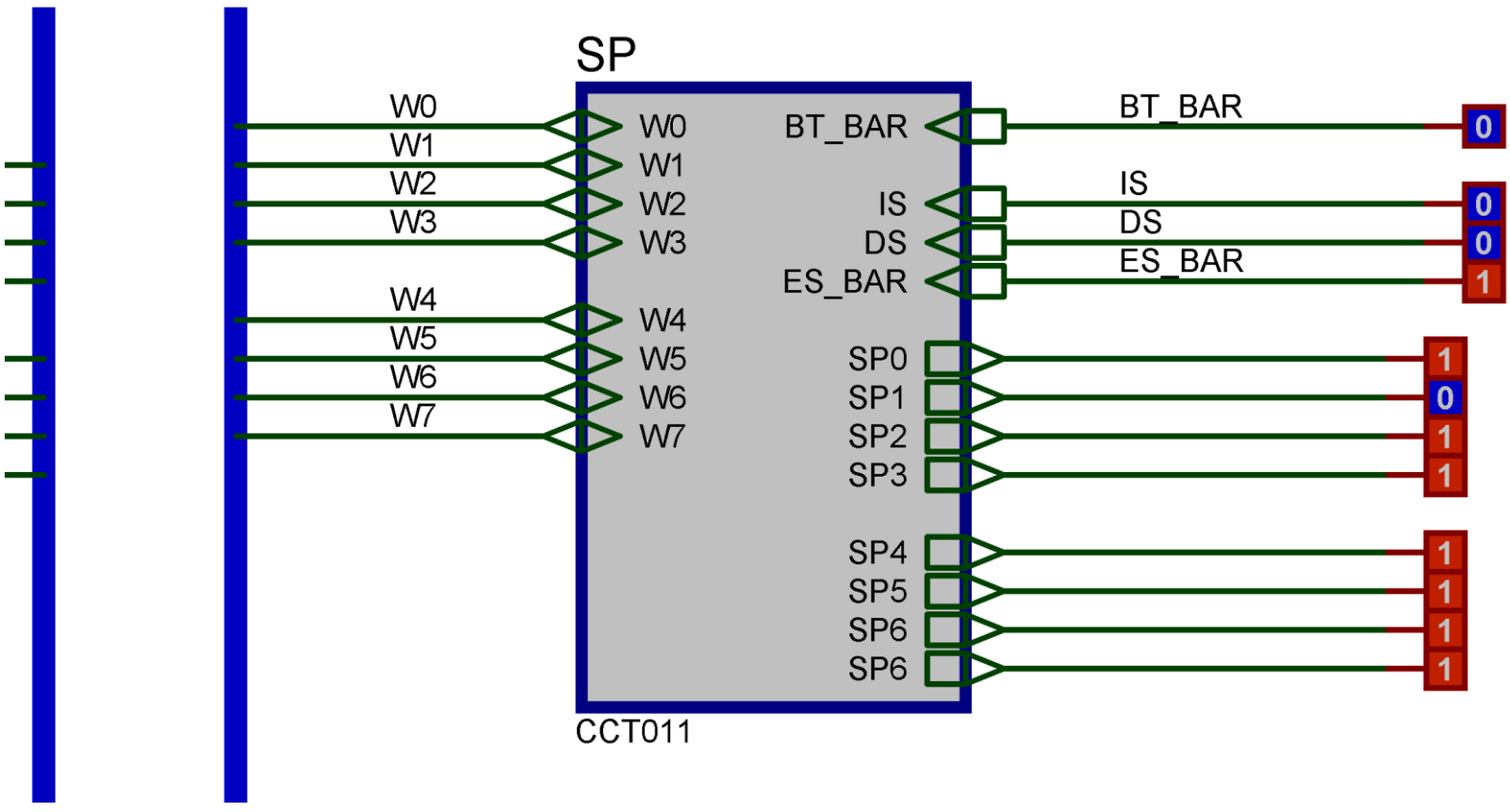

U101
4008

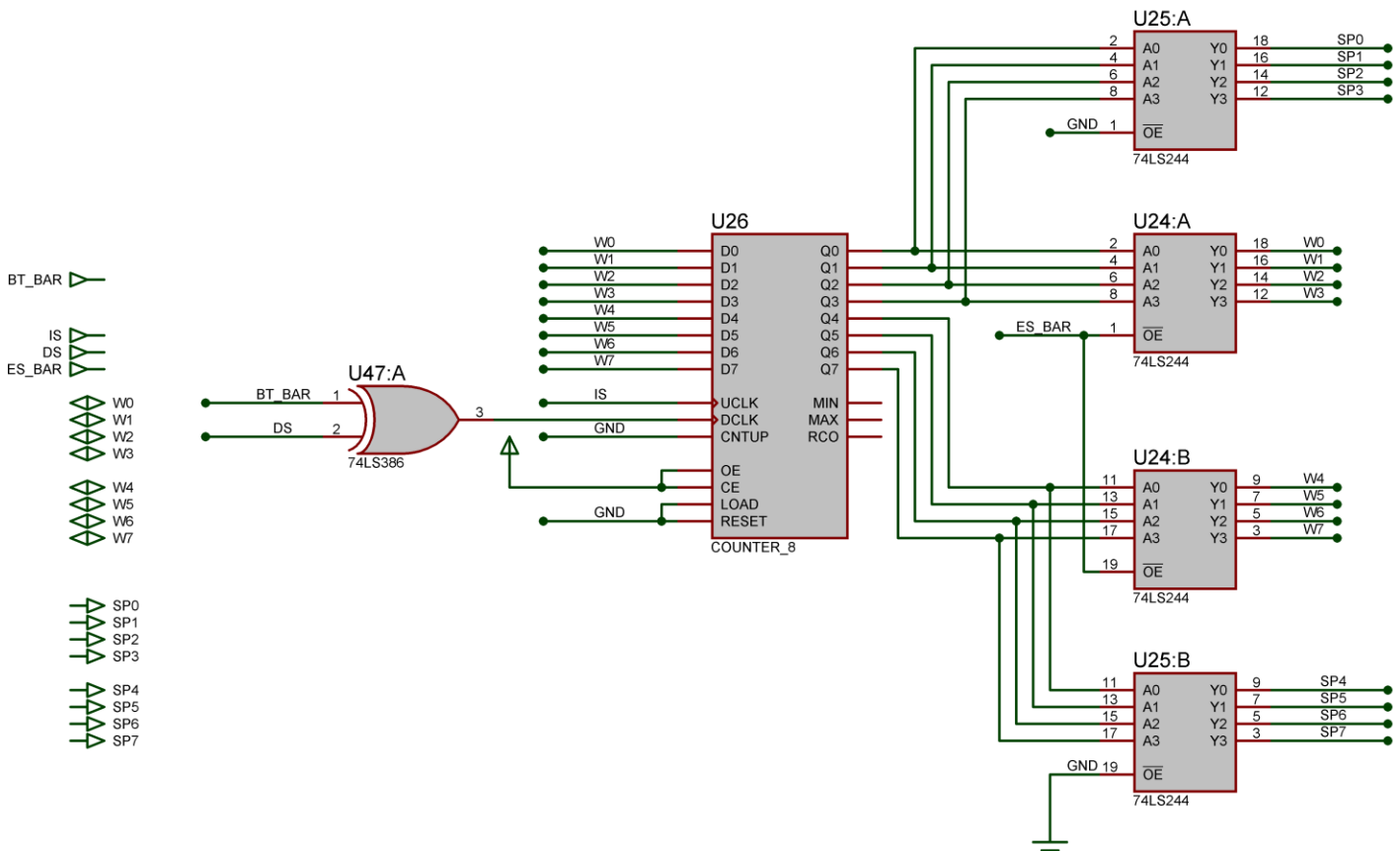
U72
74LS153
U73
74173
U69
AND_3
U70
AND_3
U71:A
74LS32
U35:B
74LS244
U35:A
74LS244
U95
74LS157
U74
74LS157
U81
74LS157
U28
74LS181
U30:C
U30:D
U30:E
U30:F
74LS04
U29:A
U29:B
U29:C
U29:D
U29:E
U29:F
U30:A
U30:B
U27:D
U32:A
U32:D
74LS08
U76
74LS173
U48:A
74LS244
U102
74LS157
U49:A
U49:B
U49:C
U50
AND_3
U56:B
U56:C
74LS08
U59
OR_3
U78
AND_5
U79:A
U80:A
U80:B
U80:C
U83
NOT
U82
4008
ALU

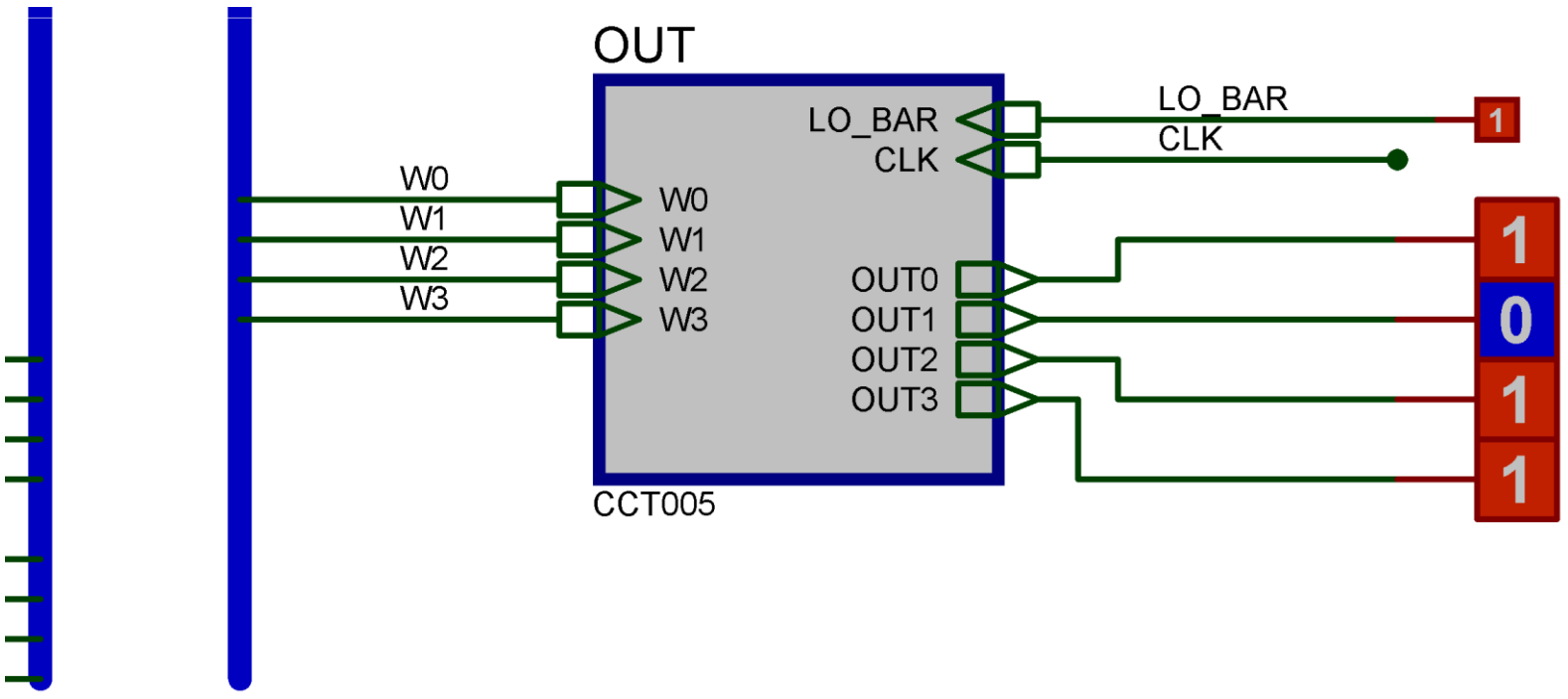

TEMP
W0
W1
W2
W3
W4
W5
W6
W7
T0
T1
T2
T3
LT_BAR
CLK
ET_BAR
CCT004
U19
74LS173
U20
74LS173
U18:B
74LS244
U21:A
74LS244
U21:B
74LS244
U46:A
74LS244
GND

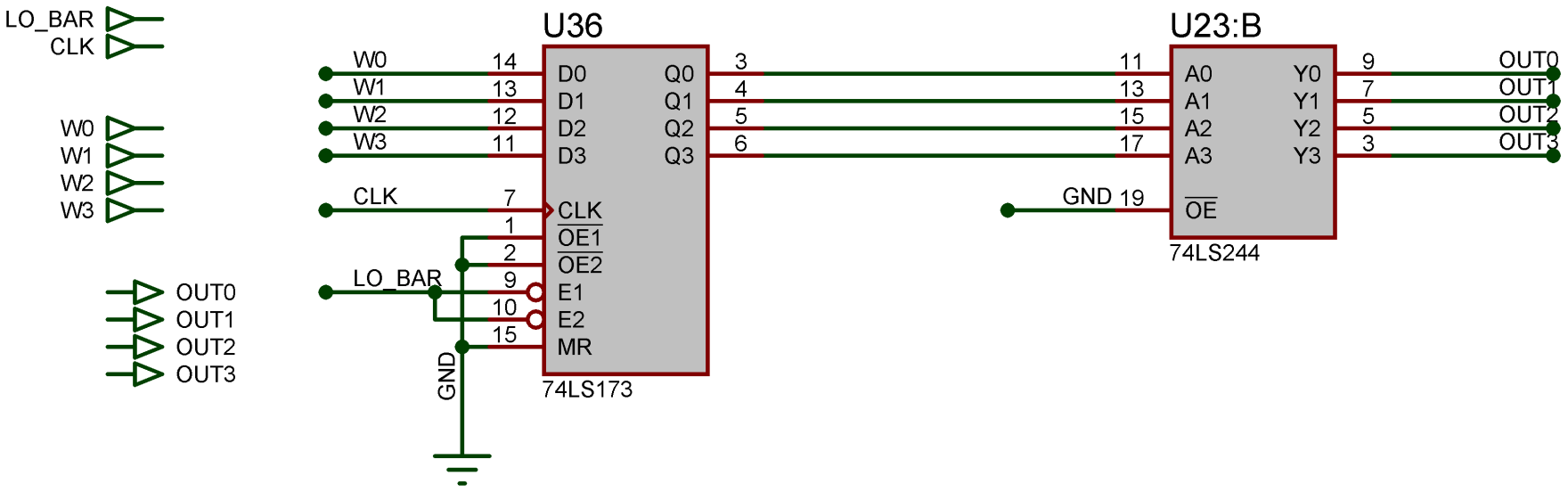

B
W0
W1
W2
W3
W0
W1
W2
W3
B0
B1
B2
B3
LB_BAR
CLK
EB_BAR
CCT010


LB_BAR
CLK
EB_BAR
W0
W1
W2
W3
B0
B1
B2
B3
U22
W0
W1
W2
W3
CLK
LB_BAR
GND
D0
D1
D2
D3
CLK
OE1
OE2
E1
E2
MR
Q0
Q1
Q2
Q3
74LS173
U23:A
EB_BAR
A0
A1
A2
A3
OE
Y0
Y1
Y2
Y3
74LS244
U46:B
GND
A0
A1
A2
A3
OE
Y0
Y1
Y2
Y3
74LS244


SP
W0
W1
W2
W3
W4
W5
W6
W7
BT_BAR
IS
DS
ES_BAR
SP0
SP1
SP2
SP3
SP4
SP5
SP6
SP6
CCT011


BT_BAR
IS
DS
ES_BAR
W0
W1
W2
W3
W4
W5
W6
W7
SP0
SP1
SP2
SP3
SP4
SP5
SP6
SP7
U47:A
BT_BAR
DS
74LS386
U26
D0
D1
D2
D3
D4
D5
D6
D7
UCLK
DCLK
CNTUP
OE
CE
LOAD
RESET
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
MIN
MAX
RCO
COUNTER_8
U25:A
U24:A
U24:B
U25:B
A0
A1
A2
A3
OE
Y0
Y1
Y2
Y3
74LS244
GND
ES_BAR


OUT
LO_BAR
CLK
W0
W1
W2
W3
OUT0
OUT1
OUT2
OUT3
CCT005
LO_BAR
CLK
1
1
0
1
1


LO_BAR
CLK
W0
W1
W2
W3
OUT0
OUT1
OUT2
OUT3
U36
74LS173
U23:B
74LS244
GND
CLK
LO_BAR
OE1
OE2
E1
E2
MR
D0
D1
D2
D3
Q0
Q1
Q2
Q3
A0
A1
A2
A3
Y0
Y1
Y2
Y3
OE

LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	FETCH	-		1
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				2
EDB_BAR, LIR_BAR	10	18	FF	9B	C8	IR ← MDR				3
LOAD	10	18	FF	DF	CA	LOAD from IR				4
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	LDA	0	4	5
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				6
LM_BAR, EDB_BAR, EM_BAR	10	18	FF	DB	8	MAR ← MDR				7
LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	88	MDR ← RAM[MAR]				8
LA_BAR, EDB_BAR, RESET	10	18	FE	DB	C9	ACC ← MDR				9
HALT	50	18	FF	DF	C8	HALT	HALT	F	9	10
LA_BAR, EIN_BAR, RESET	10	18	FE	5F	C9	ACC ← input_port	IN	2	A	11
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	STA	1	B	12
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				13
LM_BAR, EDB_BAR, EM_BAR	10	18	FF	DB	8	MAR ← MDR				14
LDR_BAR, EA_BAR, MEM_BUS, EM_BAR	10	18	FD	EF	88	MDR ← ACC				15
EDR_BAR, EM_BAR	10	18	FF	D7	88	RAM[MAR] ← MDR				16
W_BAR, EDR_BAR, EM_BAR	10	18	FF	D5	88					17
EDR_BAR, EM_BAR	10	18	FF	D7	88					18
R_BAR, RESET, EM_BAR	10	18	FF	DE	89					19
LO_BAR, EA_BAR, RESET	10	18	ED	DF	C9	output_port ← ACC	OUT	3	13	20
LB_BAR, EA_BAR, RESET	10	18	F9	DF	C8	B ← ACC	MOV B, A	4	14	21
LA_BAR, EB_BAR, RESET	10	18	F6	DF	C9	ACC ← B	MOV A, B	5	15	22
SHR,M,S3,S2,S1,S0,EU_BAR,LA_BAR, RESET	2F	90	FE	DF	C9	CF←ACC[LSB], ACC>>1	SHR	6	16	23
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	MOV A, immd	7	17	24
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				25
LA_BAR, EDB_BAR, RESET	10	18	FE	DB	C9	ACC ← MDR				26
NOP, RESET	10	18	FF	DF	C9	NOP	NOP	8	1A	27
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	JMP	9	1B	28
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				29
LP, EDB_BAR	10	18	FF	DB	CC	PC ← MDR				30
CP, LP, RESET	10	18	FF	DF	DD					31
LT_BAR, EB_BAR, S3, S0	14	98	B7	DF	C8	TEMP ← B	ADD B	A	1F	32
S3, S0	14	98	FF	DF	C8	ACC ← ACC + TEMP				33
LA_BAR, EU_BAR, S3, S0, LF_BAR, RESET	4	90	FE	DF	C9					34
LT_BAR, EB_BAR, S3, S0, CIN0	14	B8	B7	DF	C8	TEMP ← B	ADC B	B	22	35
S3, S0, CIN0	14	B8	FF	DF	C8	ACC ← ACC + TEMP + C				36
LA_BAR, EU_BAR, S3, S0, CIN0, LF_BAR, RESET	4	B0	FE	DF	C9					37
LT_BAR, EB_BAR, S2, S1, CIN1	13	58	B7	DF	C8	TEMP ← B	SUB B	C	25	38
S2, S1, CIN1	13	58	FF	DF	C8	ACC ← ACC - TEMP				39
LA_BAR, EU_BAR, S2, S1, CIN1, LF_BAR, RESET	3	50	FE	DF	C9					40
LT_BAR, EB_BAR, S2, S1, CIN1, CIN0	13	78	B7	DF	C8	TEMP ← B	SBB B	D	28	41
S2, S1, CIN1, CIN0	13	78	FF	DF	C8	ACC ← ACC - TEMP - BO				42
LA_BAR, EU_BAR, S2, S1, CIN1, CIN0, LF_BAR, RESET	3	70	FE	DF	C9					43
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	ADD Addr	E	2B	44
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				45
LM_BAR, EDB_BAR, EM_BAR	10	18	FF	DB	8	MAR ← MDR				46
LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	88	MDR ← RAM[MAR]				47
LT_BAR, EDB_BAR	10	18	BF	DB	C8	TEMP ← MDR				48
S3, S0	14	98	FF	DF	C8	ACC ← ACC + TEMP				49
LA_BAR, EU_BAR, S3, S0, LF_BAR, RESET	4	90	FE	DF	C9					50
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	SUB IMMD	10	32	51
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				52
LT_BAR, EDB_BAR, S2, S1, CIN1	13	58	BF	DB	C8	TEMP ← MDR				53
S2, S1, CIN1	13	58	FF	DF	C8	ACC ← ACC - TEMP				54
LA_BAR, EU_BAR, S2, S1, CIN1, LF_BAR, RESET	3	50	FE	DF	C9					55
LT_BAR, EB_BAR, S2, S1, CIN1	13	58	B7	DF	C8	TEMP ← B	CMP B	11	37	56
S2, S1, CIN1	13	58	FF	DF	C8	ACC - TEMP				57
S2, S1, CIN1, LF_BAR, RESET	3	58	FF	DF	C9					58
LA_BAR, EU_BAR, M	8	10	FE	DF	C8	ACC ← ACC'	NEG	12	3A	59
LA_BAR, EU_BAR, CIN1,NEG, RESET	80	50	FE	DF	C9	ACC ← ACC + 1				60
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	XOR IMMD	13	3C	61
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				62
LT_BAR, EDB_BAR, S3, S0, M	1C	98	BF	DB	C8	TEMP ← MDR				63
LA_BAR, EU_BAR, M, S3, S0, RESET	1C	90	FE	DF	C9	ACC ← ACC ⊕ TEMP				64

LT_BAR, EB_BAR	10	18	B7	DF	C8	TEMP ← B	OR B	14	40	65
LA_BAR, EU_BAR, M, S3, S1, S0, RESET	1D	90	FE	DF	C9	ACC ← ACC | TEMP				66
DS, LDR_BAR, EA_BAR, MEM_BUS, EM_BAR	10	19	FD	EF	88	SP ← SP - 1, MDR ← ACC	PUSH	15	42	67
LM_BAR, ES_BAR, EM_BAR	10	18	7F	DF	8	MAR ← SP				68
EDR_BAR, EM_BAR	10	18	FF	D7	88	RAM[MAR] ← MDR				69
W_BAR, EDR_BAR, EM_BAR	10	18	FF	D5	88					70
EDR_BAR, EM_BAR	10	18	FF	D7	88					71
R_BAR, RESET, EM_BAR	10	18	FF	DE	89					72
LM_BAR, ES_BAR, EM_BAR	10	18	7F	DF	8	MAR ← SP	POP	16	48	73
LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	88	MDR ← RAM[MAR]				74
LA_BAR, EDB_BAR, IS, RESET	10	1A	FE	DB	C9	ACC ← MDR, SP ← SP + 1				75
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	Calls a subroutine	17	4B	76
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				77
LT_BAR, EDB_BAR, DS	10	19	BF	DB	C8	TEMP ← MDR, SP ← SP - 1				78
LM_BAR, ES_BAR	10	18	7F	DF	48	MAR ← SP				79
LDR_BAR, EP_BAR, MEM_BUS	10	18	FF	EF	C0	MDR ← PC				80
EDR_BAR, EM_BAR	10	18	FF	D7	88	RAM[MAR] ← MDR				81
W_BAR, EDR_BAR, EM_BAR	10	18	FF	D5	88					82
EDR_BAR, EM_BAR	10	18	FF	D7	88					83
LP, ET_BAR	10	18	DF	DF	CC	PC ← TEMP				84
CP, LP, RESET	10	18	FF	DF	DD					85
LM_BAR, ES_BAR	10	18	7F	DF	48	MAR ← SP	eturns from current subroutir	18	55	86
LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	88	MDR ← RAM[MAR]				87
LP, EDB_BAR, IS	10	1A	FF	DB	CC	PC ← MDR, SP ← SP + 1				88
CP, LP, RESET	10	18	FF	DF	DD					89

CIN1,S3,S2,EU_BAR,LA_BAR,RESET	6	50	FE	DF	C9	A3←ACC[MSB],ACC<<1	SHL	19	59	90
CP,NOP, RESET	10	18	FF	DF	D9	PC← PC+1,NOP	JE-NOT	1A	5A	91
CP,NOP, RESET	10	18	FF	DF	D9	PC← PC+1,NOP	JO-NOT	1B	5B	92
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	JE	3A	5C	93
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				94
LP, EDB_BAR	10	18	FF	DB	CC	PC ← MDR				95
CP, LP, RESET	10	18	FF	DF	DD					96
LM_BAR, EP_BAR, EM_BAR	10	18	FF	DF	0	MAR ← PC	JO	5B	60	97
CP, LDR_BAR, R_BAR, EM_BAR	10	18	FF	CE	98	PC← PC+1, MDR ← RAM[MAR]				98
LP, EDB_BAR	10	18	FF	DB	CC	PC ← MDR				99
CP, LP, RESET	10	18	FF	DF	DD					100