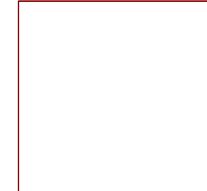


1 2 3 4 5 6

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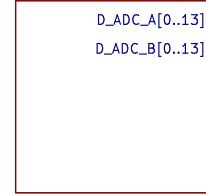
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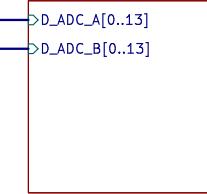
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fpga



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B

B

mcu



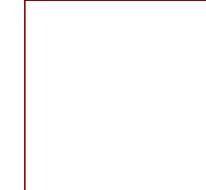
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dac



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C

C

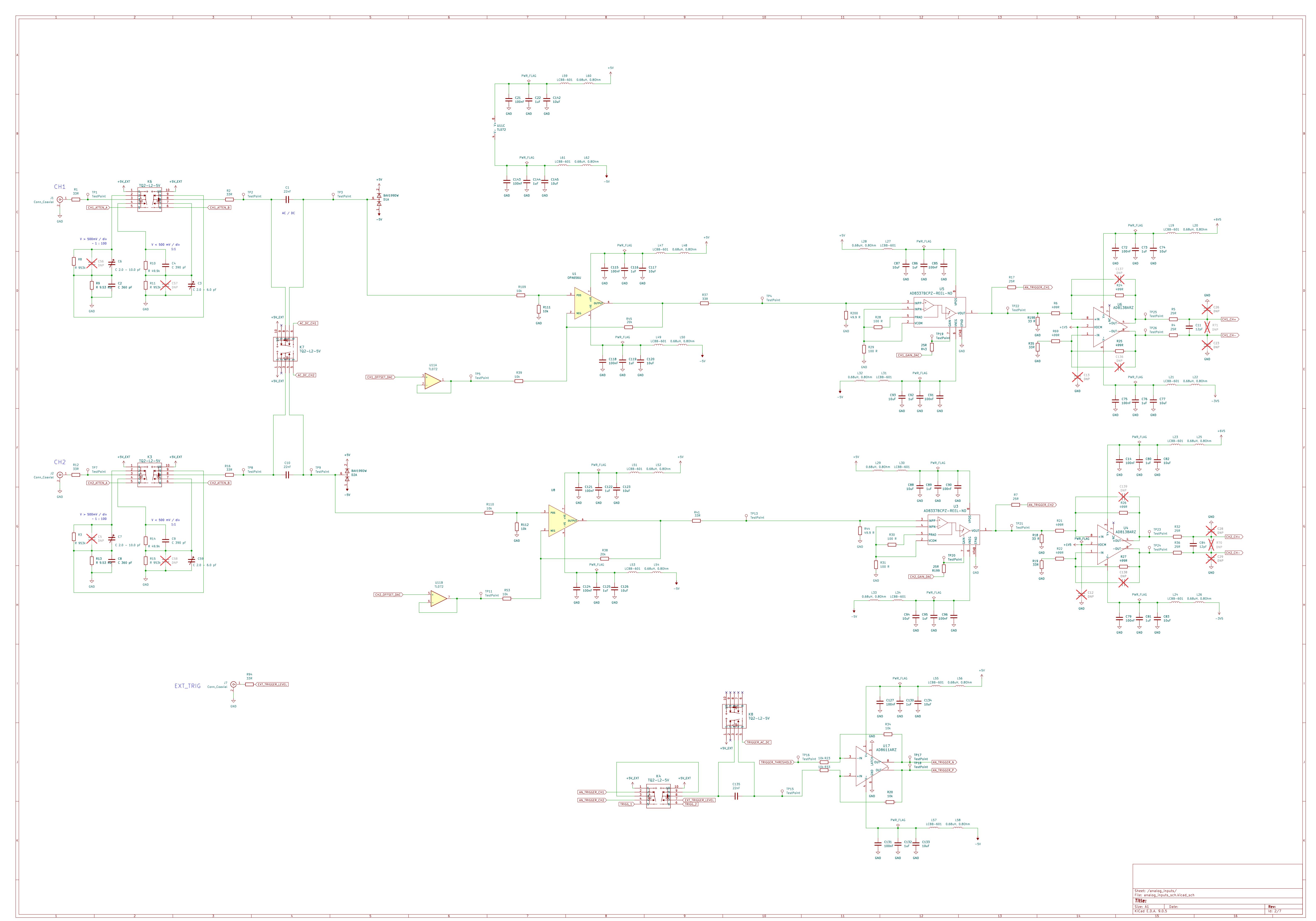
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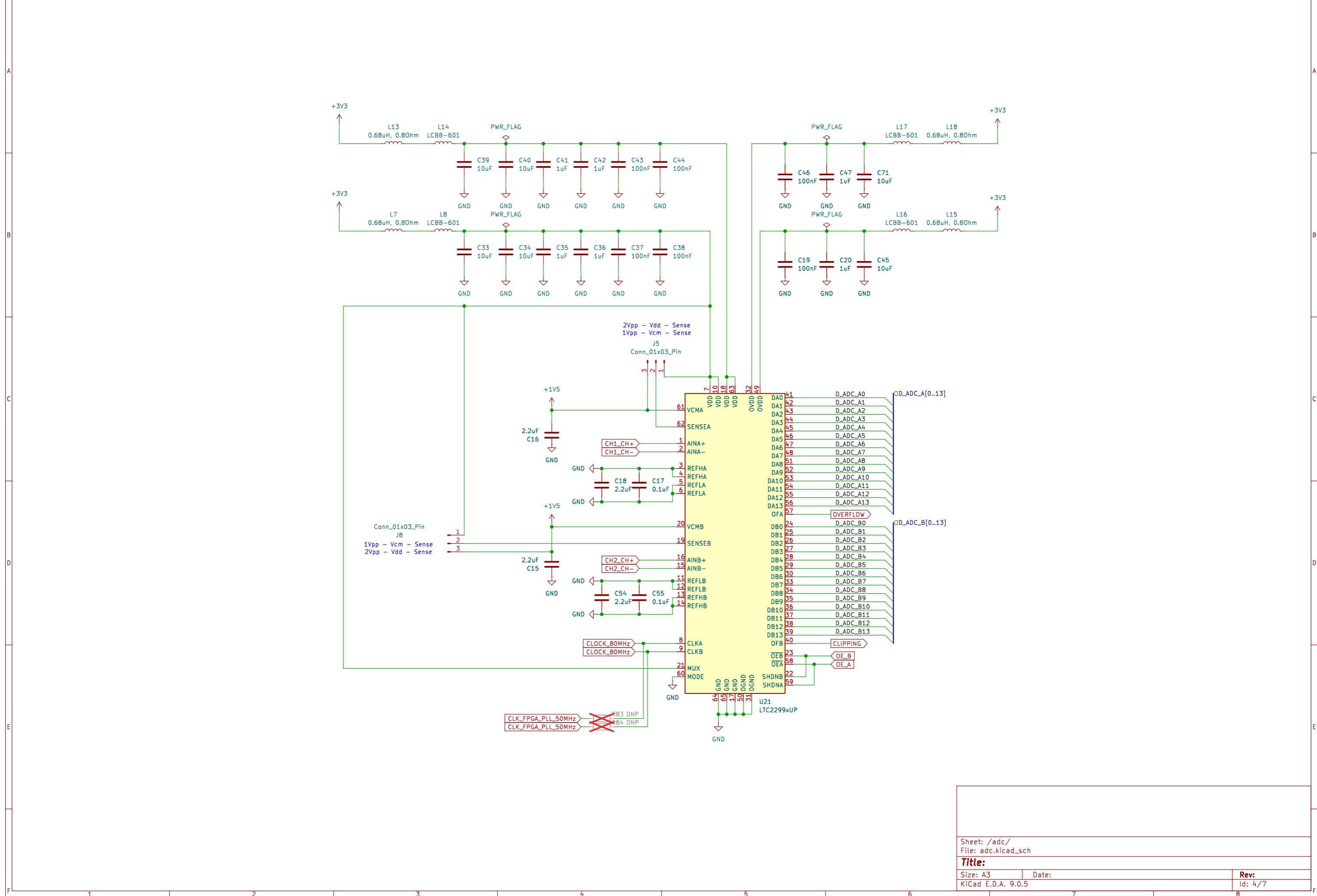
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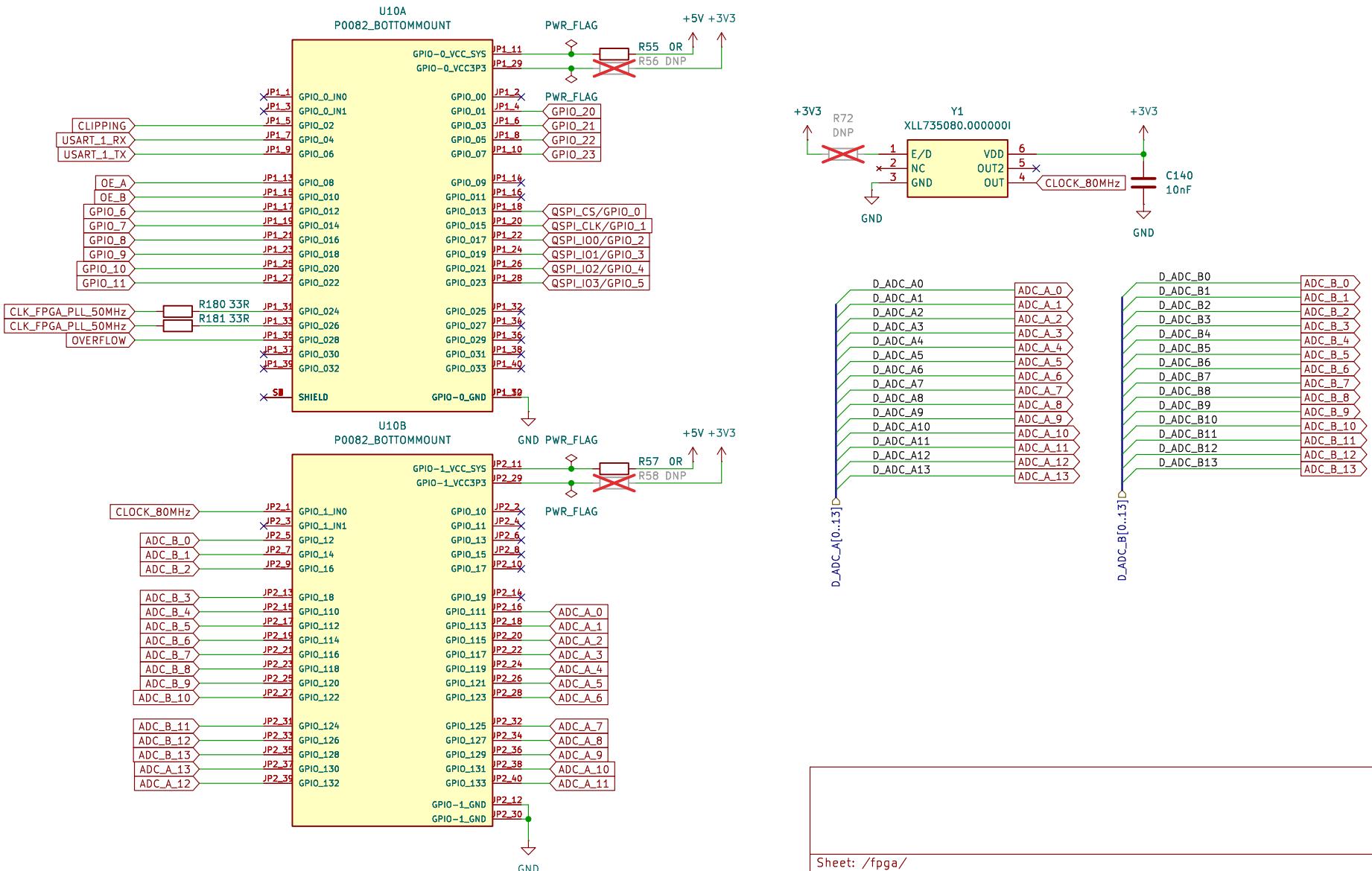
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TODO: ledy FPGA



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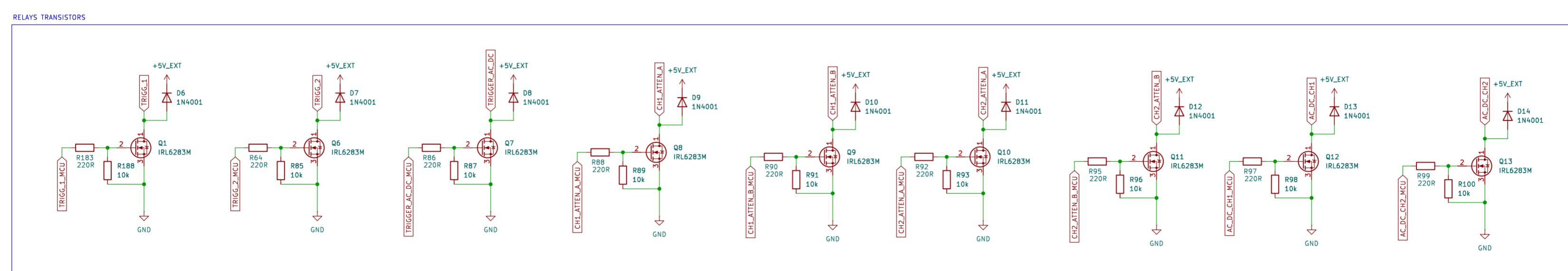
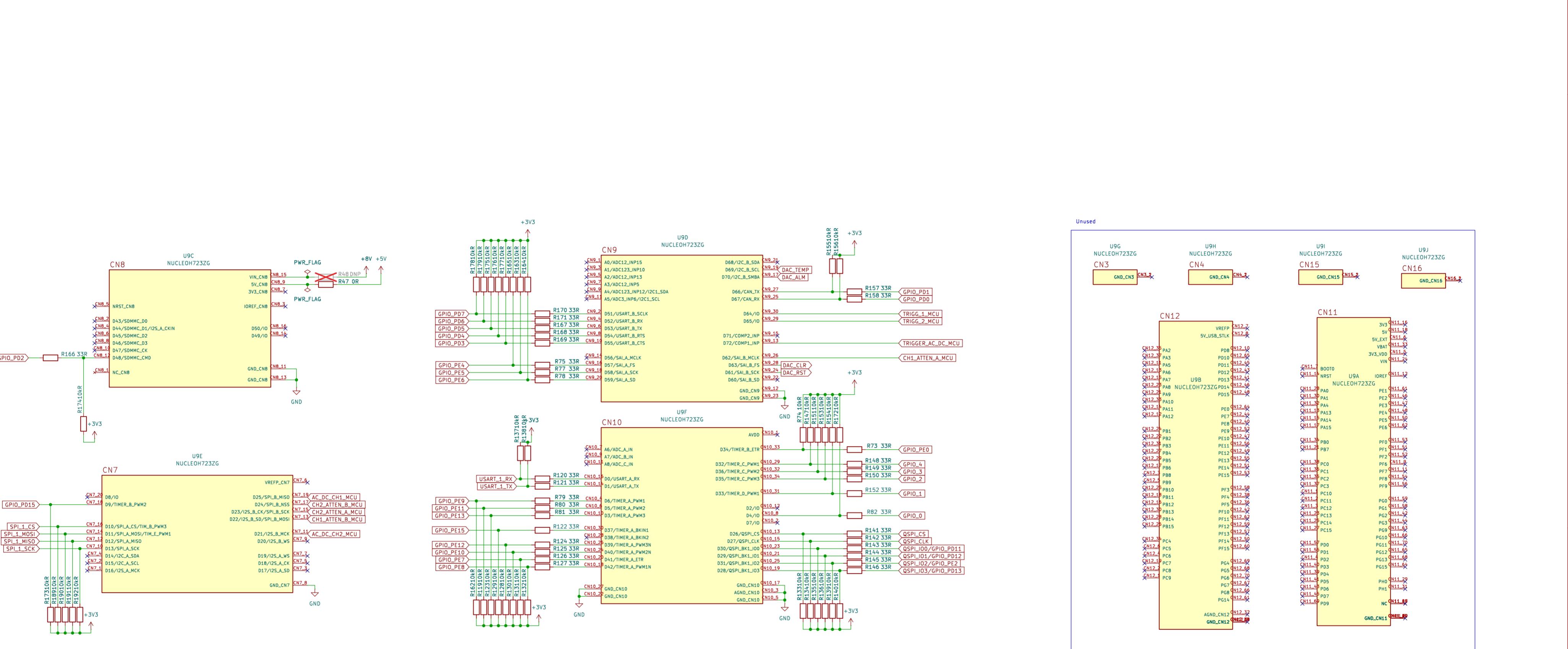
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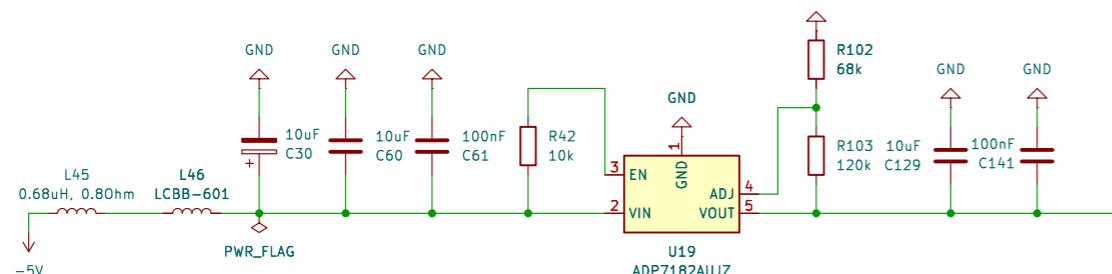
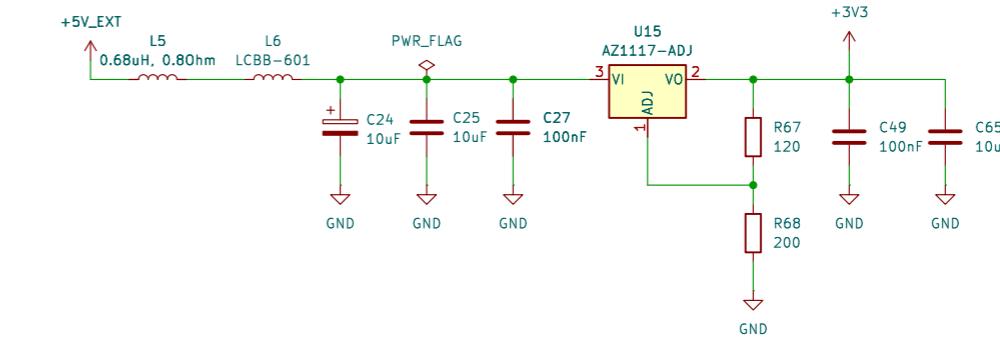
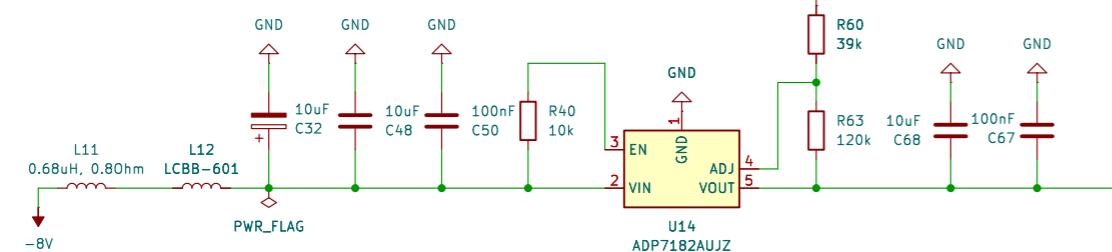
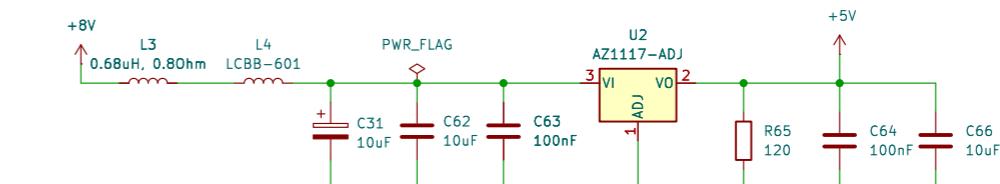
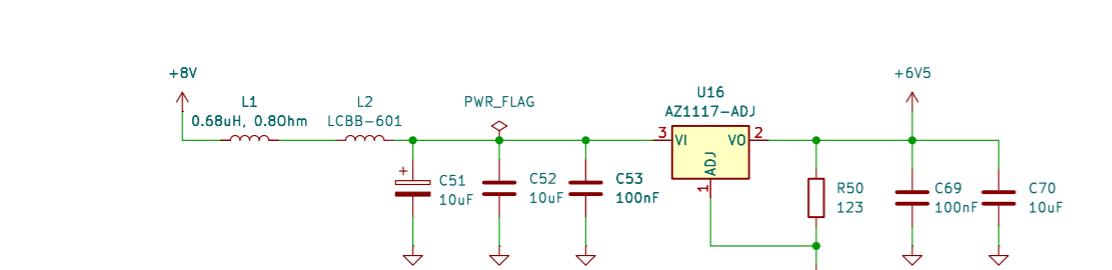
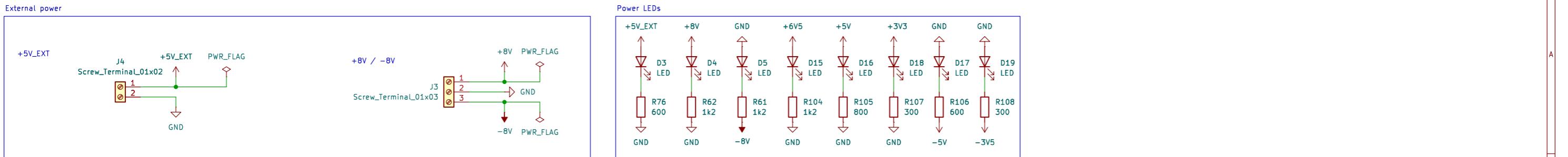
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G

H



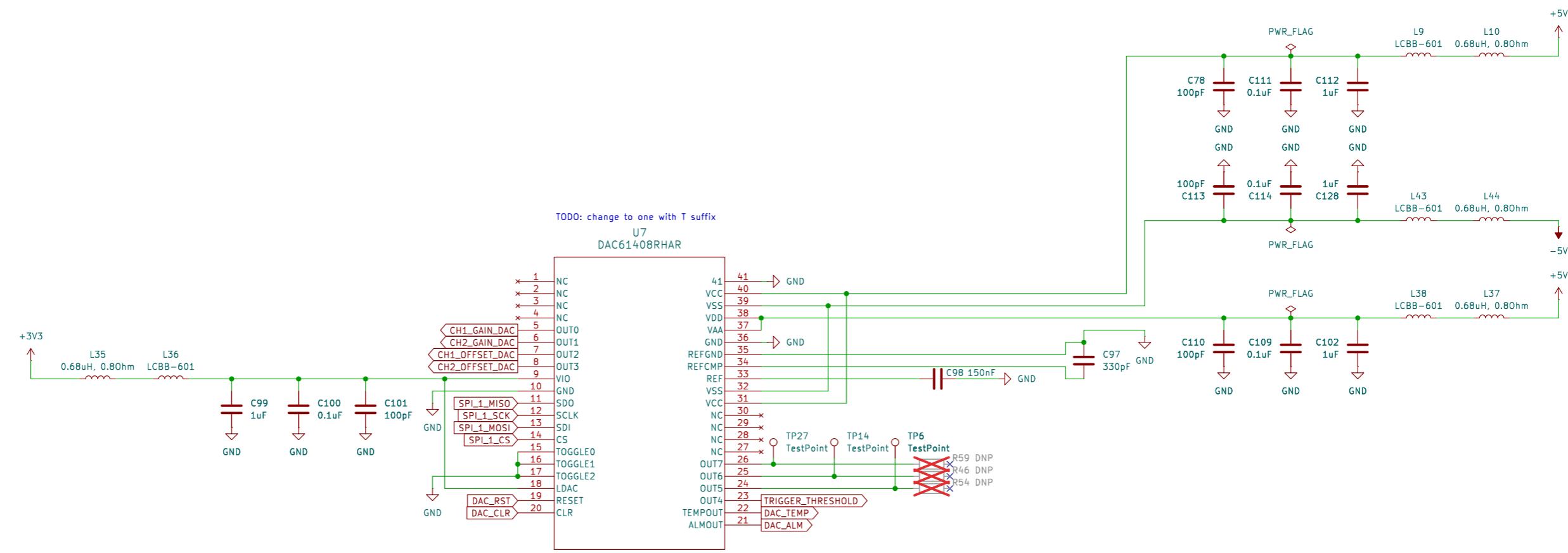


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Rev: Id: 12/7