LLVM for CORE-V

PPL presentation

Zbigniew Chamski zbigniew.chamski@invia.fr

Jean-Roch Coulon jean-roch.coulon@invia.fr

www.openhwgroup.org

Context

Preparation of “LLVM” project launch

- PPL gate planned at TG meeting 26 Oct 2020
- All TGs potentially involved in project (albeit at various stages)

- Historical compiler toolchain for RISC-V: GCC + GNU binutils
  - Well established
  - Reference for HW design and verification
  - Licensing: copyleft (full access to source code for all users)
- A rising contender: Clang/LLVM
  - New technologies with new potential (both technical and for collaborations)
  - Strict compliance to RISC-V specifications
  - Licensing: Apache (interesting for industrial users)

The challenge

Cater to the needs of industrial members

- Business ecosystem
- IP protection
- Ease of innovation

- Clang/LLVM key features
  - Modular design
  - Flexible structure (e.g., optimizations can be rearranged at each run)
  - Well known and widely taught in academic world (enables potential collaborations)
  - RISC-V support strongly compliant with RISC-V specifications
  - Apache license, more permissive than GCC's GPL
  - Base of many industrial solutions

Expectations

- Thales: seamless design, verification and deployment of CV*A6
  - **upstream open source support** of generic CV*A6 features
  - industry-strength support for adding **vendor-specific ISA extensions**
  - Ease of adding **new passes/features**
  - Attract new collaborations around compilation and CV*A6
    - Lower the **entry threshold** for newcomers
- Embecosm: a sustainable open source compiler platform
  - High added value projects
  - Industry-strength base with upstreamed/mutualized maintenance
- Additional partners: ***feel free to join!***