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Digital Circuits Project

Synchronous SAR Logic

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Overview

The Successive Approximation Register (SAR) architecture is widely used in modern Analog-to-Digital Converters (ADCs) due to its excellent balance of resolution, power efficiency, and conversion speed. The core of a SAR ADC is its digital control logic, which executes a binary search to determine the digital output code corresponding to an analog input. This project focuses on the design and verification of a fully synchronous, parameterized N-bit SAR logic controller implemented in Verilog. The controller resolves exactly one bit per clock cycle, progressing from the most significant bit (MSB) to the least significant bit (LSB), based on decisions provided by a 1-bit comparator. The design includes well-defined states for sampling, bit testing, decision making, and completing the conversion, all driven by a single system clock. A comprehensive testbench was developed to verify functionality through controlled comparator outputs and waveform analysis. The final implementation demonstrates correct timing behavior, single-cycle sample and done pulses, and stable SAR code generation, meeting all requirements specified for a synchronous SAR logic controller.

1 Preliminaries

1.1 Introduction to SAR ADCs

A Successive Approximation Register Analog-to-Digital Converter (SAR ADC) is an ADC that converts an analog voltage into a digital number by performing a step-by-step binary search. Rather than checking all possible values, it finds the correct value in the most efficient way: by narrowing the possible voltage range one bit at a time.

1.2 Advantages of SAR ADC

- **Low power consumption** — very efficient energy-per-conversion compared with pipeline/flash at the same resolution in low-to-moderate sample-rate regimes.
- **Moderate to high resolution** — commonly from 8 bits up to 16–18 bits in modern designs.
- **Medium sample rates** — common instantaneous sampling ranges from a few kS/s up to a few MS/s (depending on implementation). Excellent for kHz–low-MHz applications.
- **Deterministic conversion latency** — fixed (N+1) clock cycles per conversion for an N-bit SAR, which simplifies real-time systems and digital control.

1.3 Usecase of SAR ADC

SAR ADCs are widely used across applications where low power, moderate speed, and good resolution are essential. They are ideal for battery-powered instruments such as multimeters, portable medical devices, and sensor-based data loggers, as well as industrial and IoT sensor front-ends that benefit from deterministic latency and easy channel multiplexing. Their small area and efficiency make them suitable for column-parallel image sensors, while their accuracy and predictable timing support test equipment and automotive control systems. SAR ADCs also serve in low-rate baseband and audio applications where power efficiency is critical.

1.4 Where SAR ADC fails

A SAR ADC is not suitable for applications that demand extremely high sampling rates, typically in the tens or hundreds of megasamples per second, where flash or pipelined ADC architectures perform much better. It is also not the right choice for ultra-high-resolution systems that rely on oversampled noise-shaping techniques, since sigma-delta ADCs can achieve more than 16–18 effective bits with superior linearity and noise performance. Additionally, SAR ADCs are limited in applications requiring very high instantaneous bandwidth or sub-nanosecond timing accuracy, as their bit-by-bit conversion inherently constrains both speed and timing precision.

1.5 Timing Structure of SAR ADC

The operation of a SAR ADC follows a well-defined and orderly sequence that ensures accurate and consistent digital conversion. First, the system samples the analog input, capturing its value at a specific moment in time. This sampled value is then held constant, preventing changes throughout the decision process. The SAR logic then proceeds to resolve each bit, starting from the most significant bit (MSB) down to the least significant bit (LSB). For every bit, it begins by setting a trial bit, which instructs the DAC to generate the corresponding analog voltage. The comparator evaluates this DAC output against the held input voltage, determining whether the trial bit is too high or too low. Based on this comparison, the SAR logic either keeps the bit set or clears it, effectively narrowing the search range. This process repeats for each successive bit until the LSB is resolved. Once all bits have been evaluated, the SAR logic outputs the final digital code, completing the conversion cycle.

2 Building Blocks of a SAR ADC

A SAR ADC consists of four elemental hardware pieces working together in a timed sequence. Understanding these is crucial before studying the SAR Logic controller.

2.1 Sample-and-Hold (S/H) Circuit

The Sample-and-Hold (S/H) circuit performs two essential functions during SAR ADC operation. First, it samples the incoming analog input voltage, and then it holds this value constant throughout the digital conversion process. This is necessary because a SAR ADC requires multiple clock cycles to complete a conversion; if the input voltage were allowed to vary during this time, the resulting digital code would be inaccurate. Conceptually, the S/H operates by momentarily closing a switch to charge a capacitor to the input voltage and then opening the switch so that the capacitor maintains a stable charge. The DAC and comparator subsequently perform the binary search on this fixed voltage, ensuring a valid and consistent conversion result.

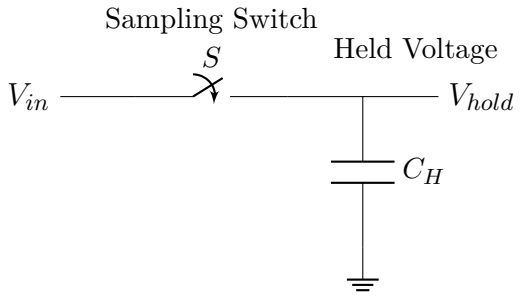

Figure 2.1: Sample-and-Hold (S/H) Circuit

2.2 Digital to Analog Converter

The Digital-to-Analog Converter (DAC) in a SAR ADC converts the digital trial code generated by the SAR logic into a corresponding analog voltage that the comparator can evaluate. During each bit trial, the SAR controller temporarily sets the current bit to one, and the DAC produces the analog equivalent of this tentative code. The comparator then determines whether the input voltage is greater than or equal to the DAC output; if so, the bit is retained, otherwise it is cleared. To ensure correct operation, the DAC must settle rapidly before each comparison and exhibit monotonic behavior so that the output voltage consistently increases with increasing digital code. Common DAC architectures used in SAR ADCs include charge-redistribution capacitor arrays, R–2R resistor ladders, and hybrid structures designed to balance speed, area, and resolution requirements.

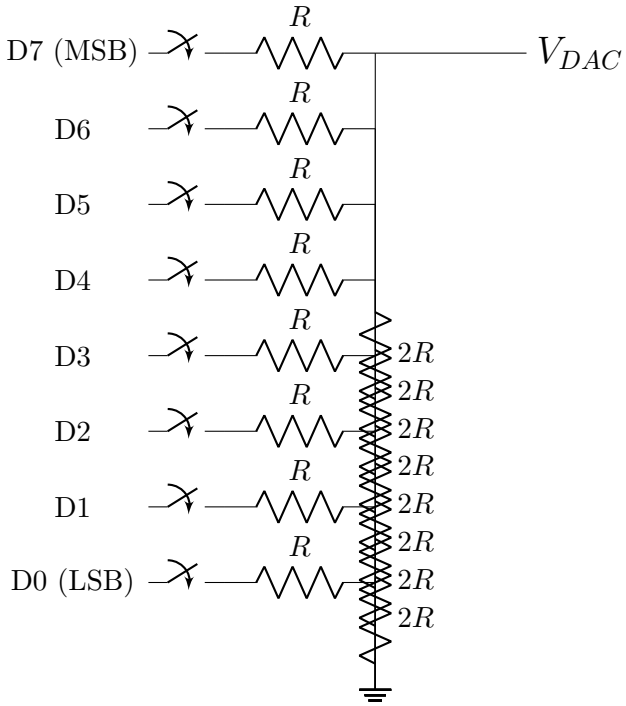

Figure 2.2: 8-bit R–2R Ladder DAC Used in SAR ADCs

2.3 Comparator

The comparator in a SAR ADC performs the essential decision-making step of the conversion process. Its function is to compare the sampled input voltage V_{in} with the DAC output voltage V_{DAC} and generate a single-bit output indicating the result. If the input voltage is greater than or equal to the DAC voltage, the comparator outputs a logic '1'; otherwise, it outputs a logic '0'. This one-bit decision is fundamental to the binary search procedure carried out by the SAR logic. The comparator must exhibit high accuracy and fast decision time, as its speed and precision directly limit the overall

performance, resolution, and conversion rate of the ADC.

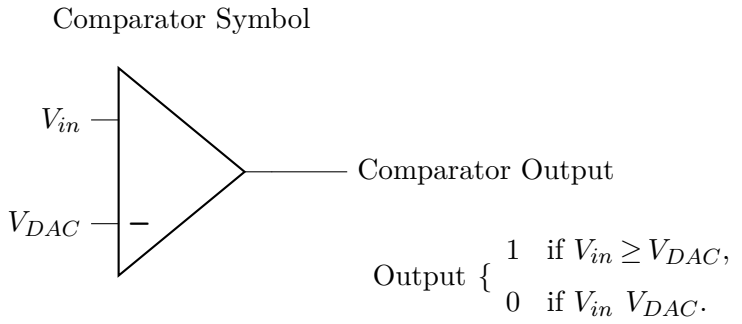

Figure 2.3: Comparator used in a SAR ADC

2.4 SAR Logic Block

The SAR logic block serves as the sequential digital controller that orchestrates the entire conversion process in a SAR ADC. Its primary responsibilities include initiating the sampling phase, iterating through the bit positions from the most significant bit (MSB) to the least significant bit (LSB), generating trial bits, reading the comparator output, and deciding whether to keep or clear each bit. It also tracks the current bit index, asserts a completion signal when the conversion is finished, and ensures the final digital output code remains stable. The controller is implemented synchronously to provide predictable timing for both the DAC and comparator, avoid hazards and metastability, and ensure compatibility with ASIC and FPGA design practices. Typically, the SAR logic is realized as a finite-state machine that uses two cycles per bit—one for applying the trial code and another for evaluating the comparator result—and generates clean, single-cycle pulses for the sampling and done signals while ignoring new start commands during an active conversion.

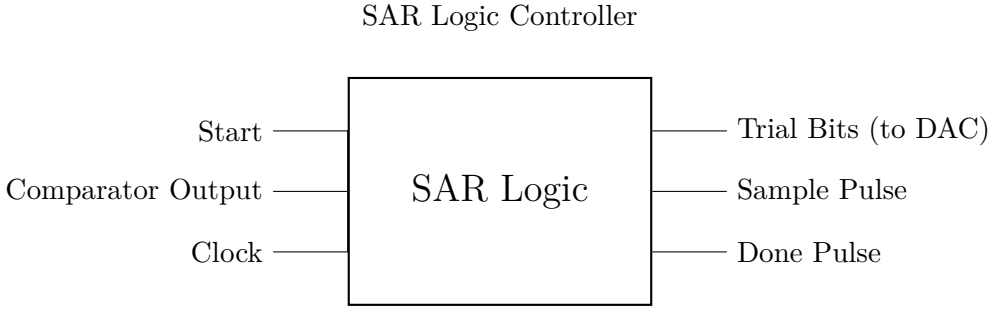

Figure 2.4: Block Diagram of the SAR Logic in a SAR ADC

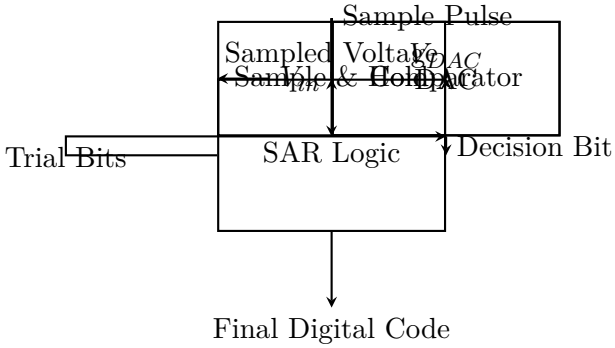

Figure 2.5: Complete Block Diagram of a SAR ADC

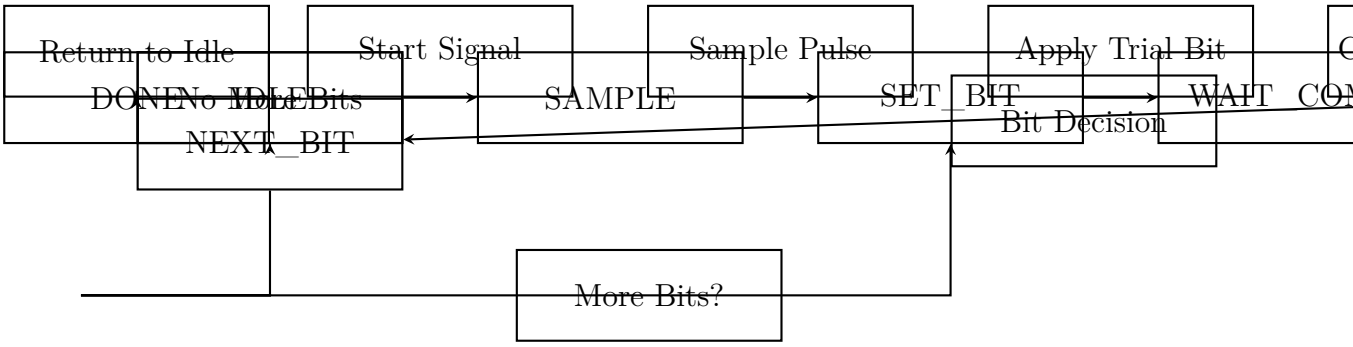

Figure 2.6: Readable Finite State Machine for the SAR Logic Controller