

# Final Project - Release Checklist

Team name: Group5\_\_\_\_\_

Team Member 1: \_\_Pierre Drege\_\_\_\_\_ Team Member 2: \_\_Payam Partow\_\_\_\_\_

Due Date: \_APRIL 15th 2022\_\_\_\_\_

Project Type: Stem Player SoC [ YES] Standard [ ]

Bonus\_\_\_\_\_

N	Statement:	(Y) - Yes (N) - No (P) -Partial	Remark
1	SD card reading, writing in baremetal software with Zynq PS. Continuous mode reading file in bursts		
2	Stem/Wave file parsing: header information, audio data		
3	I2S controller with AXIS-4 (Streaming Interface) and verification <ul style="list-style-type: none"> <li>Configurable burst and datawidth parameters</li> </ul>		
4	IIC configuration in baremetal software (44.1KHz setup)		
5	IIC hardware block integration and proper clock generation setup for mclk		
6	VGA controller amendments for play/pause/stop and animation		
7	Zynq PS setup, HP, GP, Interrupts (if applicable)		
8	DMA controller hardware setup & baremetal sw configuration		
9	Integration of DMA with I2S controller AXI-4 Stream interface		
9.1	Sound & music playing successfully		
9.2	Multiple bursts supported with uninterrupted play		
9.3	Play, pause, stop and next track functional		
10	OLED Display IP core integration		
11	Zedboard switch integration (hardware & software), fully functional		
12	SD card boot		

**REMARKS:**

(1)