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Thesis Title

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To someone very special...

Acknowledgments

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Abstract

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Sommario

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Chapter 1

Background

1.1 LLVM

The LLVM Project [**llvm**] is a collection of modular and reusable compiler toolchain technologies. It is built around an intermediated representation called LLVM-IR, and provides a set of APIs to interact with it. LLVM provides an optimizer that works on the intermediate representation, and also several code generation helpers that allow to target all the main hardware architectures.

1.1.1 LLVM-IR

The LLVM-IR is a language that resembles a generic assembly language, while also providing some high level features such as unlimited registers, explicit stack memory allocation and pointer deferentation. This allows LLVM-IR to be both the ideal target for high-level language developers, that do not have to worry about architecture specific details, and also the ideal source language for compiler backend developers, that have to implement only a translator from LLVM-IR to their target architecture's assembly language, without worrying about high-level language features.

The LLVM-IR is accesible in three formats: in-memory represantation, that allows manipulation through the LLVM APIs, binary format, used by many LLVM tools, and the human-readable textual format, that can also very conveniently be parsed by means of the APIs.

1.1.2 SSA and Phi nodes

The LLVM-IR is by definition in SSA (Static Single Assignment) form. The SSA form requires a variable to be assigned only once, and requires every variable to be defined before its uses. It is called static because it does not take into account dynamic (related to the program's runtime) considerations. For instance, an

assignment in a loop counts always as one assignment, even if at runtime it will be performed several times.
—-esempio
It is always clear which definition to use, unless a basic block has multiple predecessors. In that case it is necessary to add phi nodes that carry the information to disambiguate the uses at runtime.
—-esempio

1.1.3 Class hierarchy

The class hierarchy defined in the LLVM APIs consists of hundreds of classes, a complete and exhaustive view is given by the LLVM Doxygen Documentation. The main components of the hierarchy are:

- Module: the entire program/compile unit. Contains the global values of the program: mainly the global variables and the functions.
- Function: a function in the compile unit, contains mainly a set of arguments and it's control flow graph in the form of a set of basic blocks.
- Basic Block: a set of instructions with no branches between them.
- Instruction: An instruction of the IR.

Another key class in the LLVM class hierarchy is the Value class. It represents anything that has a type and can be used as an operand to an instruction: function arguments, constants, instructions, basic blocks and functions are all Values. A Value also carries information of what other Values it uses, and what other Values use it.

1.1.4 LLVM Metadata

The LLVM-IR allows metadata to be attached to Instructions, Functions, Global Variables or Modules. Metadata can convey extra information about the code to the optimizers and code generator. The main use of metadata is debug information, but they may also carry information about loop boundaries or other assumption that are useful during the various stages of the compilation process.

Metadata can either be a simple string attached to an instruction, or they can be a Metadata Node (MDNode). MDNodes can reference each other and are specified by other classes in the LLVM APIs. See section 1.2 or the LLVM Language Reference [**llvm-langref**] for more details.

1.1.5 LLVM Passes

LLVM passes are where most of the interesting parts of the compiler exist. Passes perform the transformations and optimizations that make up the compiler, they build the analysis results that are used by these transformations, and they are, above all, a structuring technique for compiler code.

Passes are categorized in two ways: by the granularity at which they operate, and by the fact that they perform changes on the module or not.
By the first categorization, passes are identified as:

- Module Passes: operate on an entire Module.
- Function Passes: operate on a single Function.
- Loop Passes: operate only on loops.
- Region Passes: operate on subsets of Basic Blocks of a Function, with a single entry point and a single exit point.

By the second categorization, passes are identified as:

- Analysis Passes: passes that only perform an analysis of the given entity, without modifying it.
- Transformation Passes: passes that may modify the given entity. They exploit the results of the Analysis Passes, often (but not only) in order to perform optimizations: the may add, remove, move or replace instructions and basic blocks, with the ultimate goal of improving performances or reduce the size of the binary.

Passes may depend on other passes, for instance a pass that performs an optimization may require the results of a pass that performs a specific analysis. They are therefore handled by a Pass Manager that schedules the passes, ensuring that all the dependencies for a pass are met before executing it.

1.2 How LLVM handles debug information

1.2.1 Metadata classes

1.2.2 Transformation passes guidelines

As we've seen in section 1.1.5, during the compilation a module may undergo some changes: instructions may be removed, moved, merged together, and replaced with new instructions, all in order to improve the performances of the resulting program.

This transformations have the side effect of obfuscating the correspondence between source code and binary code: before the optimization occurs, debug information provide a very clear, one to many relation between source location and LLVM-IR instructions. But as the module progresses into the optimization pipeline, it becomes more and more difficult to maintain this relation.

In general it is not possible to map unambiguously source locations to optimized code, but the LLVM project provides a set of guidelines that specify how to correctly update debug info when implementing transformation passes [**llvm-guidelines**]. Here we provide a short summary of such guidelines [1], highlighting some behaviors that, even when following them, lead to a loss of information regarding source-binary mapping. This behaviors are not bug or mistakes of the people who provided the guidelines, but are instead related to the fact that they want to provide a debugging experience as close as possible to the one that a user would have while debugging the unoptimized code.

The guiding principles for a developer that wants to update debug info are the following:

1. Do not provide misleading information: a developer should not speculate, and providing no information is better than providing wrong information that may lead a developer to wrong considerations about the behavior of his program.

2. Provide as much information as possible: when it's not misleading, information should be preserved.

In order to achieve this, when choosing what do to with the debug information of a given instruction, a developer has three alternatives:

- Preserve the original location.

- Merge two locations: two debug locations can be merged together. Locations merge is performed by computing the intersection of the two locations: the resulting location will contain only the information that the original two had in common.

- Delete the location.

Locations can be safely preserved when the modified instruction either remains in the same basic block, or its basic block is folded into a predecessor that branches unconditionally. For instance, an optimization the replaces the instruction `add x x` with a binary shift to the left (`shl x 1`) can safely keep the location of the original add.

Location should be merged when two instructions are replaced with a new instruction. An example of that is figure 1.1, in which the two stores can be merged

[1] Provided at a speech and the 2020 LLVM Conference by Adrian Pranti and Vedant Kumar

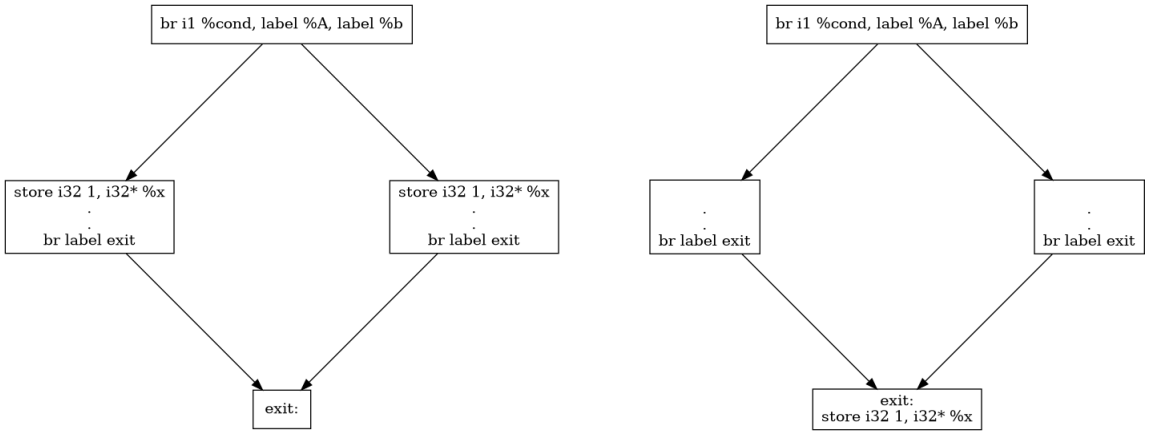

Figure 1.1: Example of optimization with merged debug location

into a new one, inserted in the exit basic block: the new instruction effectively replaces the original two, and therefore its location will be the merged location of the old ones.

In all the cases in which the previous rules do not apply, locations should be dropped. In particular, they should be dropped whenever an instruction is moved from a basic block with multiple predecessors, to one of the predecessors. This is done to avoid situations in which, while debugging, the program seems to have taken a branch in a conditional, while the actual conditions are not the one that would have resulted in the branch being taken.

Dropping locations and merging locations is a very reasonable course of action when dealing with debugging: they lead to a debugging experience that is as close as possible to the not optimized one. But they also lead to a loss of information in the source-binary mapping: when two locations are merged, we will most likely lose the information on the original source code lines, as they probably will not be equal, and when a location is dropped we will of course lose the information it carried.

We have therefore developed a methodology that allows to propagate debug locations through the optimization pipeline, while also bringing to the developers a view of the optimizations performed on their program, so that they can understand how it has been optimized by the compiler.

1.3 Program Instrumentation

Instrumenting a program means to insert additional code that was not originally in the program's source, typically in order to produce additional information (regarding some functional or non functional properties) during the program's runtime. It can be performed directly on the source code, on the executable binary, or during the compilation. An example of instrumentation are the many sanitizers that are part

of the LLVM project, they make runtime checks about memory and thread safety.

LLVM provides some helper classes to perform instrumentation on an IR Module, and in general a user may define his own transformation pass that inserts new code into the program being compiled.

Instrumentation often introduces a performance overhead, due of course to the fact that more instructions are executed while the program is running, so it is usually performed only during the development stage of an application.

1.4 Debugging

A debugger is a computer program used to test and debug other programs. It allows a programmer to run the target program in controlled conditions, pause the program's execution, check the state of variables and more.

1.4.1 Debug information

The main functionality of a debugger, over which more advanced features can be built, are setting break points and accessing the content of a variable defined in the source code.
This is achieved by means of debug information: information stored by the compiler in the program's executable, with the purpose of providing a correspondence between source level entities (variable, source code locations, data types) and low level entities (assembly instructions and memory locations).

The format used to store them may vary with the compiler/operating system used, but the stored information are mainly:

- Definition of the data types employed in the program and their layout in memory, both language-defined (eg. int, float, unsigned in C) or user defined (eg. C structs or C++ classes).

- Mapping between variables defined in the source code and memory locations in which they are stored. This allows a debugger to output the value of a variable given its name.

- Mapping between source code locations and assembly instruction. This allows the debugger to pause the program's execution when a given source code location is reached.

These information are useful not only for debugging purposes, they may also be employed by any other tool that requires a mapping between source code and binary executable, such as a profiler or a test coverage tool, that may be able to annotate the source code with the information that they have gathered.

1.4.2 DWARF format

The DWARF format [**dwarf**] is a debugging file format used by many compilers and debuggers to support source-level debugging. It is designed to be extensible with respect of the source language, and to be architecture and operating system independent.

The main data structure used to store debug information is the DIE (Debug Information Entry). DIEs are used to describe both data types and variables, and can reference each other creating a tree structure.

Another data structure that is very useful for our purposes is the Line Number Table: it contains the mapping between memory addresses of the executable code, and the source line corresponding to those addresses.
Each row of the table contains the following fields:

- Address: the program counter value of a machine instruction.
- Line: the source line number.
- Column: the column number within the line.
- File: an integer that identifies the source file.
- Statement: boolean indicating if the current instruction is the beginning of a statement.
- Block: boolean indicating if the current instruction is the beginning of a basic block.

And other fields that are described in the DWARF documentation.

Chapter 2

State of the art

2.1 Motivations

Solita pappardella + paper interview sull'energia

2.2 Instruction Level Energy modeling

Given a target's Instruction Set Architecture (ISA), an energy model is a model of the energy consumed by each instruction. They have been introduced in 1996 by Tiwari et al. [**tiwari**].

2.2.1 Characterization of an ISA Energy model

The main components of an energy model are:

- Instruction base cost (B_i, for each instruction i): the cost associated with the basic processing needed to execute an instruction.
- Effect of circuit state ($O_{i,j}$, for each pair of instruction i, j): the cost of the switching activity resulting from executing two consecutive instructions differing one from another.
- Other inter-instruction effects (E_k, for each additional effect k): any other effect that can occur in real program, such as stalls or cache misses.

Given these components and a program P, the total energy consumed by it, E_p, is given by:

$$E_p = \sum_i (B_i \times N_i) + \sum_{i,j} (O_{i,j} \times N_{i,j}) + \sum_k E_k$$

Where N_i is the number of occurrences of instruction i, and $N_{i,j}$ is the number of times there has been a switch from instruction i to instruction j.

2.2.2 Why employing an ISA energy model

The most common way to describe a processor's power consumption is through the average power consumption.

This single number may not provide enough information to characterize the energy consumed by a program running on the target processor: different programs may employ the functional units of the CPU in different ways, leading to different measurements at equal running time.

ISA Energy Models offer a more detailed view of the energy profile of the target architecture. They therefore allow to identify variations of consumed energy from one program to another, and may also guide decision of both humans (hardware/software design) and software (compilers or operating systems).

2.2.3 Producing an ISA energy model

Energy models can be produced through an experimental procedure.
In order to obtain instruction base costs, a program consisting of a large loop of a repeated instruction is written. Then one can measure the average current drawn by the processor while executing the program, $\hat{i}$, and multiply it by the supply voltage V_{cc}, obtaining the base energy consumption.
Instruction may also be grouped together, since instruction with similar functionality will have similar base cost.

In order to obtain the circuit state effects, loop of pairs of instruction are required. The difference between the instruction's base costs and the average current measured provides the circuit state overhead.

A similar approach can be employed to obtain the costs of other inter-instruction effects: writing large loops in which the examined effect occurs several times, measuring the average current and subtracting the costs that are already known (base costs and circuit state).

The main disadvantage of this approach is that several different programs must be written: for an ISA with n instructions, $\mathcal{O}(n)$ programs are required to produce base costs and $\mathcal{O}(n^2)$ for circuit state effects.
Estimation of other inter-instruction effects also gets more difficult as the complexity of the architecture increases.

On the other hand, this approach has the big advantage of not requiring a model of the circuit of the target processor, information that is often not disclosed by the manufacturing companies.

M. T.-C. Lee, V. Tiwari, S. Malik, and M. Fujita. Power analysis and minimization techniques for embedded DSP software technique to group instructions into common classes.

2.3 Energy consumption estimation

fahad: comparative study of direct measure vs rapl and direct measure vs prediction based on performance counters for intel multicore cpus. use direct measure as ground truth, it shows that both techniques have very high error.

wattch: architectural simulator that estimates CPU power consumption. it provides cycle-level power simulation, which allows to compute maximum and average power consumption, and overall energy consumption. parametrizable power model + resource usage counts obtained through cycle-level simulation. more high level than verilog (less accurate, but doesn't require full circuit design and is way faster). uses simplescalar as architectural simulator, providing it power models of the most common structures present in superscalar microprocessors. it requires power models of the subcomponents of a processor, such as register files, caches, functional units, reservation stations.

Paper eder. da leggere less is more
xmos energy model: energy modeling of multi-threaded architecture. context switching has an energy cost. extends tiwari's model by adding thread switching cost. xmprofile software suite: allows to generate load and monitor test executions. tests are generated automatically. generate tests only for instructions with no effects on control flow and no non-deterministic timing. observes that number of operands has significant impact on power consumption. data width has an impact on power consumption (low impact). they choose to generalize inter-instruction overhead. for instructions that cannot be directly tested, they propose two solutions: 1) group instructions by number of operands, and put the untestable instr in the appropriate group. 2) assign default cost to untestable instr. they obtain execution statistics by hardware simulation (this can be replaced by profiling). grouped model performs worse than individual model (16percent error vs 7percent error). both provide a consistent underestimation.

lee: energy model of risc architectures, targeting embedded systems. combining empirical method and statistical analysis. developed a model whose unknown are estimated tanks to data from empirical observations, through linear regression. they say that modeling in tiwari's way is too simplistic, since it relays only on average current. First they model the energy consumption: pipelined processor, e(X,Y) is the energy when X is executed after Y (this allows to consider switching activity). it depends on several variables (v), they consider f(vx,vy): the variation on the variable v between x and y, which depends on the hemming distance between vx and vy. they test several sets of programs: in the first set, they test same instructions, same operands different location and determine the impact of the instruction fetch stage. in the second set, they derive instruction base cost in each of the pipeline stages.

nunez-yanez: system level energy/power modeling (on chip system: memory, cpu, gpu; no camera/display). they require RTL design information (often not available), and then through linear regression they produce a power model of the whole SoC. They provide high detail, being able to characterize power consumption of different components (cpu, ram, cache), but the requirement of the RTL design is too strict.

brandolese2008: energy estimation from source code and visualization on source code. the parse tree of a C program is decorated by associating a a cost-contribution (atom) to each node. following the grammar's rule of the C language, rules to combine instruction costs are defined. the parse tree is then instrumented in order to produce a trace during the program's execution. cost coefficients are estimated through least square fitting, comparing to to the output of the ARMulator instruction set simulator. this approach relays on analyzing the parse tree. this allows source code visualization but binds to the source level language: in order to change source language, it would be required to perform a complete analysis of the grammar rule of the new language. claims to be 10k times faster than ARMulator.

rieger: misurazione diretta della corrente (campo magnetico indotto) + metodo preso da NLP. dicono loro stessi che non funziona.
rieger-survey: alcuni tool commericali, altra letteratura. molto android/java (ex. powertutor) roth: piattaforma hardware per creare energy models + xml dell'energy model per intergrarlo nel loro compilatore, il quale fornisce una stima worst case.
brandolese:
come eder Ãš llvm-based, differiscono per ir-assembly mapping. eder ha anche metodo statico-worst case.
pereira: source level view, statistical method to provide ranking, no energy estimation, just visualization.
jrapl. only intel, code segment granularity. check intel rapl

Conclusions

Appendix A

First appendix

Appendix B

Second appendix

Appendix C

Third appendix