VLSI Circuit Design
Lab 1

Yu-Chi Chu

Problem 1 - Pass Transistor and 2-1 MUX

(a) schematic

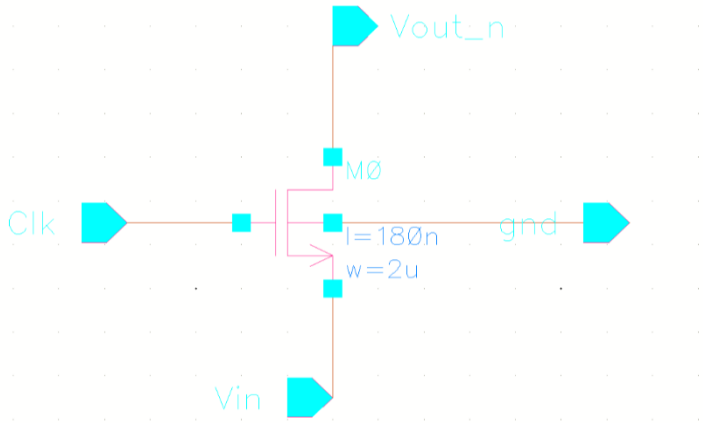

Fig 1_1 NMOS pass transistor

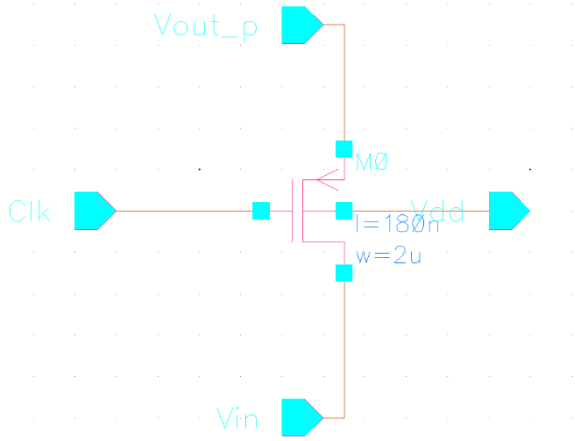

Fig 1_2 PMOS pass transistor

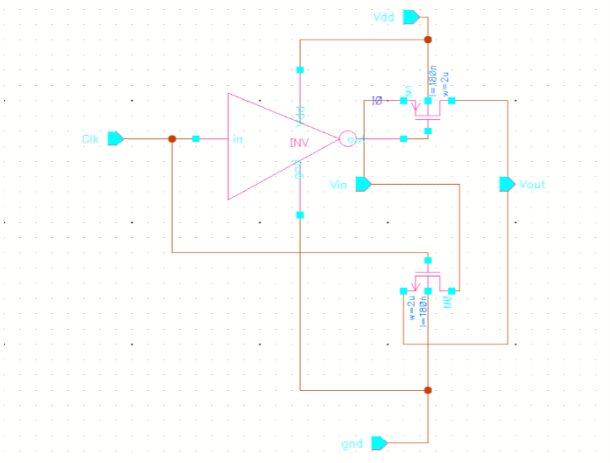

Fig 1_3 Transmission gate

(b) waveform

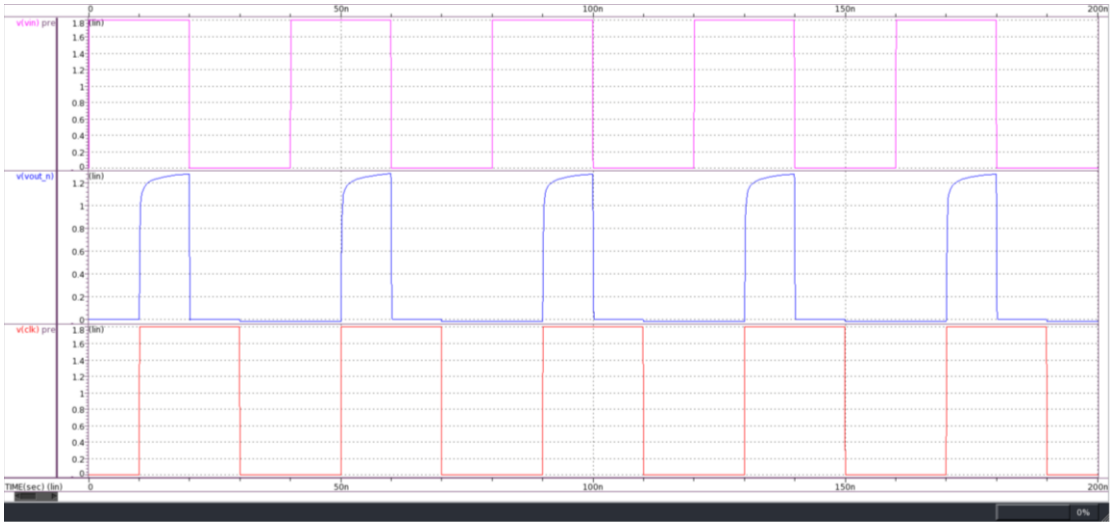

Fig 1_4 NMOS pass transistor

Fig 1_5 PMOS pass transistor

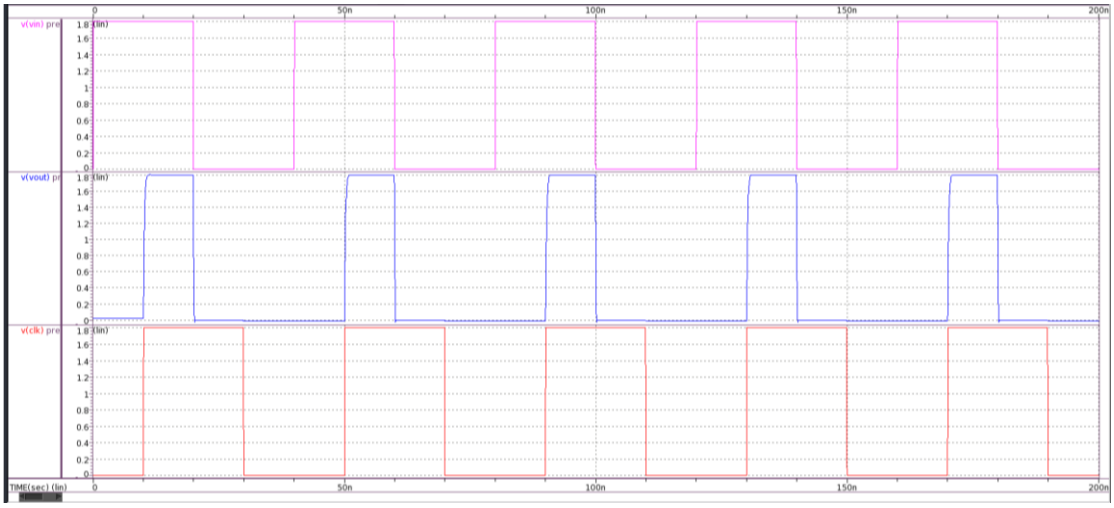

Fig 1_6 Transmission gate

(c) Explain

- **NMOS Pass Transistor:** When Clk=1 (clock high), the NMOS transistor is ON (conducting), and Vo (output voltage) is equal to Vin (input voltage). However, due to the NMOS transistor's characteristic of passing a "strong 0" but a "degraded 1," the output voltage Vo will not reach Vdd (supply voltage) completely. When Clk=0 (clock low), the NMOS transistor is OFF (non-conducting), and Vo is equal to ground (gnd=0).
- **PMOS Pass Transistor:** When Clk=0 (clock low), the PMOS transistor is ON (conducting), and Vo (output voltage) is equal to Vin (input voltage). However, due to the PMOS transistor's characteristic of passing a "strong 1" but a "degraded 0," the output voltage Vo will not reach ground (gnd=0) completely. When Clk=1 (clock high), the PMOS transistor is OFF (non-conducting), and Vo is equal to Vdd (supply voltage).
- **Transmission Gate:** When Clk=1 (clock high), both the NMOS and PMOS transistors in the transmission gate are ON (conducting), and Vo (output voltage) is equal to Vin (input voltage). Because the transmission gate combines the advantages of both NMOS and PMOS transistors (passing both "strong 0" and "strong 1"), the output voltage Vo can reach both Vdd (supply voltage) and ground (gnd=0) completely. When Clk=0 (clock low), both transistors are OFF (non-conducting), and Vo is equal to 0.

Because the transmission gate possesses the characteristics of passing both "strong 0" and "strong 1," it provides better performance compared to using a single MOS transistor and is therefore more widely used.

(d) schematic

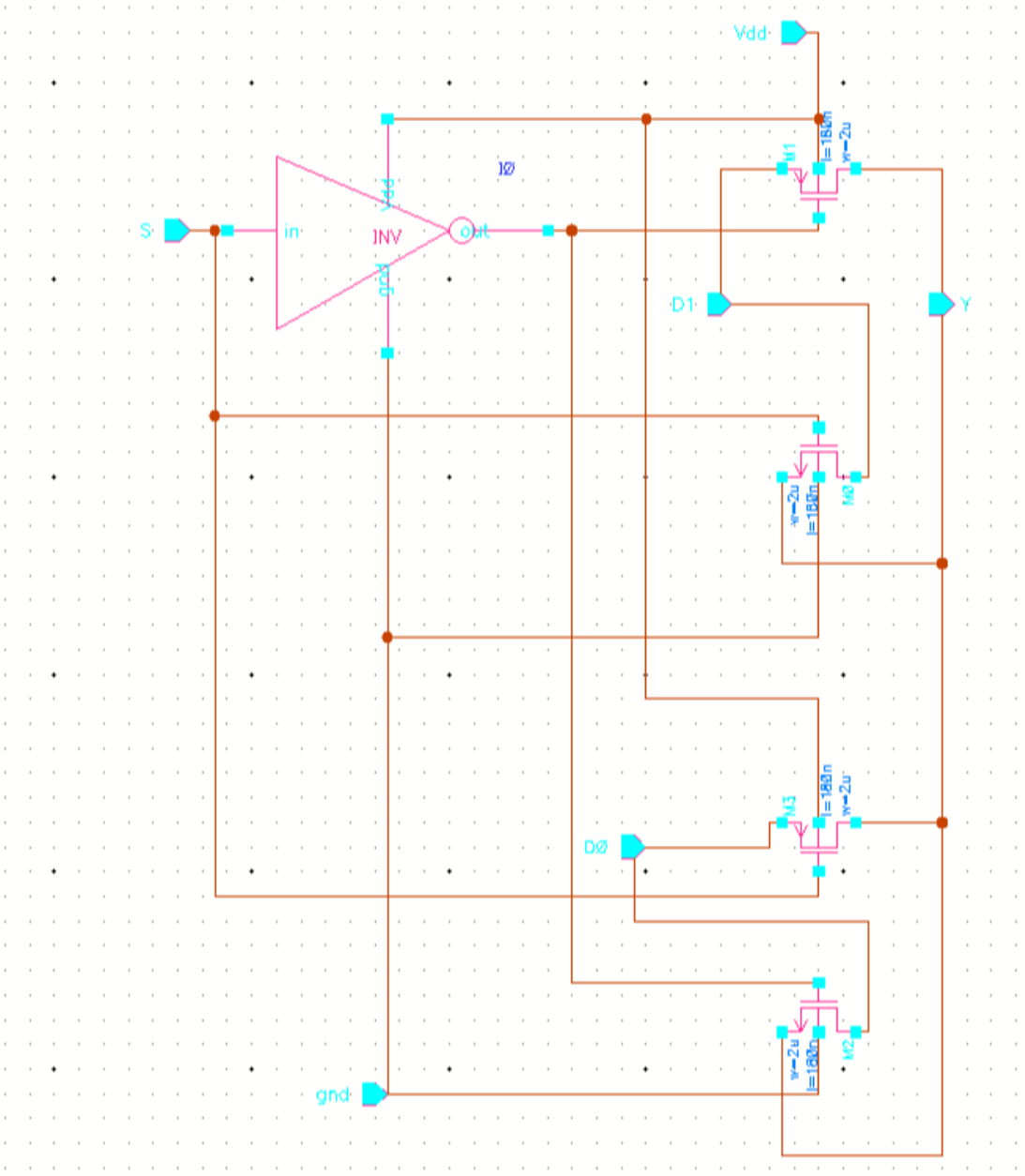

Fig 1_7 Transmission gate multiplexer

(e) waveform

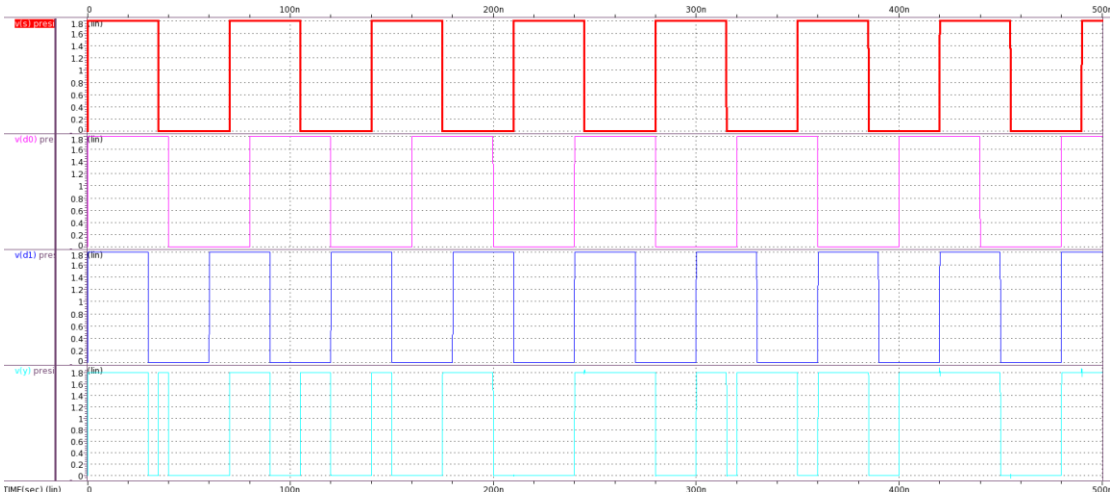

Fig 1_8 Transmission gate multiplexer

(f) layout

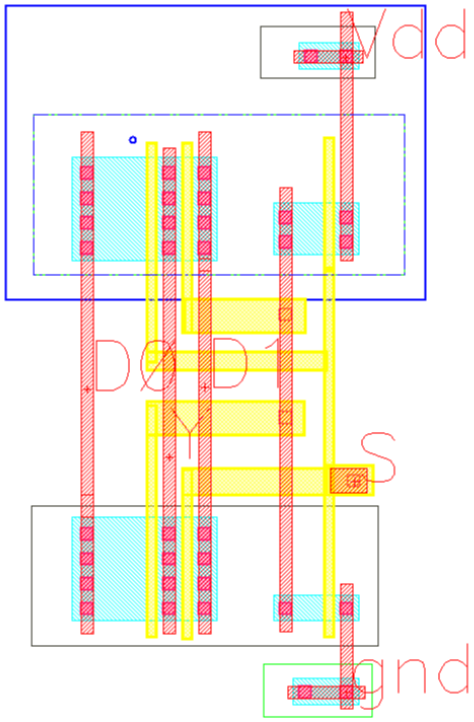

Fig 1_9 Transmission gate multiplexer layout

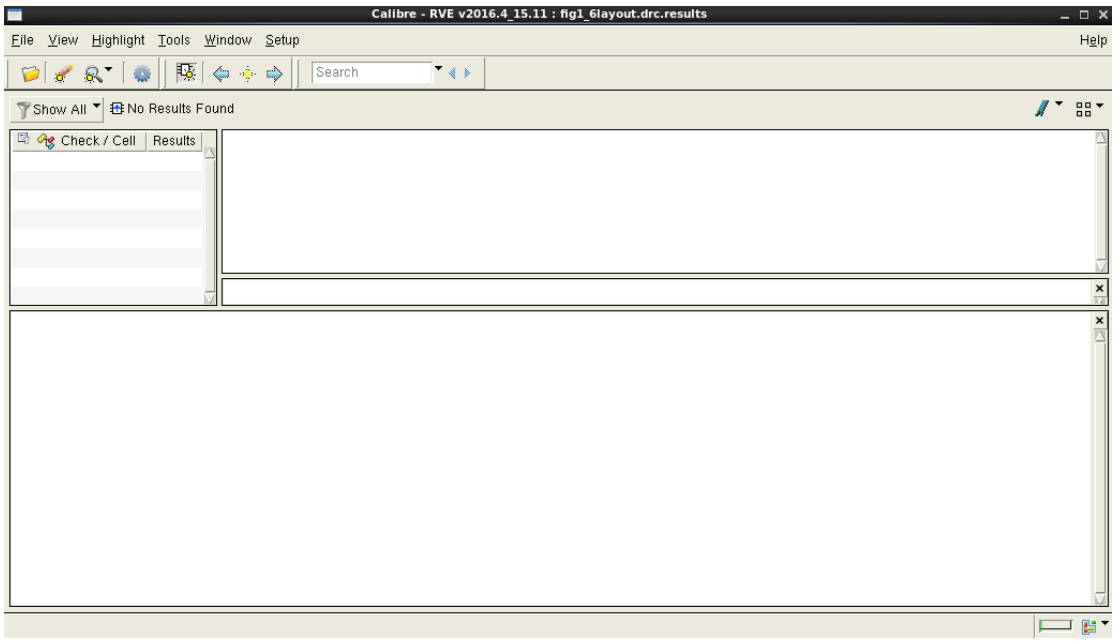

Fig 1_10 Transmission gate multiplexer DRC

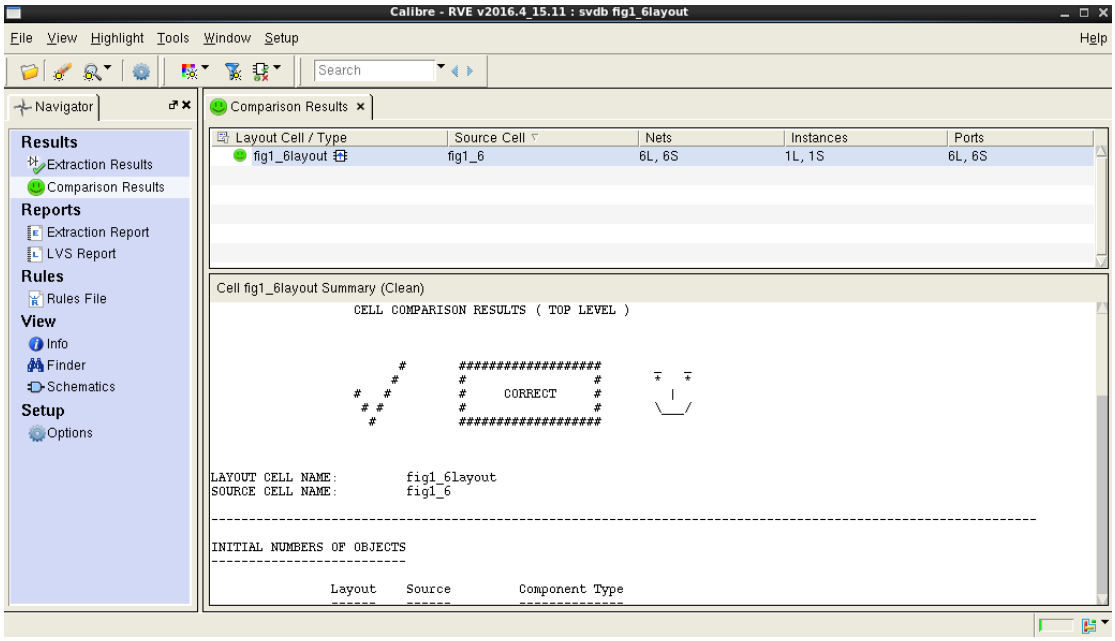

Fig 1_11 Transmission gate multiplexer LVS

(g)PEX waveform

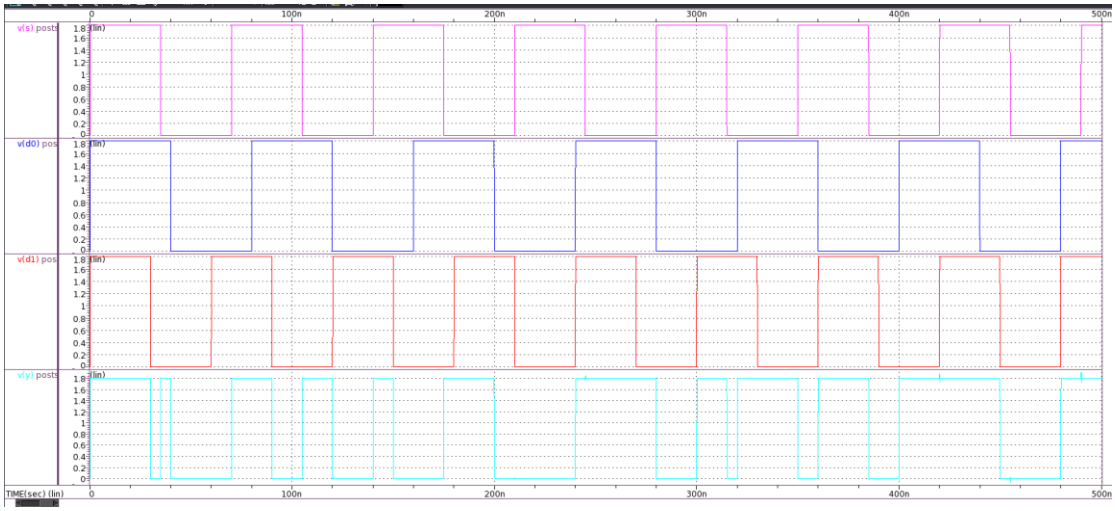

Fig 1_12 Transmission gate multiplexer PEX waveform

Problem 2 - D Latch and D Flip-Flop

(a) schematic

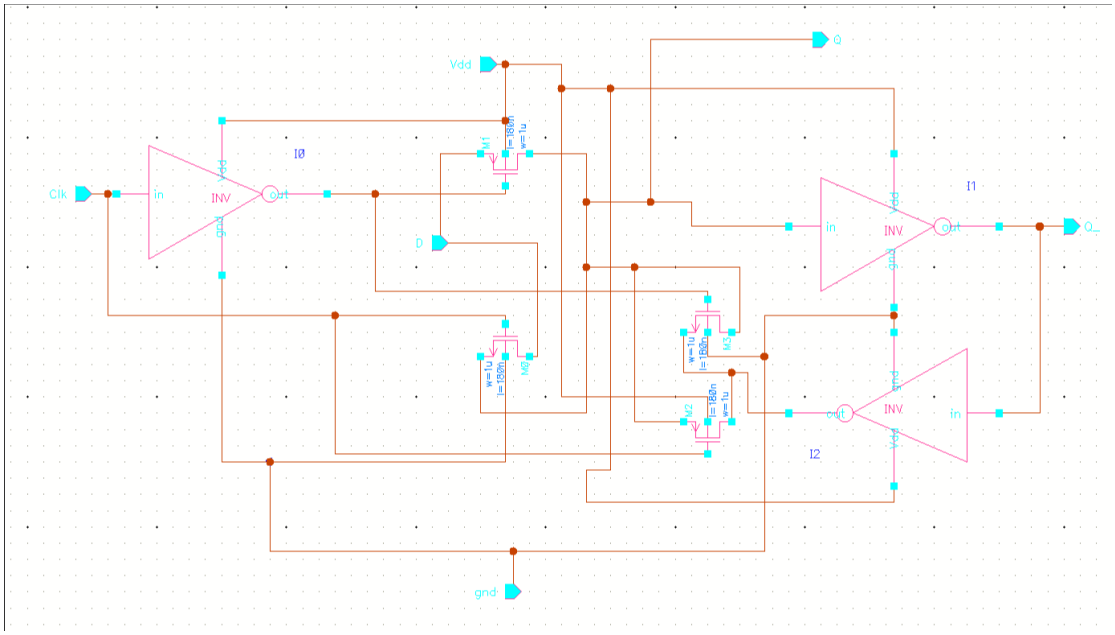

Fig 2_1 D latch

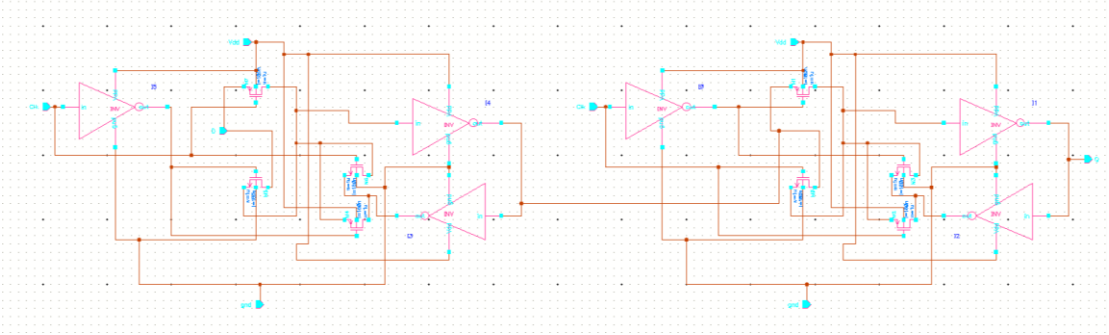

Fig 2_2 D Flip-Flop

(b) waveform

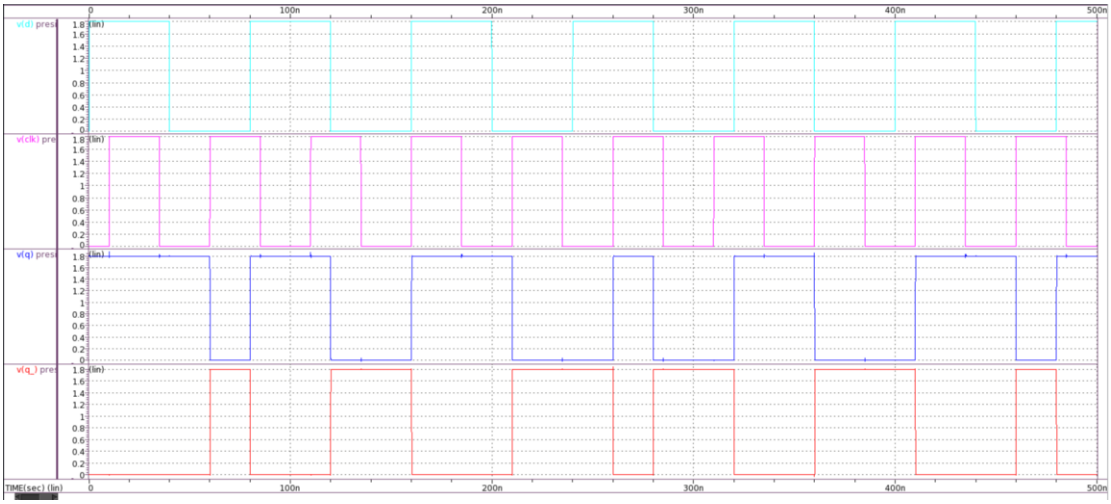

Fig 2_3 D latch

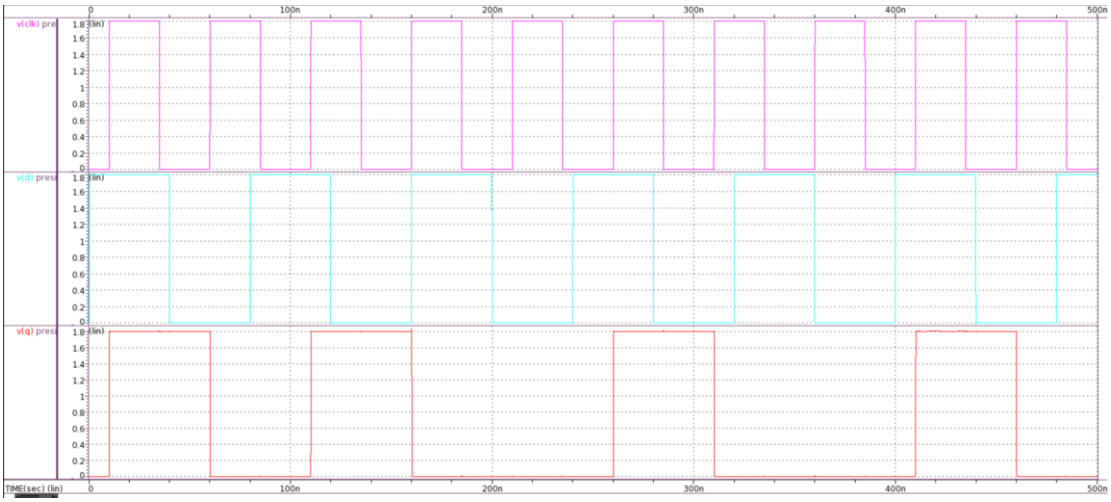

Fig 2_4 D Flip-Flop

(c) layout

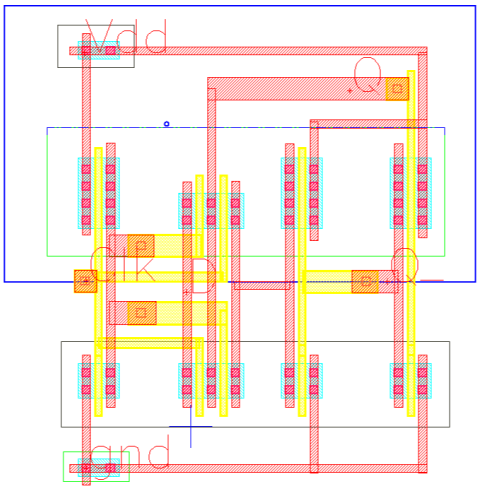

Fig 2_5 D latch layout

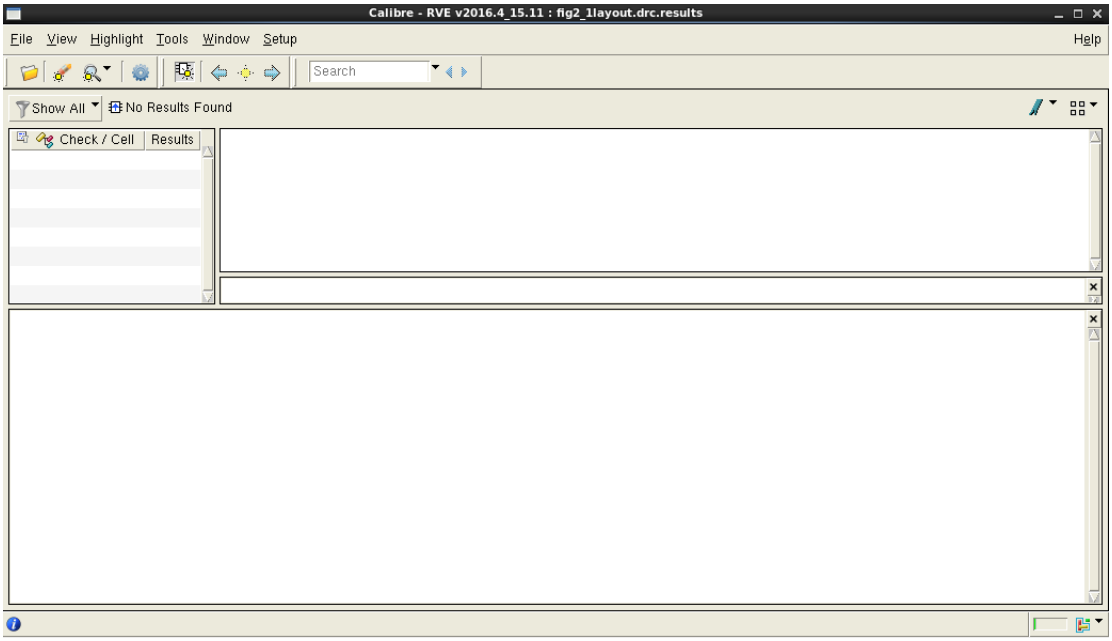

Fig 2_6 D latch DRC

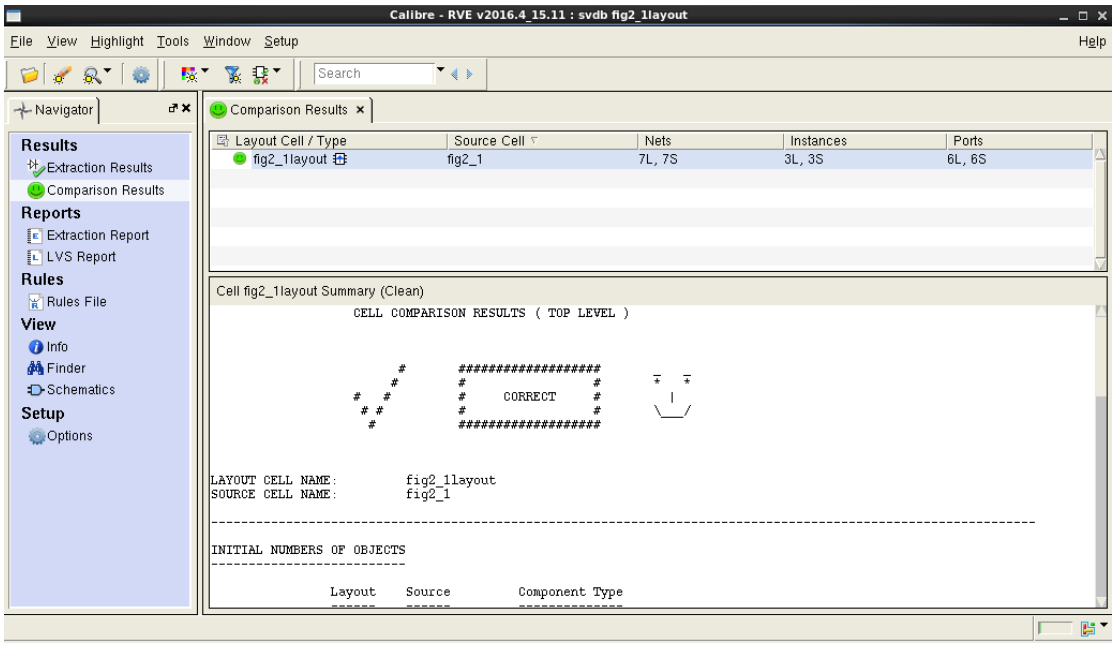

Fig 2_7 D latch LVS

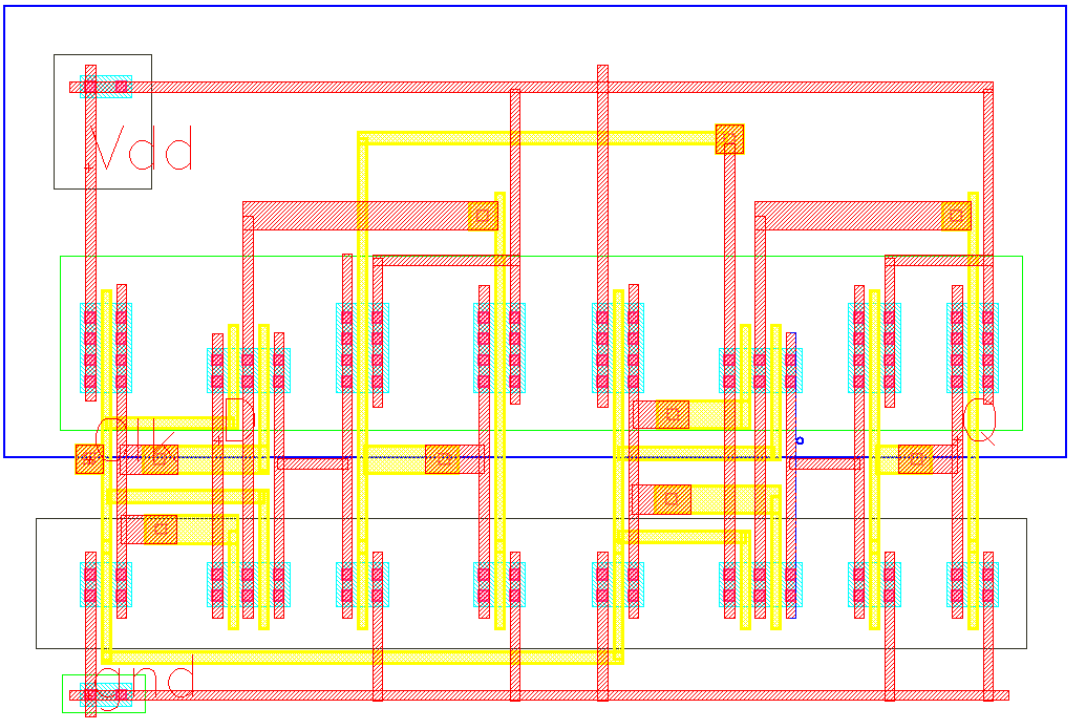

Fig 2_8 D Flip-Flop layout

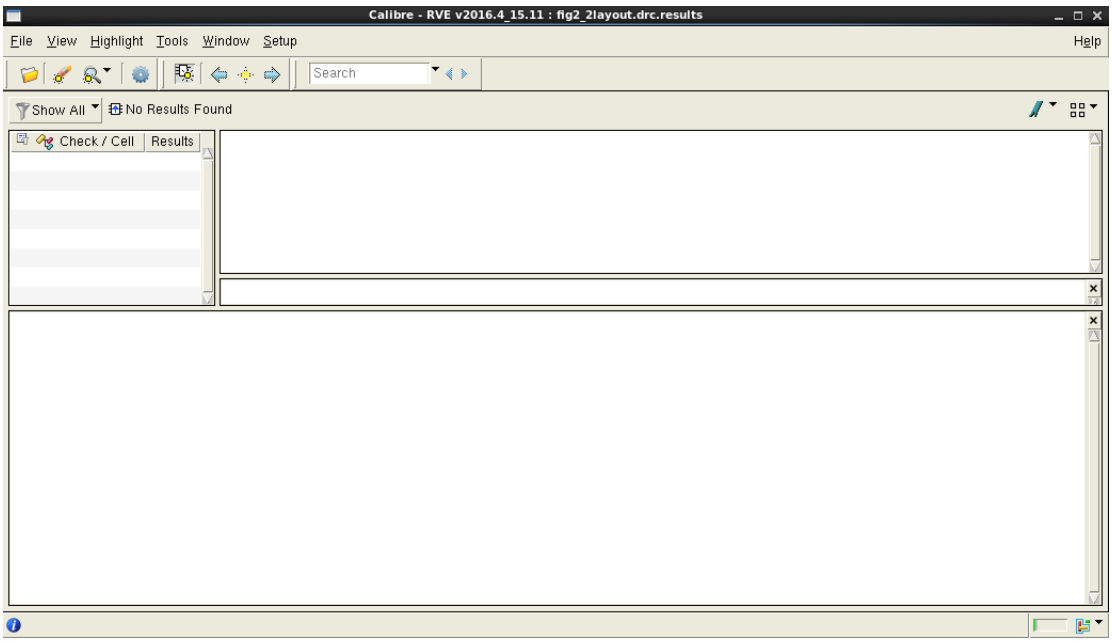

Fig 2_9 D Flip-Flop DRC

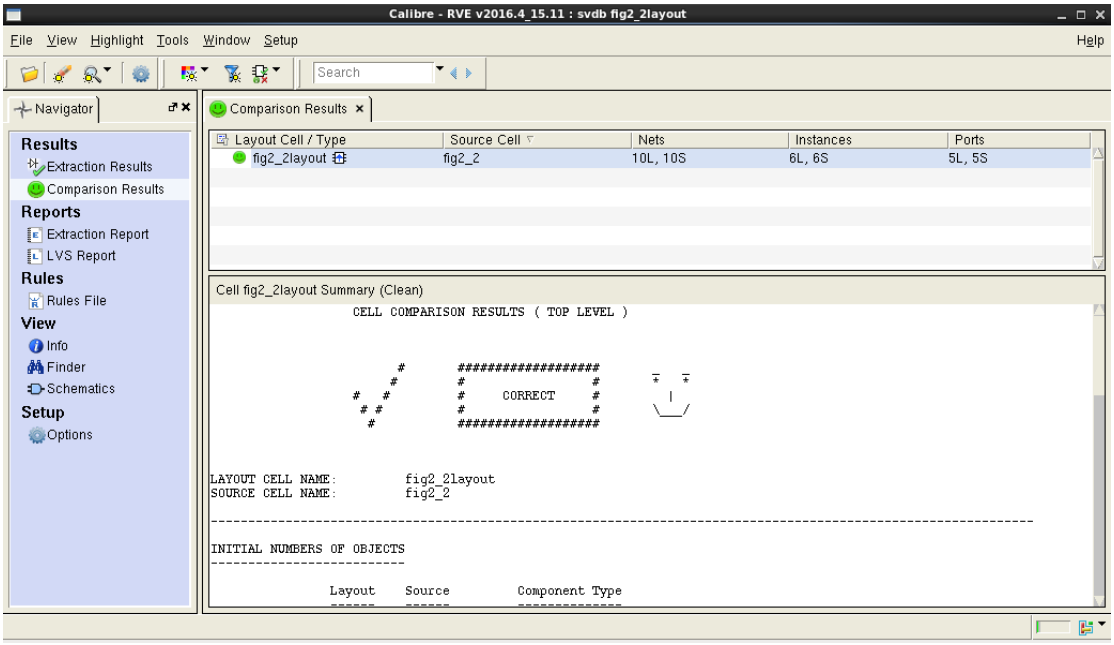

Fig 2_10 D Flip-Flop LVS

(d) PEX waveform

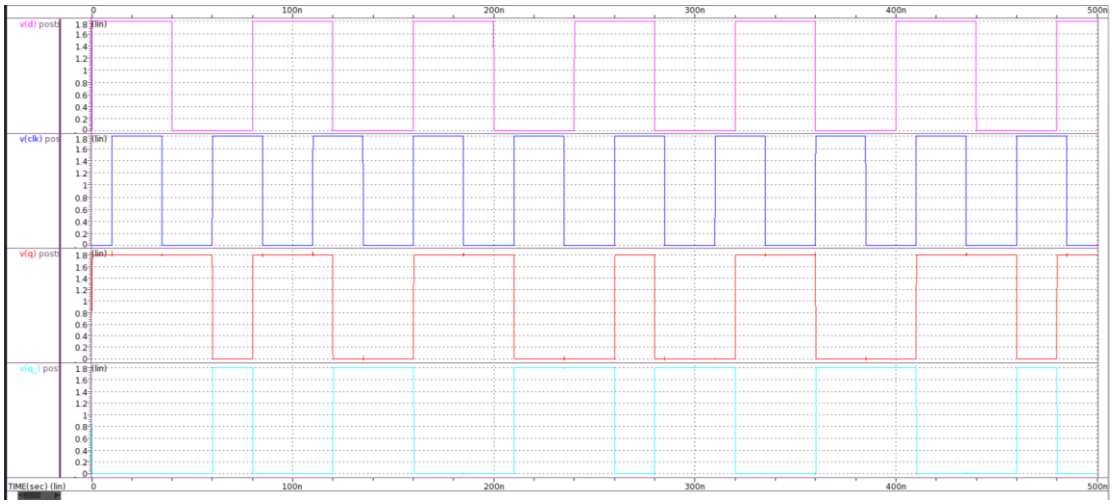

Fig 2_11 D latch PEX waveform

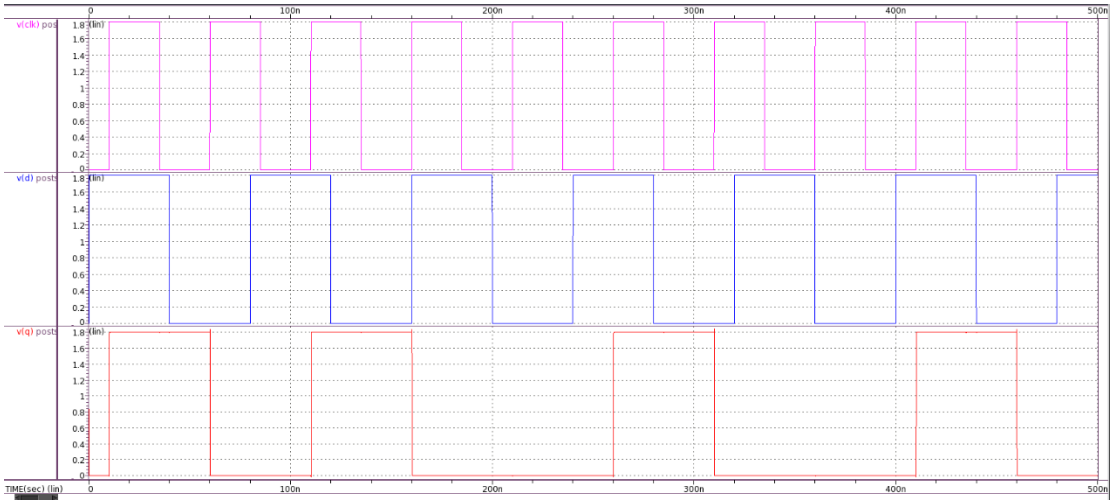

Fig 2_12 D Flip-Flop PEX waveform

Problem 3 – Combinational logic design

(a) schematic

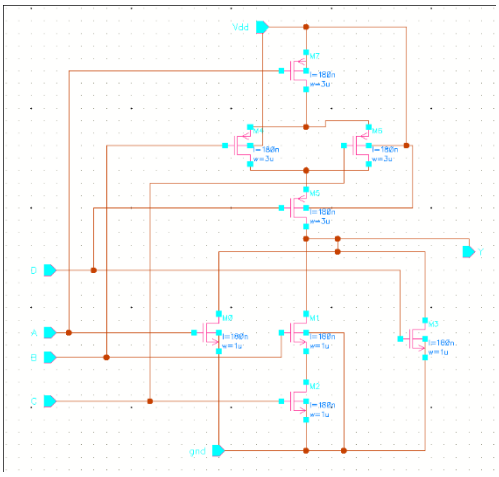

Fig 3_1 *Function* 1

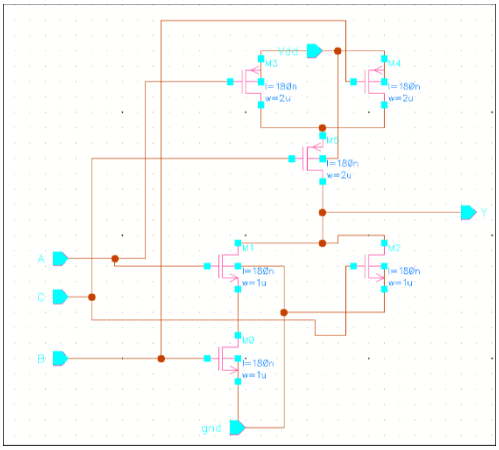

Fig 3_2 *Function* 2

(b) waveform

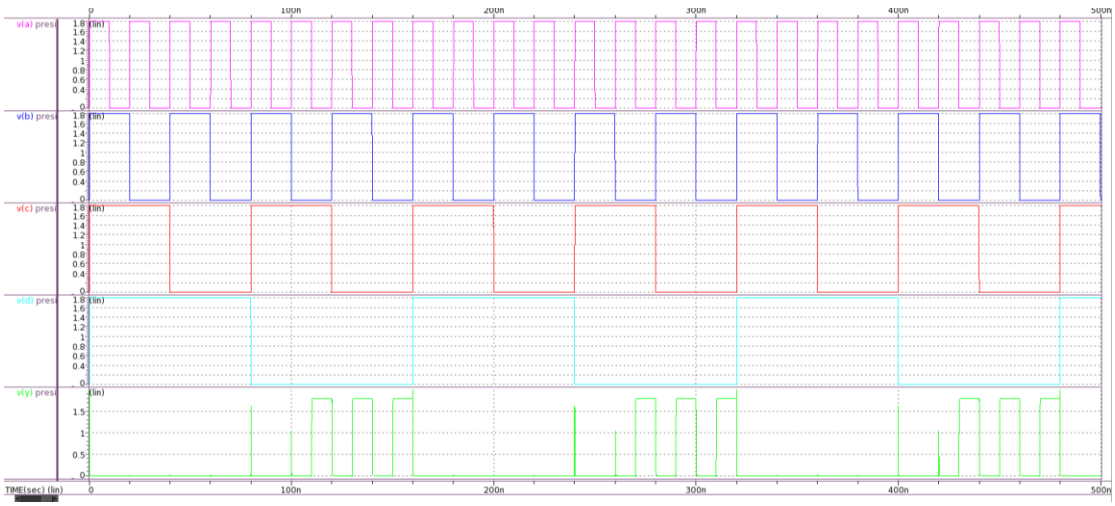

Fig 3_3 *Function* 1

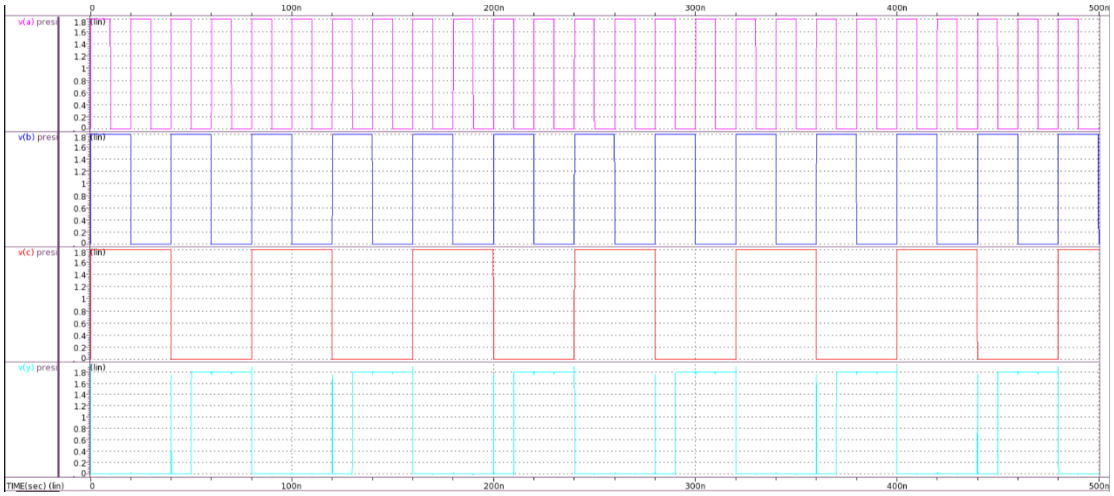

Fig 3_4 *Function* 2

(c) layout

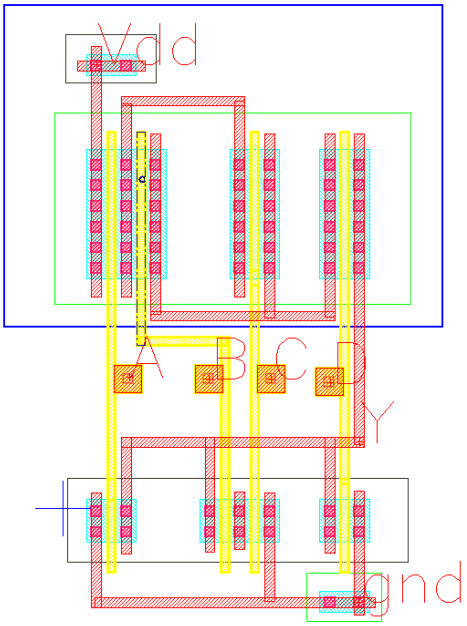

Fig 3_5 *Function* 1 layout

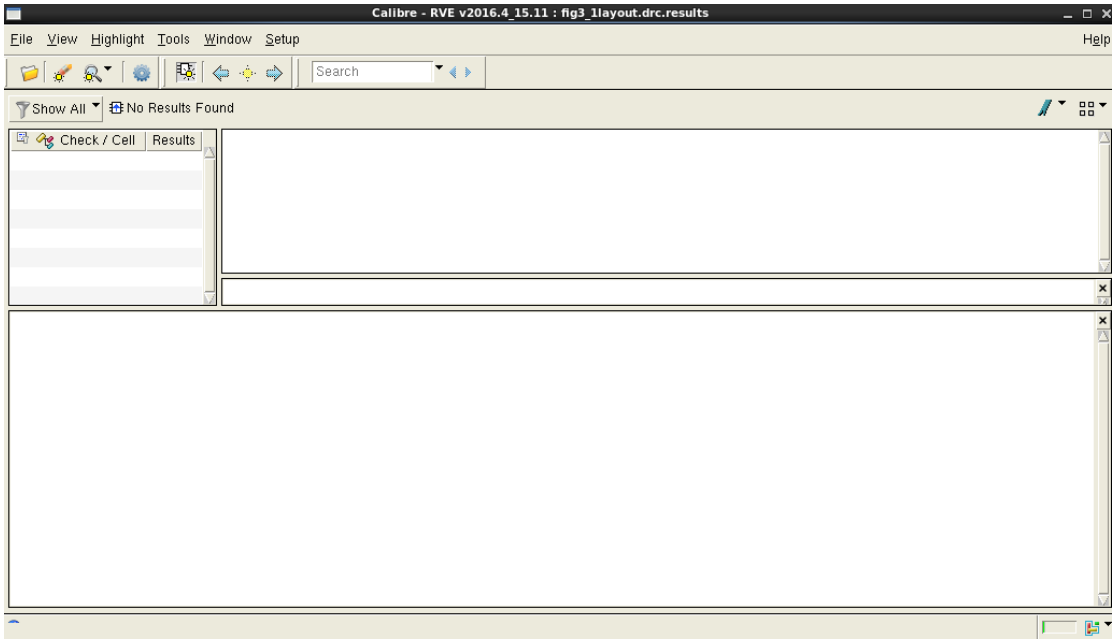

Fig 3_6 *Function* 1 DRC

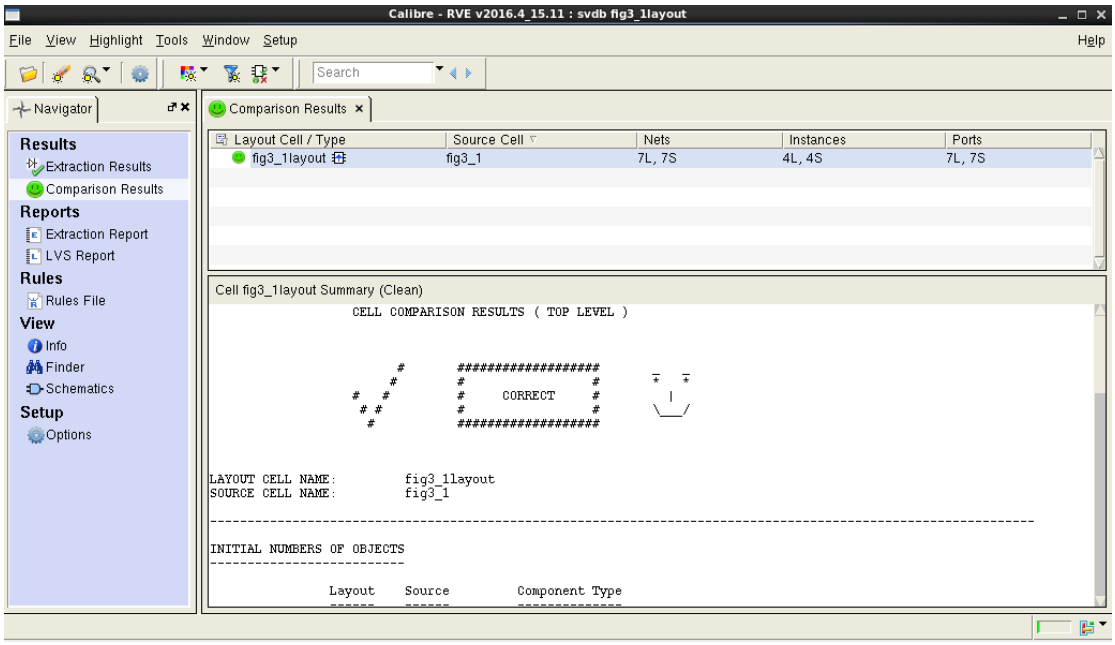

Fig 3_7 *Function* 1 LVS

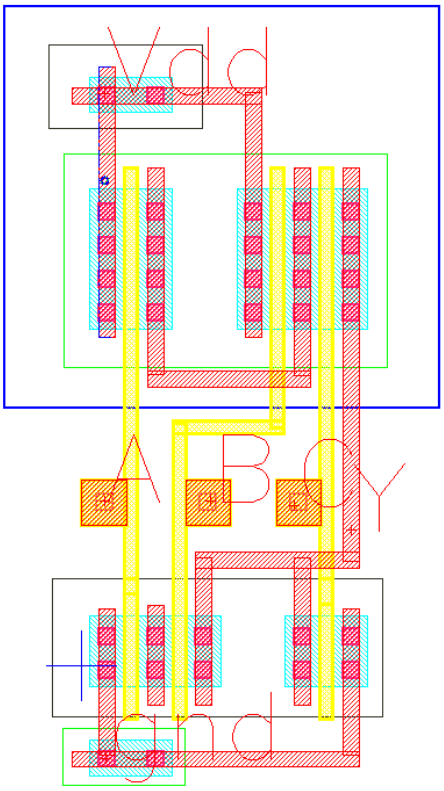

Fig 3_8 *Function* 2 layout

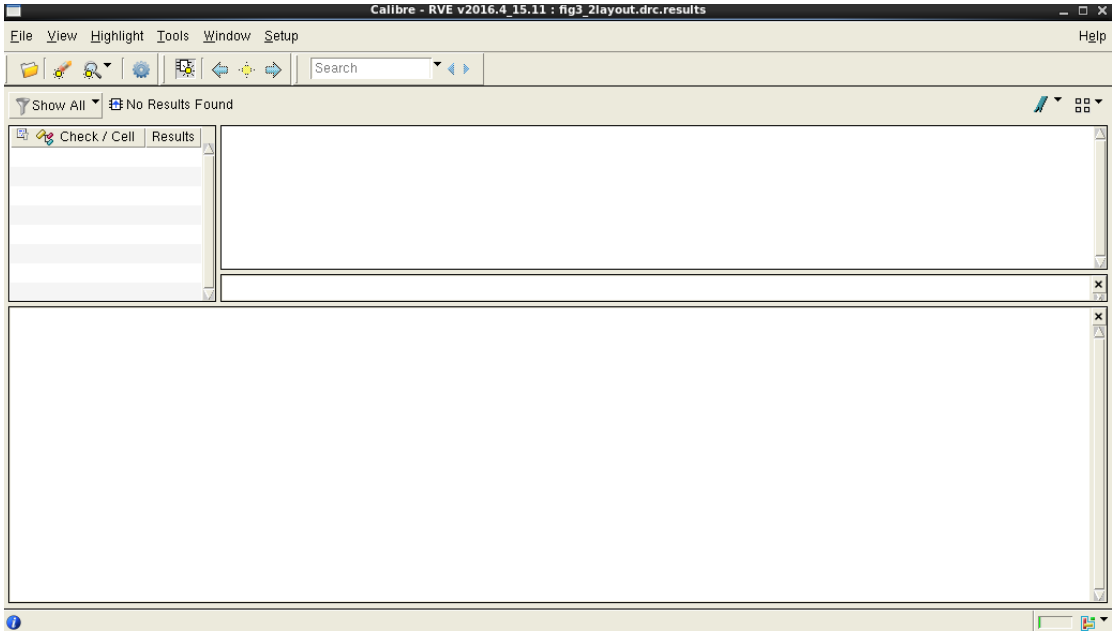

Fig 3_9 *Function* 2 DRC

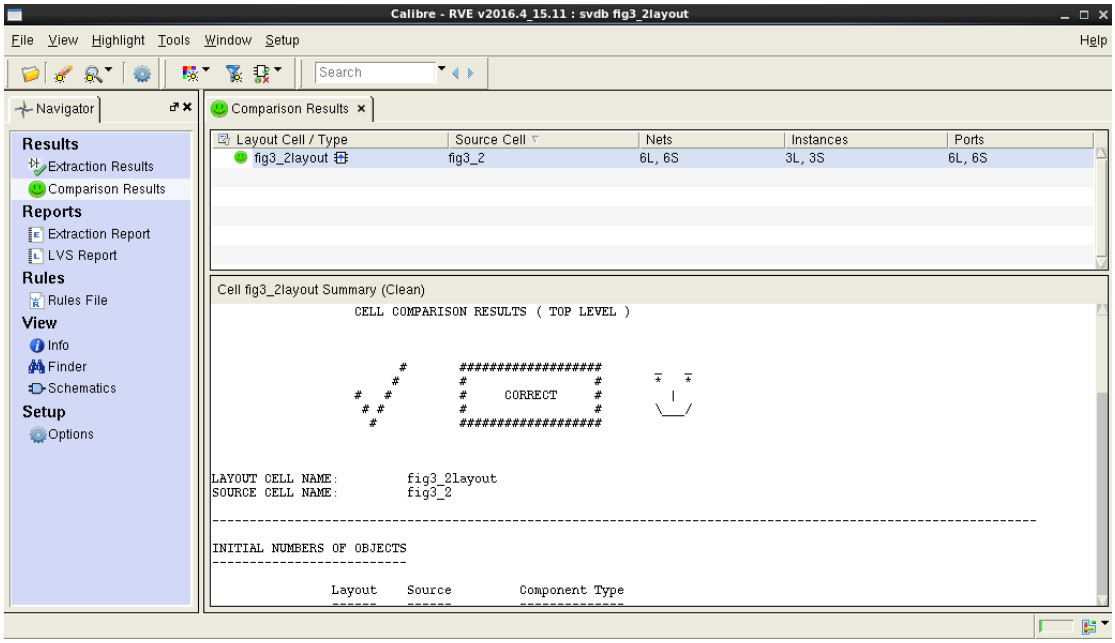

Fig 3_10 *Function* 2 LVS

(d)PEX waveform

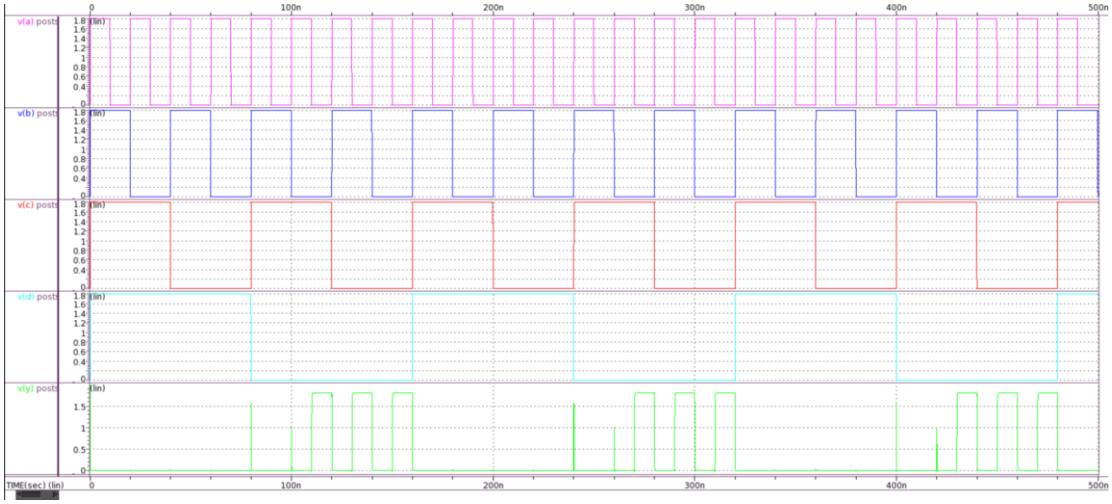

Fig 3_11 *Function* 1 PEX waveform

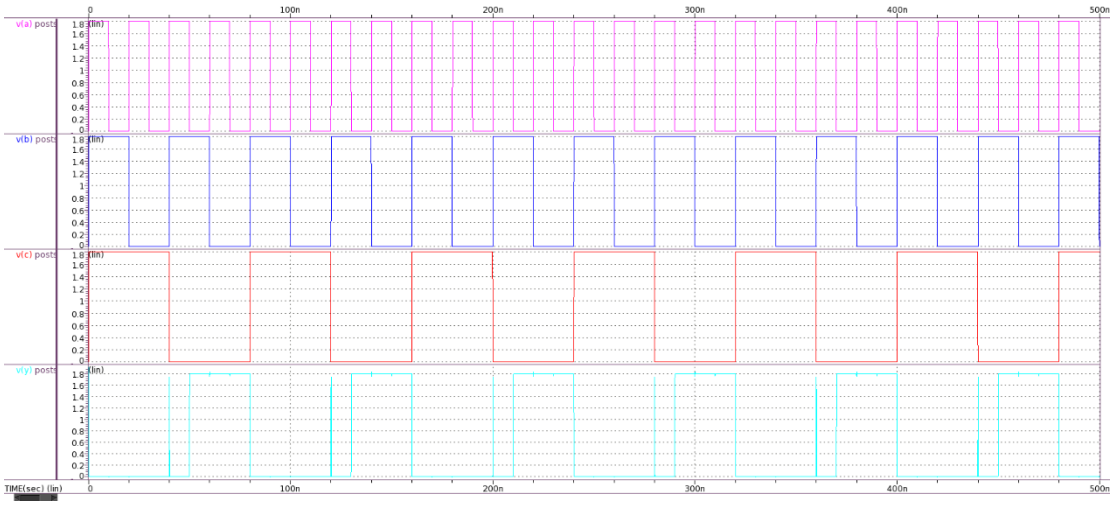

Fig 3_12 $Function$ 2 PEX waveform