VLSI Circuit Design
Lab 5

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Problem 1 – Characterizing Sequencing Element Delay

1A

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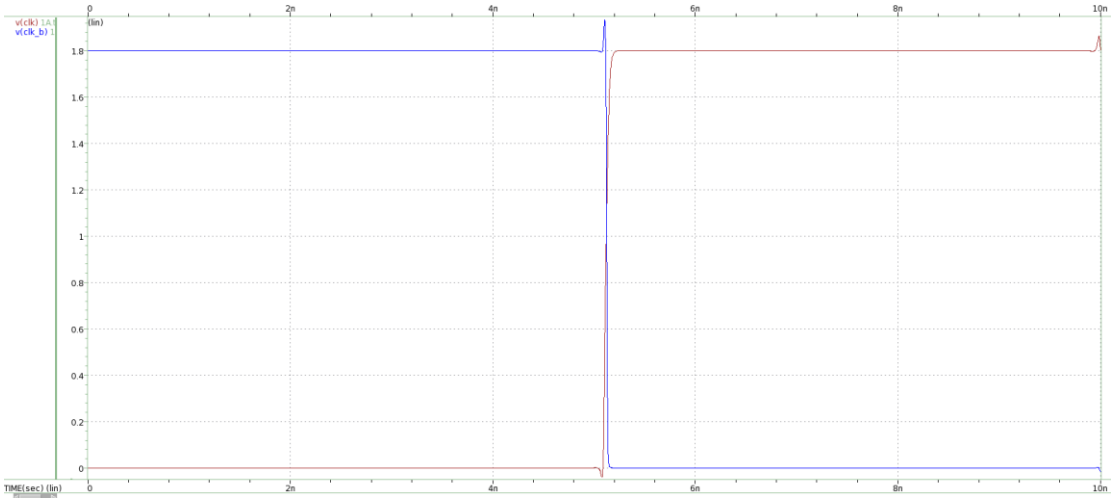
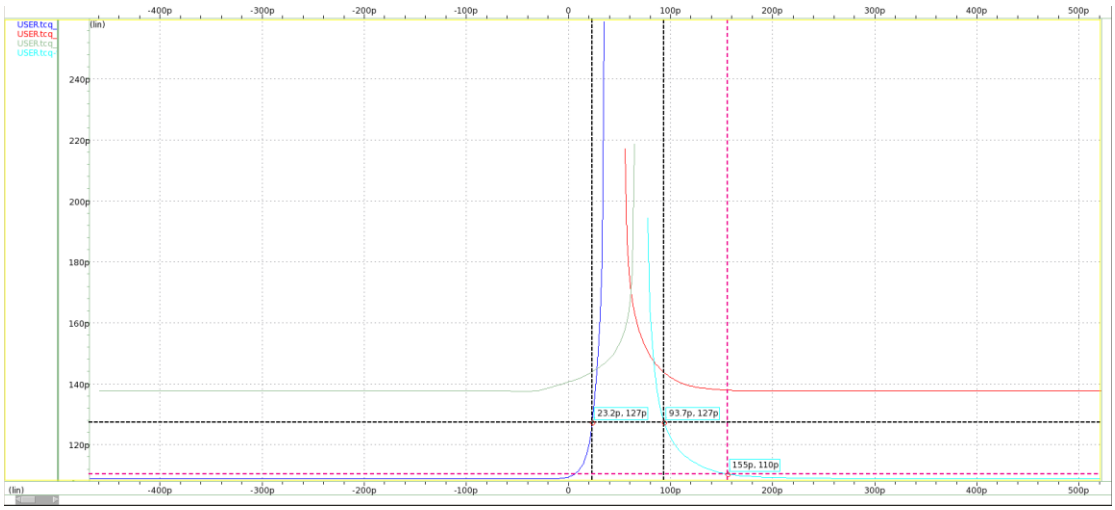
.subckt delay in out vdd gnd
m0 in  gnd out vdd p_18 W=2u L=0.18u
m1 out vdd in  gnd n_18 W=1u L=0.18u
.ends
```

The delay element I designed is similar to an always-on transmission gate, which resembles a circuit passing through only a single resistor.



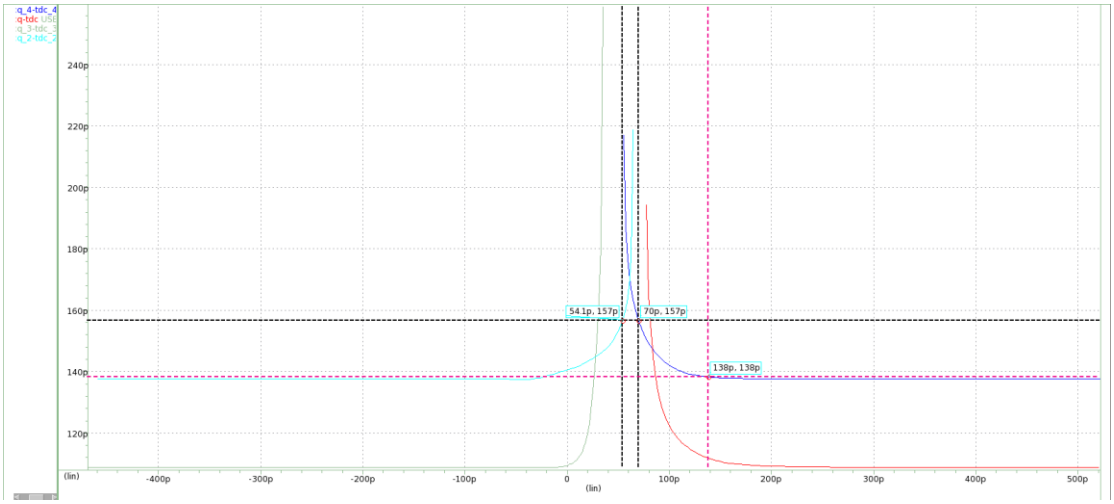
It is clearly visible from the diagram that the intersection point of Clk and Clk_bar is not 0 or 1.8. Therefore, they will not be simultaneously at 0 or simultaneously at 1.8.

1B



Cyan DRQR, Red QFDF, Gray DRQF, Blue DFQR

t_{Setup1} 93.7p -t_{hold1} 23.2p t_{pcq1} 127p t_{ccq1} 110p

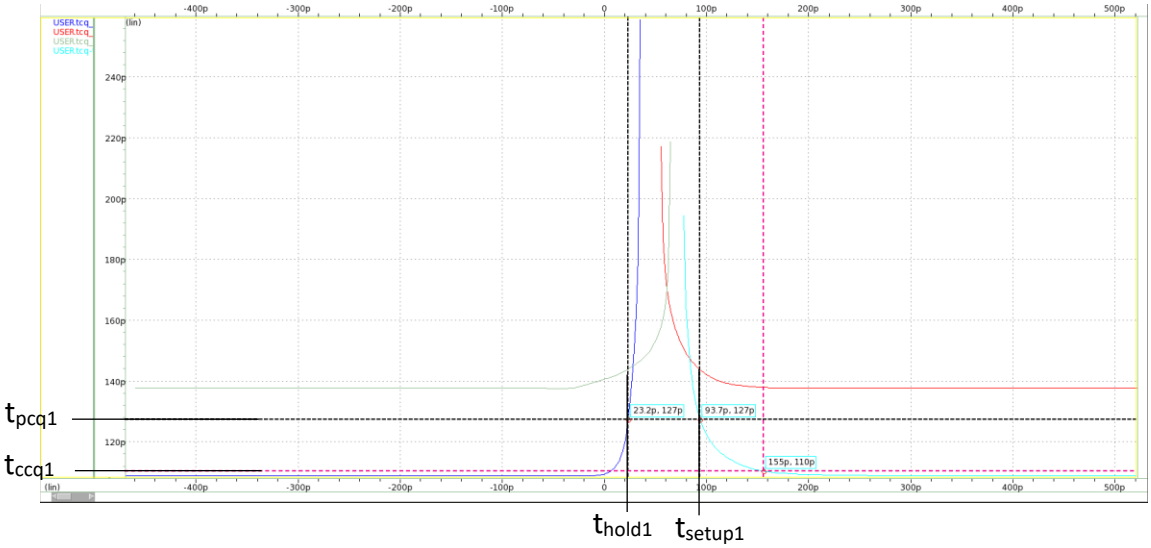


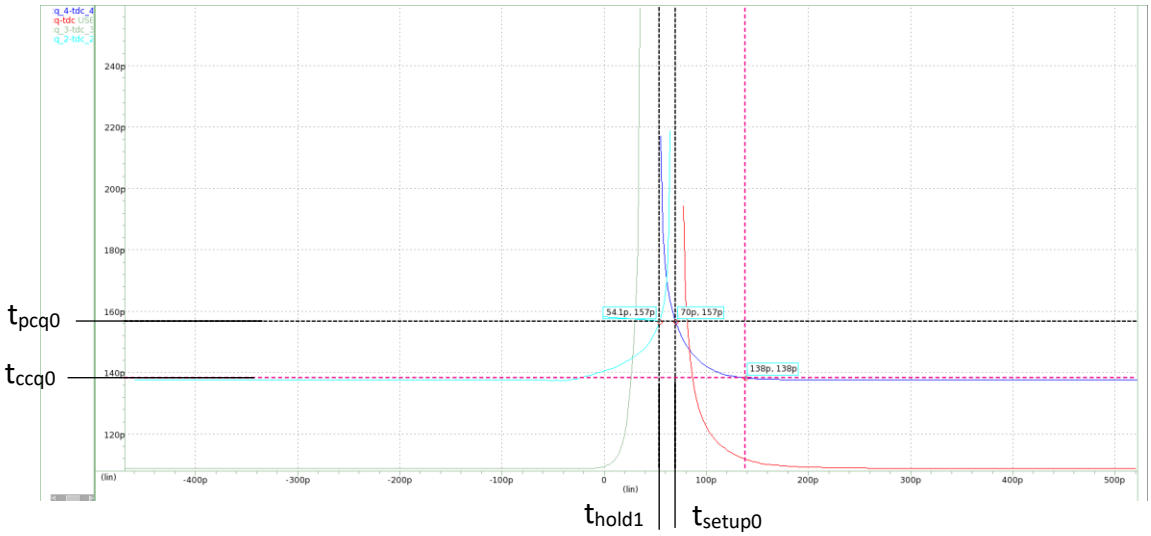
t_{Setup0} 70p $-t_{hold0}$ 54.1p t_{pcq0} 157p t_{ccq0} 138p

1C

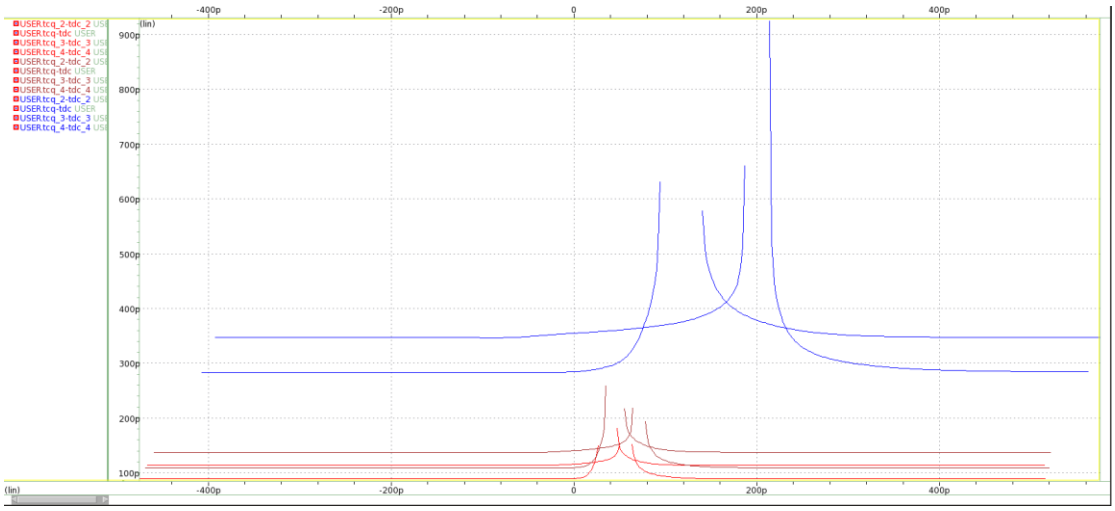
	t_{setup0}	t_{pcq0}	t_{ccq0}	$-t_{hold0}$
value	70ps	157ps	138ps	54.1ps
	t_{setup1}	t_{pcq1}	t_{ccq1}	$-t_{hold1}$
value	93.7ps	127ps	110ps	23.2ps
	t_{ar}	t_{af}		
value	39.6ps	46.8ps		

	Explanation
t_{setup0}	tDC when DFQF slope -1
t_{pcq0}	tCQ when DFQF slope -1
t_{ccq0}	Value when DFQF tCQ is almost horizontal
$-t_{hold0}$	Find DRQF tCQ = tpcq0 point, tDC = -thold0
t_{setup1}	tDC when DRQR slope -1
t_{pcq1}	tCQ when DRQR slope -1
t_{ccq1}	Value when DRQR tCQ is almost horizontal
$-t_{hold1}$	Find DRQR tCQ = tpcq0 point, tDC = -thold0
t_{ar}	tsetup1 thold0 for rise D
t_{af}	tsetup0 thold1 for fall D





2A



Brown TT corner, Blue SS corner, Red FF corner

2B

From 2A, it can be seen that the lines for the SS corner are very dispersed and also very large. The TT corner is in the middle, while the lines for the FF corner are very dense and relatively small.

Reasons:

TT is typical nmos and typical pmos. TT is the typical case, meaning the carrier mobility of both nmos and pmos is average, resulting in an average switching speed.

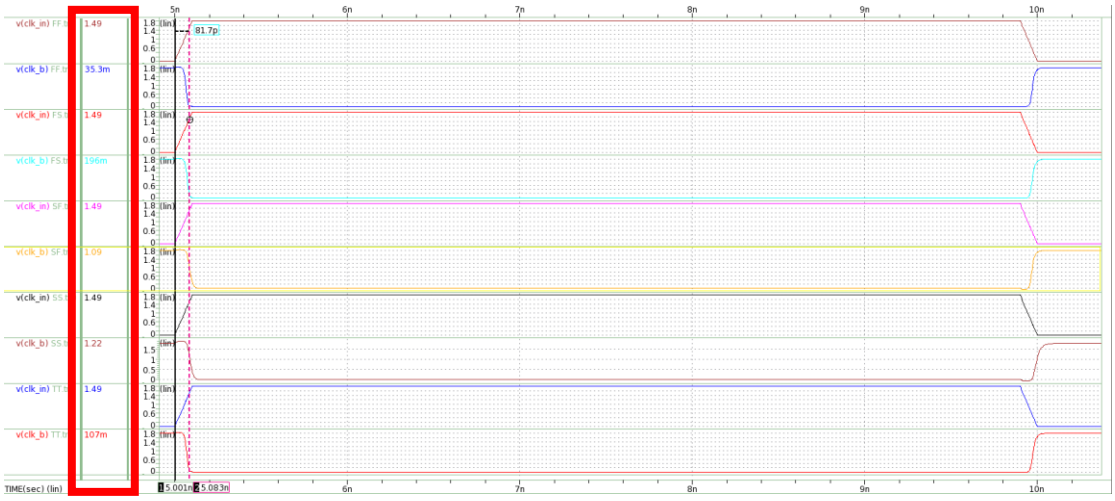
FF is fast nmos and fast pmos. FF is the best case, meaning the carrier mobility of both nmos and pmos is high, resulting in a faster switching speed. This also causes the lines to be denser and smaller.

SS is slow nmos and slow pmos. SS is the worst case, meaning the carrier mobility of both nmos and pmos is low, resulting in a slower switching speed. This also causes the lines to be dispersed and very large.

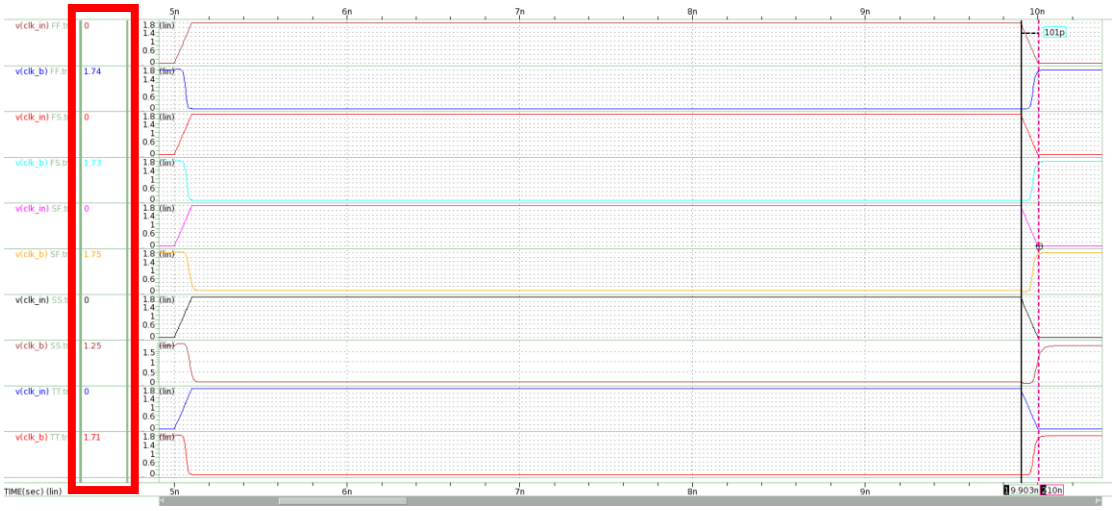
2C

Inverter:

The order is FF -> FS -> SF -> SS -> TT

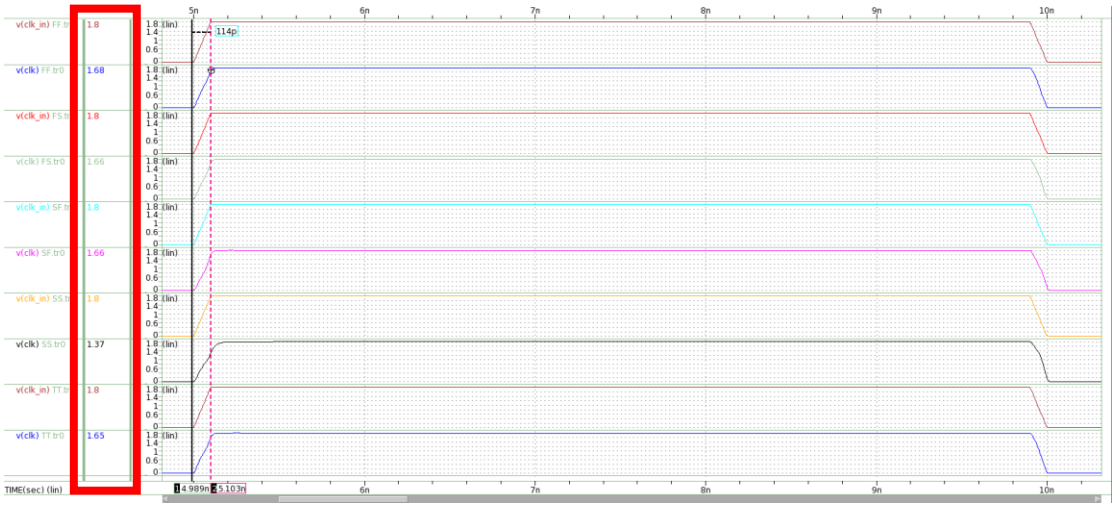


From V(clk_b), it can be observed that the speed of VDD to GND transition is FF > TT > FS > SF > SS. The VDD to GND transition mainly depends on the pull-down speed (NMOS). Since the first letter represents the NMOS speed, I believe that when it is F (Fast), the switching speed will be faster.

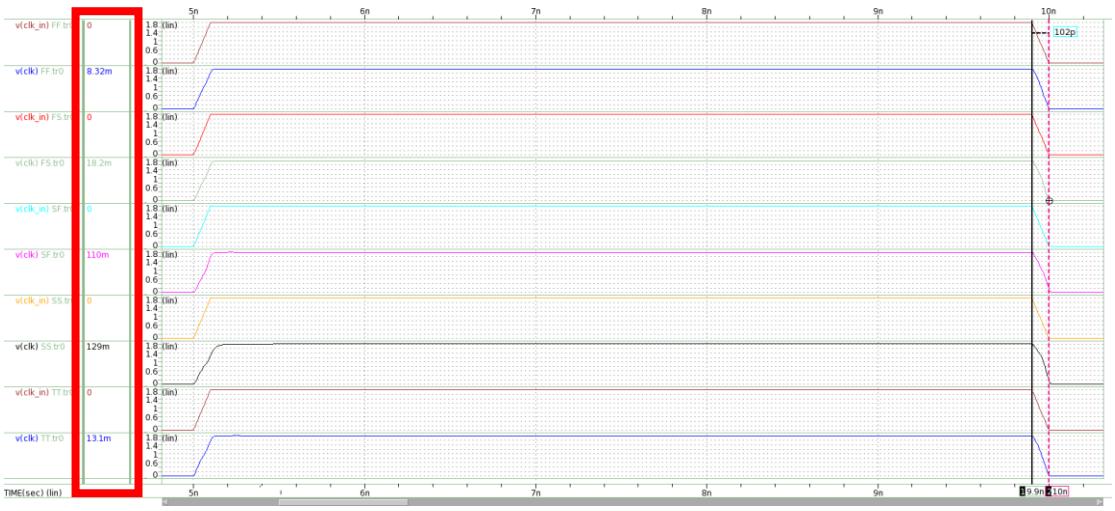


From V(clk_b), it can be observed that the speed of the GND to VDD transition is SF > FF > FS > TT > SS. The GND to VDD transition mainly depends on the pull-up speed (PMOS), because the second letter represents the PMOS speed. Therefore, I believe that when it is F (Fast), the switching speed will be faster.
However, from the results, I can see that the differences are not significant except for SS.

Transmission gate:
The order is FF->FS->SF->SS->TT

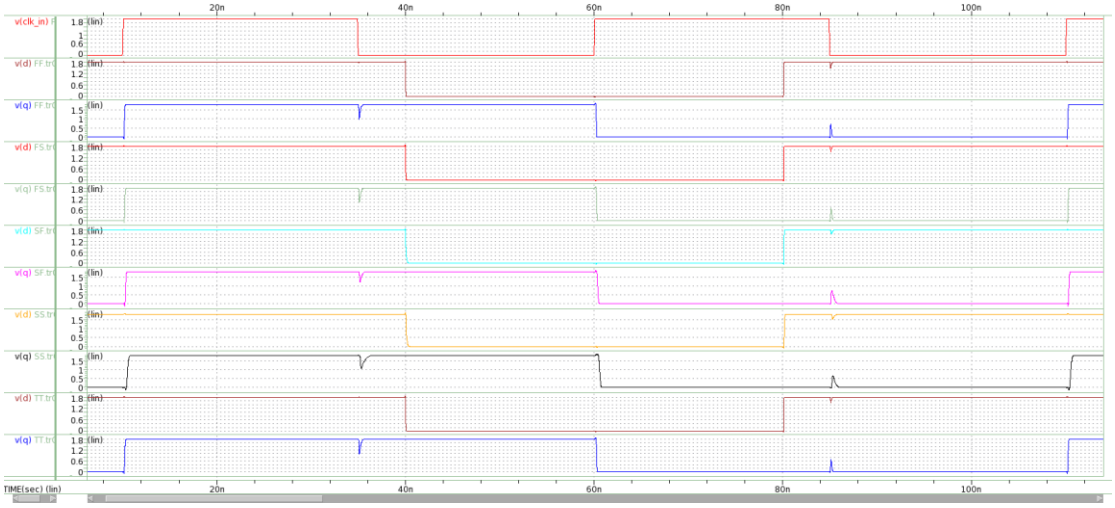


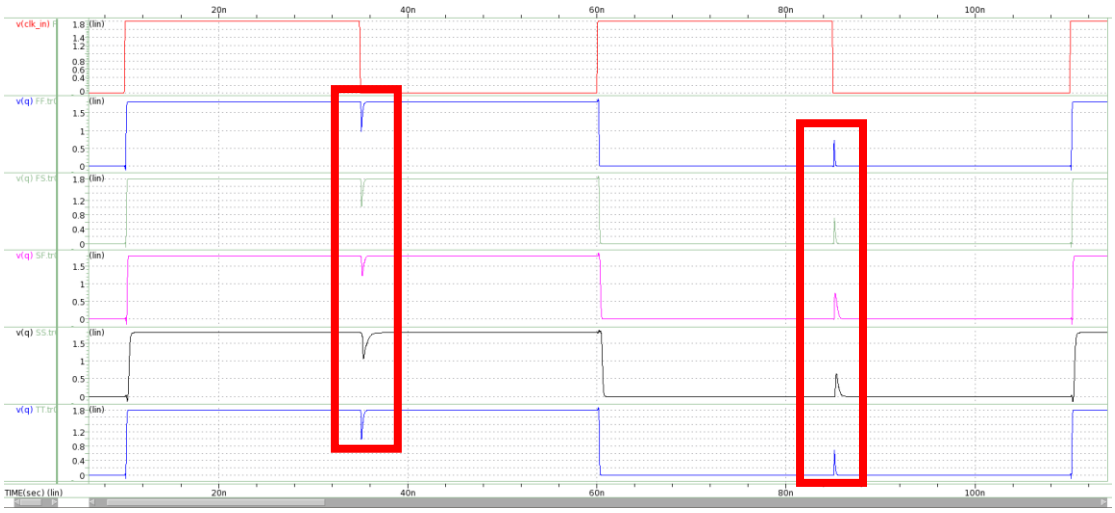
From V(clk_b), it can be observed that the speed of the GND to VDD transition is FF > FS = SF > TT > SS. Because the transmission gate has both NMOS and PMOS, I believe that when either corner is F (Fast), the switching speed will be faster.



From V(clk_b), it can be observed that the speed of the VDD to GND transition is FF > TT > FS > SF > SS. Because the transmission gate has both NMOS and PMOS transistors, I believe that when either corner is F (Fast), the switching speed will be faster.
However, from the results, I can see that the differences are not significant except for SS.

Flip-flop
The order is FF->FS->SF->SS->TT





From the waveform diagram, it can be observed that Q exhibits some fluctuations when clk switches. In the two red circles, it is clearly seen that the settling time for SS is the longest, while it is the shortest for FF. TT is relatively average. In the first red circle, the settling time is SF < FS, while in the second red circle, it is FS > SF. I believe this is related to the MOS transistors. When the first letter of the corner is F, the pull-down capability is stronger, so in the second red circle, the settling speed of FS is faster than SF. When the second letter of the corner is F, the pull-up capability is stronger, so in the first red circle, the settling speed of FS is slower than SF. The settling speed can affect the subsequent circuits and cause logical problems.