VLSI Circuit Design
Lab 3

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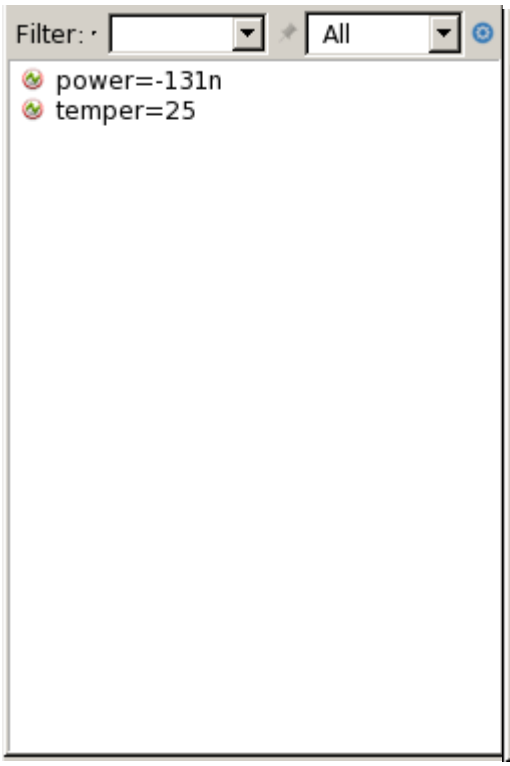
Problem 1 – Power

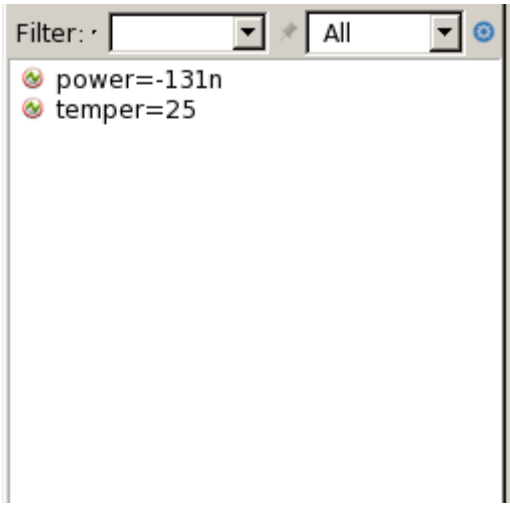
B



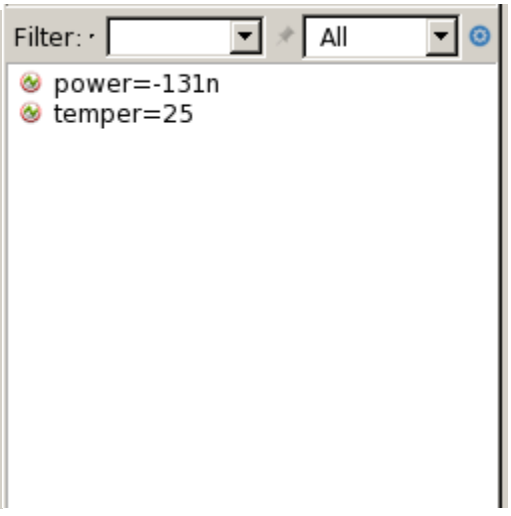
C

Compared to 'b', 'c' consumes more power. This is because the increased edge rates lead to a rise in short-circuit current, which in turn increases dynamic power dissipation.

b’



c’



Adding a 2-stage inverter buffer results in a more stable voltage, leading to more consistent power consumption that is less susceptible to variations in edge time.

Problem 2 – Ring Oscillator

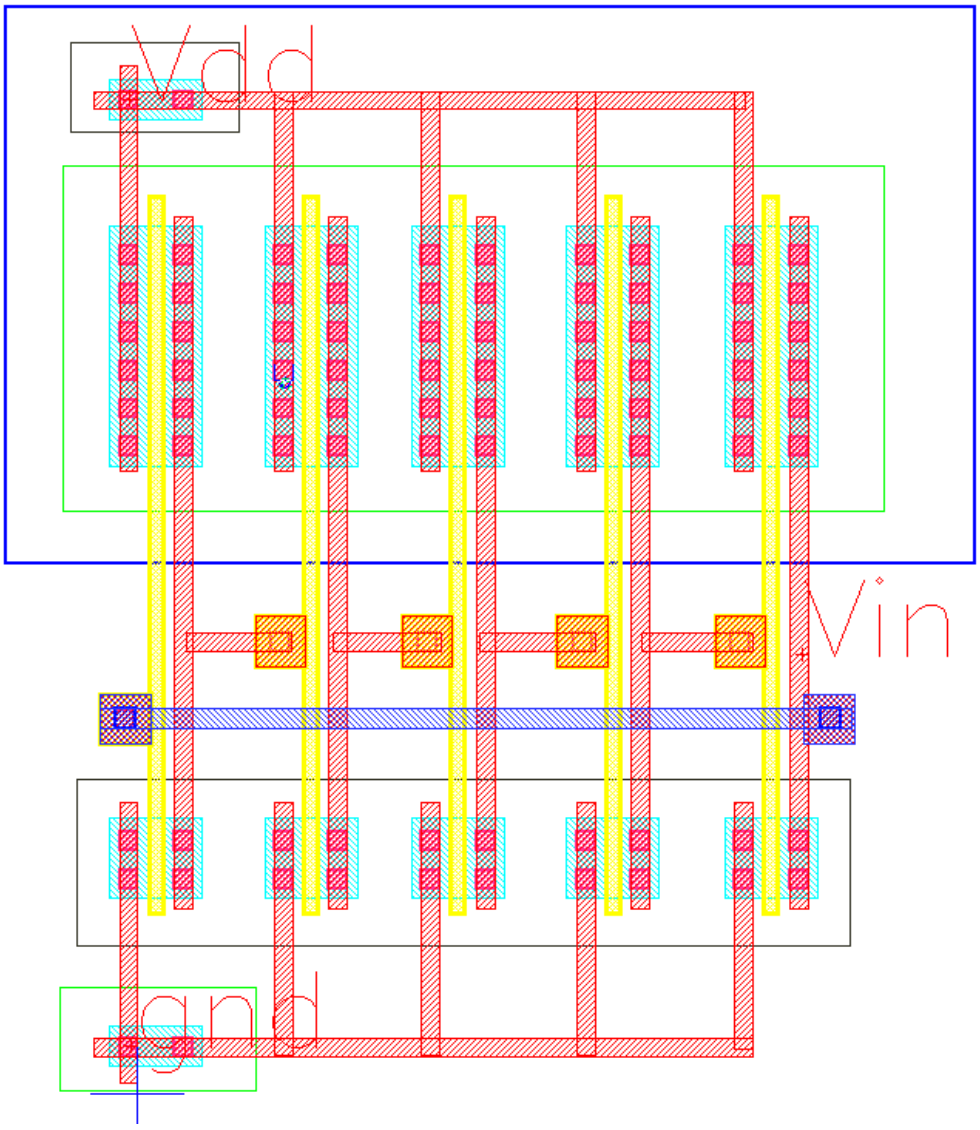
2A

Initially, a 7-stage design was assumed. However, it was found that no matter how much the width (w) of the PMOS transistors was adjusted, the design could not meet the required specifications. Therefore, the number of stages was reduced to 5. The optimal PMOS width was then investigated. A coarse search was performed in 1µm increments, revealing that the specifications were met when the width was between 4µm and 5µm. The interval was then narrowed, and it was found that the specifications were met when the PMOS width was 4.85µm. The NMOS transistor size was kept constant at 1µm throughout this process.

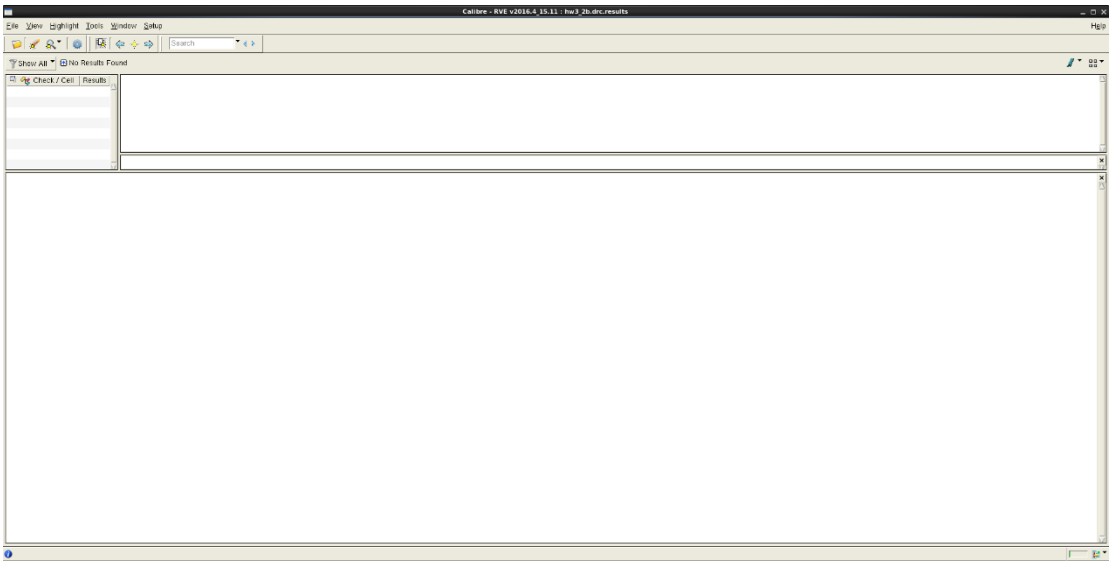
```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=1
.TITLE '.protect'
 wl               period           frequency        t_on
                  duty_cycle       temper           alter#
  4.000e-06        3.594e-10        2.783e+09        1.842e-10
                   5.125e-01        2.500e+01       1
  4.050e-06        3.608e-10        2.771e+09        1.850e-10
                   5.128e-01        2.500e+01       1
  4.100e-06        3.623e-10        2.760e+09        1.859e-10
                   5.130e-01        2.500e+01       1
  4.150e-06        3.637e-10        2.749e+09        1.867e-10
                   5.133e-01        2.500e+01       1
  4.200e-06        3.652e-10        2.739e+09        1.876e-10
                   5.138e-01        2.500e+01       1
  4.250e-06        3.666e-10        2.728e+09        1.885e-10
                   5.140e-01        2.500e+01       1
  4.300e-06        3.681e-10        2.717e+09        1.893e-10
                   5.143e-01        2.500e+01       1
  4.350e-06        3.696e-10        2.706e+09        1.902e-10
                   5.146e-01        2.500e+01       1
  4.400e-06        3.711e-10        2.695e+09        1.910e-10
                   5.148e-01        2.500e+01       1
  4.450e-06        3.725e-10        2.685e+09        1.919e-10
                   5.152e-01        2.500e+01       1
  4.500e-06        3.740e-10        2.674e+09        1.928e-10
                   5.155e-01        2.500e+01       1
  4.550e-06        3.755e-10        2.663e+09        1.937e-10
                   5.158e-01        2.500e+01       1
  4.600e-06        3.770e-10        2.653e+09        1.945e-10
                   5.160e-01        2.500e+01       1
  4.650e-06        3.785e-10        2.642e+09        1.954e-10
                   5.163e-01        2.500e+01       1
  4.700e-06        3.800e-10        2.632e+09        1.963e-10
                   5.166e-01        2.500e+01       1
  4.750e-06        3.814e-10        2.622e+09        1.972e-10
                   5.169e-01        2.500e+01       1
  4.800e-06        3.829e-10        2.612e+09        1.980e-10
                   5.172e-01        2.500e+01       1
  4.850e-06        3.843e-10        2.602e+09        1.988e-10
                   5.174e-01        2.500e+01       1
  4.900e-06        3.858e-10        2.592e+09        1.997e-10
                   5.177e-01        2.500e+01       1
  4.950e-06        3.872e-10        2.582e+09        2.006e-10
                   5.179e-01        2.500e+01       1
  5.000e-06        3.888e-10        2.572e+09        2.014e-10
                   5.181e-01        2.500e+01       1
```

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '.protect'
 period           frequency        t_on             duty_cycle
 temper           alter#
  3.844e-10        2.601e+09        1.989e-10        5.174e-01
  2.500e+01       1
```

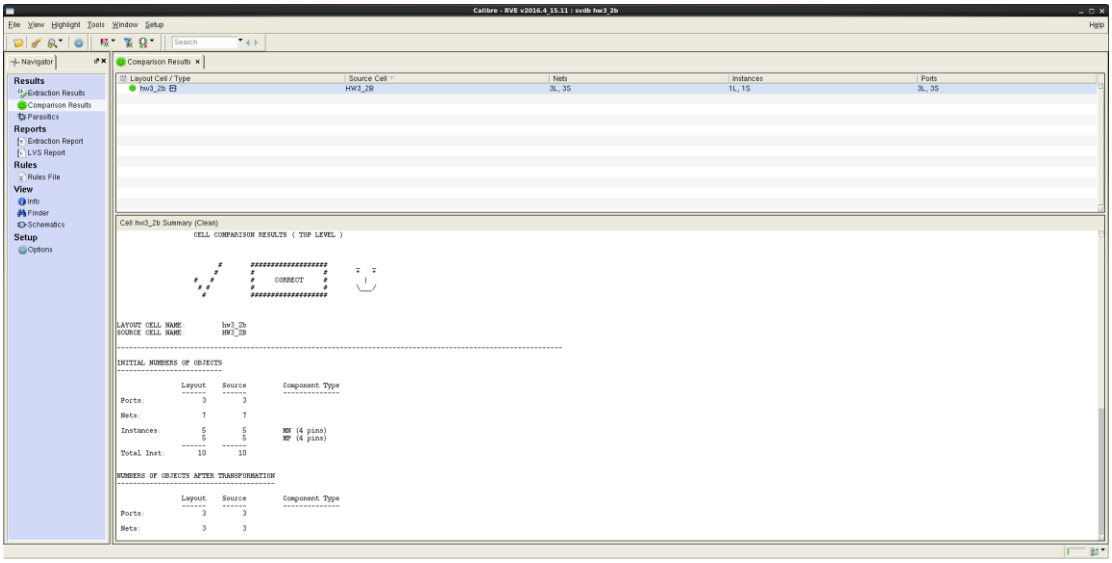
2B



Layout



DRC



LVS

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '.protect'
 period            frequency        t_on             duty_cycle
 temper            alter#
  3.845e-10         2.601e+09        1.935e-10         5.034e-01
  2.500e+01        1
```

After several adjustments, it was found that when the PMOS was 3μm and the NMOS was 1μm, the design met the required specifications after layout.

2C

Initially, I assumed a 3-stage design for this problem. Then, keeping the size of all NMOS transistors fixed, I adjusted the size of the PMOS transistors to see if the required specifications could be met. I assumed that the PMOS transistor closer to Vctrl (control voltage) - PMOS1 - is responsible for

adjusting the duty cycle, while the one farther away - PMOS2 - is responsible for adjusting the frequency. When Vctrl=Vctrlb=0.9V, I first tried to adjust the duty cycle to approximately 50%, and then adjusted the frequency to 2.6GHz. After several adjustments, the size of PMOS1 was determined to be 7.8μm, and the size of PMOS2 was 1.9μm. Then, using a sweep analysis, I checked if the frequency coverage from 2.5GHz to 2.7GHz when Vctrl = 0.7~1.1V and Vctrlb= 1.8V – Vctrl meets the required specifications.

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=1
.TITLE '.protect'
 x                period           frequency        t_on
                  duty_cycle       temper           alter#
   7.000e-01       2.918e-10        3.427e+09        1.441e-10
                   4.937e-01        2.500e+01       1
   8.000e-01       3.260e-10        3.067e+09        1.618e-10
                   4.964e-01        2.500e+01       1
   9.000e-01       3.843e-10        2.602e+09        1.924e-10
                   5.008e-01        2.500e+01       1
   1.000e+00       4.946e-10        2.022e+09        2.521e-10
                   5.098e-01        2.500e+01       1
   1.100e+00       7.409e-10        1.350e+09        3.922e-10
                   5.293e-01        2.500e+01       1
```

Problem 3 - Power Delay Product

3C

w1: NMOS size

	w1	power	rising_delay	falling_delay
		delay_avg	pdp	temper
		alter#		
42	1.600e-06	-2.569e-06	1.980e-10	1.980e-10
43		1.980e-10	-5.087e-16	2.500e+01
44		1		
45	1.650e-06	-2.583e-06	1.962e-10	1.962e-10
46		1.962e-10	-5.066e-16	2.500e+01
47		1		
48	1.700e-06	-2.596e-06	1.947e-10	1.947e-10
49		1.947e-10	-5.053e-16	2.500e+01
50		1		
51	1.750e-06	-2.610e-06	1.934e-10	1.934e-10
52		1.934e-10	-5.047e-16	2.500e+01
53		1		
54	1.800e-06	-2.623e-06	1.923e-10	1.923e-10
55		1.923e-10	-5.044e-16	2.500e+01
56		1		
57	1.850e-06	-2.636e-06	1.912e-10	1.912e-10
58		1.912e-10	-5.041e-16	2.500e+01
59		1		
60	1.900e-06	-2.650e-06	1.903e-10	1.903e-10
61		1.903e-10	-5.041e-16	2.500e+01
62		1		
63	1.950e-06	-2.664e-06	1.895e-10	1.895e-10
64		1.895e-10	-5.047e-16	2.500e+01
65		1		
66	2.000e-06	-2.677e-06	1.888e-10	1.888e-10
67		1.888e-10	-5.053e-16	2.500e+01
68		1		
69	2.050e-06	-2.690e-06	1.882e-10	1.882e-10
70		1.882e-10	-5.063e-16	2.500e+01
71		1		

Find min PDP

NMOS size=1.85um PMOS size=5.55um

80		1		
81	2.250e-06	-2.744e-06	1.868e-10	1.868e-10
82		1.868e-10	-5.125e-16	2.500e+01
83		1		
84	2.300e-06	-2.758e-06	1.867e-10	1.867e-10
85		1.867e-10	-5.149e-16	2.500e+01
86		1		
87	2.350e-06	-2.772e-06	1.866e-10	1.866e-10
88		1.866e-10	-5.172e-16	2.500e+01
89		1		
90	2.400e-06	-2.786e-06	1.865e-10	1.865e-10
91		1.865e-10	-5.196e-16	2.500e+01
92		1		
93	2.450e-06	-2.800e-06	1.866e-10	1.866e-10
94		1.866e-10	-5.223e-16	2.500e+01
95		1		
96	2.500e-06	-2.813e-06	1.866e-10	1.866e-10
97		1.866e-10	-5.250e-16	2.500e+01
98		1		
99	2.550e-06	-2.828e-06	1.868e-10	1.868e-10
100		1.868e-10	-5.282e-16	2.500e+01
101		1		
102	2.600e-06	-2.842e-06	1.869e-10	1.869e-10
103		1.869e-10	-5.311e-16	2.500e+01

Find min delay_avg
NMOS size=2.4um PMOS size=7.2um

Inverter size	t_{pdr}	t_{pdf}	t_{pd}	P_{avg}	t_{pd}* P_{avg}
P:5.55um N:1.85um	1.912e-10	1.912e-10	1.912e-10	2.636e-06	5.041e-16

Table.1 the best sizeds chosen from the minimum PDP

According to the formula $P=\alpha CVDD^2f$, when C increases, P also increases. D=2+128/4w+4w/2, therefore it can be observed that D resembles a curve, and a minimum value can be found.
Therefore, to find the minimum PDP, it is necessary to know where the minimum D occurs. However, since P increases with C, the minimum D does not necessarily correspond to the minimum PDP. Thus, only the approximate range of PDP can be determined. Finally, sweeping can be used to obtain the minimum PDP.