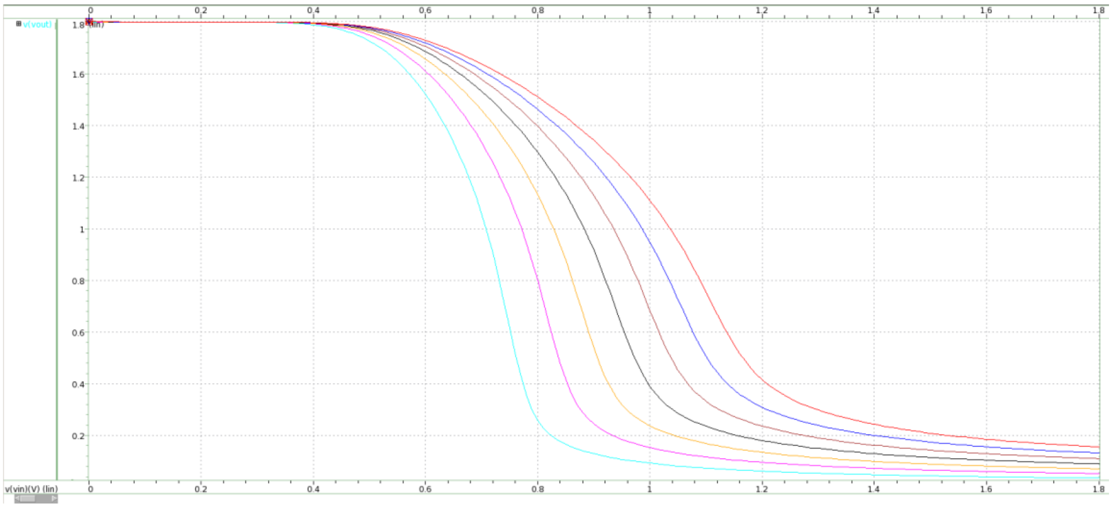
VLSI Circuit Design
Lab 4

Yu-Chi Chu

Problem 1 – Pseudo-nMOS Inverter analysis

1A



Vout versus Vin (Vin as x-axis) with various widths of pMOS

1B

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=1
.TITLE '.protect'
 alpha            vil              vol              vih
                  voh              nmh              nml
                  temper           alter#
  5.000e-07        4.917e-01        1.597e-01        8.568e-01
                   1.736e+00        8.794e-01        3.320e-01
                   2.500e+01       1
  7.500e-07        5.222e-01        1.945e-01        9.392e-01
                   1.729e+00        7.894e-01        3.277e-01
                   2.500e+01       1
  1.000e-06        5.504e-01        2.246e-01        1.012e+00
                   1.720e+00        7.073e-01        3.257e-01
                   2.500e+01       1
  1.250e-06        5.787e-01        2.523e-01        1.080e+00
                   1.709e+00        6.287e-01        3.264e-01
                   2.500e+01       1
  1.500e-06        6.087e-01        2.781e-01        1.145e+00
                   1.696e+00        5.511e-01        3.306e-01
                   2.500e+01       1
  1.750e-06        6.417e-01        3.029e-01        1.206e+00
                   1.680e+00        4.733e-01        3.388e-01
                   2.500e+01       1
  2.000e-06        6.786e-01        3.267e-01        1.266e+00
                   1.660e+00        3.941e-01        3.519e-01
                   2.500e+01       1
```

α	Vil(V)	Vih(V)	Vol(V)	Voh(V)	NMH(V)	NML(V)
0.5	0.4917	0.8568	0.1597	1.736	0.8794	0.3320
0.75	0.5222	0.9392	0.1945	1.729	0.7894	0.3277
1	0.5504	1.012	0.2246	1.720	0.7073	0.3257
1.25	0.5787	1.080	0.2523	1.709	0.6287	0.3264
1.5	0.6087	1.145	0.2781	1.696	0.5511	0.3306
1.75	0.6417	1.206	0.3029	1.680	0.4733	0.3388
2	0.6786	1.266	0.3267	1.660	0.3941	0.3519

Measurement

why noise NML is much smaller than NMH?

NML (Noise Margin Low) is related to the NMOS transistor's ability to pull the output voltage down to ground. NMH (Noise Margin High) is related to the PMOS transistor's ability to pull the output voltage up to VDD (supply voltage). Initially, when α (alpha/duty cycle) is small, the PMOS pull-up capability is weak, resulting in a larger NMH, significantly greater than NML. However, as α increases, NMH gradually decreases, and the difference between NMH and NML diminishes. Since the NMOS size remains unchanged, NML remains almost constant.

1C

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=1
.TITLE '.protect'
 alpha            trise            temper           alter#
  5.000e-07        1.708e-09        2.500e+01        1
  7.500e-07        1.177e-09        2.500e+01        1
  1.000e-06        9.034e-10        2.500e+01        1
  1.250e-06        7.314e-10        2.500e+01        1
  1.500e-06        6.155e-10        2.500e+01        1
  1.750e-06        5.297e-10        2.500e+01        1
  2.000e-06        4.656e-10        2.500e+01        1
```

Problem 2 – Gate Comparison

2B

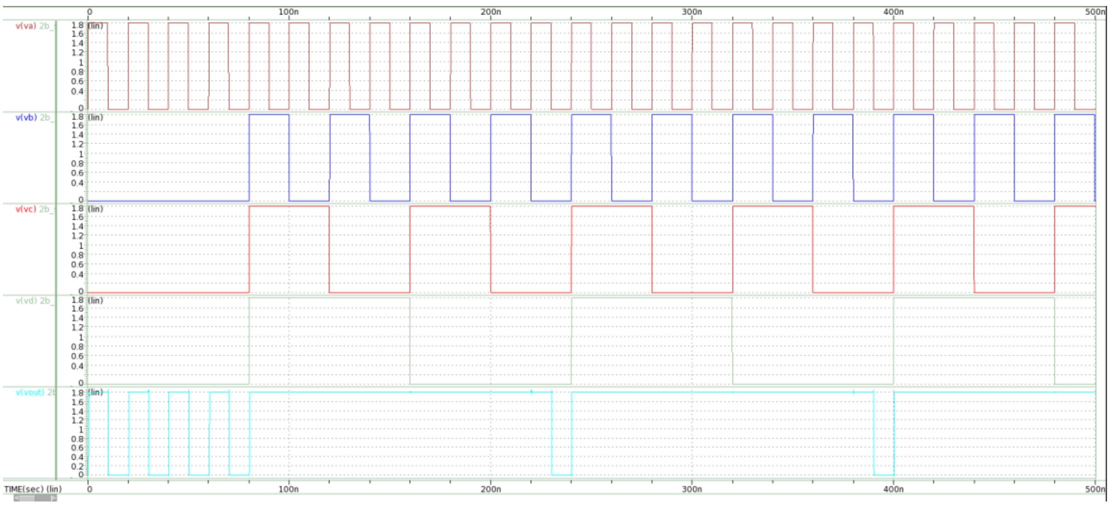
In 2A, I have calculated the theoretically minimum delay size. In the simulation results, I used a sweep to adjust the size of 2A to minimize the delay as much as possible.

(1) Static

I fixed the NMOS size and multiplied the PMOS size by W1. I found that the minimum delay occurred when W1=1. Therefore, the PMOS size calculated in 2A was multiplied by 1.

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=1
.TITLE '.protect'
 w1                 trise             tfall             tdelay_avg
                    temper            alter#
   5.000e-01         1.545e-10         1.371e-10         1.458e-10
                     2.500e+01        1
   5.500e-01         1.492e-10         1.336e-10         1.414e-10
                     2.500e+01        1
   6.000e-01         1.457e-10         1.308e-10         1.382e-10
                     2.500e+01        1
   6.500e-01         1.431e-10         1.284e-10         1.358e-10
                     2.500e+01        1
   7.000e-01         1.413e-10         1.263e-10         1.338e-10
                     2.500e+01        1
   7.500e-01         1.402e-10         1.246e-10         1.324e-10
                     2.500e+01        1
   8.000e-01         1.393e-10         1.231e-10         1.312e-10
                     2.500e+01        1
   8.500e-01         1.390e-10         1.217e-10         1.304e-10
                     2.500e+01        1
   9.000e-01         1.390e-10         1.206e-10         1.298e-10
                     2.500e+01        1
   9.500e-01         1.393e-10         1.196e-10         1.295e-10
                     2.500e+01        1
   1.000e+00         1.398e-10         1.188e-10         1.293e-10
                     2.500e+01        1
   1.050e+00         1.405e-10         1.181e-10         1.293e-10
                     2.500e+01        1
   1.100e+00         1.415e-10         1.174e-10         1.294e-10
                     2.500e+01        1
   1.150e+00         1.425e-10         1.168e-10         1.296e-10
                     2.500e+01        1
   1.200e+00         1.436e-10         1.163e-10         1.300e-10
                     2.500e+01        1
   1.250e+00         1.449e-10         1.159e-10         1.304e-10
                     2.500e+01        1
   1.300e+00         1.463e-10         1.156e-10         1.309e-10
                     2.500e+01        1
   1.350e+00         1.477e-10         1.153e-10         1.315e-10
                     2.500e+01        1
```

Whenever the input = 0, output = 0



Delay after size adjustment

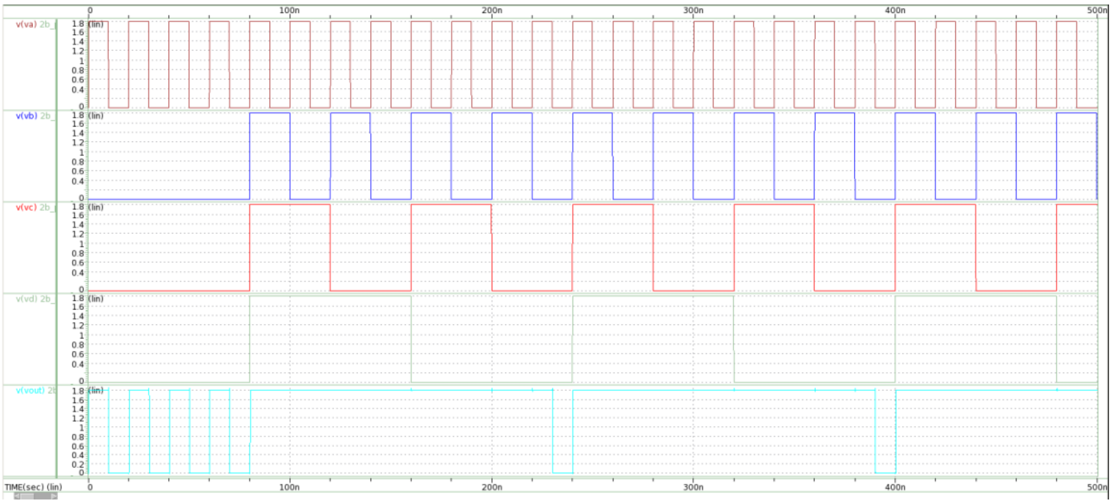
```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '.protect'
 trise            tfall            tdelay_avg       temper
 alter#
  1.398e-10        1.188e-10        1.293e-10        2.500e+01
1
```

(2) Pseudo nMOS

I fixed the PMOS size and multiplied the NMOS size by W1. I found that the minimum delay occurred when W1=0.5. Therefore, the NMOS size calculated in 2A was multiplied by 0.5.

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=1
.TITLE '.protect'
 w1               trise            tfall            tdelay_avg
                  temper           alter#
  5.000e-01        6.248e-11        7.888e-11        7.068e-11
                   2.500e+01       1
  5.500e-01        6.343e-11        8.067e-11        7.205e-11
                   2.500e+01       1
  6.000e-01        6.436e-11        8.276e-11        7.356e-11
                   2.500e+01       1
  6.500e-01        6.524e-11        8.499e-11        7.512e-11
                   2.500e+01       1
  7.000e-01        6.614e-11        8.729e-11        7.672e-11
                   2.500e+01       1
  7.500e-01        6.699e-11        8.978e-11        7.839e-11
                   2.500e+01       1
  8.000e-01        6.790e-11        9.229e-11        8.009e-11
                   2.500e+01       1
  8.500e-01        6.871e-11        9.483e-11        8.177e-11
                   2.500e+01       1
  9.000e-01        6.959e-11        9.740e-11        8.349e-11
                   2.500e+01       1
  9.500e-01        7.040e-11        1.000e-10        8.521e-11
                   2.500e+01       1
  1.000e+00        7.123e-11        1.027e-10        8.695e-11
                   2.500e+01       1
  1.050e+00        7.210e-11        1.053e-10        8.872e-11
                   2.500e+01       1
  1.100e+00        7.295e-11        1.079e-10        9.045e-11
                   2.500e+01       1
  1.150e+00        7.379e-11        1.106e-10        9.220e-11
                   2.500e+01       1
  1.200e+00        7.463e-11        1.132e-10        9.394e-11
                   2.500e+01       1
  1.250e+00        7.546e-11        1.159e-10        9.569e-11
                   2.500e+01       1
  1.300e+00        7.627e-11        1.186e-10        9.741e-11
                   2.500e+01       1
  1.350e+00        7.708e-11        1.212e-10        9.915e-11
                   2.500e+01       1
  1.400e+00        7.789e-11        1.239e-10        1.009e-10
                   2.500e+01       1
  1.450e+00        7.871e-11        1.265e-10        1.026e-10
                   2.500e+01       1
```

Whenever the input = 0, output = 0



Delay after size adjustment

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '.protect'
 trise            tfall            tdelay_avg       temper
 alter#
  6.248e-11        7.888e-11        7.068e-11        2.500e+01
1
```

(3) Domino

In the domino circuit, I only adjusted the size of the input NMOS, excluding the high skew inverter. I found that the minimum delay occurred when W1=2. Therefore, the NMOS size calculated in 2A was multiplied by 2.

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=1
.TITLE '.protect'
 w1               trise            temper           alter#
  1.500e+00        1.086e-10        2.500e+01       1
  1.550e+00        1.083e-10        2.500e+01       1
  1.600e+00        1.080e-10        2.500e+01       1
  1.650e+00        1.078e-10        2.500e+01       1
  1.700e+00        1.076e-10        2.500e+01       1
  1.750e+00        1.074e-10        2.500e+01       1
  1.800e+00        1.073e-10        2.500e+01       1
  1.850e+00        1.072e-10        2.500e+01       1
  1.900e+00        1.071e-10        2.500e+01       1
  1.950e+00        1.071e-10        2.500e+01       1
  2.000e+00        1.070e-10        2.500e+01       1
  2.050e+00        1.070e-10        2.500e+01       1
  2.100e+00        1.070e-10        2.500e+01       1
  2.150e+00        1.070e-10        2.500e+01       1
  2.200e+00        1.070e-10        2.500e+01       1
  2.250e+00        1.071e-10        2.500e+01       1
  2.300e+00        1.071e-10        2.500e+01       1
  2.350e+00        1.072e-10        2.500e+01       1
  2.400e+00        1.073e-10        2.500e+01       1
  2.450e+00        1.074e-10        2.500e+01       1
  2.500e+00        1.075e-10        2.500e+01       1
```

At abcd = 0 or clk = 0, output = 0

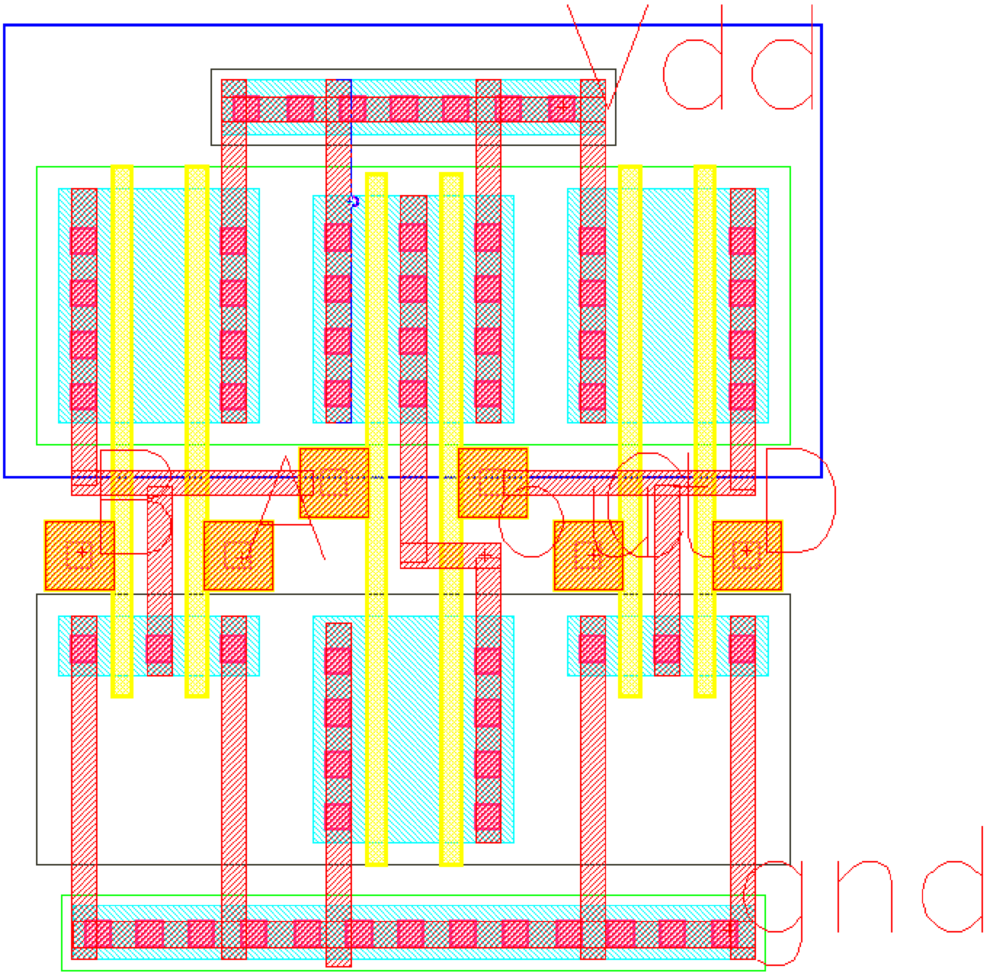
Delay after size adjustment

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '.protect'
 trise            temper           alter#
  1.070e-10        2.500e+01       1
```

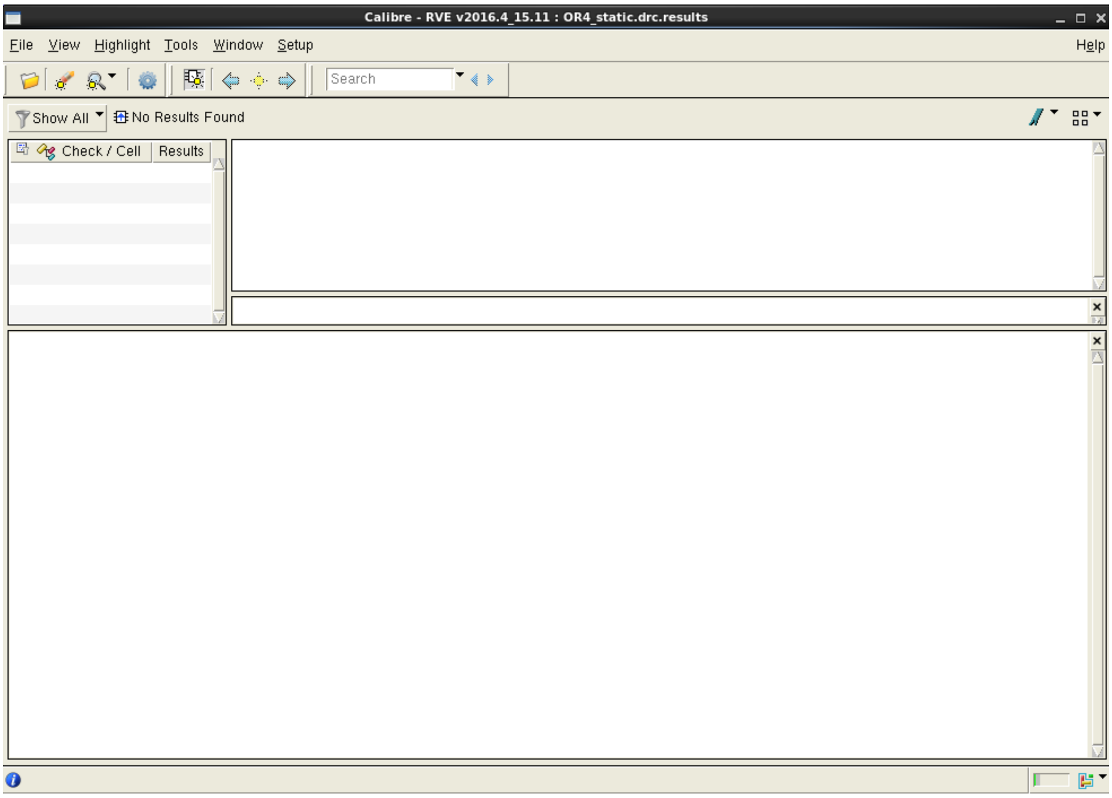
2C

(1) Static

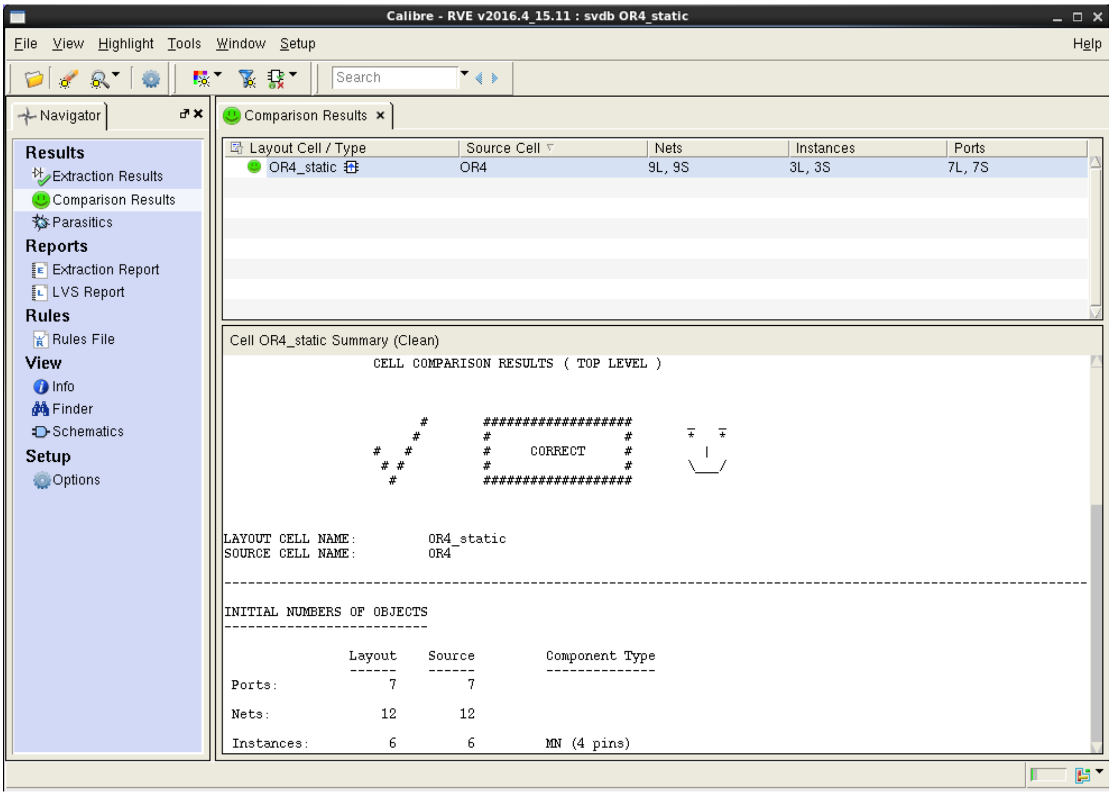
layout



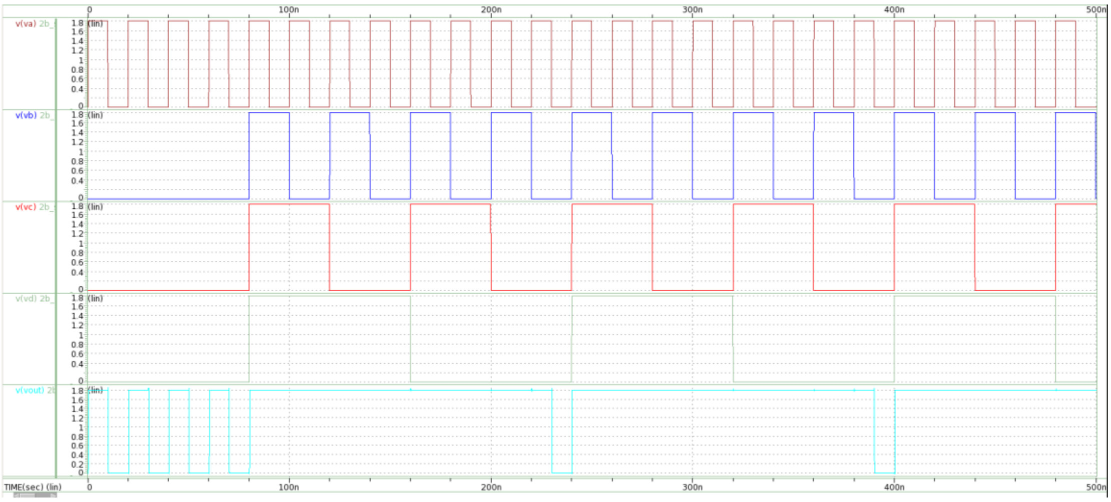
DRC


Calibre - RVE v2016.4_15.11 : OR4_static.drc.results
File View Highlight Tools Window Setup
Help
Search
Show All
No Results Found
Check / Cell
Results

LVS


Calibre - RVE v2016.4_15.11 : svdb OR4_static
File View Highlight Tools Window Setup
Help
Search
Navigator
Results
Extraction Results
Comparison Results
Parasitics
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
OR4_static
OR4
9L, 9S
3L, 3S
7L, 7S
Cell OR4_static Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: OR4_static
SOURCE CELL NAME: OR4
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 7 7
Nets: 12 12
Instances: 6 6 MN (4 pins)

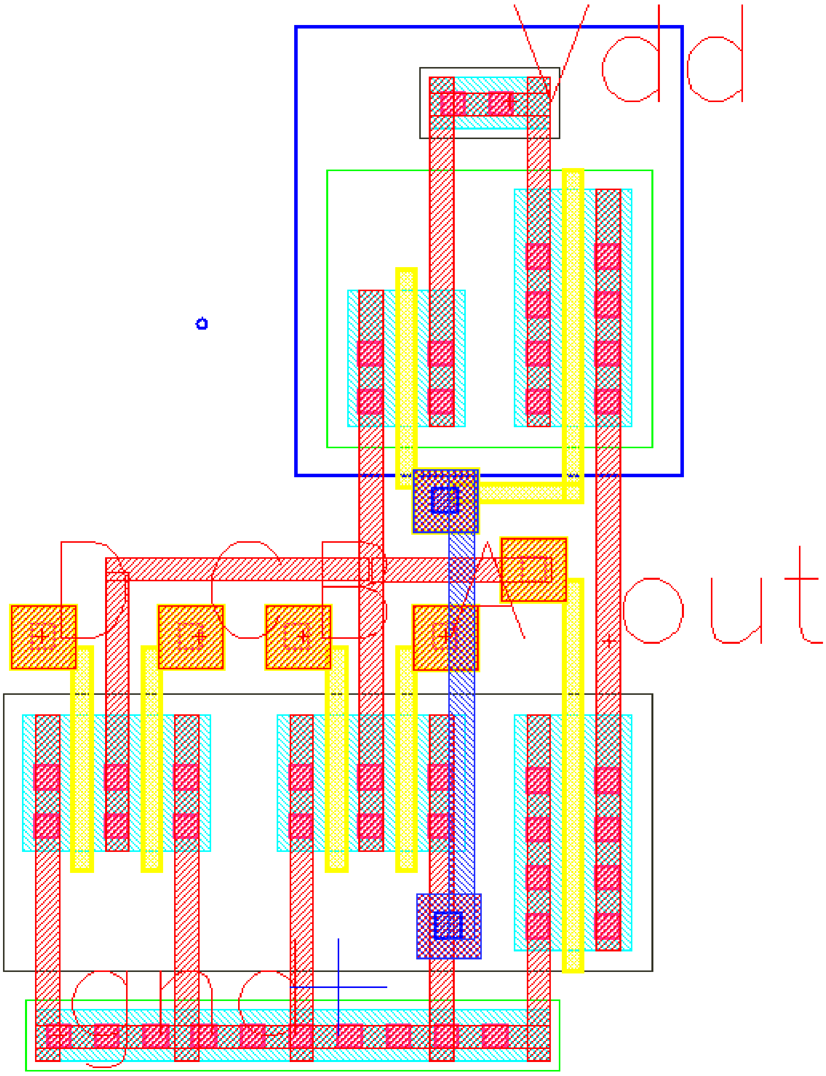
Simulation



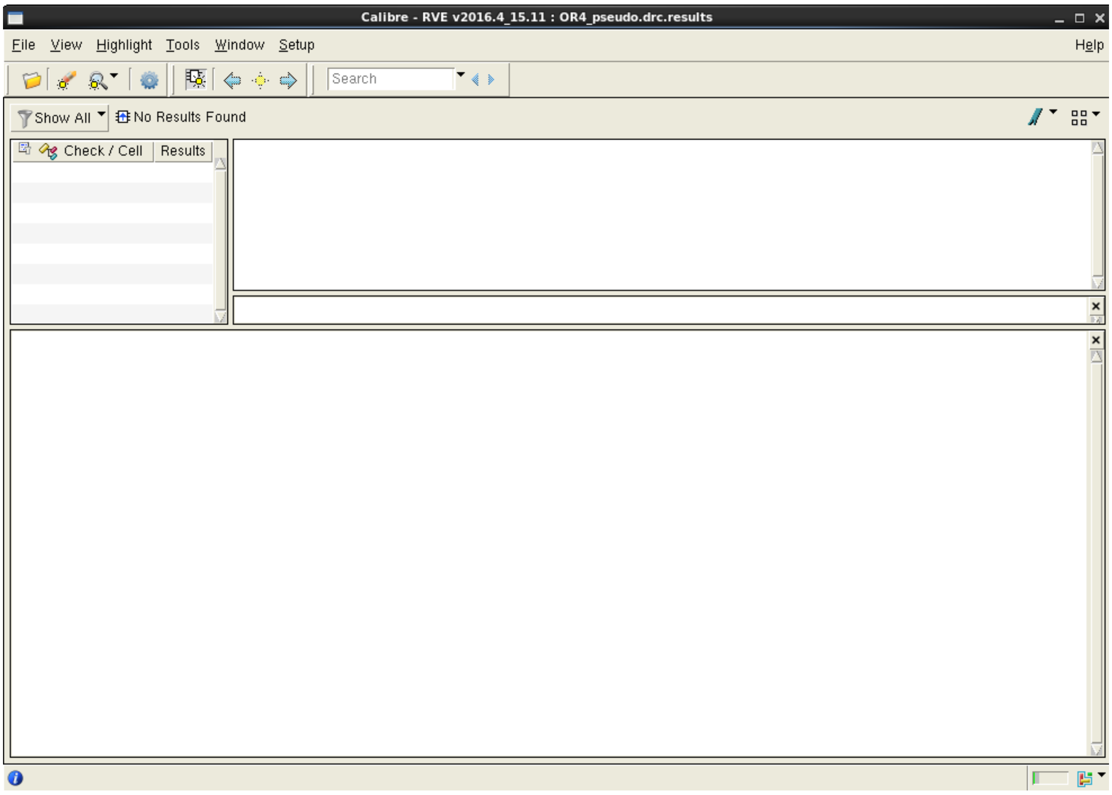

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '.protect'
 trise             tfall             tdelay_avg        temper
 alter#
  1.521e-10         1.237e-10         1.379e-10         2.500e+01
1
```

(2) Pseudo nMOS

Layout

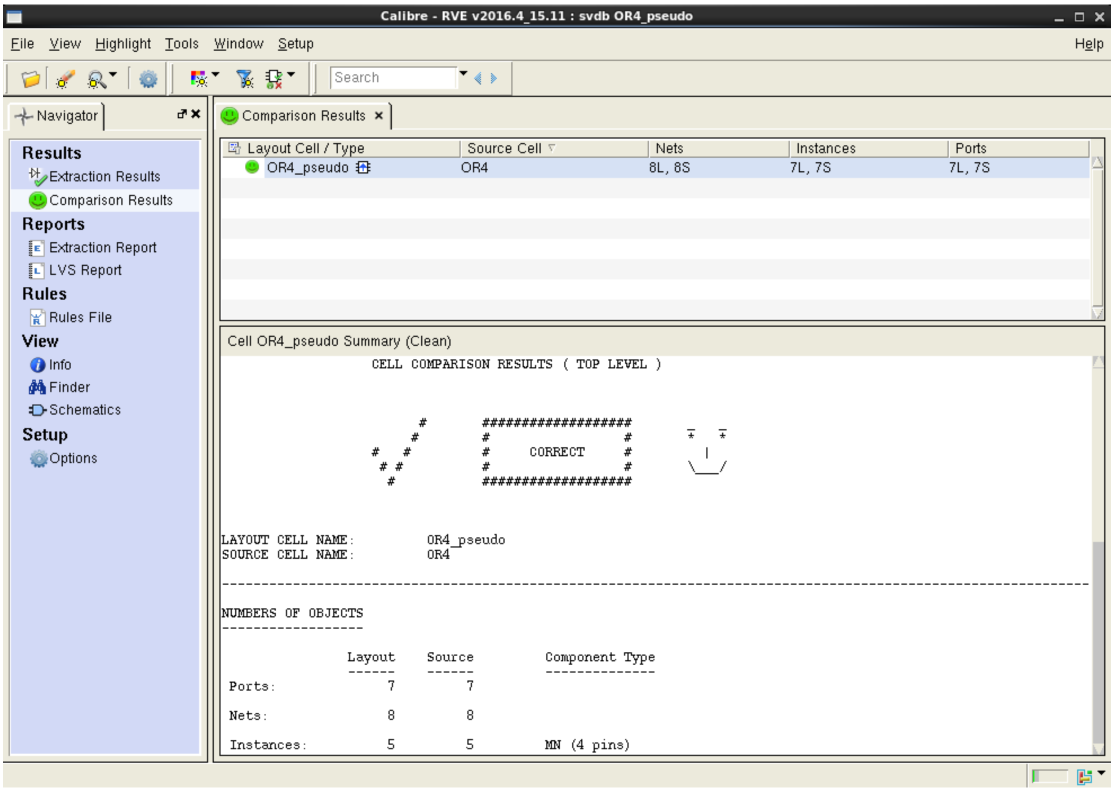


DRC



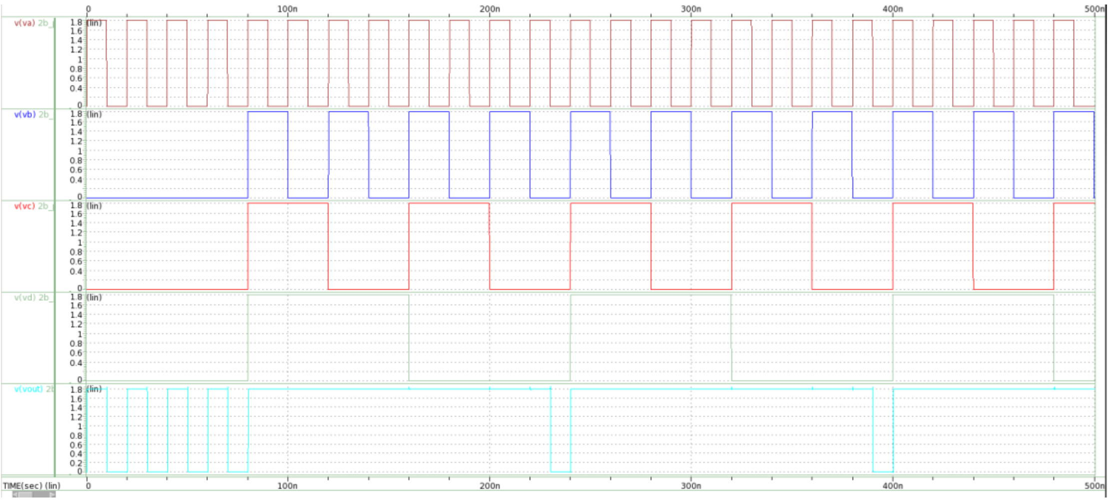
Calibre - RVE v2016.4_15.11 : OR4_pseudo.drc.results
File View Highlight Tools Window Setup
Help
Search
Show All
No Results Found
Check / Cell
Results

LVS



Calibre - RVE v2016.4_15.11 : svdb OR4_pseudo
File View Highlight Tools Window Setup
Help
Search
Navigator
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
OR4_pseudo
OR4
8L, 8S
7L, 7S
7L, 7S
Cell OR4_pseudo Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: OR4_pseudo
SOURCE CELL NAME: OR4
NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 7 7
Nets: 8 8
Instances: 5 5 MN (4 pins)

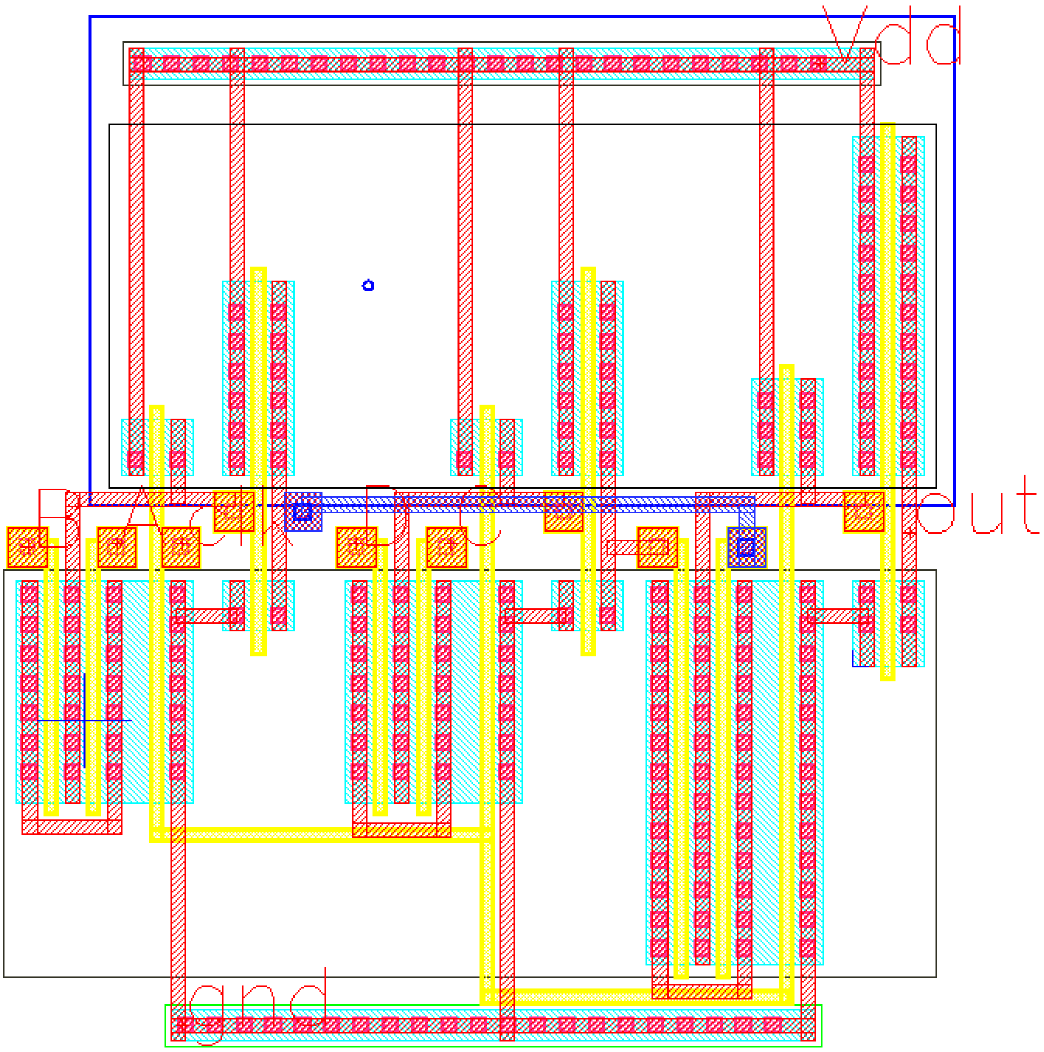
Simulation



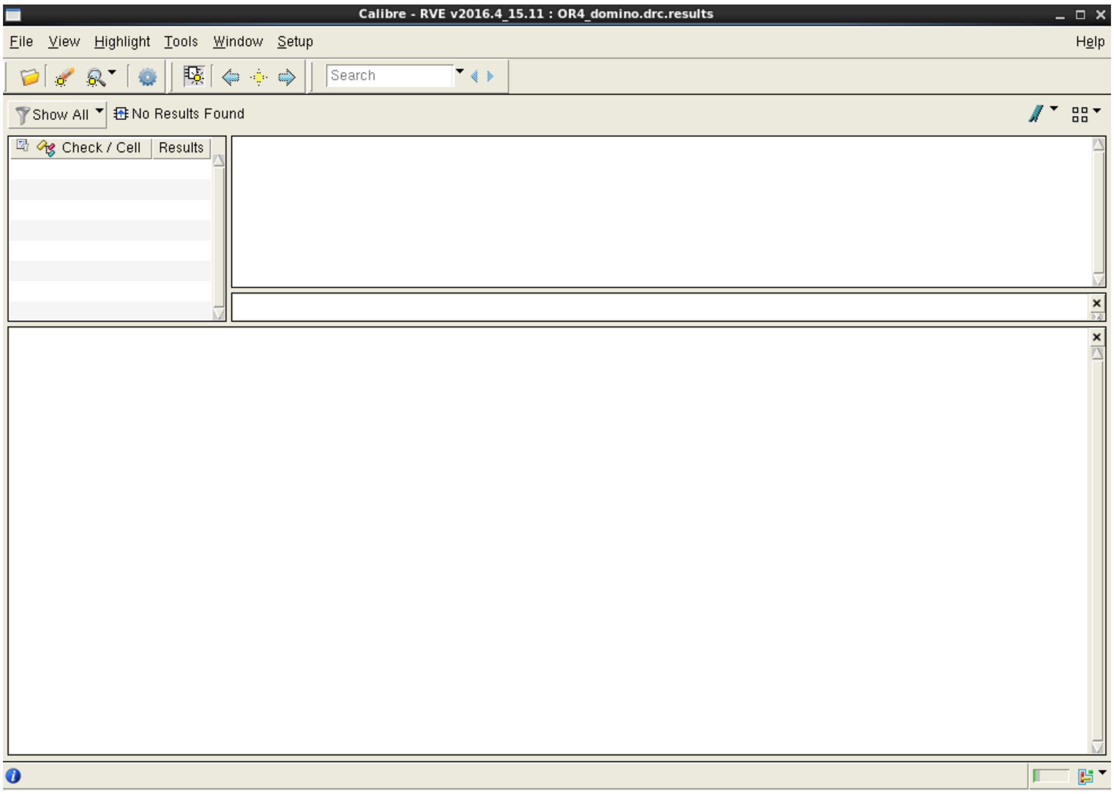

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '.protect'
 trise            tfall            tdelay_avg       temper
 alter#
  6.474e-11        8.091e-11        7.283e-11        2.500e+01
1
```

(3) Domino

Layout

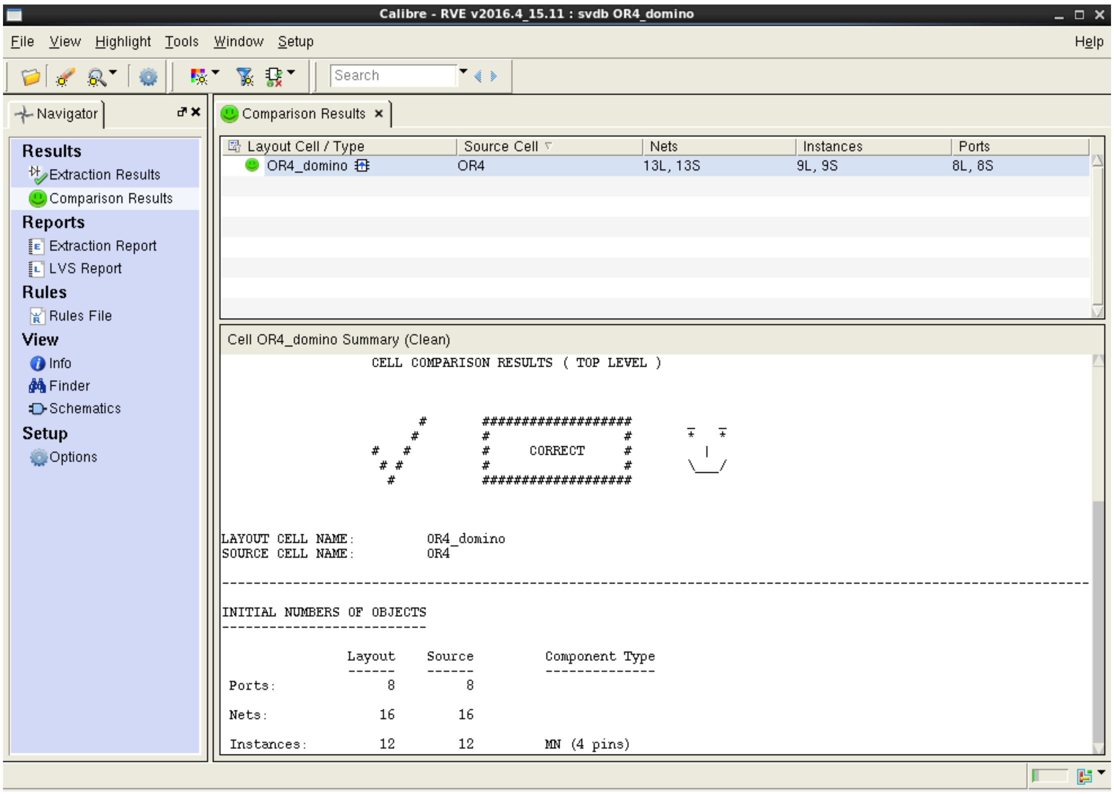


DRC



Calibre - RVE v2016.4_15.11 : OR4_domino.drc.results
File View Highlight Tools Window Setup
Help
Search
Show All
No Results Found
Check / Cell
Results

LVS



Calibre - RVE v2016.4_15.11 : svdb OR4_domino
File View Highlight Tools Window Setup
Help
Search
Navigator
Comparison Results
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
Nets
Instances
Ports
OR4_domino
OR4
13L, 13S
9L, 9S
8L, 8S
Cell OR4_domino Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: OR4_domino
SOURCE CELL NAME: OR4
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 8 8
Nets: 16 16
Instances: 12 12 MN (4 pins)

Simulation


```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '.protect'
 trise           temper          alter#
  1.162e-10       2.500e+01       1
```