2022 Introduction to VLSI CAD

Lab 9

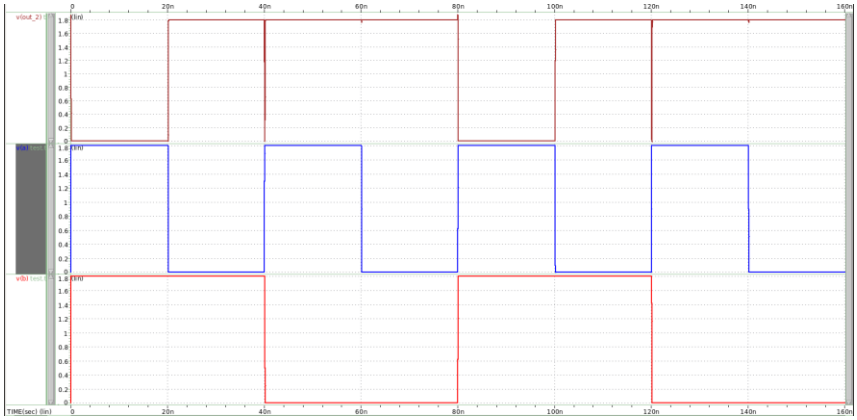
A. NAND

1. Presim

i. 請截取 terminal 顯示 job concluded 的圖

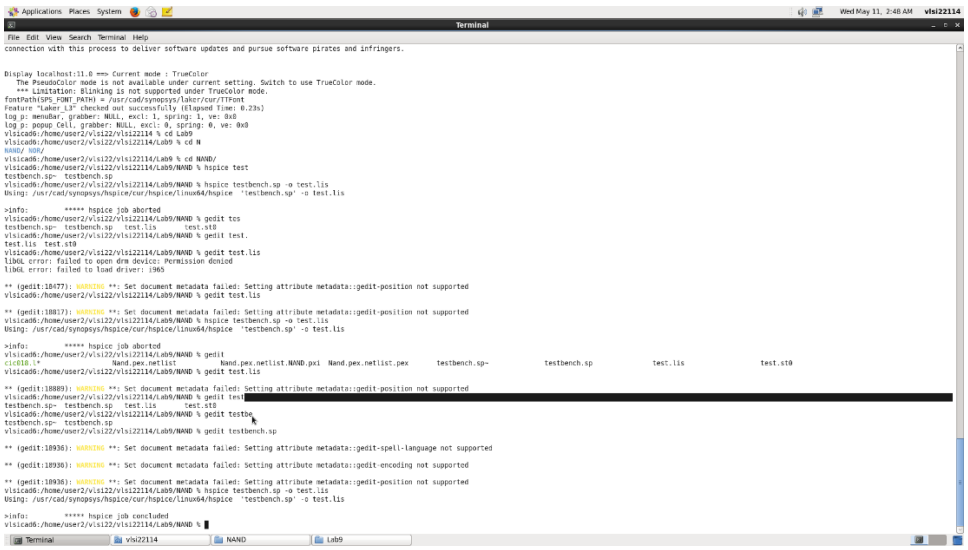
```
vlsicad9:/home/user2/vlsi22/vlsi22114 % hspice testbench.sp -o test.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice  'testbench.sp' -o test.lis

>info:          ***** hspice job concluded
vlsicad9:/home/user2/vlsi22/vlsi22114 % wv &
[1] 15379
```

ii. 請截取 WaveView 中的波形

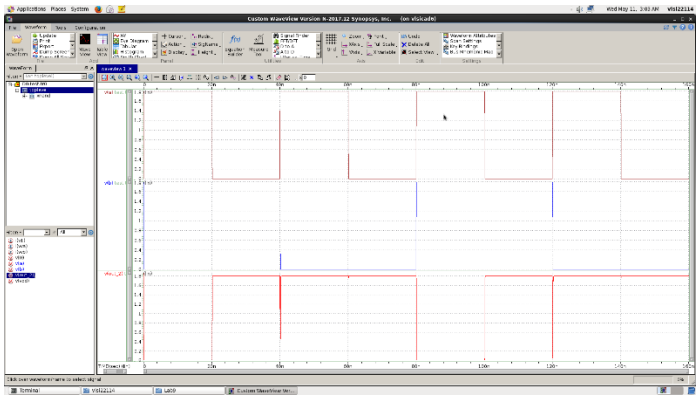


2. Post-sim

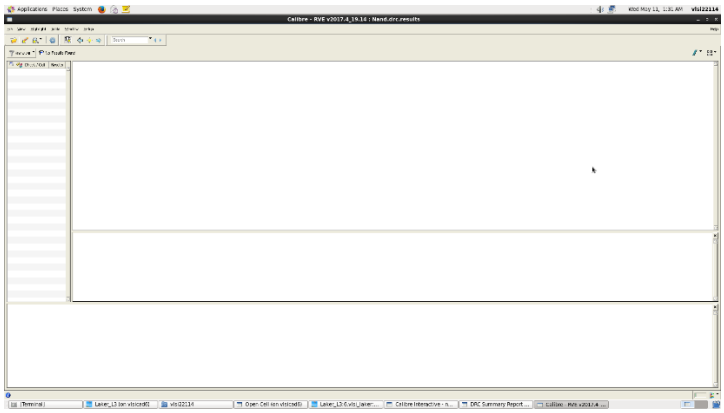
i. 請截取 terminal 顯示 job concluded 的圖

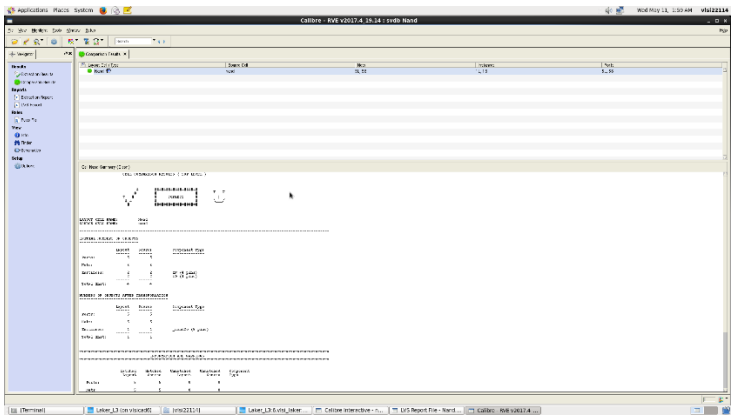


ii. 請截取 WaveView 中的波形

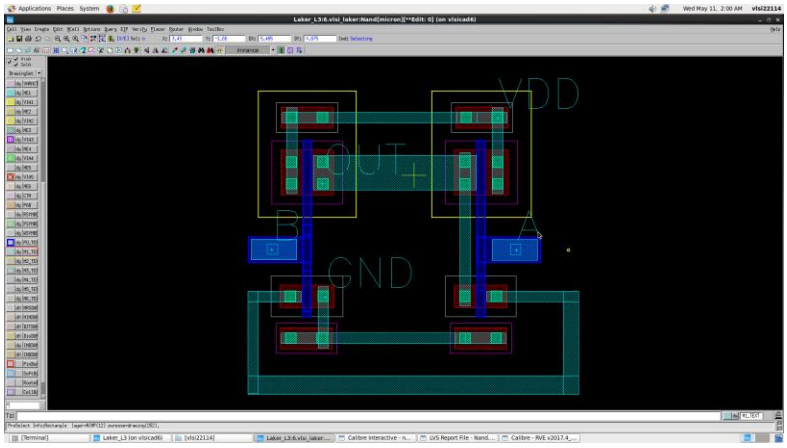


iii. DRC/LVS 結果





iv. Layout 截圖



B. NOR

1. Presim

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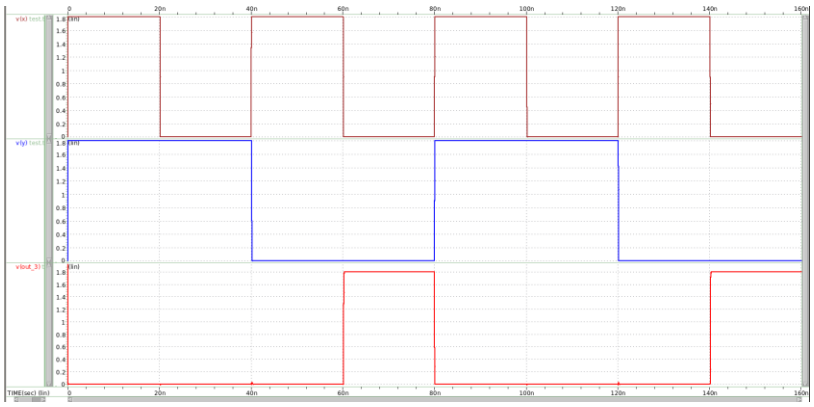
```
vlsicad9:/home/user2/vlsi22/vlsi22114 % hspice testbench.sp -o test.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice  'testbench.sp' -o test.lis

>info:          ***** hspice job concluded
vlsicad9:/home/user2/vlsi22/vlsi22114 % wv &
[1] 15379
```

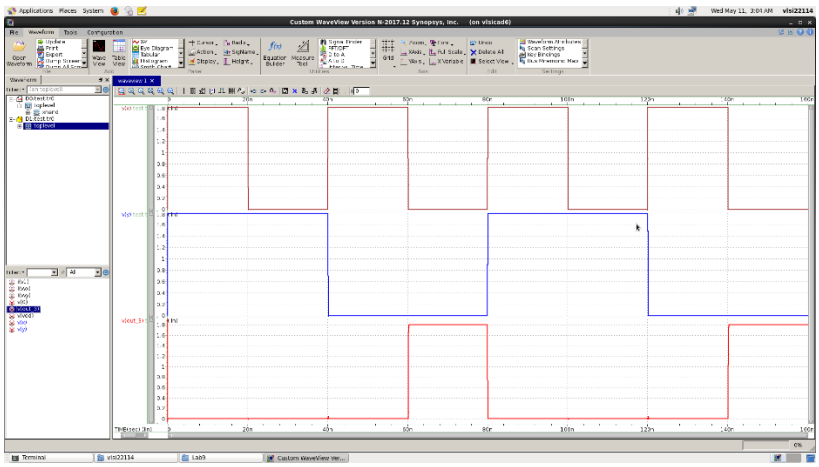
ii. 請截取 WaveView 中的波形



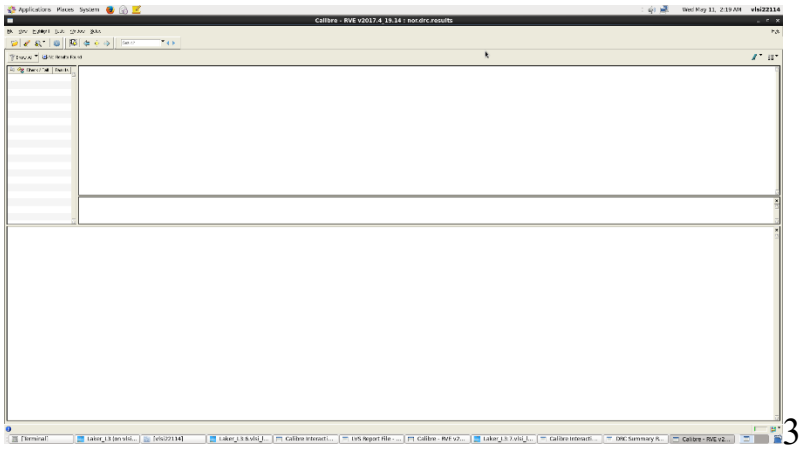
2. Post-sim

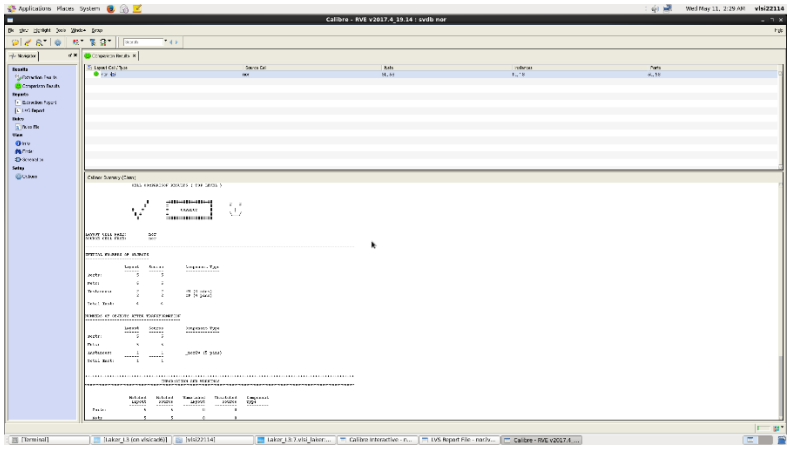
i. 請截取 terminal 顯示 job concluded 的圖

ii. 請截取 WaveView 中的波形



iii. DRC/LVS 結果





iv. Layout 截圖