VLSI Circuit Design
Lab 2

Yu-Chi Chu

Problem 1 – Device and logic effort

1A

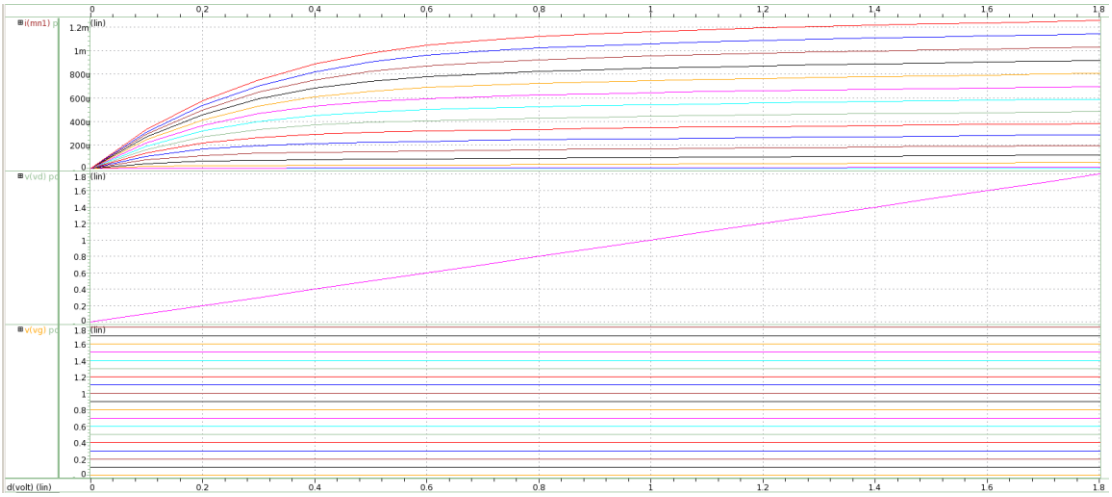


Fig 1_1 I_{DS} vs. V_{DS} for different V_{GS}

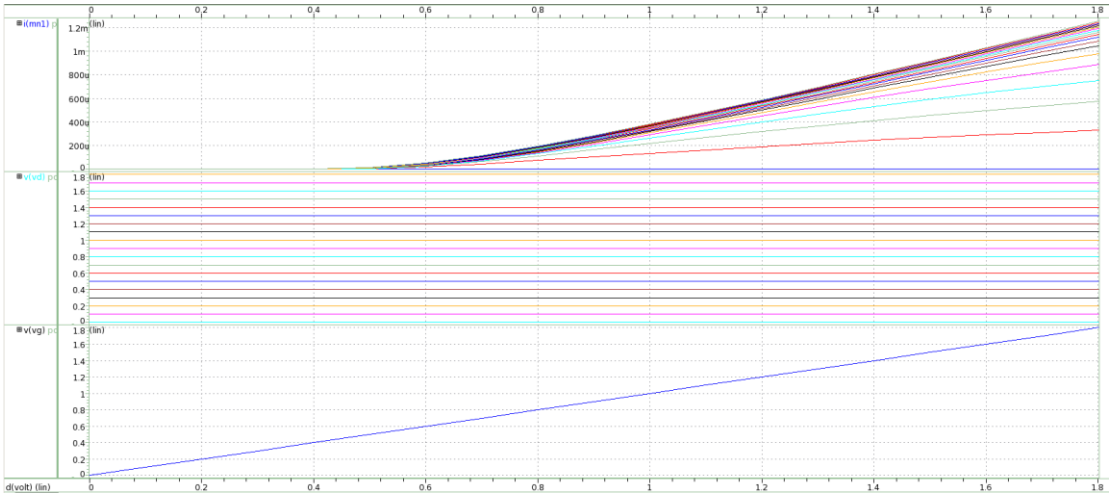


Fig 1_2 I_{DS} vs V_{GS} for different V_{DS}

1B

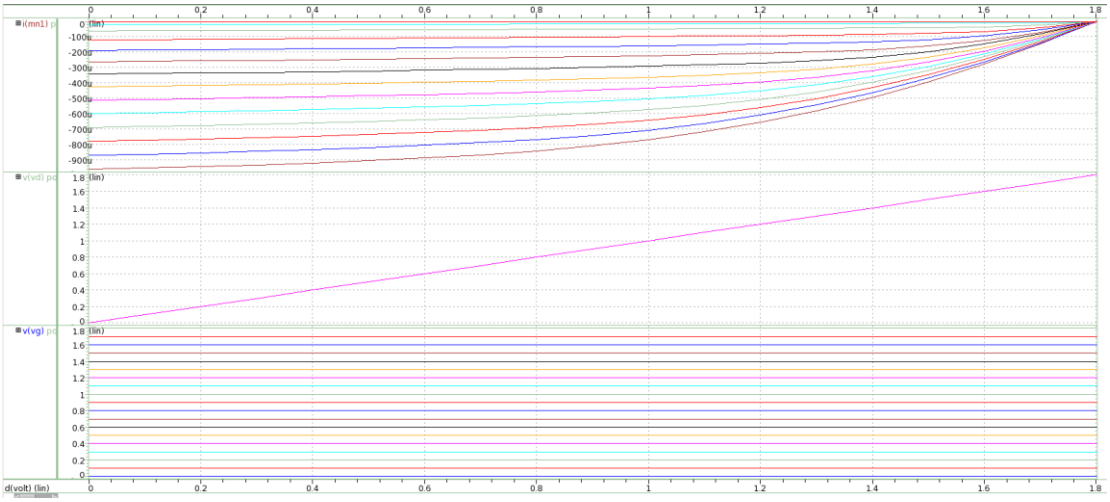


Fig 1_3 I_{DS} vs V_{DS} for different V_{GS}

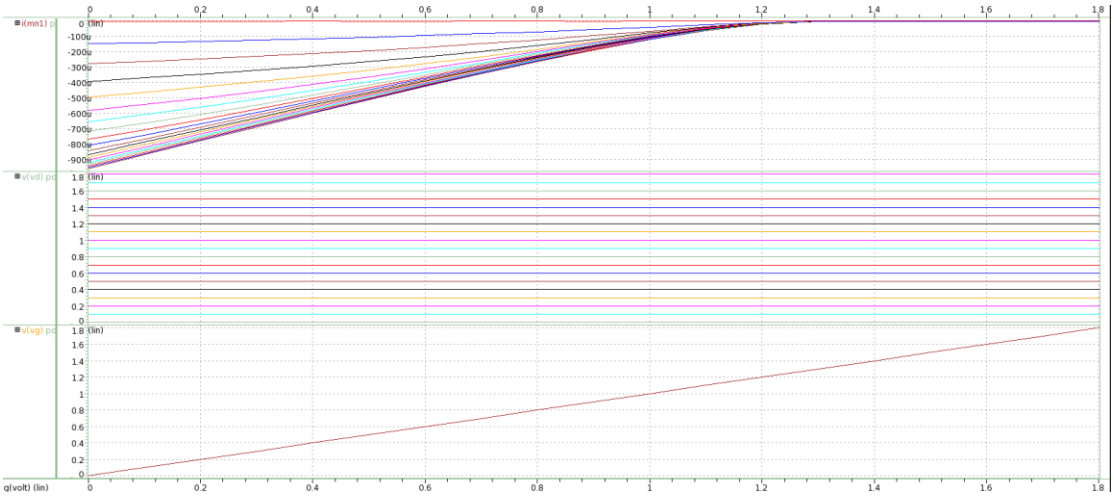


Fig 1_4 I_{DS} vs V_{GS} for different V_{DS}

1C

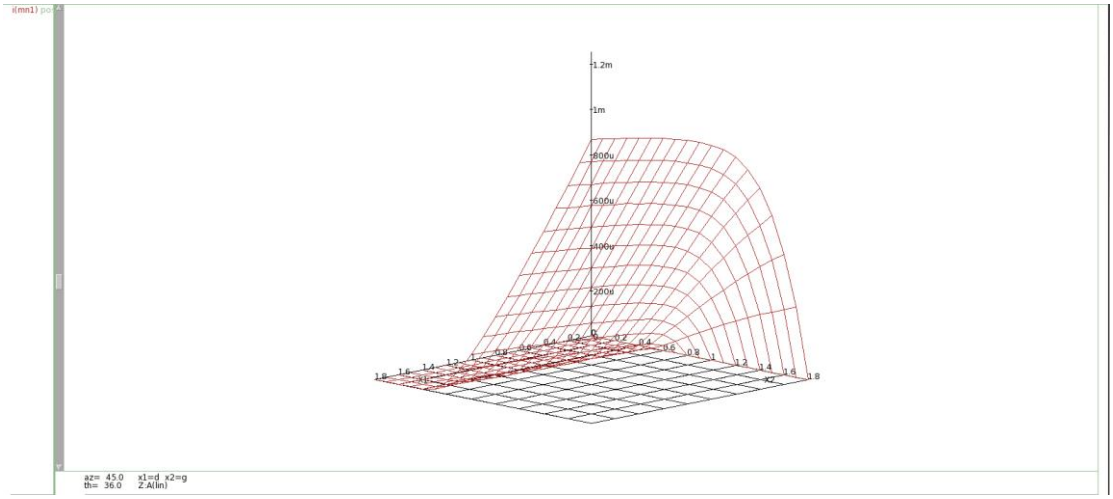


Fig 1_5 3D curve

1D

Vth=845mV is not equal toVDD/2(0.9V)

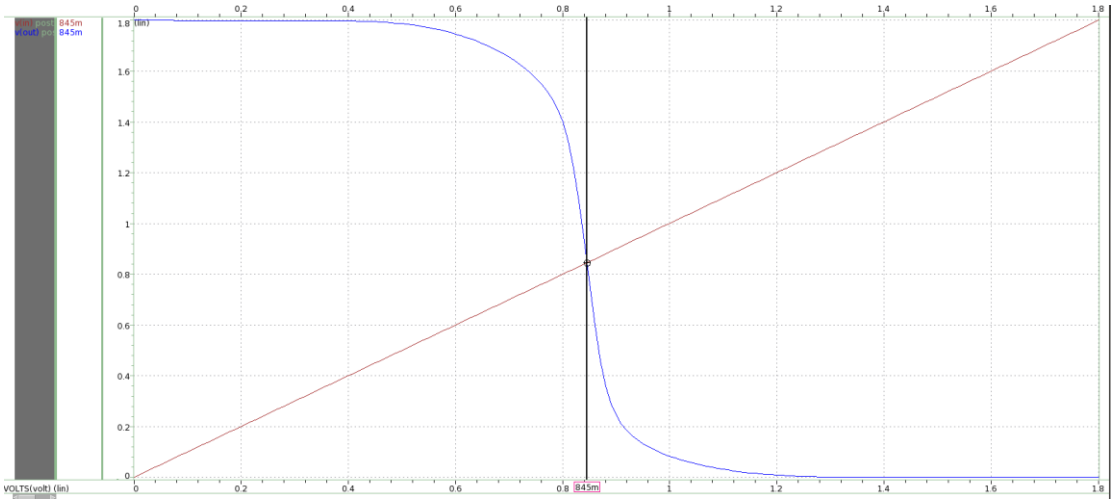


Fig 1_6 Vth=0.845V

Use sweep to find Vth by altering W. When W=5.98um, Vth=0.9001V

493	5.890e-06	8.979e-01	2.500e+01	1
494	5.900e-06	8.982e-01	2.500e+01	1
495	5.910e-06	8.984e-01	2.500e+01	1
496	5.920e-06	8.987e-01	2.500e+01	1
497	5.930e-06	8.989e-01	2.500e+01	1
498	5.940e-06	8.991e-01	2.500e+01	1
499	5.950e-06	8.994e-01	2.500e+01	1
500	5.960e-06	8.996e-01	2.500e+01	1
501	5.970e-06	8.999e-01	2.500e+01	1
502	5.980e-06	9.001e-01	2.500e+01	1
503	5.990e-06	9.003e-01	2.500e+01	1
504	6.000e-06	9.006e-01	2.500e+01	1
505	6.010e-06	9.008e-01	2.500e+01	1
506	6.020e-06	9.010e-01	2.500e+01	1
507	6.030e-06	9.012e-01	2.500e+01	1
508	6.040e-06	9.015e-01	2.500e+01	1
509	6.050e-06	9.017e-01	2.500e+01	1
510	6.060e-06	9.019e-01	2.500e+01	1
511	6.070e-06	9.021e-01	2.500e+01	1
512	6.080e-06	9.024e-01	2.500e+01	1
513	6.090e-06	9.026e-01	2.500e+01	1
514	6.100e-06	9.028e-01	2.500e+01	1
515	6.110e-06	9.030e-01	2.500e+01	1
516	6.120e-06	9.033e-01	2.500e+01	1
517	6.130e-06	9.035e-01	2.500e+01	1
518	6.140e-06	9.037e-01	2.500e+01	1
519	6.150e-06	9.039e-01	2.500e+01	1
520	6.160e-06	9.041e-01	2.500e+01	1
521	6.170e-06	9.044e-01	2.500e+01	1
522	6.180e-06	9.046e-01	2.500e+01	1
523	6.190e-06	9.048e-01	2.500e+01	1
524	6.200e-06	9.050e-01	2.500e+01	1
525	6.210e-06	9.053e-01	2.500e+01	1
526	6.220e-06	9.055e-01	2.500e+01	1
527	6.230e-06	9.057e-01	2.500e+01	1
528	6.240e-06	9.059e-01	2.500e+01	1
529	6.250e-06	9.061e-01	2.500e+01	1
530	6.260e-06	9.064e-01	2.500e+01	1
531	6.270e-06	9.066e-01	2.500e+01	1
532	6.280e-06	9.068e-01	2.500e+01	1
533	6.290e-06	9.070e-01	2.500e+01	1
534	6.300e-06	9.072e-01	2.500e+01	1
535	6.310e-06	9.075e-01	2.500e+01	1

Fig 1_7 sweep W

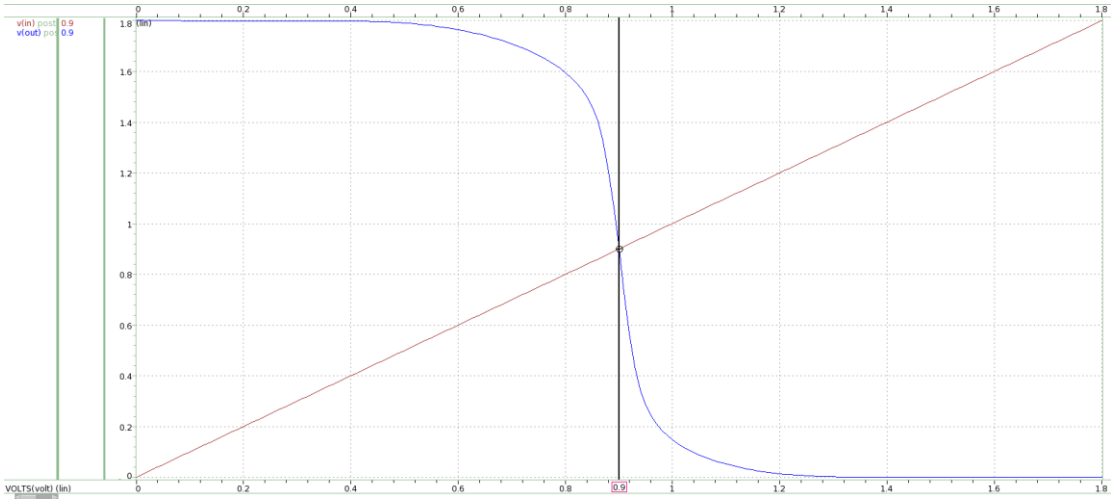
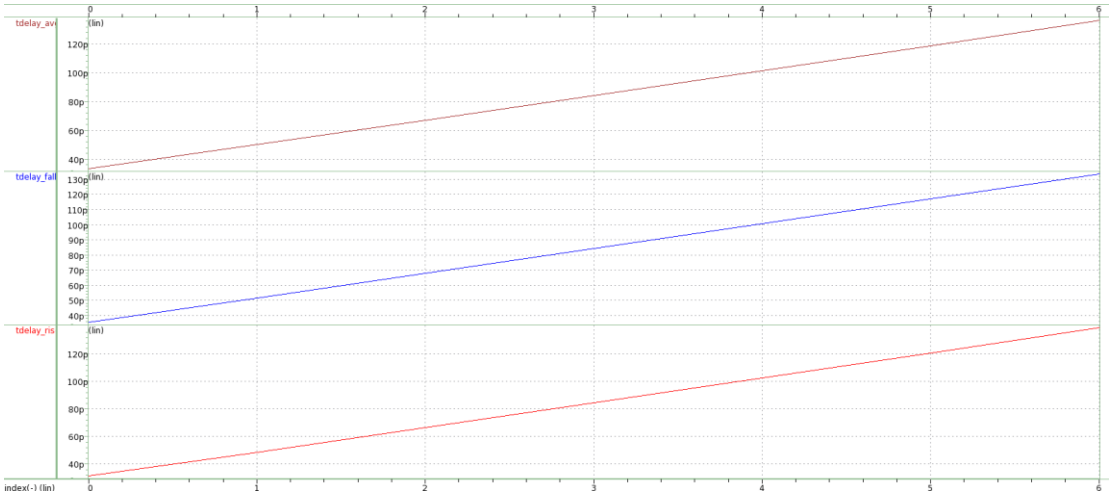


Fig 1_8 Vth=0.9V

1E




```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=1
.TITLE '.protect'
 h1                tdelay_rise       tdelay_fall       tdelay_avg
                   temper            alter#
   1.000e+00        3.115e-11         3.526e-11         3.320e-11
                    2.500e+01        1
   2.000e+00        4.871e-11         5.142e-11         5.007e-11
                    2.500e+01        1
   3.000e+00        6.663e-11         6.778e-11         6.720e-11
                    2.500e+01        1
   4.000e+00        8.475e-11         8.413e-11         8.444e-11
                    2.500e+01        1
   5.000e+00        1.028e-10         1.005e-10         1.016e-10
                    2.500e+01        1
   6.000e+00        1.209e-10         1.169e-10         1.189e-10
                    2.500e+01        1
   7.000e+00        1.390e-10         1.333e-10         1.362e-10
                    2.500e+01        1
```

Fig 1_9 time_delay_INV

Delay = $t_{parasitic} + t_{gate} \times h$. t_{gate}=1.7181e-11 s、$t_{parasitic}$ =1.5793e-11 s

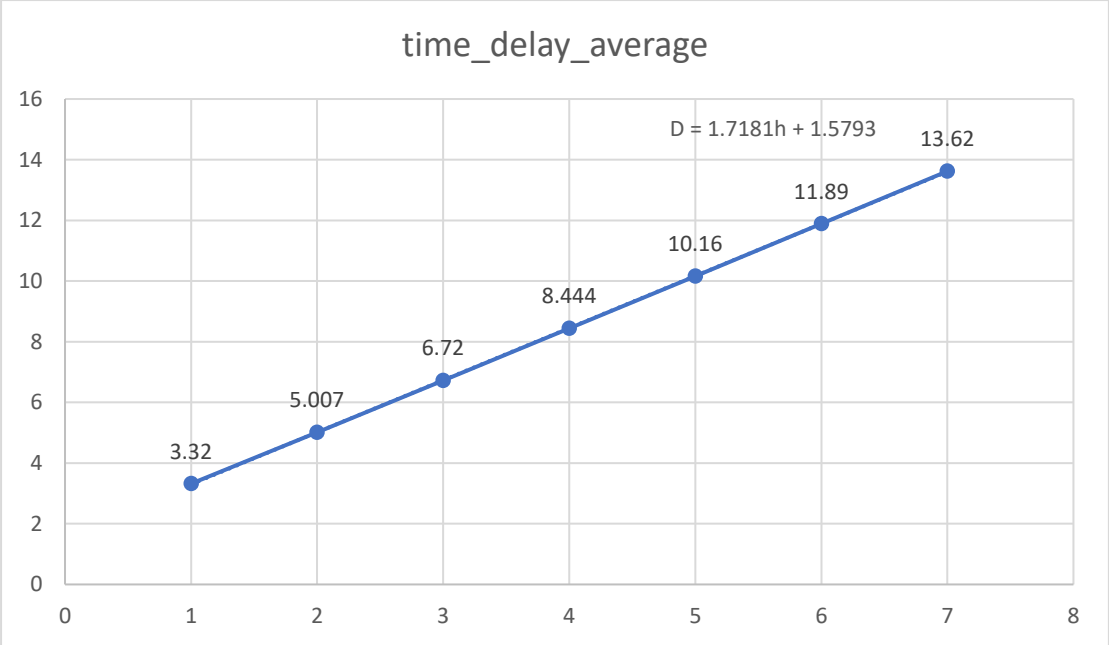


Fig 1_10 time_delay

1F

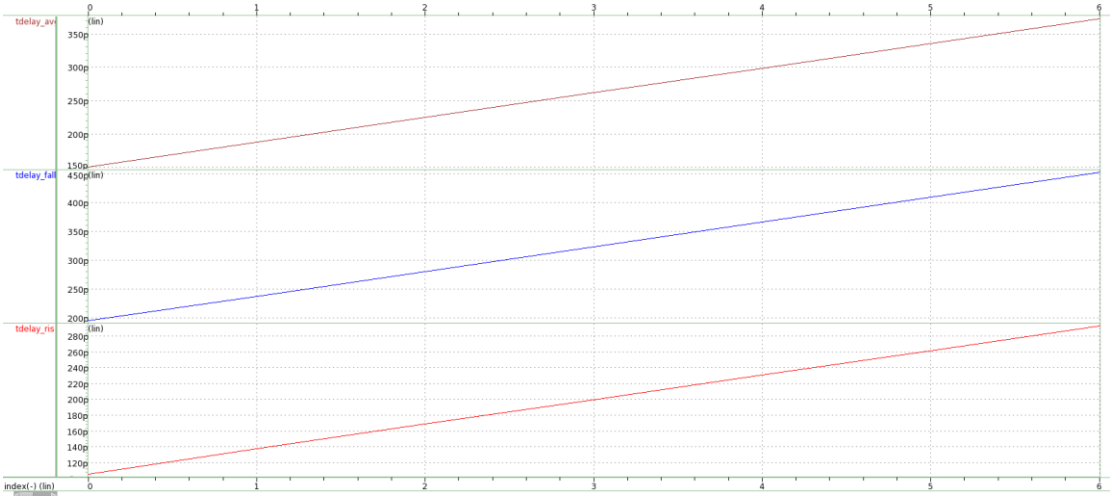


Fig 1_11 time_delay_NOR

```
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.TITLE '.protect'
 h1               tdelay_rise      tdelay_fall      tdelay_avg
                  temper           alter#
  1.000e+00        1.048e-10        1.945e-10        1.497e-10
                   2.500e+01       1
  2.000e+00        1.373e-10        2.375e-10        1.874e-10
                   2.500e+01       1
  3.000e+00        1.688e-10        2.803e-10        2.245e-10
                   2.500e+01       1
  4.000e+00        1.999e-10        3.232e-10        2.615e-10
                   2.500e+01       1
  5.000e+00        2.311e-10        3.660e-10        2.985e-10
                   2.500e+01       1
  6.000e+00        2.616e-10        4.089e-10        3.353e-10
                   2.500e+01       1
  7.000e+00        2.926e-10        4.518e-10        3.722e-10
                   2.500e+01       1
```

Fig 1_12 time_delay_NOR

Delay = $t_{parasitic}$ + t_{gate} × **h**. t_{gate}=0.3705e-10 s、$t_{parasitic}$ =1.1311e-10 s

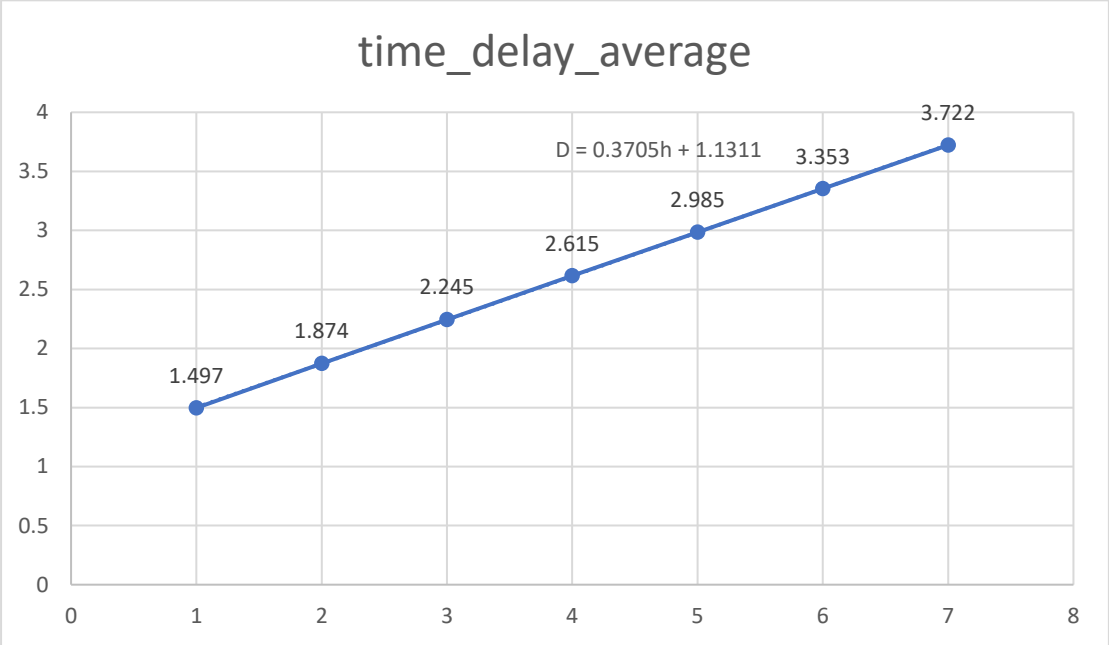


Fig 1_13 time_delay_方程式

1G

1E t_{gate}=1.7181e-11 s、$t_{parasitic}$ =1.5793e-11 s

1F t_{gate}=0.3705e-10 s、$t_{parasitic}$ =1.1311e-10 s

The ratio of t_{gate} and $t_{parasitic}$

	t_{gate}	$t_{parasitic}$
1E	1	1
1F	7/3	3

Problem 2 – Delay Estimation and Optimization

2A

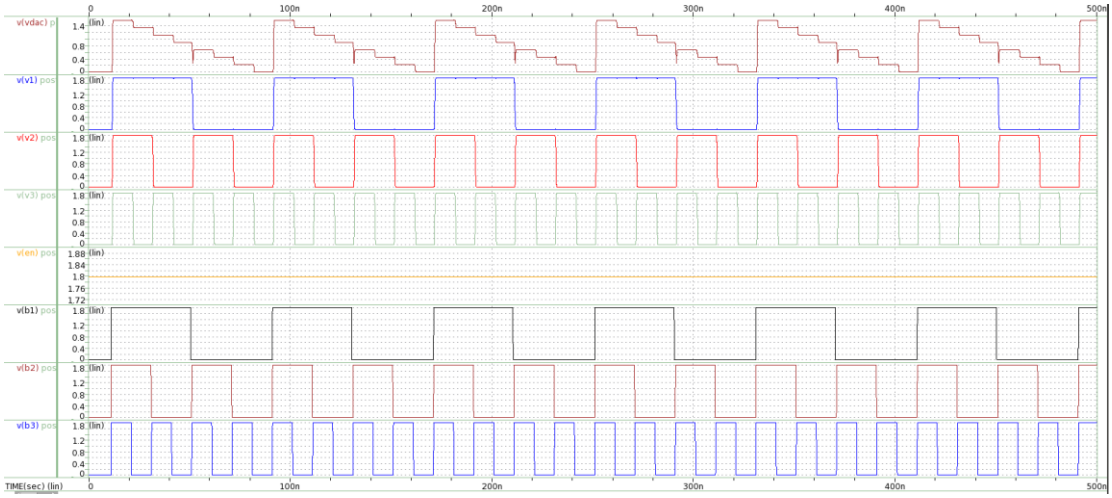


Fig 2_1 CDAC waveform

Vdac is composed of 8 bits from 000 to 111, Vc=001, Vb=010, Va=100

When Va=Vc=Vdd, Vb=gnd, Vdac=100+000+001=101

2B

Fig 2_2 CDAC with switch waveform

2C

tdelay_avg1=NAN
tdelay_avg2=NAN
tdelay_avg3=NAN
tdelay_fall1=NAN
tdelay_fall2=NAN
tdelay_fall3=NAN
tdelay_rise1=NAN
tdelay_rise2=NAN
tdelay_rise3=NAN
temper=25

Input=000

tdelay_avg1=NAN
tdelay_avg2=NAN
tdelay_avg3=15.8n
tdelay_fall1=NAN
tdelay_fall2=NAN
tdelay_fall3=16.8n
tdelay_rise1=NAN
tdelay_rise2=NAN
tdelay_rise3=14.9n
temper=25

Input=001

tdelay_avg1=NAN
tdelay_avg2=5.82n
tdelay_avg3=NAN
tdelay_fall1=NAN
tdelay_fall2=6.78n
tdelay_fall3=NAN
tdelay_rise1=NAN
tdelay_rise2=4.87n
tdelay_rise3=NAN
temper=25

Input=010

tdelay_avg1=NAN
tdelay_avg2=5.82n
tdelay_avg3=15.8n
tdelay_fall1=NAN
tdelay_fall2=6.78n
tdelay_fall3=16.8n
tdelay_rise1=NAN
tdelay_rise2=4.87n
tdelay_rise3=14.9n
temper=25

Input=011

tdelay_avg1=5.84n
tdelay_avg2=NAN
tdelay_avg3=NAN
tdelay_fall1=6.8n
tdelay_fall2=NAN
tdelay_fall3=NAN
tdelay_rise1=4.88n
tdelay_rise2=NAN
tdelay_rise3=NAN
temper=25

Input=100

tdelay_avg1=5.84n
tdelay_avg2=NAN
tdelay_avg3=15.8n
tdelay_fall1=6.8n
tdelay_fall2=NAN
tdelay_fall3=16.7n
tdelay_rise1=4.88n
tdelay_rise2=NAN
tdelay_rise3=14.8n
temper=25

Input=101

tdelay_avg1=5.8n
tdelay_avg2=5.79n
tdelay_avg3=NAN
tdelay_fall1=6.76n
tdelay_fall2=6.75n
tdelay_fall3=NAN
tdelay_rise1=4.85n
tdelay_rise2=4.84n
tdelay_rise3=NAN
temper=25

Input=110

tdelay_avg1=5.8n
tdelay_avg2=5.79n
tdelay_avg3=15.8n
tdelay_fall1=6.76n
tdelay_fall2=6.75n
tdelay_fall3=16.7n
tdelay_rise1=4.85n
tdelay_rise2=4.84n
tdelay_rise3=14.8n
temper=25

Input=111

worst case: V3

Relationship between Delay and Input: Due to the reset signal, the pulses at V1 and V2 are discharged prematurely, resulting in a decrease in their delays. Because the delay in the middle of the pulse is small, and V3 is not affected by the reset (its pulse is not discharged prematurely), its delay will not

decrease. As shown in Figure 2_3, the areas circled in red indicate where the reset signal has an effect.

Fig 2_3 CDAC with switch waveform

2D

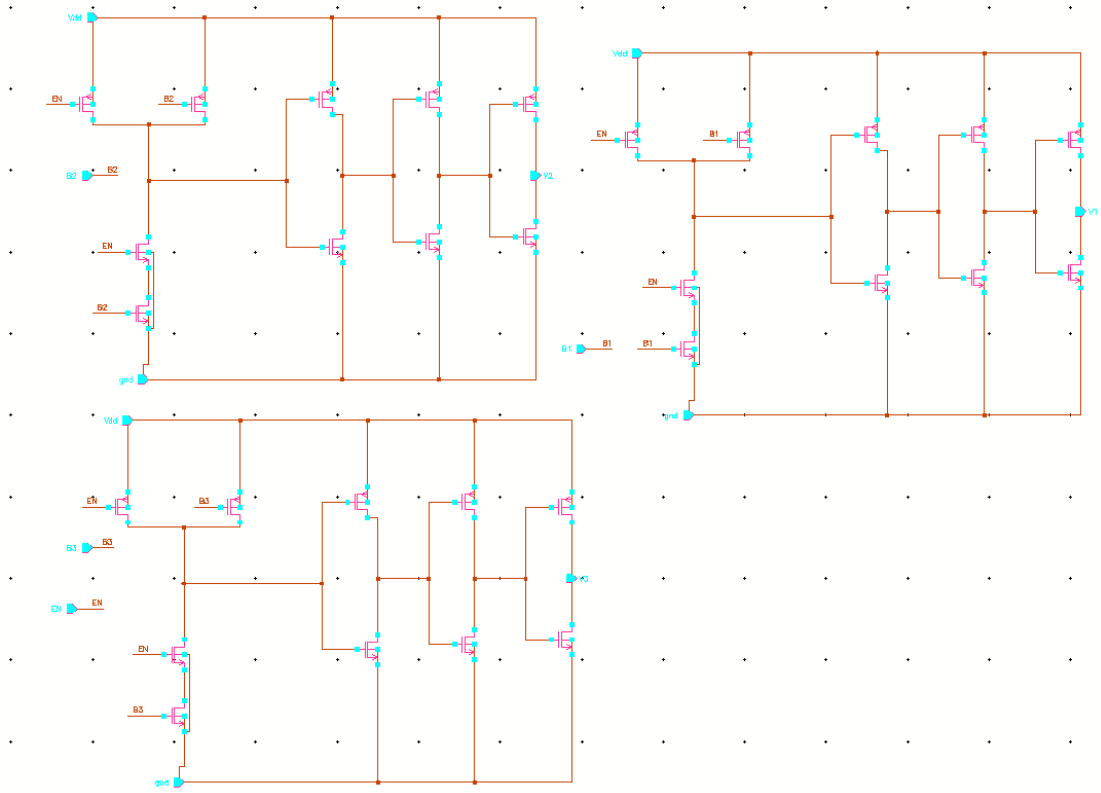
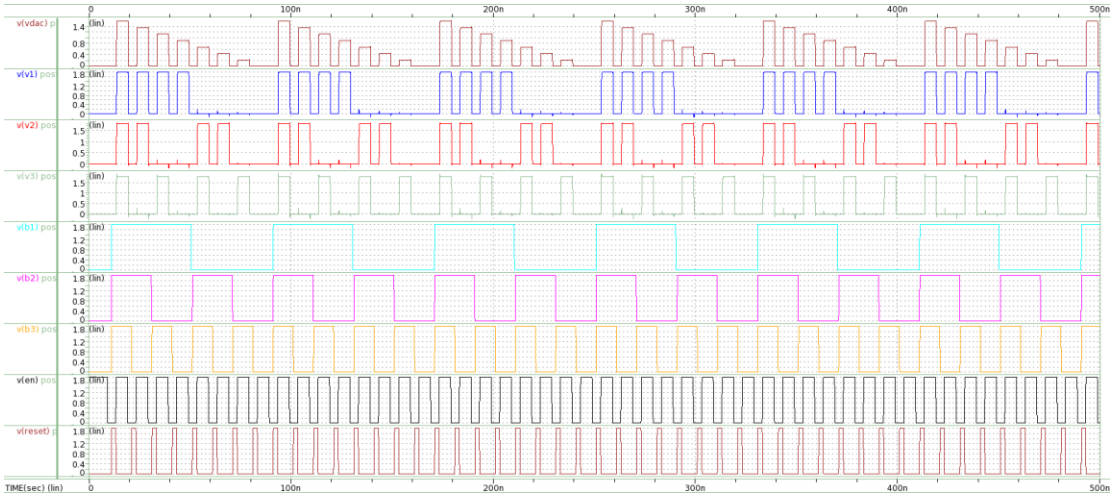


Fig 2_3 3 AND



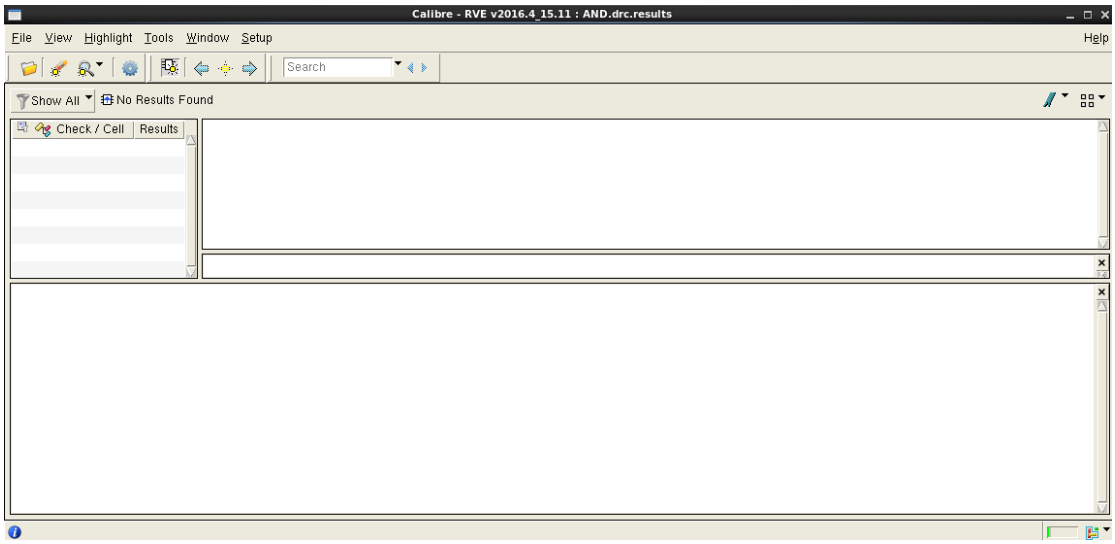
tdelay_avg1=5.33n
tdelay_avg2=5.31n
tdelay_avg3=15.3n
tdelay_fall1=6.14n
tdelay_fall2=6.12n
tdelay_fall3=16.1n
tdelay_rise1=4.51n
tdelay_rise2=4.49n
tdelay_rise3=14.5n
temper=25

bufffer

tdelay_avg1=5.8n
tdelay_avg2=5.79n
tdelay_avg3=15.8n
tdelay_fall1=6.76n
tdelay_fall2=6.75n
tdelay_fall3=16.7n
tdelay_rise1=4.85n
tdelay_rise2=4.84n
tdelay_rise3=14.8n
temper=25

no buffer

2E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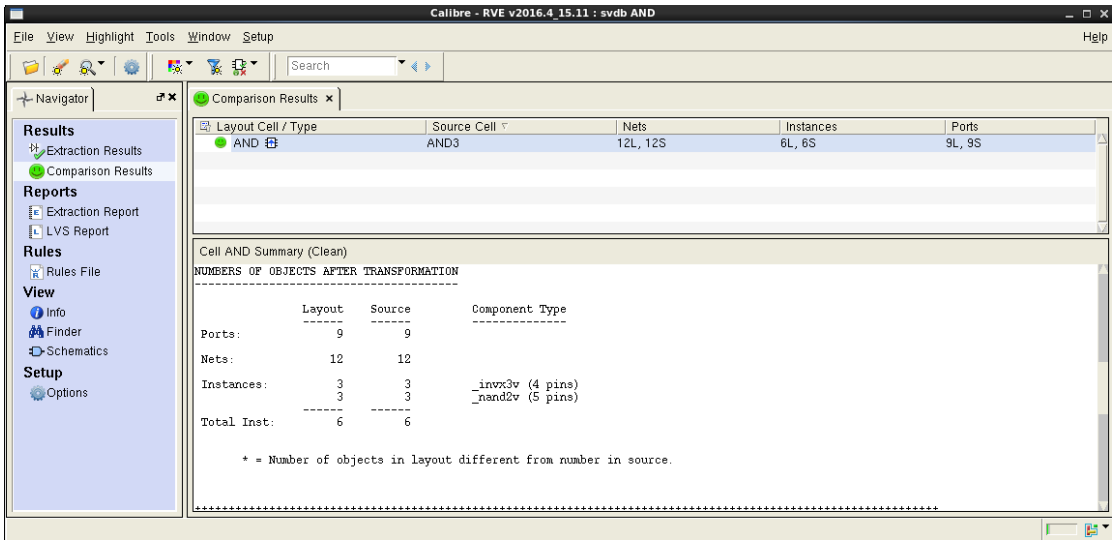
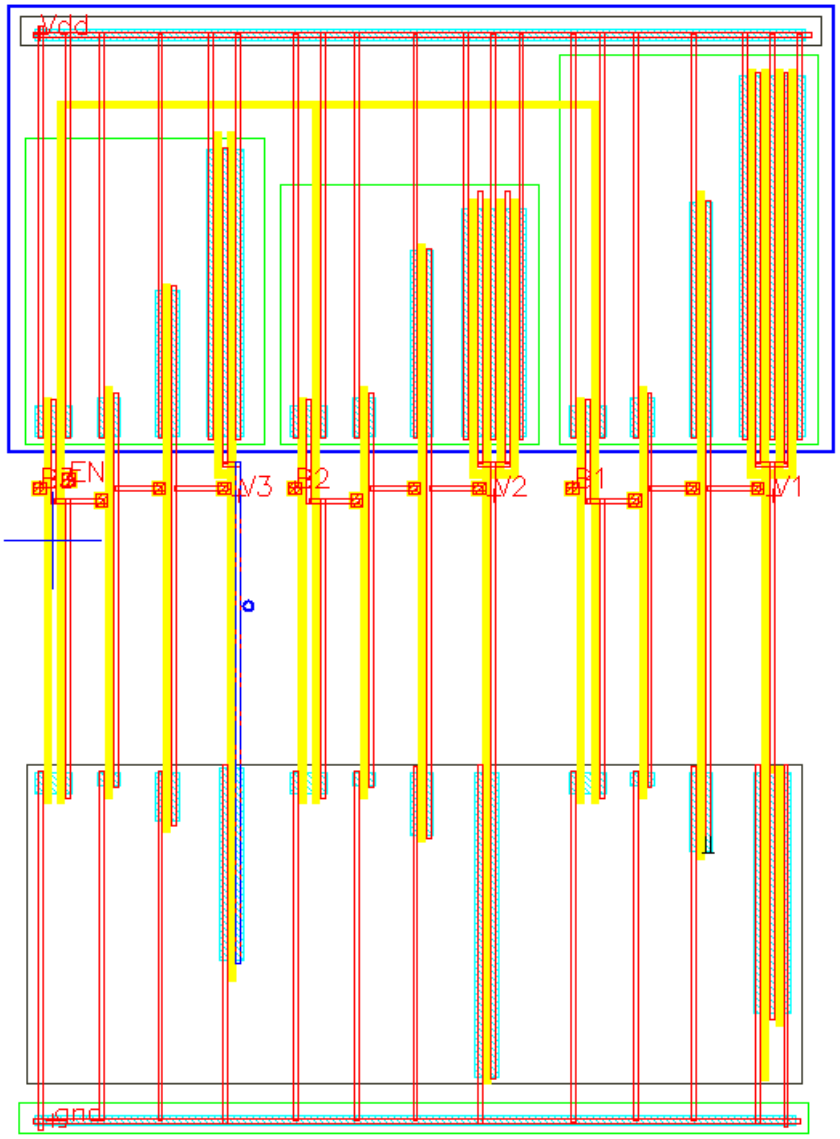
File View Highlight Tools Window Setup
Help
Search
Show All
No Results Found
Check / Cell
Results

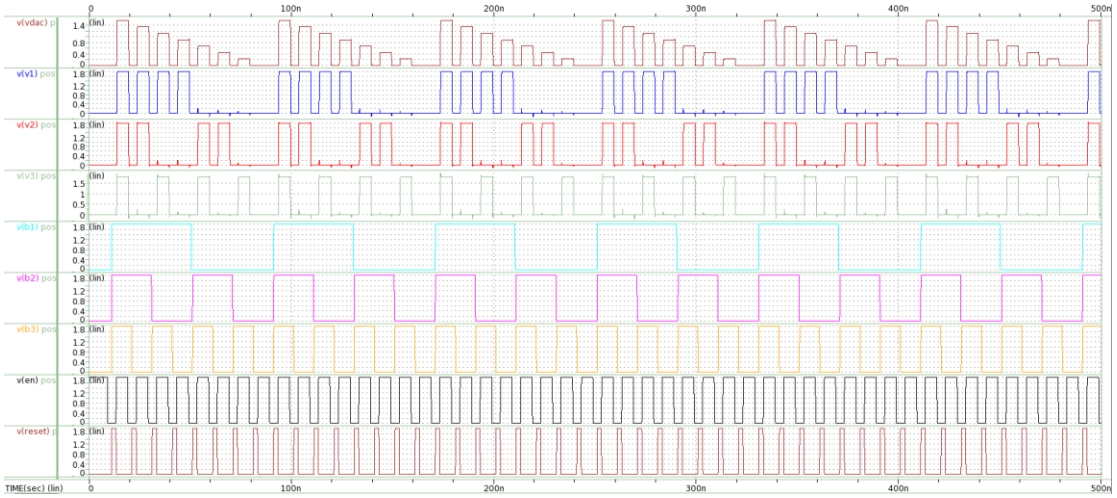
DRC


Calibre - RVE v2016.4_15.11 : svdb AND
File View Highlight Tools Window Setup
Help
Search
Navigator
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
AND
AND3
12L, 12S
6L, 6S
9L, 9S
Cell AND Summary (Clean)
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 9 9
Nets: 12 12
Instances: 3 3 _invx3v (4 pins)
3 3 _nand2v (5 pins)
Total Inst: 6 6
* = Number of objects in layout different from number in source.

LVS


Vdd
EN
V3
V2
V1
gnd

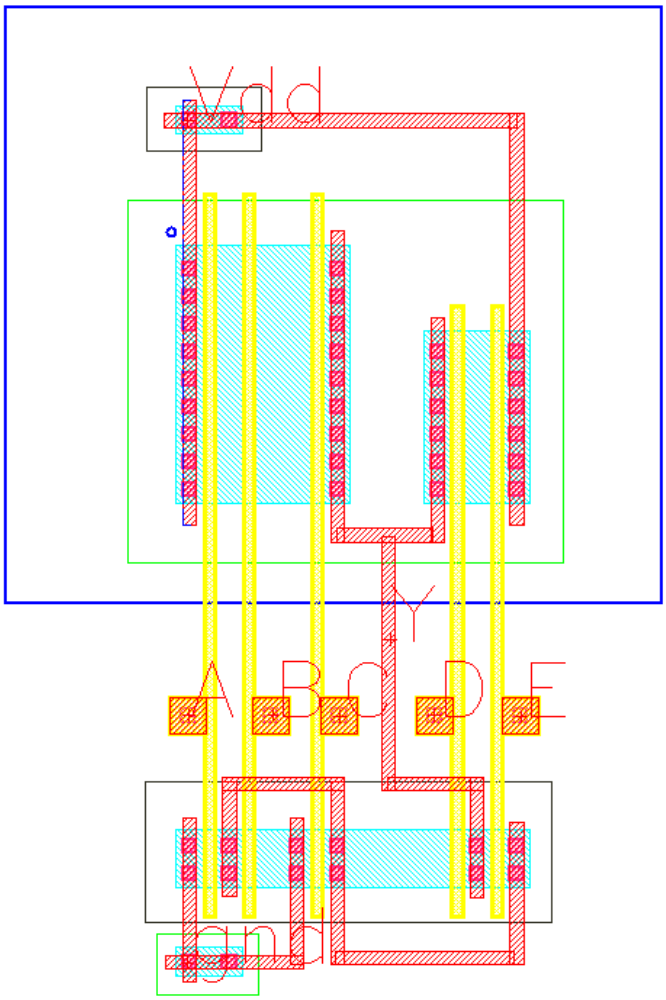
layout


0
100n
200n
300n
400n
500n
v(vdac) p
v(v1) pos
v(v2) pos
v(v3) pos
v(b1) pos
v(b2) pos
v(b3) pos
v(en) pos
v(reset) p
TIME(sec) (lin)

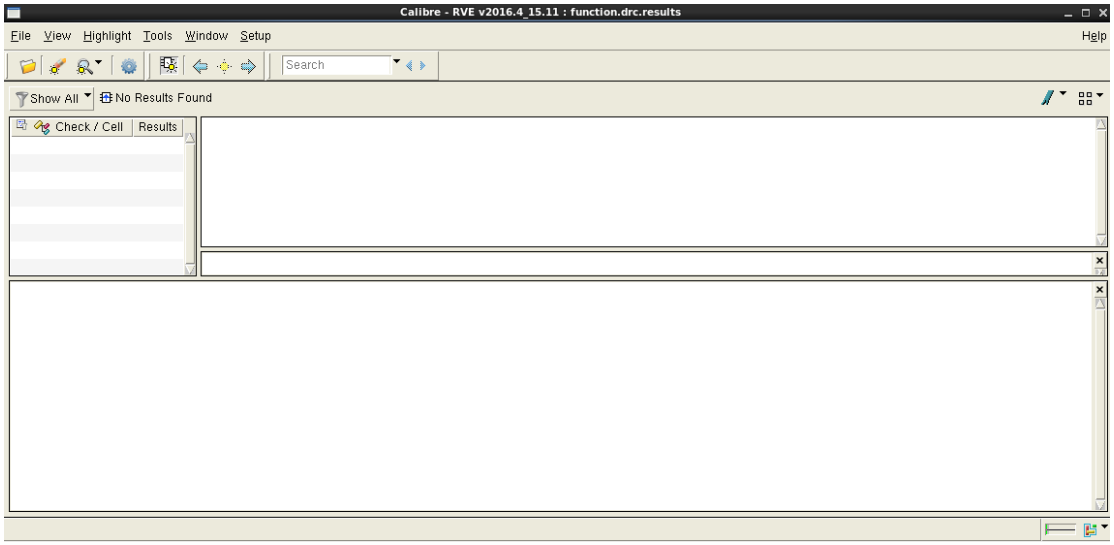
bufffer(layout)

nobuffer

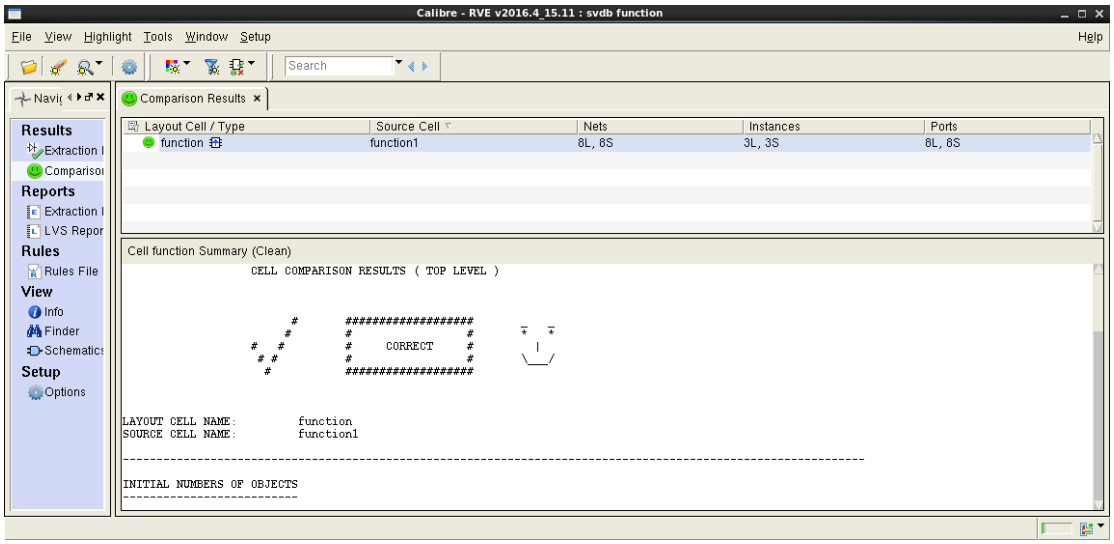
Problem 3 – Elmore Delay Model and Layout Effect on Diffusion Capacitance 3D



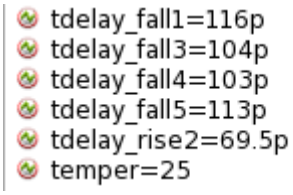
layout



DRC



LVS



3E

Pattern1: τ =116/33=3.515

Pattern2: τ =69.5/22=3.16

Pattern3: τ =104/21=4.95

Pattern4: τ =103/26=3.9615

Pattern5: τ =113/38.75=2.91613

τ_avg = (3.515+3.16+4.95+3.9615+2.91613)/5=3.7ps