

Qualitative models and experimental investigation of chaotic NOR gates and set/reset flip-flops

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Abstract

It has been observed through experiments and *SPICE* simulations that logical circuits based upon Chua's circuit exhibit complex dynamical behavior. This behavior can be used to design analogs of more complex logic families and some properties can be exploited for electronics applications. Some of these circuits have been modeled as systems of ordinary differential equations. However, as the number of components in newer circuits increases so does the complexity. This renders continuous dynamical systems models impractical and necessitates new modeling techniques. In recent years some discrete dynamical models have been developed using various simplifying assumptions. To create a robust modeling framework for chaotic logical circuits, we developed both deterministic and stochastic discrete dynamical models, which exploit the natural recurrence behavior, for two chaotic NOR gates and a chaotic set/reset flip-flop (RSFF). This work presents a complete applied mathematical investigation of logical circuits. Experiments on our own designs of the above circuits are modeled and the models are rigorously analyzed and simulated showing surprisingly close qualitative agreement with the experiments. Furthermore, the models are designed to accommodate dynamics of similarly designed circuits. This will allow researchers to develop ever more complex chaotic logical circuits with a simple modeling framework.

Keywords: Set/Reset flip-flop circuit, NOR gate, chaos, stochastic dynamical system
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1 Introduction

Since the 1990s there has been growing interest in controlling chaotic circuits starting from synchronization [1, 2], and leading to logical circuits [3]. Constructions of chaotic logical circuits mainly employ the usual circuit elements such as resistors, capacitors, and inductors, and a less common component called a *nonlinear resistor*. The most well-known nonlinear resistor is Chua's diode, invented by Leon Chua in 1983 and used as an integral element in Chua's circuit [4, 5, 6, 7]. For more complex logical circuits, components called *threshold control units* (TCUs)[8] have been employed [9, 10, 11].

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This may seem counterintuitive since throughout the latter half of the 20th century we have constructed ever more stable electronic components to be used in computers and other devices. This has been a triumph for electrical engineering and physics. However, not all logical systems are electronic nor man-made [12], and as we may observe, nature is often unstable. Since it is easier to study electrical systems, these chaotic logical circuits can help us better understand naturally occurring logical systems. Furthermore, the chaotic/logical properties of the circuits can be exploited for the purposes of encryption or secure communication.

While there has been an abundance of *SPICE* simulations and some experimental investigations in the literature, such as [3, 9, 10], there is a dearth of models for the more complex chaotic logical circuits. This is understandable since the usual modeling techniques become ever more difficult to implement as the number of components increase. Traditionally, logical circuits have been modeled as systems of ordinary differential equations (see [13, 3]) because resistors, capacitors, and inductors are related via different rates of change. Furthermore, *SPICE* simulations are often employed as a means of studying circuit designs, but the computational costs become unreasonable as circuits become more complex. However, more recently, there has been some effort in modeling logical circuits as simple discrete dynamical systems [14, 15, 16] and developing a mathematical framework for studying chaos in boolean networks [17, 18].

To facilitate the development of models of more complex chaotic logical circuits, we created a modeling framework by investigating two chaotic NOR gates and a chaotic Set/Reset flip-flop (RSFF). We modified the chaotic RSFF/dual NOR gate design of Cafagna and Grassi [11] and simulated our design in *MultiSIM* (a software based on *SPICE*) to verify agreement with the *PSPICE* simulations of [11]. Once the design was satisfactory, we built the circuits and recorded the same measurements as the simulations for the sake of having compatible data sets. These empirical observations and information about the physics from previous investigations were then used to develop the models. This was followed by analysis and simulations of our models, which showed surprising agreement with the experiments and *SPICE* based simulations.

Since the full schematic of the circuits (3 in 1) is quite complex and similar to those in the aforementioned works, it have been relegated to the appendix. However, the “black box” schematics of both types of circuits are quite simple, and will be referred to throughout this work. For example, a NOR gate acts as the negation of the disjunctive operator, i.e. it will output high voltage if and only if it receives low voltage inputs. The RSFF employs two NOR gates with feedbacks as shown in Fig 1.

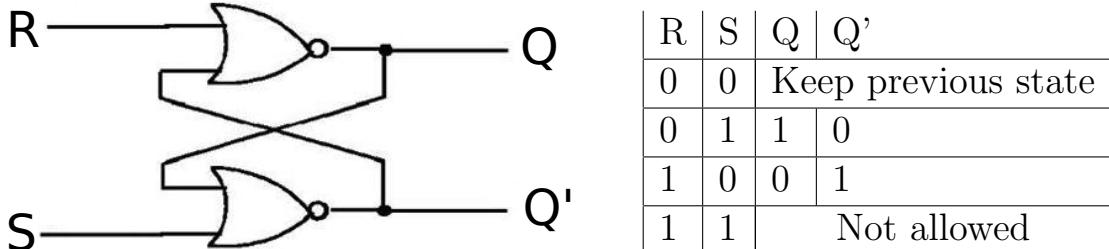


Figure 1: Black box schematic and table of operations for the Set/Reset flip-flop circuit.

The body of this work is organized into two main parts: experiments and extensive modeling, analysis, and simulations. In section 2 we briefly refer to past *SPICE* simulations and discuss experimental results of our circuit designs in order to motivate the models. Section 3 contains the focus of this article. We first derive deterministic discrete dynamical models for two types of chaotic NOR gates and analyze certain properties of the models including the existence of chaotic dynamics. Then we use the NOR gate models to derive the RSFF model and compare their simulations with the experiments. Next, in Section 4 we derive a stochastic discrete dynamical model for the RSFF in order to incorporate *races* (when two parallel signals do not have the same “speed”) and compare their simulations with experiments. We end by discussing unexpected predictive capabilities of the models for components that were not explicitly accounted for.

2 Experiments and *SPICE* Simulations

In this section we discuss previous *PSPICE* simulations for chaotic NOR gate and RSFF constructions and present our own design and experimental results to demonstrate the robustness of the circuit design even in the midst of chaos.

2.1 Previous investigations

Murali *et al.* developed and tested a chaotic NOR gate construction in [9] and with more detail in [10]. Then Cafagna and Grassi designed an RSFF [11] using similar principles to the NOR gate of Murali *et al.*, which is now the inspiration for our own RSFF.

The RSFF is designed with Chua’s circuit at its core and two TCUs to realize each NOR gate. Two switches are used to convert the circuit from operating as two separate NOR gates to operating as an RSFF and vice versa. Cafagna and Grassi provide plots of the inputs, outputs, and threshold voltages for both NOR gates, the inputs and outputs of the RSFF, and finally the voltages across the two capacitors. We recreate the same types of plots for our design in order to facilitate comparisons.

2.2 Set/reset flip-flop design and experiment

Since the circuit of Cafagna and Grassi [11] uses components that have become unavailable, we needed to design a modern chaotic RSFF/dual NOR gate. The schematic of our circuit design is shown in Fig. 11. For the *MultiSIM* simulations we use the components shown in Table 2. The chaotic backbone of the circuit comes from Chua’s circuit, and we employ threshold control units to produce the logical outputs. The *MultiSIM* plots for the dual NOR gate are shown in Fig. 12. We then made a physical realization of the circuit with mostly the same components (Table 2) as the *MultiSIM* simulations. The experimental setup is shown in Fig. 13. In order to power the circuit and get readings we used a DC power supply, wave form generator, *Arduino Due*®, and an oscilloscope. From the physical realization we reproduced the *MultiSIM* plots. To activate the dual NOR gate we keep switches 1 and 2 in Fig. 11 closed and switches 3 and 4 open. The experimental results for the dual NOR gate setup are shown in Fig. 2. In Figs. 2c and 2d we notice windows of what looks like chaotic

dynamics. This is also observed in the *MultiSIM* simulations. It should be noted that the threshold behavior of the *MultiSIM* circuit and the physical realization are slightly different due to a change in op-amps. We take a detailed look at the dynamics in Sec. 3.

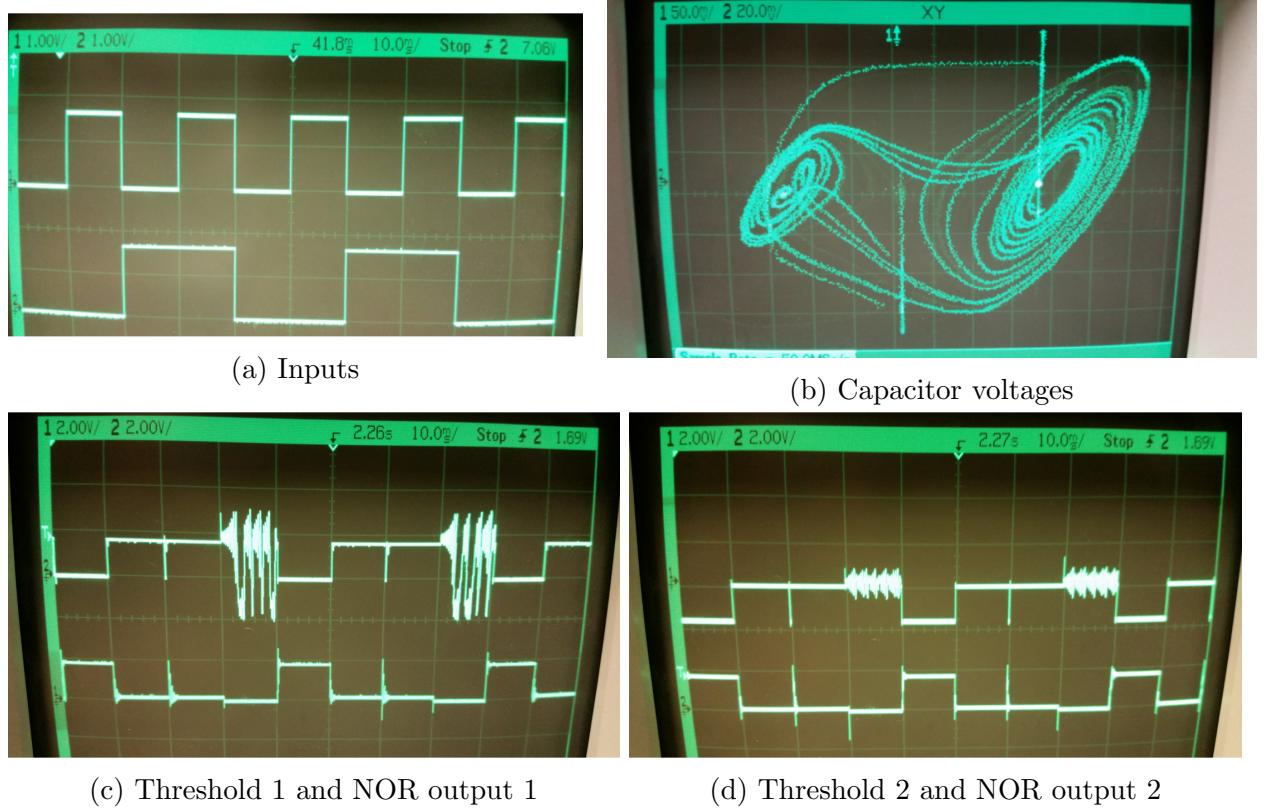


Figure 2: Experimental results for the dual NOR gate setup. For (a), (c), and (d) the abscissa represents time and the ordinate represents voltage. In (b) the plot shows the phase space produced by the two capacitors. In (a) the plot shows the two input voltages. In (c) and (d) the plot shows the respective threshold voltage and NOR outputs.

To deactivate the dual NOR gate we open switches 1 and 2 in Fig. 11. To properly activate the RSFF we need to close switches 3 and 4, however we get the RSFF outputs even with the switches open. When we close the switches we notice the race conditions for the “1-1” input causing wild oscillations, which is completely missed in the simulations. This shows that the design has implicit feedbacks, through the op-amps, which results in RSFF operations. However, when the two NOR gates are explicitly connected with one another (i.e. the output of one NOR gate feeds back to the input of the other NOR gate) the race condition exacerbates the oscillations. The experimental results for the RSFF setup are shown in Fig. 3. While the experiments of the RSFF mainly work as expected, the *MultiSIM* simulations are not able to properly capture this behavior.

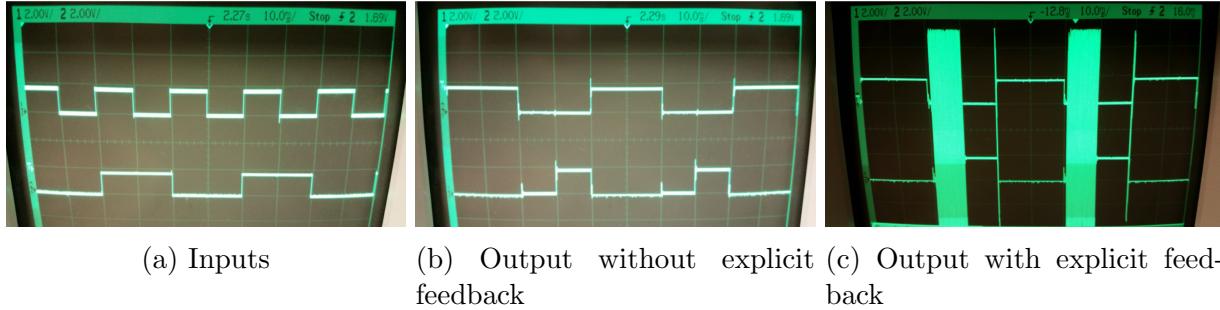


Figure 3: Experimental results for the RSFF setup. For (a), (b), and (c) the abscissa represents time and the ordinate represents voltage. In (a) the plot shows the two input voltages. In (b) the voltage was measured when switches 3 and 4 in Fig. 11 are open. In (c) the voltage was measured when switches 3 and 4 in Fig. 11 are closed.

3 Deterministic models

We first model the NOR gates, then we use those models to model the RSFF. This is accomplished by constructing continuous extensions and approximating the behavior of the TCU and Chua’s circuit. We have also provided simplified schematics in Fig. 4 to help illustrate the modeling process. It should be noted, that while in the experiments we use a high voltage of 1.84 volts, in our models this is normalized to 1.

One may suggest solving Matsumoto’s equation [4] for Chua’s circuit as part of the model. While this would be a legitimate approach, the goal of the article is to formulate the simplest model in terms of derivation and simulation. Having to solve the ordinary differential equation at each time step would be reasonable for a two gate circuit, but would not be scalable to large chaotic logical circuits with many gates. For these reasons, we forgo explicitly modeling the capacitor voltages, and instead develop models for the threshold voltages and the outputs, then show that the derived capacitor voltages agree reasonably well with experiments and *MultiSIM* simulations in addition to showing the threshold and outputs agree surprisingly well with the experiments and simulations.

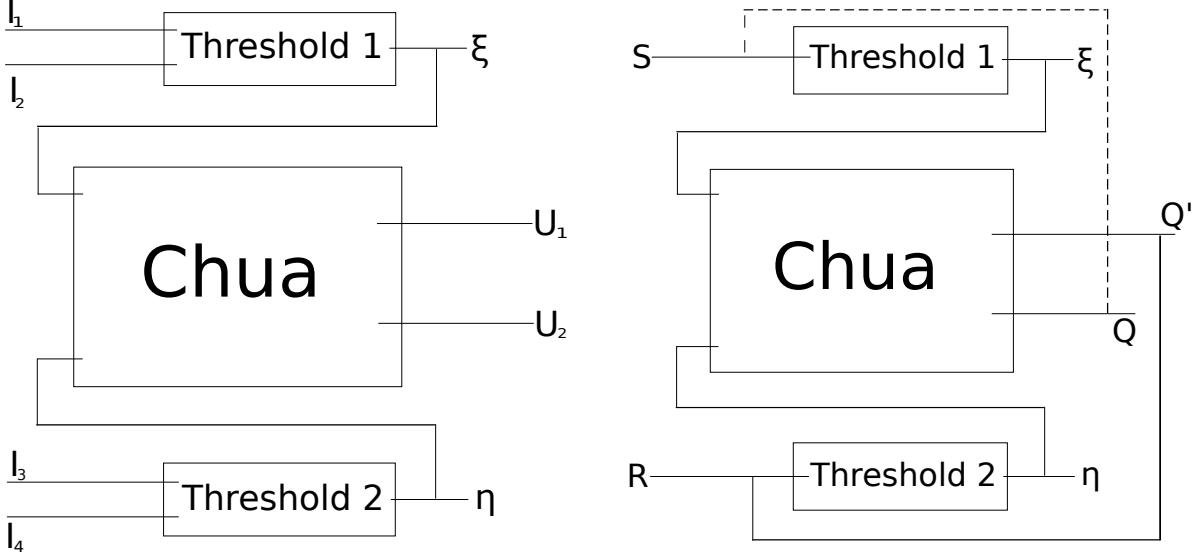
3.1 NOR gate

Here we derive and analyze the NOR gate models. The schematic for the gates given in Fig. 11 may be simplified to Fig. 4a in order to get a general picture of the circuit. It should be noted that the blocks are not absolutely accurate as the block labeled “Chua” has additional op-amps to that of the traditional Chua circuit and feedback from the “Chua” block to the threshold blocks are not explicitly shown.

3.1.1 Derivation

We begin by formulating the simplest continuous extension of the NOR operator: $x \bar{\vee} y = (1 - x)(1 - y)$. This gives us the equation,

$$\begin{aligned} U_1 &= (1 - I_1)(1 - I_2), \\ U_2 &= (1 - I_3)(1 - I_4); \end{aligned} \quad (1)$$



(a) Simplified schematic of two chaotic NOR gates via Chua's circuit and TCUs

(b) Simplified schematic of a chaotic RS flip-flop via Chua's circuit and TCUs

Figure 4: Simplified schematics used to illustrate the building blocks of the models.

where U are the respective outputs and I are the respective inputs as shown in Fig. 4a. This naïve extension is enough to approximate the behavior for the NOR gate outputs, and we shall also modify them later to simulate certain subtle aspects of the circuit. However, the more interesting dynamics are observed in the TCUs.

First, let us define the maps, $f : [0, 1]^2 \times [-2, 2] \rightarrow [-2, 2]$ and $g : [0, 1]^2 \times [-1, 1] \rightarrow [-1, 1]$, where the chosen intervals are the operating domains of the TCUs by design. We apply these maps to the inputs and current time threshold voltages to get the next time threshold voltages,

$$\begin{aligned} \xi_{n+1} &= f(I_1, I_2, \xi_n), \\ \eta_{n+1} &= g(I_1, I_2, \eta_n); \end{aligned} \quad (2)$$

where ξ and η are the respective threshold voltages as shown in Fig. 4a.

Next, we tabulate our observations from Figs. 2 and 12 in (3), and formulate functions f and g that qualitatively reproduce the observed behavior. It should be noted that henceforth we shall denote a seemingly random voltage (in the chaotic regime) by a star (\star), where \star is not a number to be measured, but rather denotes chaotic behavior.

$$\begin{aligned} f(0, 0, 0) &= 0 & f(1, 0, 1) &= f(0, 1, 1) = 1 & f(1, 1, \star) &= \star, \\ g(0, 0, -1) &= -1 & g(1, 0, 0) &= g(0, 1, 0) = 0 & g(1, 1, \star) &= \star. \end{aligned} \quad (3)$$

In order to satisfy these criteria, we first define the maps, $y_f : [-2, 2] \rightarrow [-2, 2]$ and $y_g : [-1, 1] \rightarrow [-1, 1]$, then

$$\begin{aligned} f(I_1, I_2, x_1) &:= |I_1 - I_2| + I_1 I_2 y_f(x_1), \\ g(I_3, I_4, x_2) &:= |I_3 - I_4| - 1 + I_3 I_4 y_g(x_2); \end{aligned} \quad (4)$$

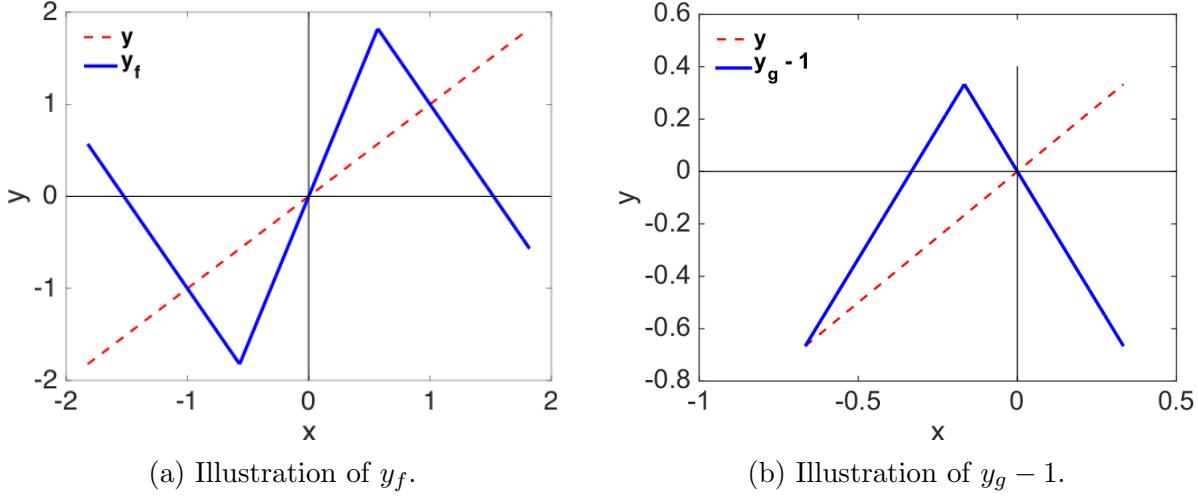


Figure 5: Plots of y_f and y_g for fixed values of $\mu_f, \nu_f, \mu_g, \nu_g$.

satisfies each property except chaotic behavior.

Now, we must formulate y_f and y_g such that (4) reproduces the qualitative behavior of the threshold voltages for $(I_1, I_2) = (1, 1)$ and $(I_3, I_4) = (1, 1)$ as shown in Fig. 2. We postulate y_f and y_g will be tent map - like, which is reasonable in the physical sense since these op-amps influence the signal in an approximately piecewise linear manner. Furthermore, the NOR gate developed by Murali *et al.* employed a TCU designed to behave in a similar manner to that of a logistic map [9], and a tent map is topologically conjugate to a logistic map. For y_f we write,

$$y_f(x) := \begin{cases} \frac{1+\mu_f}{1-\mu_f}(x + \nu_f) - \mu_f\nu_f & x \in [-\mu_f\nu_f, -\nu_f], \\ \mu_f x & x \in [-\nu_f, \nu_f], \\ \frac{1+\mu_f}{1-\mu_f}(x - \nu_f) + \mu_f\nu_f & x \in [\nu_f, \mu_f\nu_f]; \end{cases} \quad (5)$$

and we write y_g as,

$$y_g(x) := \nu_g + \mu_g \begin{cases} 1 + x - \nu_g & \nu_g - 1 \leq x \leq \nu_g - 1/2, \\ \nu_g - x & \nu_g - 1/2 \leq x \leq \nu_g. \end{cases} \quad (6)$$

We illustrate (5) and (6) in Fig. 5. In Fig. 5a and (5), μ_f is the slope of the middle line segment and it also determines the slope of the other two line segments, whereas ν_f mainly affects the domain of the map. In Fig. 5b and (6), μ_g is twice the height of the map and $1 - \nu_g$ is the amount the new interval is translated from the interval $[0, 1]$. Moreover, all parameters are positive.

This gives us a model of the thresholding in the two NOR gate operation of the circuit.

3.1.2 Basic properties

Since the interesting behavior arises for $(I_1, I_2) = (1, 1)$ and $(I_3, I_4) = (1, 1)$, it suffices to analyze $f(1, 1, x)$ and $g(1, 1, x)$. First we search for the fixed points. From empirical observations we require $g(1, 1, x)$ and $f(1, 1, x)$ to have a fixed point at the origin and $f(1, 1, x)$ to

have two other nonzero fixed points. By definition, the latter has a fixed point at the origin and two nonzero fixed points. However, for the former, we require the right branch to intersect the origin. In order to achieve this, we set $g(1, 1, x) = x = 0$ for $x \in [\nu_g - 1/2, \nu_g]$ (the right branch),

$$0 = -1 + \nu_g + \mu_g \nu_g \Rightarrow \nu_g = \frac{1}{1 + \mu_g}.$$

Furthermore, in order to ensure the inequality, $\nu_g - 1/2 \leq x \leq \nu_g$, we require $\nu_g \leq 1/2$, i.e. $\mu_g \geq 1$.

Now let us identify any additional fixed points for $g(1, 1, x)$, which necessarily lies on the left branch, i.e. $x \in [\nu_g - 1, \nu_g - 1/2]$,

$$\begin{aligned} x_* &= -1 + \nu_g + \mu_g - \nu_g \mu_g + \mu_g x_* \\ \Rightarrow (1 - \mu_g)x_* &= -1 + \frac{1}{1 + \mu_g} + \mu_g - \frac{\mu_g}{1 + \mu_g} = -(1 - \mu_g) + \frac{1 - \mu_g}{1 + \mu_g} \\ \Rightarrow x_* &= -1 + \frac{1}{1 + \mu_g} = -\frac{\mu_g}{1 + \mu_g}. \end{aligned}$$

Next, we identify the two nonzero fixed points for $f(1, 1, x)$. For $x \in [\pm \nu_f, \pm \nu_f \mu_f]$,

$$x_* = \frac{1 + \mu_f}{1 - \mu_f} x_* \pm \left(\mu_f \nu_f - \nu_f \frac{1 + \mu_f}{1 - \mu_f} \right) \Rightarrow \left(\frac{-2\mu_f}{1 - \mu_f} \right) x_* = \mp \nu_f \frac{1 + \mu_f^2}{1 - \mu_f} \Rightarrow x_* = \pm \nu_f \frac{1 + \mu_f^2}{2\mu_f}.$$

For the sake of convenience, we outline the fixed points in Table 1.

To analyze the stability of the fixed points of $g(1, 1, x)$, let us take the derivative,

$$\frac{dg(1, 1, x)}{dx} = \begin{cases} \mu_g & \nu_g - 1 \leq x \leq \nu_g - 1/2, \\ -\mu_g & \nu_g - 1/2 \leq x \leq \nu_g; \end{cases} \quad (7)$$

Both fixed points are sources when $\mu_g > 1$. For $\mu_g = 1$, there is a line of fixed points on the left branch such that it constitutes a global attracting set. Clearly, this case is unphysical, and hence we require $\mu_g > 1$.

Taking the derivative for $f(1, 1, x)$ gives,

$$\frac{df(1, 1, x)}{dx} = \begin{cases} \frac{1+\mu_f}{1-\mu_f} & x \in [-\mu_f \nu_f, -\nu_f], \\ \mu_f & x \in [-\nu_f, \nu_f], \\ \frac{1+\mu_f}{1-\mu_f} & x \in [\nu_f, \mu_f \nu_f]; \end{cases} \quad (8)$$

By definition, $\mu_f \geq 1$, since otherwise the two outer branches would be undefined. If $\mu_f = 1$, there is a line of fixed points on the middle branch, and hence this too is unphysical. Therefore, we require $\mu_f > 1$, which shows the origin is a source. For the other two fixed points, if $(1 + \mu_f)/(1 - \mu_f) < -1$ they are sinks and if $(1 + \mu_f)/(1 - \mu_f) > -1$ they are sources. Notice that $(1 + \mu_f)/(1 - \mu_f) = -1$ only when $\mu = 0$, which we showed was impossible. Now, if $(1 + \mu_f)/(1 - \mu_f) < -1$, $1 < -1$, which is false. If $(1 + \mu_f)/(1 - \mu_f) > -1$, $1 > -1$, which is true. Therefore, these fixed points are always sources.

The fixed points along with the conditions on the parameters required to yield physical results are summarized in the table below,

Equation	Fixed points	Conditions
$g(1, 1, x)$	$x_* = 0, -\frac{\mu_g}{1 + \mu_g}$	$\mu_g > 1$
$f(1, 1, x)$	$x_* = 0, \pm \nu_f \frac{1 + \mu_f^2}{2\mu_f}$	$\mu_f > 1$ and $\nu_f > 0$

Table 1: Summary of fixed points and conditions on parameters to cause all fix points to be sources.

3.1.3 Chaos

Here we shall prove the maps $g(1, 1, x)$ and $f(1, 1, x)$ become chaotic for certain parameters. First we prove this for $g(1, 1, x)$, which employs a simple translation to the tent map.

Theorem 1. *The map $g(1, 1, x)$ is chaotic for $\mu_g \geq 2$. In addition, it has a nonwandering set in the form of a translated Cantor set on $[1 - \nu_g, \nu_g]$ for $\mu_g > 2$. Moreover, for $\mu = 3$, the nonwandering set is the middle-third Cantor set translated to the interval $[1 - \nu_g, \nu_g]$.*

Proof. Consider the translation $(u, v) = H(x, y) : [1 - \nu_g, \nu_g]^2 \rightarrow [0, 1]^2$, defined as $(u, v) = (x + 1 - \nu_g, g(1, 1, x) + 1 - \nu_g)$, applied to $g(1, 1, x)$. This produces the map $v = T_{\mu_g(u)} : [0, 1] \rightarrow [0, 1]$, which is exactly the tent map. Since H is a homeomorphism, it suffices to analyze the tent map. It is well known that when $\mu \geq 2$, the tent map is chaotic. Furthermore, for $\mu > 2$, the nonwandering set is a Cantor set, and for $\mu = 3$, it is precisely the middle-third Cantor set. This shows the map $g(1, 1, x)$ is also chaotic for $\mu_g \geq 2$, and has a nonwandering set in the form of a translated Cantor set, thereby completing the proof. \square

Now we prove $f(1, 1, x)$ is chaotic in the physical parameter regime outlined in Table 1. For the sake of brevity, we assume the parameters are in this regime for our next theorem. The main idea of the proof is to search for 3-cycles and use the main theorem by Li and Yorke [19]. Since the formula for f^3 becomes overly complex, we shall use properties of f^3 to show the existence of a 3-cycle rather than finding it explicitly, and we provide visual aids to illustrate the proof.

Theorem 2. *For every $n \in \mathbb{N}$ there exists a periodic point $p_n \in [-\mu_f \nu_f, \mu_f \nu_f]$ of the map $f(1, 1, x)$ having period n and $[-\mu_f \nu_f, \mu_f \nu_f]$ contains chaotic orbits of f . Furthermore, there exists an uncountable set $S \subset [-\mu_f \nu_f, \mu_f \nu_f]$ containing no periodic orbits.*

Proof. It is shown in [19] that a 3-cycle implies chaos. Now, we show there exists a 3-cycle for all parameter values in the physical regime. This is done by finding the roots of f^3 not including the fixed points, or rather showing they exist.

First, let P_n be the set of roots of f^n , then $P_3 \setminus P_1$ is the set of points having period 3. We observe f^3 (Fig. 6) has 17 linear branches. Since these are linear, each branch may intersect the line $y = x$ at most once. The two outermost branches will never intersect the

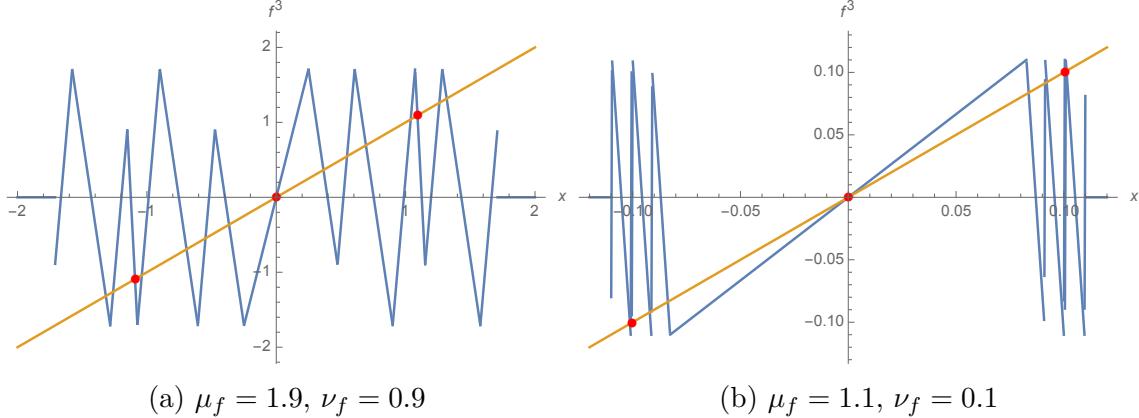


Figure 6: Plots of f^3 for parameters in the physical regime of Table 1 with parameters similar to that of the experiments and simulation and parameters just within the physical regime respectively. It should be noted that the gaps between certain branches in Fig. 6b are due to computational inaccuracy and in reality all branches connect.

line $y = x$ for the parameter regime outlined in Table 1. Then $\max(\text{card}(P_3)) = 15$ and $\text{card}(P_1) = 3$ (i.e. f has three fixed points), hence $\max(\text{card}(P_3 \setminus P_1)) = 12$. Notice, a 3-cycle exists only if $\text{card}(P_3 \setminus P_1) \in \{6, 12\}$ due to the symmetry.

We observe (Fig. 6a) $\text{card}(P_3 \setminus P_1) = 12$ for the parameters near that used in simulations. If μ_f and ν_f are varied forward we maintain $\text{card}(P_3 \setminus P_1) = 12$. If we vary them backward, the first instance $\text{card}(P_3 \setminus P_1) \neq 12$ occurs when the cusps of the second and third branches from the left, and respectively from the right, lie on the line $f(1, 1, x) = x$. The cusps are located at

$$\hat{x} = \pm \left(\nu_f + \mu_f \nu_f \frac{\mu_f - 1}{\mu_f + 1} - \frac{\nu_f (\mu_f - 1)}{\mu_f (\mu_f + 1)} \right), \quad f(1, 1, \hat{x}) = \pm \mu_f \nu_f.$$

Then, solving $\hat{x} = f(1, 1, \hat{x})$ for μ_f , gives $\mu_f = 1$, which is unphysical. Since $\text{card}(P_3 \setminus P_1) = 12$ in the parameter regime of Table 1, 3-cycles (in fact, four of them) exist. Therefore, the hypotheses of [19] is satisfied, thereby completing the proof. \square

3.2 Set/reset flip-flop

Now that we have a model for the NOR gates we can derive the model of the RSFF. Just as with the NOR gate, we sketch a simplified schematic of the RSFF in Fig. 4b. For the traditional RSFF, the outputs from each NOR gate is fed back into the other. Therefore, we replace I_1 and I_3 with R and S and I_2 and I_4 with Q and Q' in (4) and (1),

$$\begin{aligned} f(R, Q', x_1) &:= |R - Q'| + RQ'y_f(x_1), \\ g(S, Q, x_2) &:= |S - Q| - 1 + SQy_g(x_2); \end{aligned} \tag{9}$$

$$\begin{aligned} Q_{n+1} &= (1 - R)(1 - Q'_n), \\ Q'_{n+1} &= (1 - S)(1 - Q_n). \end{aligned} \tag{10}$$

It should be noted that (9) must be used in conjunction with (2).

3.3 Comparison with experiments

From the models of the circuit we can simulate the NOR gate and RSFF operations. The codes for the simulations are quite simple with the majority of it dedicated to iterating (2) for both operations. For both the NOR gate and RSFF, we assume there is a “circuit frequency”, which we define as the amount of time it takes a signal to traverse the entire circuit, and is on the order of 100 microseconds. We also set the following parameters: $\mu_f = 3.2$, $\nu_f = 0.5694$, $\mu_g = 2$, and $\nu_g = 1/3$.

Furthermore, for the NOR gate, while the model is not stochastic (no added noise), we do make small deterministic perturbations in the inputs to approximate the effects of noise and demonstrate sensitivity to initial conditions. For I_2 and I_4 , from the 20 millisecond mark to the 40 millisecond mark we add 10^{-9} , and from the 60 millisecond mark to the 80 millisecond mark we subtract 10^{-9} . This equates to less than a nano-volt difference (recall the voltage used in the experiments is 1.84 volts). The simulations are plotted in Fig. 7.

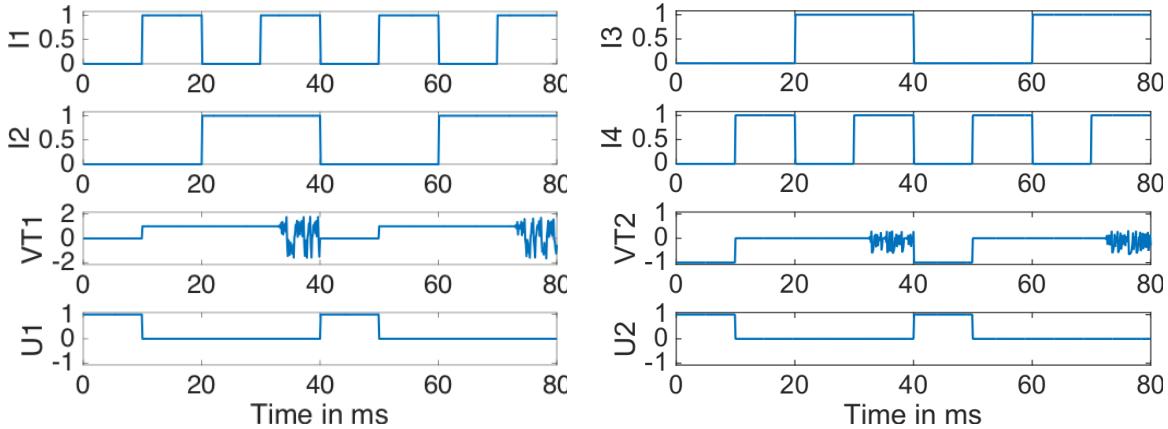
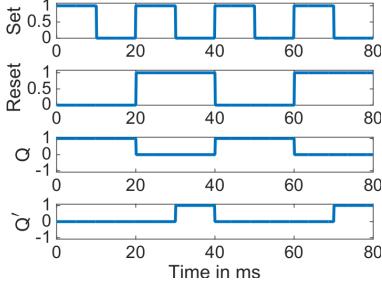


Figure 7: Simulations of the two input voltages, threshold voltage, and output voltages respectively for NOR gate operations.

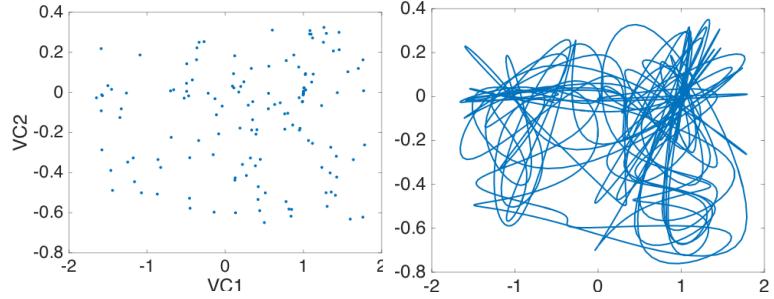
Notice, we have surprisingly close agreement with Fig. 2. The model even replicates the lag observed in the second threshold (in Fig. 2 the second threshold voltage seems to remain close to zero for a few milliseconds). The only dynamics that were missed are the effects on the outputs at the clock edges. This shall be rectified in the sequel.

For the RSFF, we employ the same circuit frequency and perturbation on the initial conditions. This is plotted in Fig. 8a. Moreover, in the circuit design, the outputs are achieved by taking the difference between the voltage across the capacitors and their respective threshold voltages. However, we approach this from the other direction where we have a model for the outputs and threshold voltages and take the sum to predict the voltage across the capacitors. Since our system is discrete and the phase plane of Chua’s circuit is continuous, we interpolate between the respective points. While this is not perfectly accurate, it illustrates a more complete picture of the dynamics than the purely discrete case. This is plotted in Fig. 8b.

Again, as with the NOR gate, we are able to reproduce the behavior for the RSFF except for the clock edge effects. We also plot the iterate plane for the capacitor voltages. This can be thought of as iterates of a Poincaré map of the double scroll attractor. After interpolating



(a) Plots of two input voltages and simulation of two output voltages respectively for RSFF operations.



(b) Simulation of the capacitor voltages. On the left we plot the individual points from the model. On the right we interpolate between these plots using 2000 points between each two iterates.

Figure 8: Simulation of RSFF operation.

between the iterates, we observe a double scroll like projection in the plane. However, it is not exactly a double scroll projection, nor can it be due to the artificial interpolation.

4 Stochastic model for set/reset flip-flop

4.1 Derivation

Now let us rectify the discrepancies between Figs. 7, 8a and Figs. 2, 3. Physically, the oscillations observed at certain clock edges are caused by a non-binary difference in the capacitor voltage and threshold voltage (recall that the outputs are calculated by subtracting the threshold voltage from the capacitor voltage). However, we take a different approach, developing a model for the threshold voltages and output voltages rather than determining the output voltages via the other two as explained in Sec. 3. In order to accomplish this, we must still rely on the physical intuition of the thresholding mechanism.

Whenever the inputs are such that they cause a threshold to change its state drastically (not including the gradual transition to chaos), the TCU attempts to synchronize the capacitor voltage with the threshold voltage for the proper output. This causes a competition between the capacitor voltage (under the influence of the previous input) and the TCU (stimulated by the current input), which the TCU finally wins. During this process, due to the chaotic nature of both the capacitor voltages and threshold voltages, each path to synchronization is different. Since we do not have the explicit model for the capacitor voltages, we will treat this competition as a stochastic process.

During the transitions that lead to the edge effect, we assume there is a probability at each time step that the output will either accept the new inputs or be induced by the weighted average of inputs from previous time steps, where the weights are also determined randomly (or rather, pseudo-randomly). Here we define time step as the reciprocal of the circuit frequency.

Consider the sequences $\{m\}_1^M$, $\{n\}_0^N$, and $\{t\}_0^T$, such that $T = N + 1$ and $M = T$. Let N be the number of time steps in the past that affect future outcomes and T be the number of

time steps after the edge that the output is affected (usually about 1 millisecond). Further, let $\{w_j^{(t)}, \dots, w_j^{(t-n+1)}, w_j^{(t-n)}, w_j^{(t-n-1)}, \dots, w_j^{(t-N)}\} \subseteq \{m\}_1^M$ be the weights applied, with the same probability, out of $\{m\}_1^M$, to the respective inputs, $I_j^{(t-n)}$ for $j = \{1, 2, 3, 4\}$. Let $p(t) = \{0, 1\}$ be some random variable for each time t , with not necessarily identical distributions. In addition, let

$$A_j^{(t)} = \begin{cases} I_j^{(t)} & \text{if } p(t) = 0, \\ \left(\sum_{n=0}^N w_j^{(t-n)} I_j^{(t-n)}\right) / \sum_{n=0}^N w_j^{(t-n)} & \text{if } p(t) = 1; \end{cases} \quad (11)$$

be the perceived input. Then we substitute $A_j^{(t)}$ into (1) for the respective inputs,

$$\begin{aligned} U_1(t) &= \left(1 - A_1^{(t)}\right) \left(1 - A_2^{(t)}\right), \\ U_2(t) &= \left(1 - A_3^{(t)}\right) \left(1 - A_4^{(t)}\right); \end{aligned} \quad (12)$$

to model the effects at the transition points. It should be noted that besides the transition points, which last about a millisecond, the outputs behave as described by the continuous extensions. Finally, In order to simulate noise produced by the wave generator, we add/subtract a small random term, $\epsilon \in \mathbb{R}$, to the inputs (i.e. $I_j \rightarrow I_j + \epsilon$).

For the RSFF, we use the same technique, except this time we plug (11) in only for the R and S . Hence, for the transitions, (10) becomes,

$$\begin{aligned} Q_{n+1}(t) &= \left(1 - A_1^{(t)}\right) (1 - Q'_n), \\ Q'_{n+1}(t) &= \left(1 - A_3^{(t)}\right) (1 - Q_n). \end{aligned} \quad (13)$$

4.2 Comparison with experiments

To simulate the models we use the same values for parameters in y_f and y_g , and for the circuit frequency, as Sec. 3.3. For the NOR gate and RSFF we set $M = N + 1 = T = 11$ (i.e. approximately 1 millisecond) and $\epsilon = \pm O(10^{-8})$. The choice of ϵ describes a physical signal which has less than 1 nano-volt of noise, on average. The simulations for the NOR gate are plotted in Fig. 9. We observe that these are precisely the type of damped oscillations seen in Fig. 2.

The RSFF and capacitor voltage simulations are plotted in Fig. 10a and 10b respectively. Observe that the oscillations match the type in Fig. 3b. Furthermore, Fig. 10b is now qualitatively more similar to Fig. 2b.

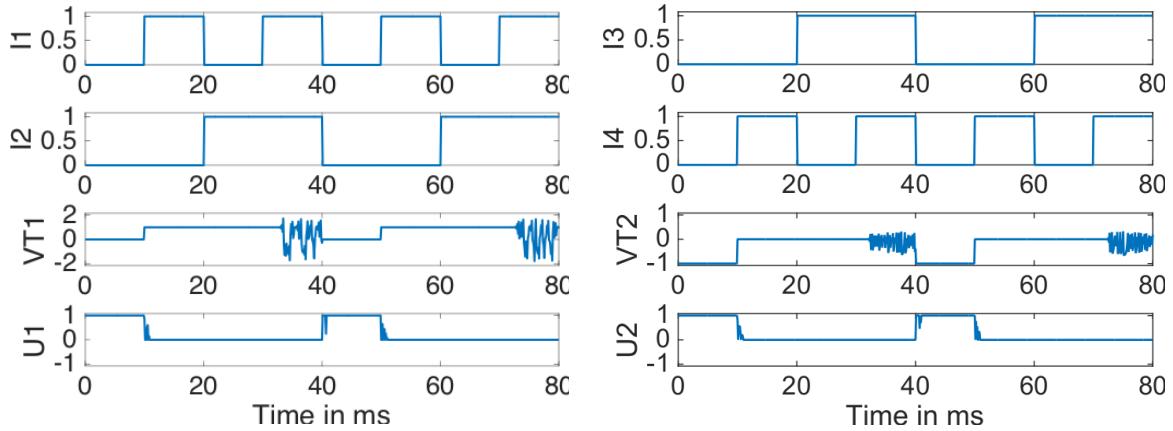
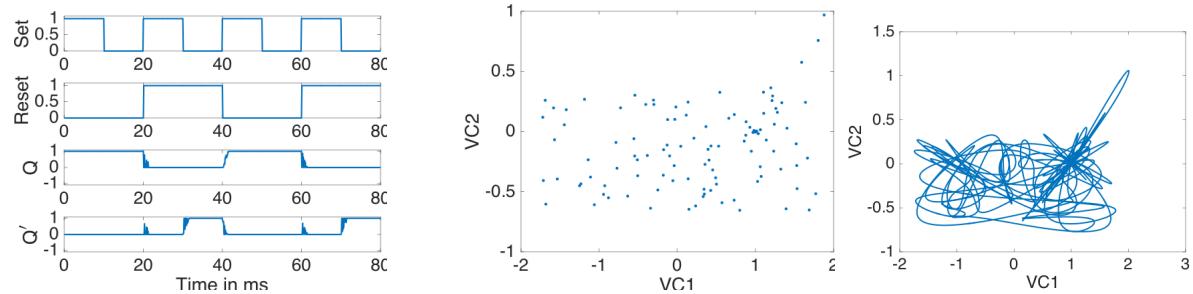


Figure 9: Stochastic simulations of the two input voltages, threshold voltage, and output voltages respectively for NOR gate operations.



(a) Plots of two input voltages and simulation of two output voltages respectively for RSFF operations.

(b) Stochastic simulation of the capacitor voltages. On the left we plot the individual points from the model. On the right we interpolate between these plots using 2000 points between each two iterates.

Figure 10: Simulation of RSFF operation.

5 Conclusions

In the context of chaotic logical circuits there has been many *SPICE* simulations, some experiments, and only a few models. Simpler chaotic logical circuits are modeled as ordinary differential equations [3, 13]. More complex ones are generally studied using *SPICE* simulations [9, 10, 11] and physical realizations [9, 10]. We studied the RSFF/dual NOR gate through experiments, dynamical modeling, simulations, and analysis of the models.

By modifying the circuit in [11] we designed an RSFF/dual NOR gate using modern components. We then simulated the circuit using *MultiSIM* to confirm the new design produces the proper outputs. Next we put together a physical realization of the circuit and conducted experiments to show agreement with *MultiSIM*. By observing the behavior of the circuit and using properties of TCUs as seen in [9, 10] we are able to model the dynamics of the circuit as difference equations. The chaotic behavior of the models are verified by standard dynamical systems analysis for one-dimensional maps. Finally, we simulate our models to show agreement with both experiments and *MultiSIM*. It was expected that the original deterministic models would not be sufficient to replicate the “race” behavior observed in the outputs. Therefore, we inserted probabilistic elements to show this edge-trigger phenomenon, thereby deriving a stochastic model.

While we are able to capture much of the behavior, there is a need for more sophisticated models to replicate the more complex “race” behavior. Furthermore, as this is a rich problem, and we have a physical realization, many new phenomena may arise. It shall be useful to study various physical bifurcations as we make changes in the circuit and make connections with topological bifurcations. We predict this will lead to local bifurcations such as transcritical, pitchfork, and Neimark–Sacker as observed in other models [16, 18], and novel global bifurcations previously unobserved in the literature. We shall also endeavor to build other more complex circuits to study analogs of other logic families and exploit the chaotic and logical properties for the purposes of encryption and secure communication.

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A *MultiSIM* and Physical Realization

Type	Quantity	Code	Comments
1 $k\Omega$ Resistor	9		
100 $k\Omega$ Resistor	14		
1.6 $k\Omega$ Resistor	2		
22 $k\Omega$ Resistor	2		
220 $k\Omega$ Resistor	2		
2.2 $k\Omega$ Resistor	1		
3.3 $k\Omega$ Resistor	1		
100 nF Capacitor	1		
10 nF Capacitor	1		
18 mH Inductor	1		
Op-Amp	6	AD713JN	Used only in <i>MultiSIM</i>
Op-Amp	1	LM759CP	Used only in <i>MultiSIM</i>
Op-Amp	7	NTE858m	Used only in physical realization

Table 2: List of components.

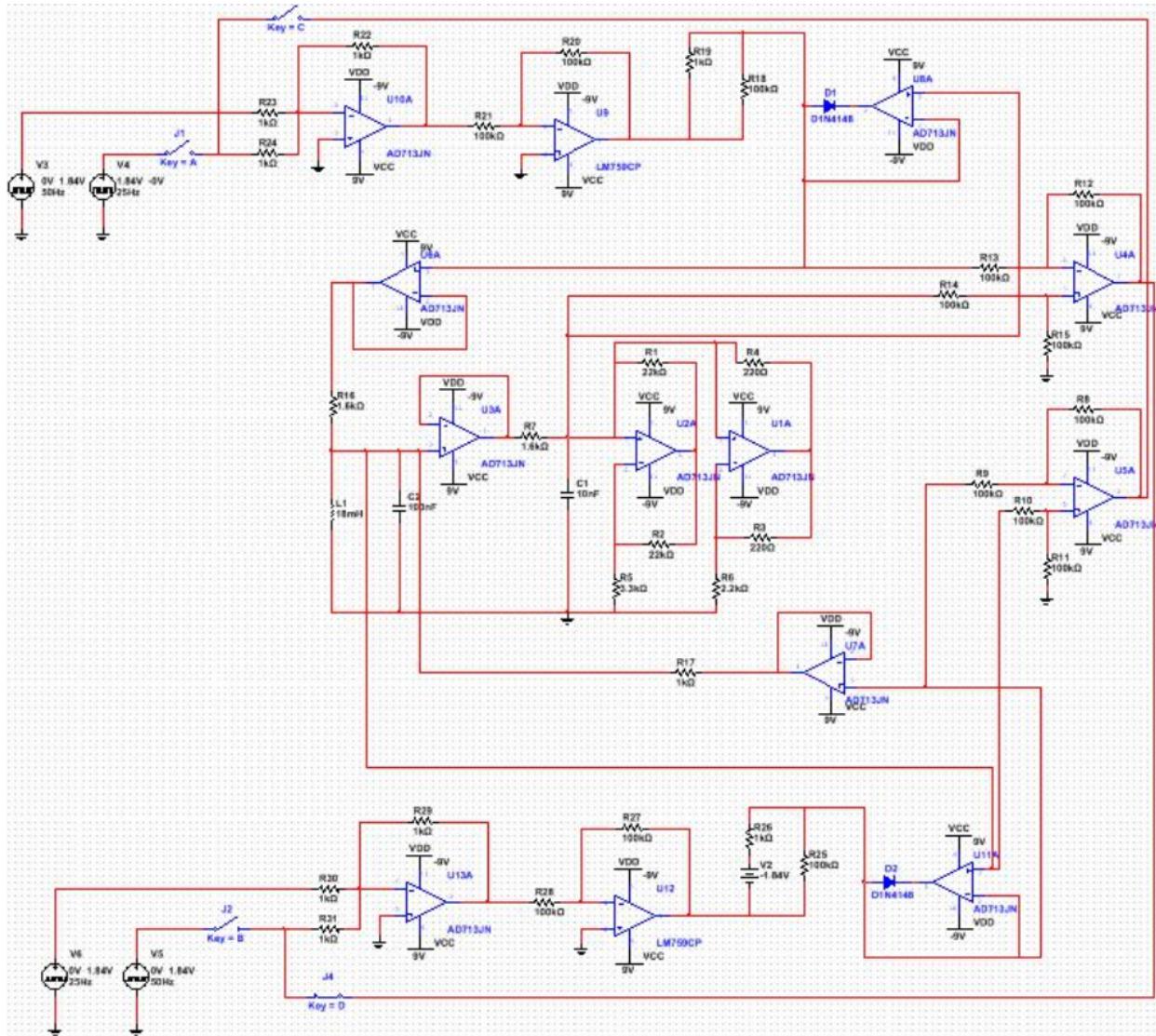


Figure 11: Full schematic of the RSFF/dual NOR design.

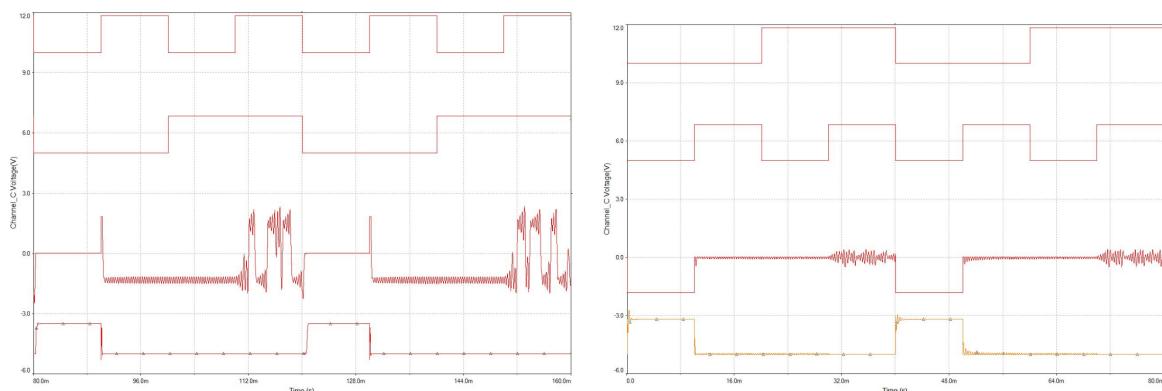


Figure 12: *MultiSIM* plots of the two input voltages, threshold voltage, and output voltages respectively for the two separate NOR gates.

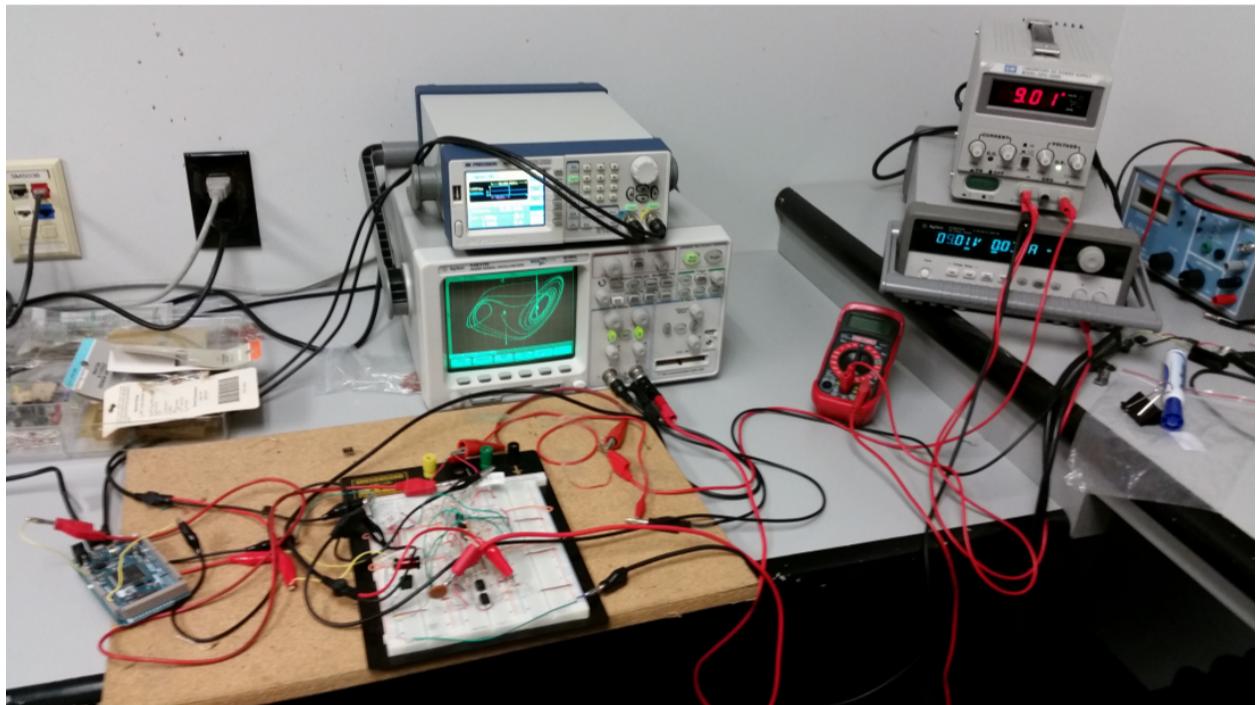


Figure 13: Experimental setup