Run Length Encoding 之

電路設計與後端

Digital-Based Design Flow

流程實作

學號:M16131111

姓名:童品綸

1. 電路功能介紹與應用:

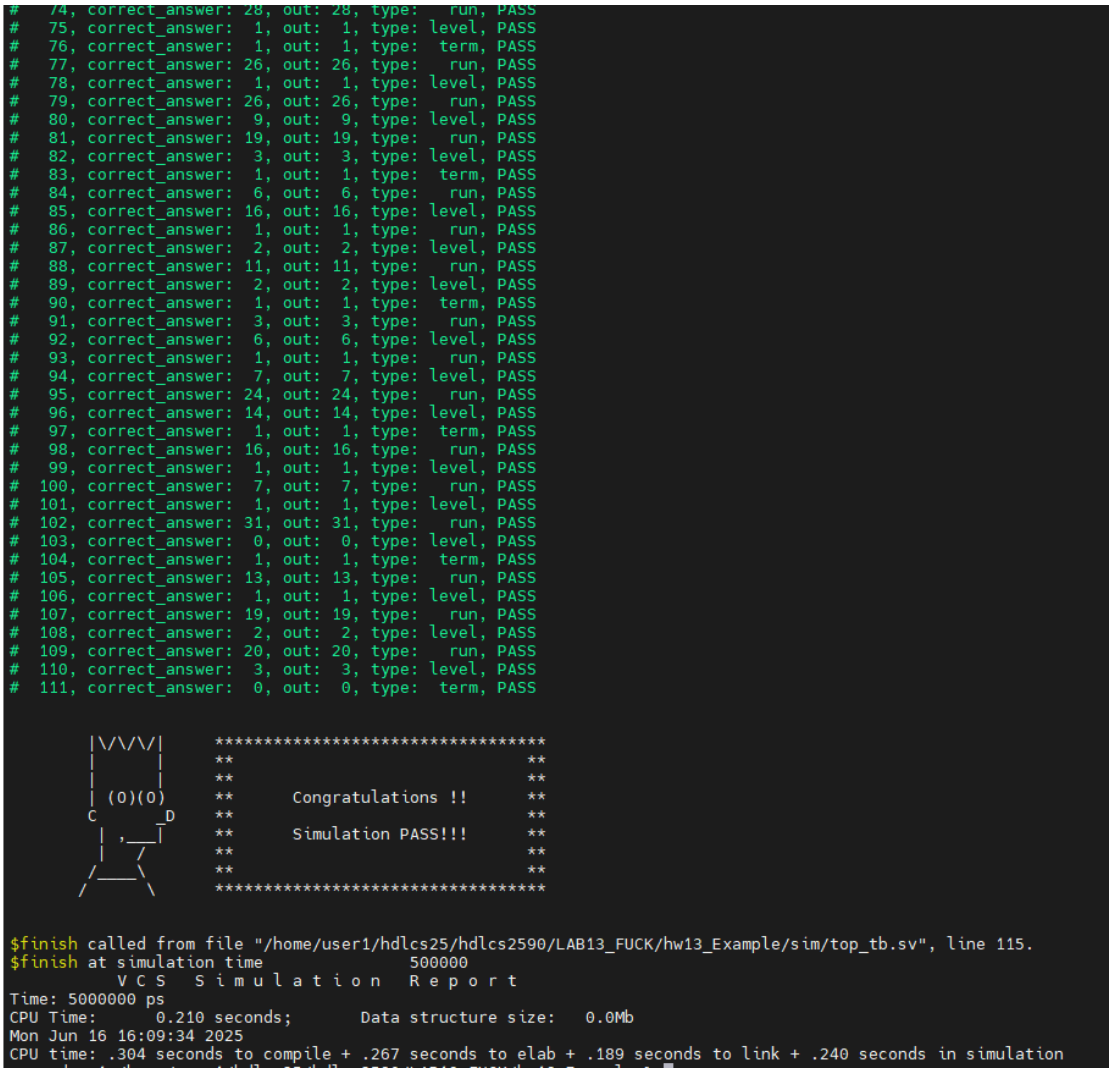
此次電路是 RLE，是一種可變長度編碼，可以讓資料有大量 0 時，大幅降低資料 symbol 數量，再會出現大量 0 的場景，如人工智慧模型中經過 ReLU 運算或權重剪枝後，資料會出現大量的 0，因此可以在傳回 DRAM 時可以經過編碼，從 DRAM 讀出來後再進行解碼，如此一來可以大幅降低與 DRAM 傳輸之資料量。

電路功能驗證:

RTL_SIM TEST=0:

```
#   67, correct_answer:  1, out:  1, type:   run, PASS
#   68, correct_answer: 10, out: 10, type: level, PASS
#   69, correct_answer:  1, out:  1, type:  term, PASS
#   70, correct_answer: 22, out: 22, type:   run, PASS
#   71, correct_answer:  2, out:  2, type: level, PASS
#   72, correct_answer:  1, out:  1, type:   run, PASS
#   73, correct_answer: 11, out: 11, type: level, PASS
#   74, correct_answer: 29, out: 29, type:   run, PASS
#   75, correct_answer: 11, out: 11, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer:  0, out:  0, type:   run, PASS
#   78, correct_answer:  5, out:  5, type: level, PASS
#   79, correct_answer:  2, out:  2, type:   run, PASS
#   80, correct_answer:  1, out:  1, type: level, PASS
#   81, correct_answer:  9, out:  9, type:   run, PASS
#   82, correct_answer:  3, out:  3, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer:  1, out:  1, type:   run, PASS
#   85, correct_answer:  3, out:  3, type: level, PASS
#   86, correct_answer: 24, out: 24, type:   run, PASS
#   87, correct_answer:  8, out:  8, type: level, PASS
#   88, correct_answer: 24, out: 24, type:   run, PASS
#   89, correct_answer:  4, out:  4, type: level, PASS
#   90, correct_answer:  1, out:  1, type:  term, PASS
#   91, correct_answer:  1, out:  1, type:   run, PASS
#   92, correct_answer:  4, out:  4, type: level, PASS
#   93, correct_answer: 15, out: 15, type:   run, PASS
#   94, correct_answer:  1, out:  1, type: level, PASS
#   95, correct_answer: 31, out: 31, type:   run, PASS
#   96, correct_answer:  0, out:  0, type: level, PASS
#   97, correct_answer:  1, out:  1, type:  term, PASS
#   98, correct_answer: 31, out: 31, type:   run, PASS
#   99, correct_answer:  0, out:  0, type: level, PASS
#  100, correct_answer: 31, out: 31, type:   run, PASS
#  101, correct_answer:  0, out:  0, type: level, PASS
#  102, correct_answer: 10, out: 10, type:   run, PASS


       |\/\/\/|     **********************************
       |      |     **                              **
       |      |     **                              **
       | (O)(O)     **      Congratulations !!      **
       C      _D    **                              **
        | ,__|      **      Simulation PASS!!!      **
        |  /        **                              **
       /___\        **                              **
      /     \       **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/hw13_Example/sim/top_tb.sv", line 115.
$finish at simulation time              500000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.220 seconds;       Data structure size:   0.0Mb
Mon Jun 16 16:08:08 2025
CPU time: .314 seconds to compile + .277 seconds to elab + .183 seconds to link + .257 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/hw13_Example %
```

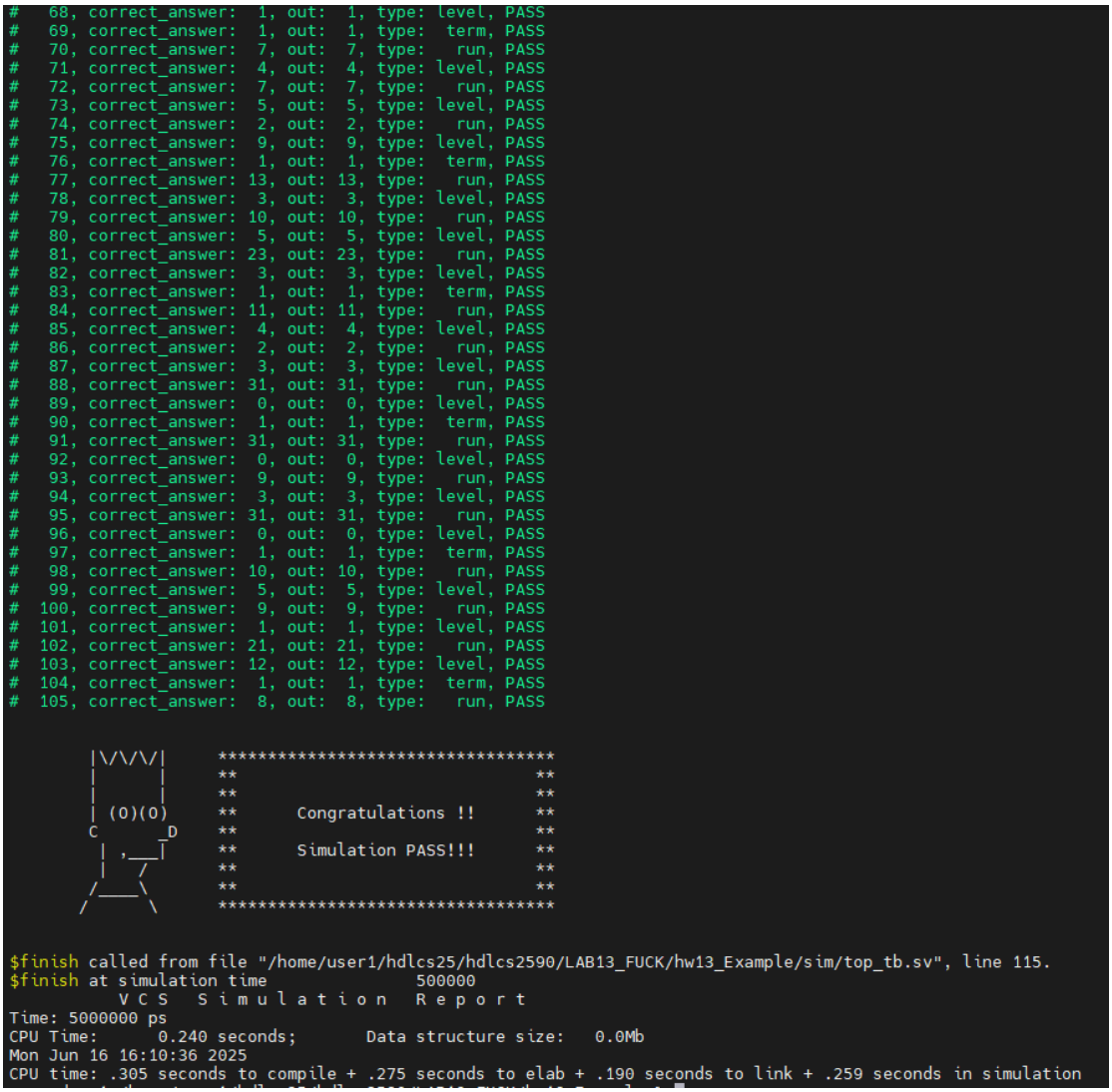
RTL_SIM TEST=1:



RTL_SIM TEST=2:

```
#   57, correct_answer:  0, out:  0, type: level, PASS
#   58, correct_answer: 10, out: 10, type:   run, PASS
#   59, correct_answer:  6, out:  6, type: level, PASS
#   60, correct_answer: 31, out: 31, type:   run, PASS
#   61, correct_answer:  0, out:  0, type: level, PASS
#   62, correct_answer:  1, out:  1, type:  term, PASS
#   63, correct_answer: 16, out: 16, type:   run, PASS
#   64, correct_answer:  5, out:  5, type: level, PASS
#   65, correct_answer:  5, out:  5, type:   run, PASS
#   66, correct_answer:  3, out:  3, type: level, PASS
#   67, correct_answer: 11, out: 11, type:   run, PASS
#   68, correct_answer:  6, out:  6, type: level, PASS
#   69, correct_answer:  1, out:  1, type:  term, PASS
#   70, correct_answer:  8, out:  8, type:   run, PASS
#   71, correct_answer:  6, out:  6, type: level, PASS
#   72, correct_answer:  3, out:  3, type:   run, PASS
#   73, correct_answer:  4, out:  4, type: level, PASS
#   74, correct_answer: 20, out: 20, type:   run, PASS
#   75, correct_answer:  8, out:  8, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer:  0, out:  0, type:   run, PASS
#   78, correct_answer:  3, out:  3, type: level, PASS
#   79, correct_answer:  4, out:  4, type:   run, PASS
#   80, correct_answer:  7, out:  7, type: level, PASS
#   81, correct_answer: 10, out: 10, type:   run, PASS
#   82, correct_answer:  2, out:  2, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer: 10, out: 10, type:   run, PASS
#   85, correct_answer:  8, out:  8, type: level, PASS
#   86, correct_answer: 15, out: 15, type:   run, PASS
#   87, correct_answer:  5, out:  5, type: level, PASS
#   88, correct_answer: 24, out: 24, type:   run, PASS
#   89, correct_answer:  2, out:  2, type: level, PASS
#   90, correct_answer:  1, out:  1, type:  term, PASS
#   91, correct_answer:  1, out:  1, type:   run, PASS
#   92, correct_answer: 10, out: 10, type: level, PASS
#   93, correct_answer:  6, out:  6, type:   run, PASS
#   94, correct_answer:  1, out:  1, type: level, PASS


       |\/\/\/|     **********************************
       |      |     **                              **
       |      |     **                              **
       | (O)(O)     **      Congratulations !!      **
       C      _D    **                              **
        | ,___|     **      Simulation PASS!!!      **
        |   /       **                              **
       /____\       **                              **
      /      \      **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/hw13_Example/sim/top_tb.sv", line 115.
$finish at simulation time              500000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.220 seconds;       Data structure size:   0.0Mb
Mon Jun 16 16:10:12 2025
CPU time: .307 seconds to compile + .284 seconds to elab + .199 seconds to link + .245 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/hw13_Example %
```

RTL_SIM TEST=3:



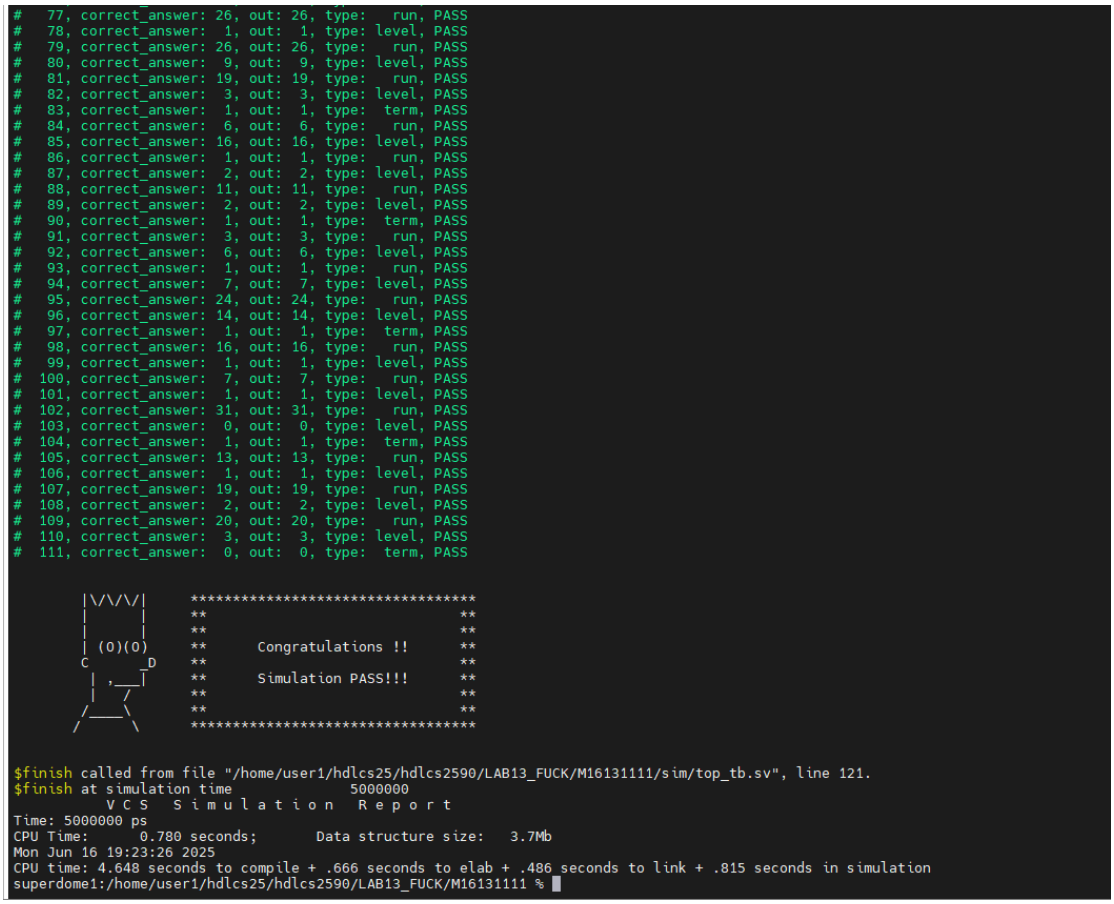
RTL_SIM TEST=4

```
#   56, correct_answer: 16, out: 16, type:   run, PASS
#   57, correct_answer:  4, out:  4, type: level, PASS
#   58, correct_answer: 31, out: 31, type:   run, PASS
#   59, correct_answer:  0, out:  0, type: level, PASS
#   60, correct_answer:  1, out:  1, type:   run, PASS
#   61, correct_answer: 14, out: 14, type: level, PASS
#   62, correct_answer:  1, out:  1, type:  term, PASS
#   63, correct_answer:  8, out:  8, type:   run, PASS
#   64, correct_answer:  5, out:  5, type: level, PASS
#   65, correct_answer: 31, out: 31, type:   run, PASS
#   66, correct_answer:  0, out:  0, type: level, PASS
#   67, correct_answer:  7, out:  7, type:   run, PASS
#   68, correct_answer:  5, out:  5, type: level, PASS
#   69, correct_answer:  1, out:  1, type:  term, PASS
#   70, correct_answer:  3, out:  3, type:   run, PASS
#   71, correct_answer:  4, out:  4, type: level, PASS
#   72, correct_answer: 20, out: 20, type:   run, PASS
#   73, correct_answer:  2, out:  2, type: level, PASS
#   74, correct_answer: 24, out: 24, type:   run, PASS
#   75, correct_answer: 10, out: 10, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer:  5, out:  5, type:   run, PASS
#   78, correct_answer:  2, out:  2, type: level, PASS
#   79, correct_answer: 31, out: 31, type:   run, PASS
#   80, correct_answer:  0, out:  0, type: level, PASS
#   81, correct_answer:  6, out:  6, type:   run, PASS
#   82, correct_answer:  3, out:  3, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer: 30, out: 30, type:   run, PASS


        |\/\/\/|     **********************************
        |      |     **                              **
        |      |     **                              **
        | (O)(O)     **      Congratulations !!      **
        C      _D    **                              **
         | ,___|     **      Simulation PASS!!!      **
         |   /       **                              **
        /____\       **                              **
       /      \      **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111/sim/top_tb.sv", line 121.
$finish at simulation time                  500000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.210 seconds;       Data structure size:   0.0Mb
Mon Jun 16 19:22:01 2025
CPU time: .498 seconds to compile + .258 seconds to elab + .181 seconds to link + .238 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111 %
```

POST_SYN_SIM TEST=0

```
#   69, correct_answer:  1, out:  1, type:  term, PASS
#   70, correct_answer: 22, out: 22, type:   run, PASS
#   71, correct_answer:  2, out:  2, type: level, PASS
#   72, correct_answer:  1, out:  1, type:   run, PASS
#   73, correct_answer: 11, out: 11, type: level, PASS
#   74, correct_answer: 29, out: 29, type:   run, PASS
#   75, correct_answer: 11, out: 11, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer:  0, out:  0, type:   run, PASS
#   78, correct_answer:  5, out:  5, type: level, PASS
#   79, correct_answer:  2, out:  2, type:   run, PASS
#   80, correct_answer:  1, out:  1, type: level, PASS
#   81, correct_answer:  9, out:  9, type:   run, PASS
#   82, correct_answer:  3, out:  3, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer:  1, out:  1, type:   run, PASS
#   85, correct_answer:  3, out:  3, type: level, PASS
#   86, correct_answer: 24, out: 24, type:   run, PASS
#   87, correct_answer:  8, out:  8, type: level, PASS
#   88, correct_answer: 24, out: 24, type:   run, PASS
#   89, correct_answer:  4, out:  4, type: level, PASS
#   90, correct_answer:  1, out:  1, type:  term, PASS
#   91, correct_answer:  1, out:  1, type:   run, PASS
#   92, correct_answer:  4, out:  4, type: level, PASS
#   93, correct_answer: 15, out: 15, type:   run, PASS
#   94, correct_answer:  1, out:  1, type: level, PASS
#   95, correct_answer: 31, out: 31, type:   run, PASS
#   96, correct_answer:  0, out:  0, type: level, PASS
#   97, correct_answer:  1, out:  1, type:  term, PASS
#   98, correct_answer: 31, out: 31, type:   run, PASS
#   99, correct_answer:  0, out:  0, type: level, PASS
#  100, correct_answer: 31, out: 31, type:   run, PASS
#  101, correct_answer:  0, out:  0, type: level, PASS
#  102, correct_answer: 10, out: 10, type:   run, PASS


       |\/\/\/|     **********************************
       |      |     **                              **
       |      |     **                              **
       | (O)(O)     **      Congratulations !!      **
       C      _D    **                              **
        | ,___|     **      Simulation PASS!!!      **
        |   /       **                              **
       /____\       **                              **
      /      \      **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111/sim/top_tb.sv", line 121.
$finish at simulation time                  5000000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.930 seconds;       Data structure size:   3.7Mb
Mon Jun 16 19:22:48 2025
CPU time: 7.088 seconds to compile + .665 seconds to elab + .493 seconds to link + .968 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111 %
```

POST_SYN_SIM TEST=1



POST_SYN_SIM TEST=2

```
#   62, correct_answer:  1, out:  1, type:  term, PASS
#   63, correct_answer: 16, out: 16, type:   run, PASS
#   64, correct_answer:  5, out:  5, type: level, PASS
#   65, correct_answer:  5, out:  5, type:   run, PASS
#   66, correct_answer:  3, out:  3, type: level, PASS
#   67, correct_answer: 11, out: 11, type:   run, PASS
#   68, correct_answer:  6, out:  6, type: level, PASS
#   69, correct_answer:  1, out:  1, type:  term, PASS
#   70, correct_answer:  8, out:  8, type:   run, PASS
#   71, correct_answer:  6, out:  6, type: level, PASS
#   72, correct_answer:  3, out:  3, type:   run, PASS
#   73, correct_answer:  4, out:  4, type: level, PASS
#   74, correct_answer: 20, out: 20, type:   run, PASS
#   75, correct_answer:  8, out:  8, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer:  0, out:  0, type:   run, PASS
#   78, correct_answer:  3, out:  3, type: level, PASS
#   79, correct_answer:  4, out:  4, type:   run, PASS
#   80, correct_answer:  7, out:  7, type: level, PASS
#   81, correct_answer: 10, out: 10, type:   run, PASS
#   82, correct_answer:  2, out:  2, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer: 10, out: 10, type:   run, PASS
#   85, correct_answer:  8, out:  8, type: level, PASS
#   86, correct_answer: 15, out: 15, type:   run, PASS
#   87, correct_answer:  5, out:  5, type: level, PASS
#   88, correct_answer: 24, out: 24, type:   run, PASS
#   89, correct_answer:  2, out:  2, type: level, PASS
#   90, correct_answer:  1, out:  1, type:  term, PASS
#   91, correct_answer:  1, out:  1, type:   run, PASS
#   92, correct_answer: 10, out: 10, type: level, PASS
#   93, correct_answer:  6, out:  6, type:   run, PASS
#   94, correct_answer:  1, out:  1, type: level, PASS


        |\/\/\/|     **********************************
        |      |     **                              **
        |      |     **                              **
        | (O)(O)     **      Congratulations !!      **
        C      _D    **                              **
         | ,___|     **      Simulation PASS!!!      **
         |   /       **                              **
        /____\       **                              **
       /      \      **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111/sim/top_tb.sv", line 121.
$finish at simulation time             5000000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.780 seconds;       Data structure size:   3.7Mb
Mon Jun 16 19:24:08 2025
CPU time: 4.577 seconds to compile + .660 seconds to elab + .495 seconds to link + .801 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111 %
```

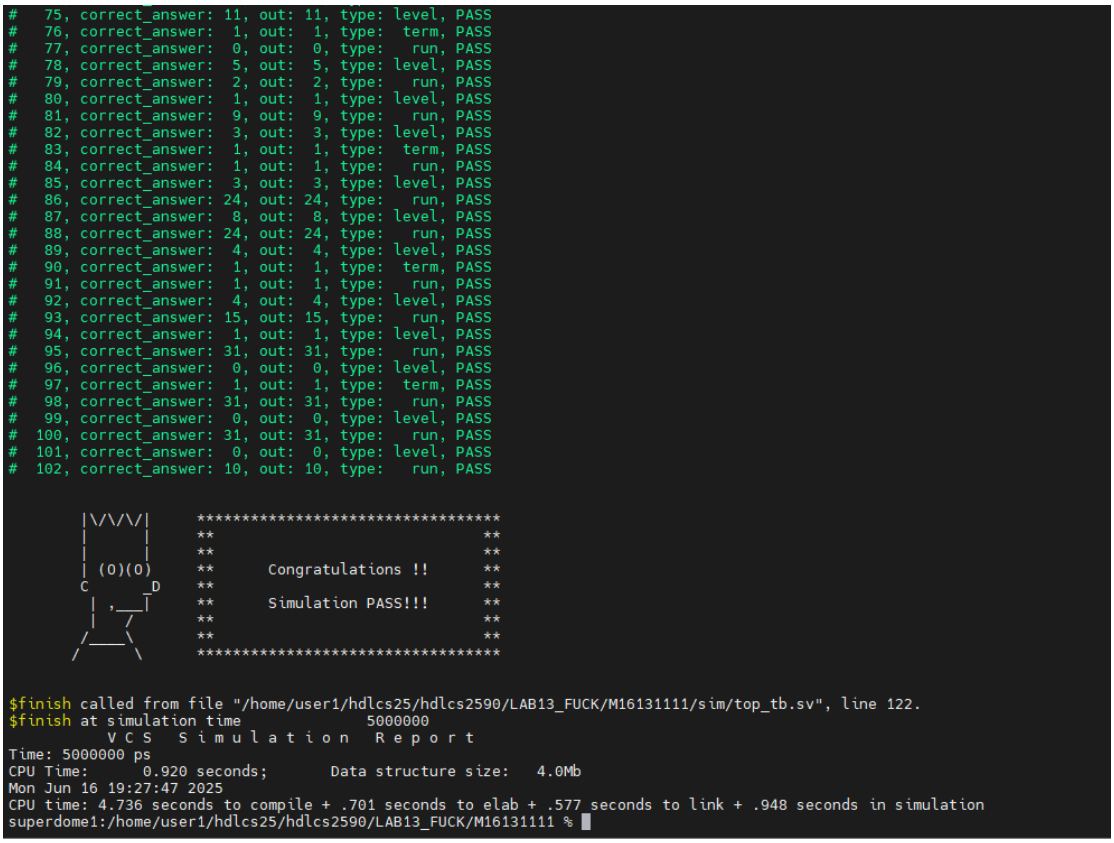
POST_SYN_SIM TEST=3

```
#   74, correct_answer:  2, out:  2, type:   run, PASS
#   75, correct_answer:  9, out:  9, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer: 13, out: 13, type:   run, PASS
#   78, correct_answer:  3, out:  3, type: level, PASS
#   79, correct_answer: 10, out: 10, type:   run, PASS
#   80, correct_answer:  5, out:  5, type: level, PASS
#   81, correct_answer: 23, out: 23, type:   run, PASS
#   82, correct_answer:  3, out:  3, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer: 11, out: 11, type:   run, PASS
#   85, correct_answer:  4, out:  4, type: level, PASS
#   86, correct_answer:  2, out:  2, type:   run, PASS
#   87, correct_answer:  3, out:  3, type: level, PASS
#   88, correct_answer: 31, out: 31, type:   run, PASS
#   89, correct_answer:  0, out:  0, type: level, PASS
#   90, correct_answer:  1, out:  1, type:  term, PASS
#   91, correct_answer: 31, out: 31, type:   run, PASS
#   92, correct_answer:  0, out:  0, type: level, PASS
#   93, correct_answer:  9, out:  9, type:   run, PASS
#   94, correct_answer:  3, out:  3, type: level, PASS
#   95, correct_answer: 31, out: 31, type:   run, PASS
#   96, correct_answer:  0, out:  0, type: level, PASS
#   97, correct_answer:  1, out:  1, type:  term, PASS
#   98, correct_answer: 10, out: 10, type:   run, PASS
#   99, correct_answer:  5, out:  5, type: level, PASS
#  100, correct_answer:  9, out:  9, type:   run, PASS
#  101, correct_answer:  1, out:  1, type: level, PASS
#  102, correct_answer: 21, out: 21, type:   run, PASS
#  103, correct_answer: 12, out: 12, type: level, PASS
#  104, correct_answer:  1, out:  1, type:  term, PASS
#  105, correct_answer:  8, out:  8, type:   run, PASS


       |\/\/\/|     **********************************
       |      |     **                              **
       |      |     **                              **
       | (0)(0)     **      Congratulations !!      **
       C      _D    **                              **
        | ,___|     **      Simulation PASS!!!      **
        |   /       **                              **
       /____\       **                              **
      /      \      **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111/sim/top_tb.sv", line 121.
$finish at simulation time                5000000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.770 seconds;       Data structure size:   3.7Mb
Mon Jun 16 19:24:45 2025
CPU time: 4.509 seconds to compile + .686 seconds to elab + .501 seconds to link + .798 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111 %
```

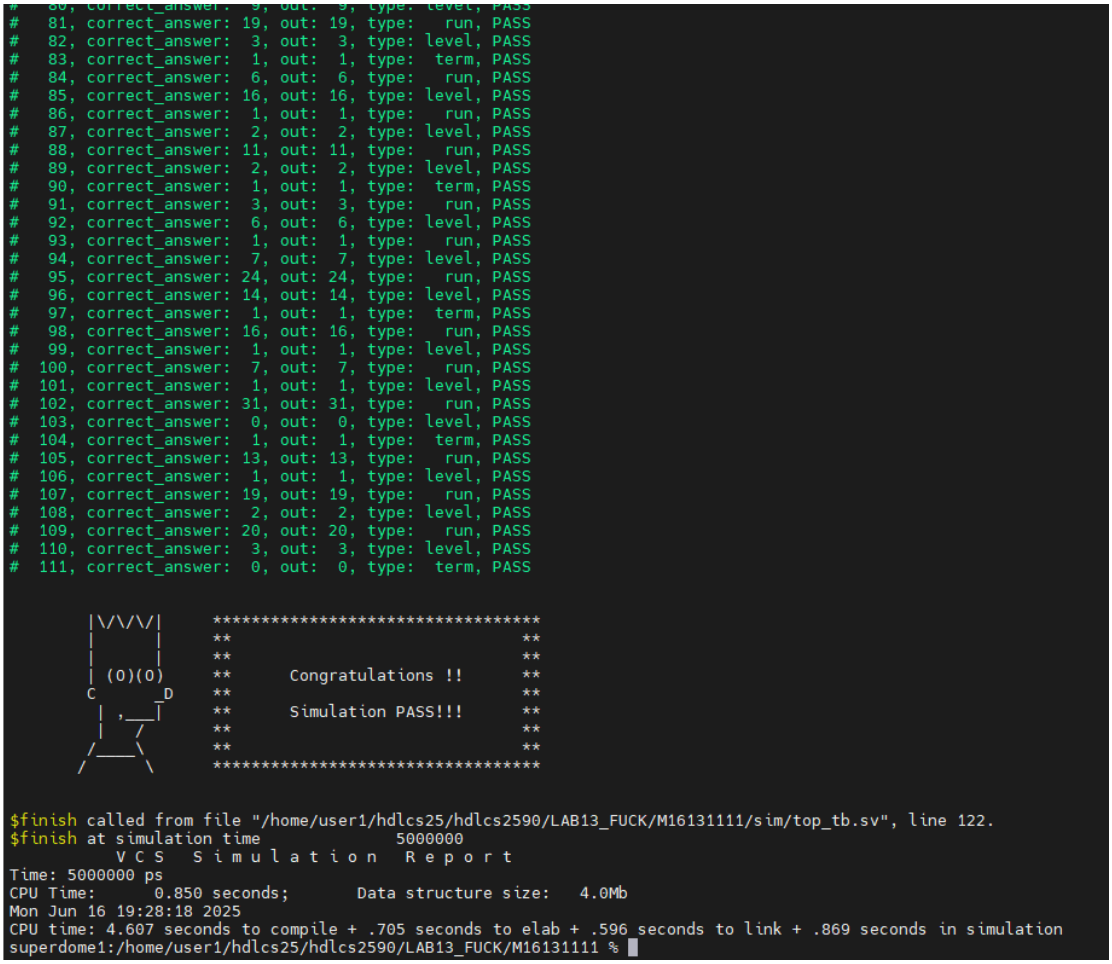
POST_SYN_SIM TEST=4

```
#   55, correct_answer:  1, out:  1, type:  term, PASS
#   56, correct_answer: 16, out: 16, type:   run, PASS
#   57, correct_answer:  4, out:  4, type: level, PASS
#   58, correct_answer: 31, out: 31, type:   run, PASS
#   59, correct_answer:  0, out:  0, type: level, PASS
#   60, correct_answer:  1, out:  1, type:   run, PASS
#   61, correct_answer: 14, out: 14, type: level, PASS
#   62, correct_answer:  1, out:  1, type:  term, PASS
#   63, correct_answer:  8, out:  8, type:   run, PASS
#   64, correct_answer:  5, out:  5, type: level, PASS
#   65, correct_answer: 31, out: 31, type:   run, PASS
#   66, correct_answer:  0, out:  0, type: level, PASS
#   67, correct_answer:  7, out:  7, type:   run, PASS
#   68, correct_answer:  5, out:  5, type: level, PASS
#   69, correct_answer:  1, out:  1, type:  term, PASS
#   70, correct_answer:  3, out:  3, type:   run, PASS
#   71, correct_answer:  4, out:  4, type: level, PASS
#   72, correct_answer: 20, out: 20, type:   run, PASS
#   73, correct_answer:  2, out:  2, type: level, PASS
#   74, correct_answer: 24, out: 24, type:   run, PASS
#   75, correct_answer: 10, out: 10, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer:  5, out:  5, type:   run, PASS
#   78, correct_answer:  2, out:  2, type: level, PASS
#   79, correct_answer: 31, out: 31, type:   run, PASS
#   80, correct_answer:  0, out:  0, type: level, PASS
#   81, correct_answer:  6, out:  6, type:   run, PASS
#   82, correct_answer:  3, out:  3, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer: 30, out: 30, type:   run, PASS


        |\/\/\/|     **********************************
        |      |     **                              **
        |      |     **                              **
        | (0)(0)     **      Congratulations !!      **
        C      _D    **                              **
         | ,___|     **      Simulation PASS!!!      **
         |   /       **                              **
        /____\       **                              **
       /      \      **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111/sim/top_tb.sv", line 121.
$finish at simulation time             5000000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.790 seconds;       Data structure size:   3.7Mb
Mon Jun 16 19:25:16 2025
CPU time: 4.594 seconds to compile + .668 seconds to elab + .506 seconds to link + .825 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111 %
```

POST_LAYOUT_SUM TEST=0



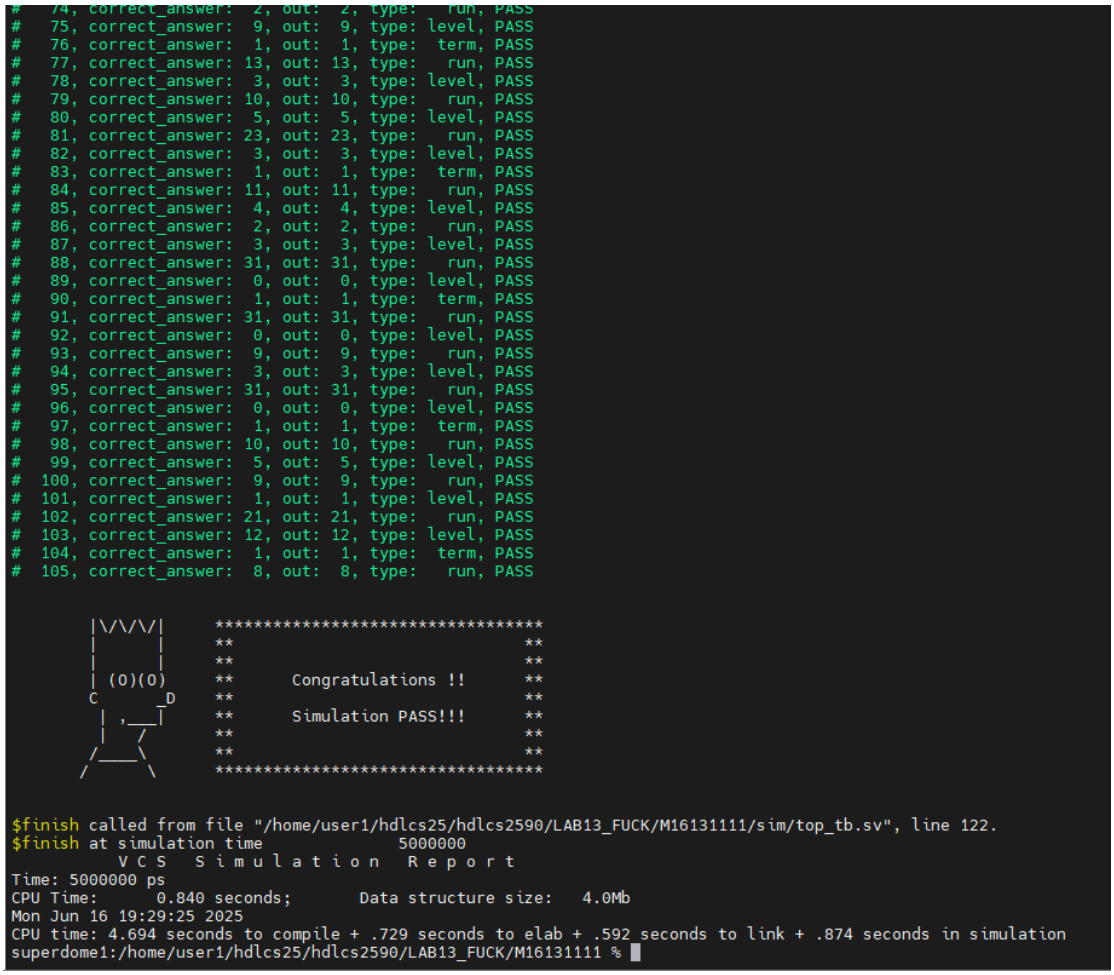
POST_LAYOUT_SUM TEST=1



POST_LAYOUT_SUM TEST=2

```
#   61, correct_answer:  0, out:  0, type: level, PASS
#   62, correct_answer:  1, out:  1, type:  term, PASS
#   63, correct_answer: 16, out: 16, type:   run, PASS
#   64, correct_answer:  5, out:  5, type: level, PASS
#   65, correct_answer:  5, out:  5, type:   run, PASS
#   66, correct_answer:  3, out:  3, type: level, PASS
#   67, correct_answer: 11, out: 11, type:   run, PASS
#   68, correct_answer:  6, out:  6, type: level, PASS
#   69, correct_answer:  1, out:  1, type:  term, PASS
#   70, correct_answer:  8, out:  8, type:   run, PASS
#   71, correct_answer:  6, out:  6, type: level, PASS
#   72, correct_answer:  3, out:  3, type:   run, PASS
#   73, correct_answer:  4, out:  4, type: level, PASS
#   74, correct_answer: 20, out: 20, type:   run, PASS
#   75, correct_answer:  8, out:  8, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer:  0, out:  0, type:   run, PASS
#   78, correct_answer:  3, out:  3, type: level, PASS
#   79, correct_answer:  4, out:  4, type:   run, PASS
#   80, correct_answer:  7, out:  7, type: level, PASS
#   81, correct_answer: 10, out: 10, type:   run, PASS
#   82, correct_answer:  2, out:  2, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer: 10, out: 10, type:   run, PASS
#   85, correct_answer:  8, out:  8, type: level, PASS
#   86, correct_answer: 15, out: 15, type:   run, PASS
#   87, correct_answer:  5, out:  5, type: level, PASS
#   88, correct_answer: 24, out: 24, type:   run, PASS
#   89, correct_answer:  2, out:  2, type: level, PASS
#   90, correct_answer:  1, out:  1, type:  term, PASS
#   91, correct_answer:  1, out:  1, type:   run, PASS
#   92, correct_answer: 10, out: 10, type: level, PASS
#   93, correct_answer:  6, out:  6, type:   run, PASS
#   94, correct_answer:  1, out:  1, type: level, PASS


        |\/\/\/|     **********************************
        |      |     **                              **
        |      |     **                              **
        | (O)(O)     **      Congratulations !!      **
        C      _D    **                              **
         | ,___|     **      Simulation PASS!!!      **
         |   /       **                              **
        /____\       **                              **
       /      \      **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111/sim/top_tb.sv", line 122.
$finish at simulation time                5000000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.850 seconds;       Data structure size:   4.0Mb
Mon Jun 16 19:28:54 2025
CPU time: 4.617 seconds to compile + .721 seconds to elab + .597 seconds to link + .878 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111 %
```

POST_LAYOUT_SUM TEST=3



POST_LAYOUT_SUM TEST=4

```
#   50, correct_answer:  0, out:  0, type: level, PASS
#   51, correct_answer: 11, out: 11, type:   run, PASS
#   52, correct_answer:  3, out:  3, type: level, PASS
#   53, correct_answer: 10, out: 10, type:   run, PASS
#   54, correct_answer: 12, out: 12, type: level, PASS
#   55, correct_answer:  1, out:  1, type:  term, PASS
#   56, correct_answer: 16, out: 16, type:   run, PASS
#   57, correct_answer:  4, out:  4, type: level, PASS
#   58, correct_answer: 31, out: 31, type:   run, PASS
#   59, correct_answer:  0, out:  0, type: level, PASS
#   60, correct_answer:  1, out:  1, type:   run, PASS
#   61, correct_answer: 14, out: 14, type: level, PASS
#   62, correct_answer:  1, out:  1, type:  term, PASS
#   63, correct_answer:  8, out:  8, type:   run, PASS
#   64, correct_answer:  5, out:  5, type: level, PASS
#   65, correct_answer: 31, out: 31, type:   run, PASS
#   66, correct_answer:  0, out:  0, type: level, PASS
#   67, correct_answer:  7, out:  7, type:   run, PASS
#   68, correct_answer:  5, out:  5, type: level, PASS
#   69, correct_answer:  1, out:  1, type:  term, PASS
#   70, correct_answer:  3, out:  3, type:   run, PASS
#   71, correct_answer:  4, out:  4, type: level, PASS
#   72, correct_answer: 20, out: 20, type:   run, PASS
#   73, correct_answer:  2, out:  2, type: level, PASS
#   74, correct_answer: 24, out: 24, type:   run, PASS
#   75, correct_answer: 10, out: 10, type: level, PASS
#   76, correct_answer:  1, out:  1, type:  term, PASS
#   77, correct_answer:  5, out:  5, type:   run, PASS
#   78, correct_answer:  2, out:  2, type: level, PASS
#   79, correct_answer: 31, out: 31, type:   run, PASS
#   80, correct_answer:  0, out:  0, type: level, PASS
#   81, correct_answer:  6, out:  6, type:   run, PASS
#   82, correct_answer:  3, out:  3, type: level, PASS
#   83, correct_answer:  1, out:  1, type:  term, PASS
#   84, correct_answer: 30, out: 30, type:   run, PASS


       |\/\/\/|     **********************************
       |      |     **                              **
       |      |     **                              **
       | (O)(O)     **      Congratulations !!      **
       C      _D    **                              **
        | ,___|     **      Simulation PASS!!!      **
        |   /       **                              **
       /____\       **                              **
      /      \      **********************************


$finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111/sim/top_tb.sv", line 122.
$finish at simulation time                5000000
           V C S   S i m u l a t i o n   R e p o r t
Time: 5000000 ps
CPU Time:      0.990 seconds;       Data structure size:   4.0Mb
Mon Jun 16 19:29:55 2025
CPU time: 4.617 seconds to compile + .744 seconds to elab + .590 seconds to link + 1.015 seconds in simulation
superdome1:/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/M16131111 %
```

2. IN/OUT Pin/Port 宣告 ：

```
module top (
                input clk,
                input rst,
                input [4:0] in_data,
                input in_valid,
                output reg [4:0] out_data,
                output reg out_valid
);
```

```
module CHIP (
    input clk,
    input rst,
    input [4:0] in_data,
    input in_valid,
    output [4:0] out_data,
    output out_valid
);
```

```
//top
PDCDG_V ipad_clk (.C(clk_core), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(clk));
PDCDG_V ipad_rst (.C(rst_core), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(rst));


//left
PDCDG_H ipad_indata0 (.C(in_data_core[0]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[0]));
PDCDG_H ipad_indata1 (.C(in_data_core[1]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[1]));
PDCDG_H ipad_indata2 (.C(in_data_core[2]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[2]));
PDCDG_H ipad_indata3 (.C(in_data_core[3]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[3]));
PDCDG_H ipad_indata4 (.C(in_data_core[4]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[4]));

//bottom
PDCDG_V ipad_in_valid (.C(in_valid_core), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_valid));
PDCDG_V opad_out_valid (.C(), .I(out_valid_core), .IE(1'b0), .OEN(1'b0), .PAD(out_valid));

//right
PDCDG_H opad_odata0 (.C(), .I(out_data_core[0]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[0]));
PDCDG_H opad_odata1 (.C(), .I(out_data_core[1]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[1]));
PDCDG_H opad_odata2 (.C(), .I(out_data_core[2]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[2]));
PDCDG_H opad_odata3 (.C(), .I(out_data_core[3]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[3]));
PDCDG_H opad_odata4 (.C(), .I(out_data_core[4]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[4]));
```

3. Design Compiler

Design constraint

```
set clk_period 4.0
create_clock -name clk    -period $clk_period    [get_ports clk]

set_dont_touch_network          [all_clocks]
set_fix_hold                    [all_clocks]
set_clock_uncertainty    0.1    [all_clocks]
set_clock_latency        0.5    [all_clocks]
set_input_transition     0.2    [all_inputs]
set_clock_transition     0.1    [all_clocks]
set_ideal_network               [all_clocks]

set_dont_touch [get_cells ipad_*]
set_dont_touch [get_cells opad_*]

set_operating_conditions -min_library
N16ADFP_StdCellff0p88v125c -min ff0p88v125c \
                                -max_library
N16ADFP_StdCellss0p72vm40c -max ss0p72vm40c

set_dont_use N16ADFP_StdCellss0p72vm40c/TIEHBWP16P90
set_dont_use N16ADFP_StdCellss0p72vm40c/TIEHBWP16P90LVT
```

```
set_dont_use N16ADFP_StdCellss0p72vm40c/TIEHBWP20P90
set_dont_use N16ADFP_StdCellss0p72vm40c/TIEHBWP20P90LVT
set_dont_use N16ADFP_StdCellss0p72vm40c/TIELBWP16P90
set_dont_use N16ADFP_StdCellss0p72vm40c/TIELBWP16P90LVT
set_dont_use N16ADFP_StdCellss0p72vm40c/TIELBWP20P90
set_dont_use N16ADFP_StdCellss0p72vm40c/TIELBWP20P90LVT
N16ADFP_StdCellff0p88vm40c/TIEHBWP16P90LVT
N16ADFP_StdCellff0p88vm40c/TIEHBWP20P90LVT
N16ADFP_StdCellff0p88vm40c/TIELBWP16P90LVT
N16ADFP_StdCellff0p88vm40c/TIELBWP20P90LVT
set_dont_use N16ADFP_StdCellff0p88v125c/TIEHBWP16P90
set_dont_use N16ADFP_StdCellff0p88v125c/TIEHBWP16P90LVT
set_dont_use N16ADFP_StdCellff0p88v125c/TIEHBWP20P90
set_dont_use N16ADFP_StdCellff0p88v125c/TIEHBWP20P90LVT
set_dont_use N16ADFP_StdCellff0p88v125c/TIELBWP16P90
set_dont_use N16ADFP_StdCellff0p88v125c/TIELBWP16P90LVT
set_dont_use N16ADFP_StdCellff0p88v125c/TIELBWP20P90
set_dont_use N16ADFP_StdCellff0p88v125c/TIELBWP20P90LVT


set input_max_clk      [expr {double(round(1000*$clk_period *
0.6))/1000}]
set input_min_clk      [expr {double(round(1000*$clk_period *
0.0))/1000}]
set output_max_clk     [expr {double(round(1000*$clk_period *
0.1))/1000}]
set output_min_clk     [expr {double(round(1000*$clk_period *
0.0))/1000}]

set_load [load_of
"N16ADFP_StdIOss0p72v1p62v125c/PDCDG_H/PAD"]
[all_outputs]
set_load [load_of
"N16ADFP_StdIOss0p72v1p62v125c/PDCDG_V/PAD"]
[all_outputs]

set_driving_cell -library N16ADFP_StdIOss0p72v1p62v125c -
lib_cell PDCDG_H -pin {C} [all_inputs]
```

set_driving_cell -library N16ADFP_StdIOss0p72v1p62v125c -lib_cell PDCDG_V -pin {C} [all_inputs]

set auto_wire_load_selection

set_wire_load_model -name ZeroWireload -library N16ADFP_StdCellss0p72vm40c

set_max_fanout 10 [all_inputs]
set_max_transition 0.1 [all_inputs]
set_max_capacitance 0.1 [all_inputs]

Area report

area.log

```
1
2  ****************************************
3  Report : area
4  Design : CHIP
5  Version: P-2019.03-SP1-1
6  Date   : Mon Jun 16 16:49:10 2025
7  ****************************************
8
9  Library(s) Used:
10
11     N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/I
12     N16ADFP_StdIOss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package/Collateral
13
14 Number of ports:                        56
15 Number of nets:                       4060
16 Number of cells:                      4000
17 Number of combinational cells:        3302
18 Number of sequential cells:            679
19 Number of macros/black boxes:           14
20 Number of buf/inv:                    1117
21 Number of references:                    3
22
23 Combinational area:            1283.091861
24 Buf/Inv area:                   635.610239
25 Noncombinational area:          774.593308
26 Macro/Black Box area:         23102.004639
27 Net Interconnect area:      undefined  (Wire load has zero net area)
28
29 Total cell area:              25159.689808
30 Total area:                 undefined
31 1
```

Power report

```
Loading db file '/usr/cad/CBDK/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM/N16ADFP_StdIOss0p72v1p62v125c.db'
Loading db file '/usr/cad/CBDK/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/N16ADFP_StdCellss0p72vm40c.db'
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : CHIP
Version: P-2019.03-SP1-1
Date   : Mon Jun 16 16:49:14 2025
****************************************


Library(s) Used:

    N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/N16ADFP_StdCellss0p72vm40c.db)
    N16ADFP_StdIOss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM/N16ADFP_StdIOss0p72v1p62v125c.db)


Operating Conditions: ss0p72vm40c   Library: N16ADFP_StdCellss0p72vm40c
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
CHIP                ZeroWireload       N16ADFP_StdCellss0p72vm40c
top                 ZeroWireload       N16ADFP_StdCellss0p72vm40c
top_DW01_inc_0      ZeroWireload       N16ADFP_StdCellss0p72vm40c
top_DW01_inc_1      ZeroWireload       N16ADFP_StdCellss0p72vm40c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 504.4058 uW   (88%)
  Net Switching Power  =  69.0963 uW   (12%)
                         ---------
Total Dynamic Power    = 573.5021 uW  (100%)

Cell Leakage Power     =   4.0422 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.1033       5.5631e-02        3.1768e+03            0.1621  (  28.06%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           0.3941       3.2542e-04          419.7646            0.3949  (  68.37%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational  7.0098e-03       1.3140e-02          445.6599        2.0596e-02  (   3.57%)
--------------------------------------------------------------------------------------------------
Total              0.5044 mW    6.9096e-02 mW     4.0422e+03 nW         0.5775 mW
1
```

Timing report

Set up:

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : CHIP
Version: P-2019.03-SP1-1
Date   : Mon Jun 16 16:49:14 2025
****************************************

Operating Conditions: ss0p72vm40c   Library: N16ADFP_StdCellss0p72vm40c
Wire Load Model Mode: segmented

  Startpoint: top/out_counter_reg_2_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: top/OUT_buffer_reg_127__0_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  CHIP               ZeroWireload          N16ADFP_StdCellss0p72vm40c
  top                ZeroWireload          N16ADFP_StdCellss0p72vm40c
  top_DW01_inc_1     ZeroWireload          N16ADFP_StdCellss0p72vm40c

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.50       0.50
  top/out_counter_reg_2_/CP (DFCNQD2BWP16P90LVT)          0.00       0.50 r
  top/out_counter_reg_2_/Q (DFCNQD2BWP16P90LVT)           0.06       0.56 f
  top/U721/Z (DEL025D1BWP20P90)                           0.05       0.61 f
  top/U2799/ZN (XNR2D1BWP16P90LVT)                        0.03       0.64 r
  top/U763/Z (AN4D2BWP16P90LVT)                           0.02       0.66 r
  top/U1656/ZN (IOA21D1BWP16P90LVT)                       0.01       0.67 r
  top/U1436/ZN (OAI21D1BWP16P90LVT)                       0.01       0.68 f
  top/U1435/ZN (AOI22D1BWP16P90LVT)                       0.01       0.69 r
  top/U1453/ZN (ND2D1BWP16P90LVT)                         0.01       0.71 f
  top/U1368/ZN (IND2D1BWP16P90LVT)                        0.02       0.73 f
  top/U1126/ZN (ND2D1BWP16P90LVT)                         0.01       0.74 r
  top/U1391/ZN (IOAI21D1BWP16P90LVT)                      0.01       0.75 f
  top/U1390/Z (BUFFD1BWP16P90LVT)                         0.03       0.78 f
  top/U1270/ZN (ND3D1BWP16P90LVT)                         0.01       0.79 r
  top/U1271/ZN (CKND1BWP16P90LVT)                         0.02       0.81 f
  top/U1002/ZN (OAI22D1BWP16P90LVT)                       0.03       0.84 r
  top/U865/ZN (ND2D1BWP16P90LVT)                          0.02       0.86 f
  top/U796/ZN (CKND1BWP16P90LVT)                          0.02       0.88 r
  top/U1600/Z (AN2D1BWP16P90LVT)                          0.02       0.90 r
  top/U1475/ZN (AOI22D1BWP16P90LVT)                       0.01       0.91 f
  top/U1597/ZN (IOA21D1BWP16P90LVT)                       0.01       0.91 r
  top/U63/Z (DEL050D1BWP20P90)                            0.08       1.00 r
  top/OUT_buffer_reg_127__0_/D (DFCNQD2BWP16P90LVT)       0.00       1.00 r
  data arrival time                                                  1.00

  clock clk (rise edge)                                   4.00       4.00
  clock network delay (ideal)                             0.50       4.50
  clock uncertainty                                      -0.10       4.40
  top/OUT_buffer_reg_127__0_/CP (DFCNQD2BWP16P90LVT)      0.00       4.40 r
  library setup time                                      0.00       4.40
  data required time                                                 4.40
  ---------------------------------------------------------------------------
  data required time                                                 4.40
  data arrival time                                                 -1.00
  ---------------------------------------------------------------------------
  slack (MET)                                                        3.40
```

Hold time:

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
        -sort_by group
Design : CHIP
Version: P-2019.03-SP1-1
Date   : Mon Jun 16 16:49:14 2025
****************************************

Operating Conditions: ff0p88v125c   Library: N16ADFP_StdCellff0p88v125c
Wire Load Model Mode: segmented

  Startpoint: top/current_state_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: top/out_valid_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  CHIP               ZeroWireload          N16ADFP_StdCellss0p72vm40c
  top                ZeroWireload          N16ADFP_StdCellss0p72vm40c

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.50       0.50
  top/current_state_reg_1_/CP (DFCNQD2BWP16P90LVT)        0.00       0.50 r
  top/current_state_reg_1_/Q (DFCNQD2BWP16P90LVT)         0.06       0.56 f
  top/U1494/ZN (CKND1BWP16P90LVT)                         0.01       0.57 r
  top/U15/ZN (CKNR2D1BWP20P90)                            0.02       0.59 f
  top/U18/Z (CKBD1BWP16P90LVT)                            0.01       0.60 f
  top/U17/Z (CKBD1BWP16P90LVT)                            0.01       0.61 f
  top/U16/Z (CKBD1BWP16P90LVT)                            0.01       0.62 f
  top/U12/ZN (INVD1BWP16P90LVT)                           0.00       0.62 r
  top/U13/ZN (INVD1BWP16P90LVT)                           0.00       0.63 f
  top/out_valid_reg/D (DFCNQD2BWP16P90LVT)                0.00       0.63 f
  data arrival time                                                  0.63

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.50       0.50
  clock uncertainty                                       0.10       0.60
  top/out_valid_reg/CP (DFCNQD2BWP16P90LVT)               0.00       0.60 r
  library hold time                                       0.03       0.63
  data required time                                                 0.63
  ---------------------------------------------------------------------------
  data required time                                                 0.63
  data arrival time                                                 -0.63
  ---------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

4. Post-Synthesis Timing/Power Report :
Primetime report

Set up time violation path:

max_timing_violati...

```
****************************************
Report : timing
  -path_type full
  -delay_type max
  -slack_lesser_than 0.00
  -max_paths 20
  -sort_by slack
Design : CHIP
Version: P-2019.03-SP5-1
Date   : Mon Jun 16 17:04:31 2025
****************************************

No paths with slack less than 0.00.

1

```

Hold time violation path:

min_timing_violatio...

```
****************************************
Report : timing
  -path_type full
  -delay_type min
  -slack_lesser_than 0.00
  -max_paths 20
  -sort_by slack
Design : CHIP
Version: P-2019.03-SP5-1
Date   : Mon Jun 16 17:04:31 2025
****************************************

No paths with slack less than 0.00.

```

Primepower report

根據 pattern 0 的 toggle 情形之 power 計算:

```
****************************************
Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date   : Mon Jun 16 17:15:56 2025
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network             3.915e-04    0.0000    0.0000 3.915e-04 (72.86%)  i
register                  1.359e-06 2.748e-07 5.172e-07 2.151e-06 ( 0.40%)
combinational             7.066e-06 8.083e-06 4.740e-07 1.562e-05 ( 2.91%)
sequential                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                    7.799e-05 4.705e-05 3.024e-06 1.281e-04 (23.83%)
black_box                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 5.541e-05   (10.31%)
  Cell Internal Power  = 4.780e-04   (88.94%)
  Cell Leakage Power   = 4.015e-06   ( 0.75%)
                         ---------
Total Power            = 5.374e-04  (100.00%)
```

根據 pattern 1 的 toggle 情形之 power 計算:

```
****************************************
Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date   : Mon Jun 16 17:18:17 2025
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network             3.916e-04    0.0000    0.0000 3.916e-04 (71.26%)  i
register                  1.409e-06 2.866e-07 5.161e-07 2.212e-06 ( 0.40%)
combinational             7.427e-06 8.544e-06 4.733e-07 1.644e-05 ( 2.99%)
sequential                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                    8.904e-05 4.721e-05 2.999e-06 1.393e-04 (25.34%)
black_box                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 5.605e-05   (10.20%)
  Cell Internal Power  = 4.894e-04   (89.07%)
  Cell Leakage Power   = 3.988e-06   ( 0.73%)
                         ---------
Total Power            = 5.495e-04  (100.00%)

1
```

根據 pattern 2 的 toggle 情形之 power 計算:

```
****************************************
Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date   : Mon Jun 16 17:19:27 2025
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                         Internal  Switching  Leakage    Total
Power Group              Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network            3.916e-04    0.0000    0.0000 3.916e-04 (72.44%)  i
register                 1.286e-06 2.623e-07 5.088e-07 2.057e-06 ( 0.38%)
combinational            6.447e-06 6.865e-06 4.749e-07 1.379e-05 ( 2.55%)
sequential                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                   8.300e-05 4.713e-05 3.010e-06 1.331e-04 (24.63%)
black_box                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 5.425e-05   (10.04%)
  Cell Internal Power  = 4.824e-04   (89.23%)
  Cell Leakage Power   = 3.993e-06   ( 0.74%)
                         ---------
Total Power            = 5.406e-04  (100.00%)
```

根據 pattern 3 的 toggle 情形之 power 計算:

```
****************************************
Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date   : Mon Jun 16 17:24:34 2025
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                         Internal  Switching  Leakage    Total
Power Group              Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network            3.916e-04    0.0000    0.0000 3.916e-04 (72.35%)  i
register                 1.333e-06 2.723e-07 5.108e-07 2.116e-06 ( 0.39%)
combinational            6.869e-06 7.562e-06 4.748e-07 1.491e-05 ( 2.75%)
sequential                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                   8.252e-05 4.712e-05 3.010e-06 1.326e-04 (24.51%)
black_box                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 5.495e-05   (10.15%)
  Cell Internal Power  = 4.823e-04   (89.11%)
  Cell Leakage Power   = 3.996e-06   ( 0.74%)
                         ---------
Total Power            = 5.413e-04  (100.00%)
```

根據 pattern 4 的 toggle 情形之 power 計算:

```
****************************************
Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date   : Mon Jun 16 17:26:46 2025
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           3.917e-04    0.0000     0.0000 3.917e-04 (73.50%)  i
register                1.201e-06 2.463e-07 5.033e-07 1.951e-06 ( 0.37%)
combinational           5.794e-06 5.869e-06 4.760e-07 1.214e-05 ( 2.28%)
sequential                 0.0000    0.0000     0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000     0.0000    0.0000 ( 0.00%)
io_pad                  7.705e-05 4.704e-05 3.048e-06 1.271e-04 (23.86%)
black_box                  0.0000    0.0000     0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 5.315e-05   ( 9.97%)
  Cell Internal Power  = 4.757e-04   (89.27%)
  Cell Leakage Power   = 4.027e-06   ( 0.76%)
                         ---------
Total Power            = 5.329e-04  (100.00%)
```

5. DFT 驗證與分析 ：

DFT Coverage

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      35359
Possibly detected                PT          7
Undetectable                     UD         29
ATPG untestable                  AU         15
Not detected                     ND          0
-----------------------------------------------
total faults                             35410
test coverage                            99.95%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                        1255
    #basic_scan patterns                  1255
-----------------------------------------------
```

Area/Power before inserting DFT

Area:

area.log

```
****************************************
Report : area
Design : CHIP
Version: P-2019.03-SP1-1
Date   : Mon Jun 16 16:49:10 2025
****************************************

Library(s) Used:

    N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/I
    N16ADFP_StdIOss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package/Collateral

Number of ports:                           56
Number of nets:                          4060
Number of cells:                         4000
Number of combinational cells:           3302
Number of sequential cells:               679
Number of macros/black boxes:              14
Number of buf/inv:                       1117
Number of references:                       3

Combinational area:               1283.091861
Buf/Inv area:                      635.610239
Noncombinational area:             774.593308
Macro/Black Box area:            23102.004639
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 25159.689808
Total area:                 undefined
1
```

Power:

```
Loading db file '/usr/cad/CBDK/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM/N16ADFP_StdIOss0p72v1p62v125c.db'
Loading db file '/usr/cad/CBDK/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/N16ADFP_StdCellss0p72vm40c.db'
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : CHIP
Version: P-2019.03-SP1-1
Date   : Mon Jun 16 16:49:14 2025
****************************************


Library(s) Used:

    N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/N16ADFP_StdCellss0p72vm40c.db)
    N16ADFP_StdIOss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM/N16ADFP_StdIOss0p72v1p62v125c.db)


Operating Conditions: ss0p72vm40c   Library: N16ADFP_StdCellss0p72vm40c
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
CHIP                    ZeroWireload      N16ADFP_StdCellss0p72vm40c
top                     ZeroWireload      N16ADFP_StdCellss0p72vm40c
top_DW01_inc_0          ZeroWireload      N16ADFP_StdCellss0p72vm40c
top_DW01_inc_1          ZeroWireload      N16ADFP_StdCellss0p72vm40c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 504.4058 uW   (88%)
  Net Switching Power  =  69.0963 uW   (12%)
                         ---------
Total Dynamic Power    = 573.5021 uW  (100%)

Cell Leakage Power     =   4.0422 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.1033       5.5631e-02       3.1768e+03            0.1621  (  28.06%)
memory             0.0000           0.0000           0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000           0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000           0.0000            0.0000  (   0.00%)
register           0.3941       3.2542e-04         419.7646            0.3949  (  68.37%)
sequential         0.0000           0.0000           0.0000            0.0000  (   0.00%)
combinational   7.0098e-03       1.3140e-02         445.6599          2.0596e-02  (   3.57%)
--------------------------------------------------------------------------------------------------
Total              0.5044 mW     6.9096e-02 mW     4.0422e+03 nW        0.5775 mW
1
```

Area/Power after inserting DFT

Area:

area.log

```
****************************************
Report : area
Design : CHIP
Version: P-2019.03-SP1-1
Date   : Mon Jun 16 16:53:01 2025
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/C
    N16ADFP_StdIOss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Packag

Number of ports:                        66
Number of nets:                       4927
Number of cells:                      4858
Number of combinational cells:        4160
Number of sequential cells:            679
Number of macros/black boxes:           14
Number of buf/inv:                    2619
Number of references:                    3

Combinational area:            2020.930578
Buf/Inv area:                  1423.059843
Noncombinational area:          915.183327
Macro/Black Box area:         23102.004639
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:              26038.118544
Total area:                 undefined
```

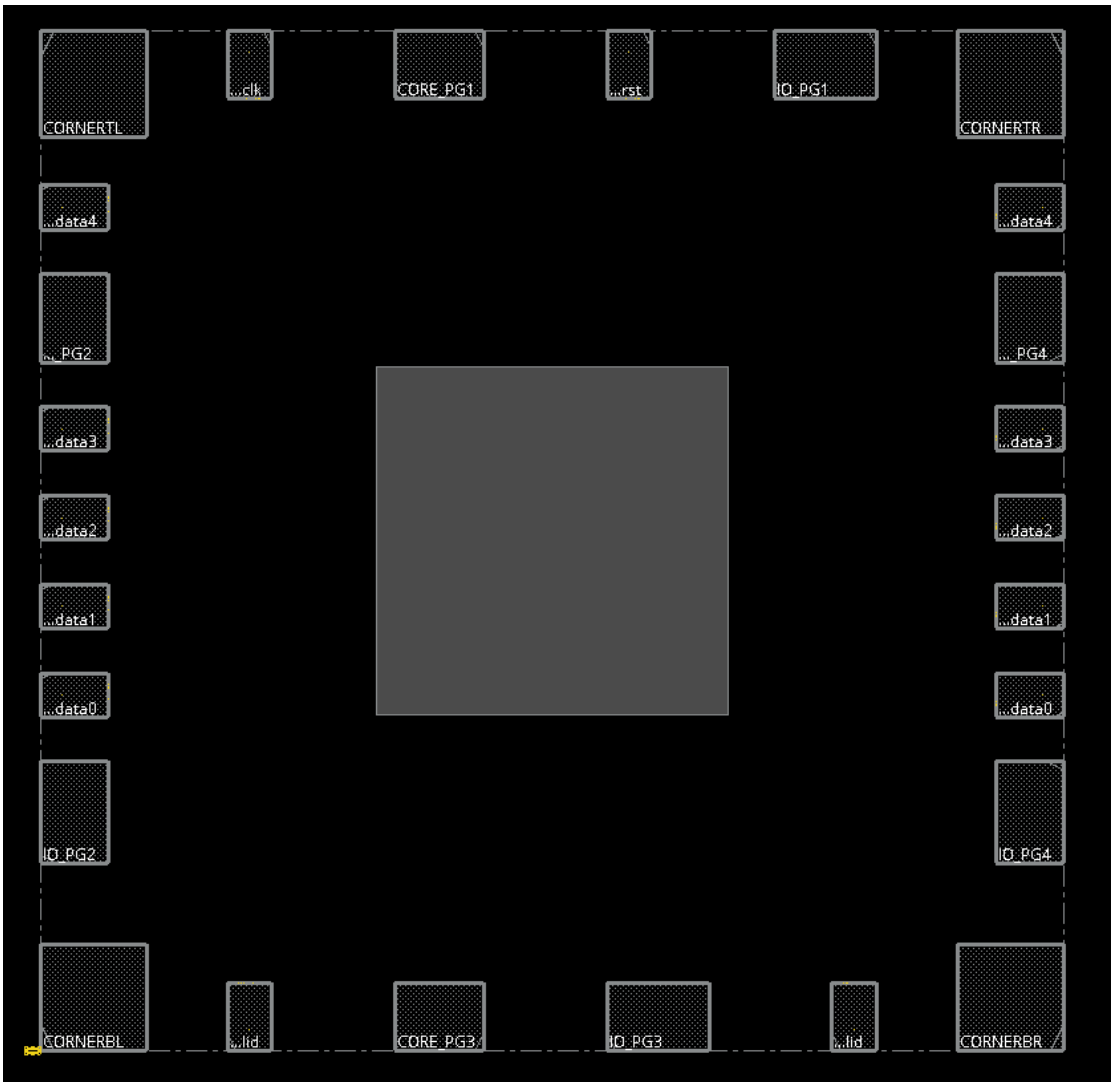
Power:

```
****************************************
Report : power
        -analysis_effort low
Design : CHIP
Version: P-2019.03-SP1-1
Date   : Mon Jun 16 16:53:05 2025
****************************************


Library(s) Used:

    N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/N16ADFP_StdCellss0p72vm40c.db)
    N16ADFP_StdIOss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM/N16ADFP_StdIOss0p72v1p62v125c.db)


Operating Conditions: ss0p72vm40c   Library: N16ADFP_StdCellss0p72vm40c
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
CHIP                ZeroWireload       N16ADFP_StdCellss0p72vm40c
top_test_1          ZeroWireload       N16ADFP_StdCellss0p72vm40c
top_DW01_inc_0      ZeroWireload       N16ADFP_StdCellss0p72vm40c
top_DW01_inc_1      ZeroWireload       N16ADFP_StdCellss0p72vm40c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 482.5706 uW   (86%)
  Net Switching Power  =  75.9865 uW   (14%)
                         ---------
Total Dynamic Power    = 558.5571 uW  (100%)

Cell Leakage Power     =   3.9787 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad         3.4391e-02       5.4254e-02        3.1266e+03        9.1772e-02  (  16.31%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           0.4217        4.6993e-04         154.8525            0.4223  (  75.07%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational  2.6490e-02       2.1262e-02         697.2756        4.8450e-02  (   8.61%)
--------------------------------------------------------------------------------------------------
Total              0.4826 mW     7.5986e-02 mW     3.9787e+03 nW         0.5625 mW
```

6. APR 實作演練與 LVS 成果 ：

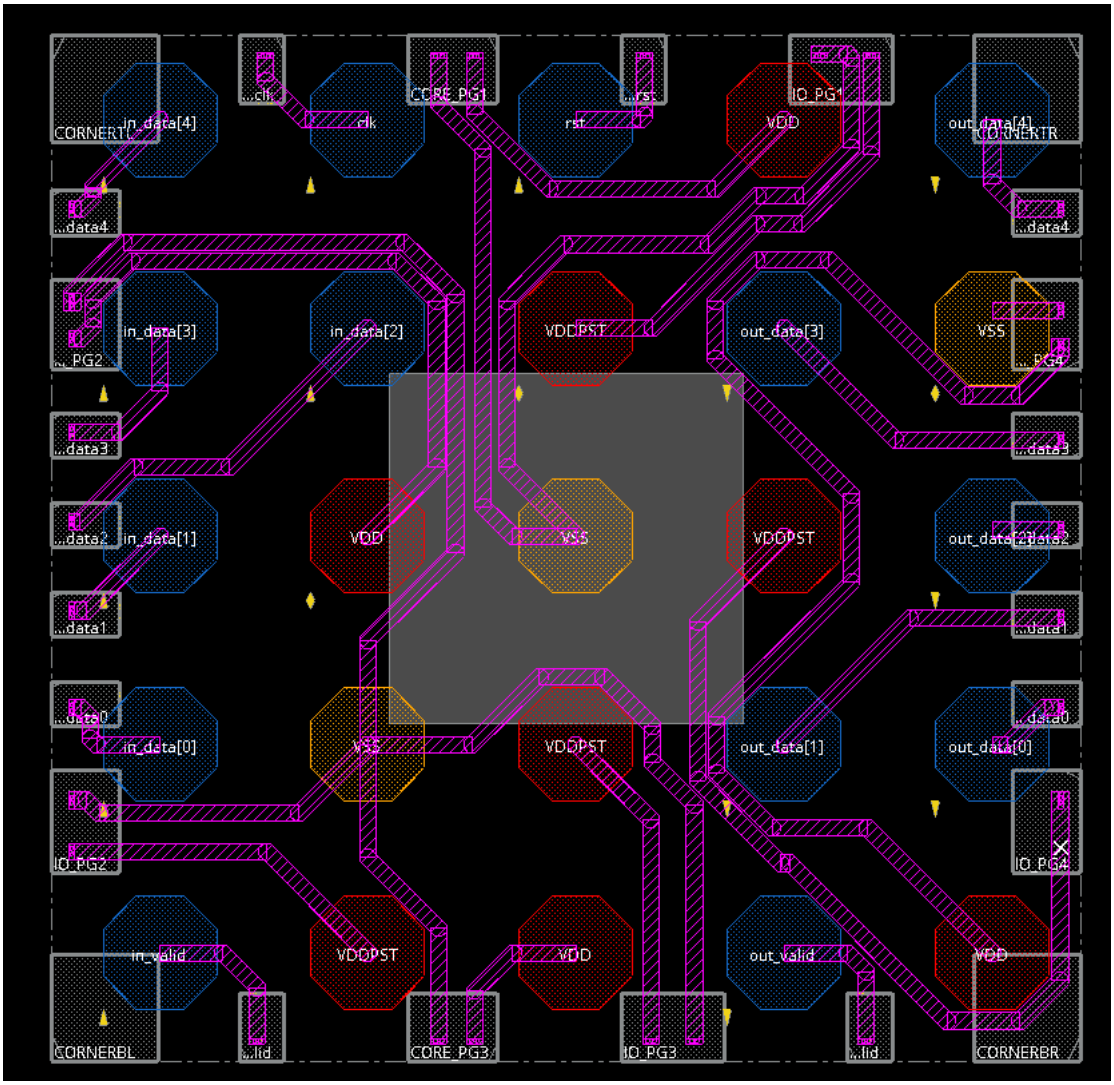
Floorplan

要先擺 IO 然後對齊 FinGrid，並且先看看這樣的擺法以及晶片大小 IO 能不能藉由 bump 出去

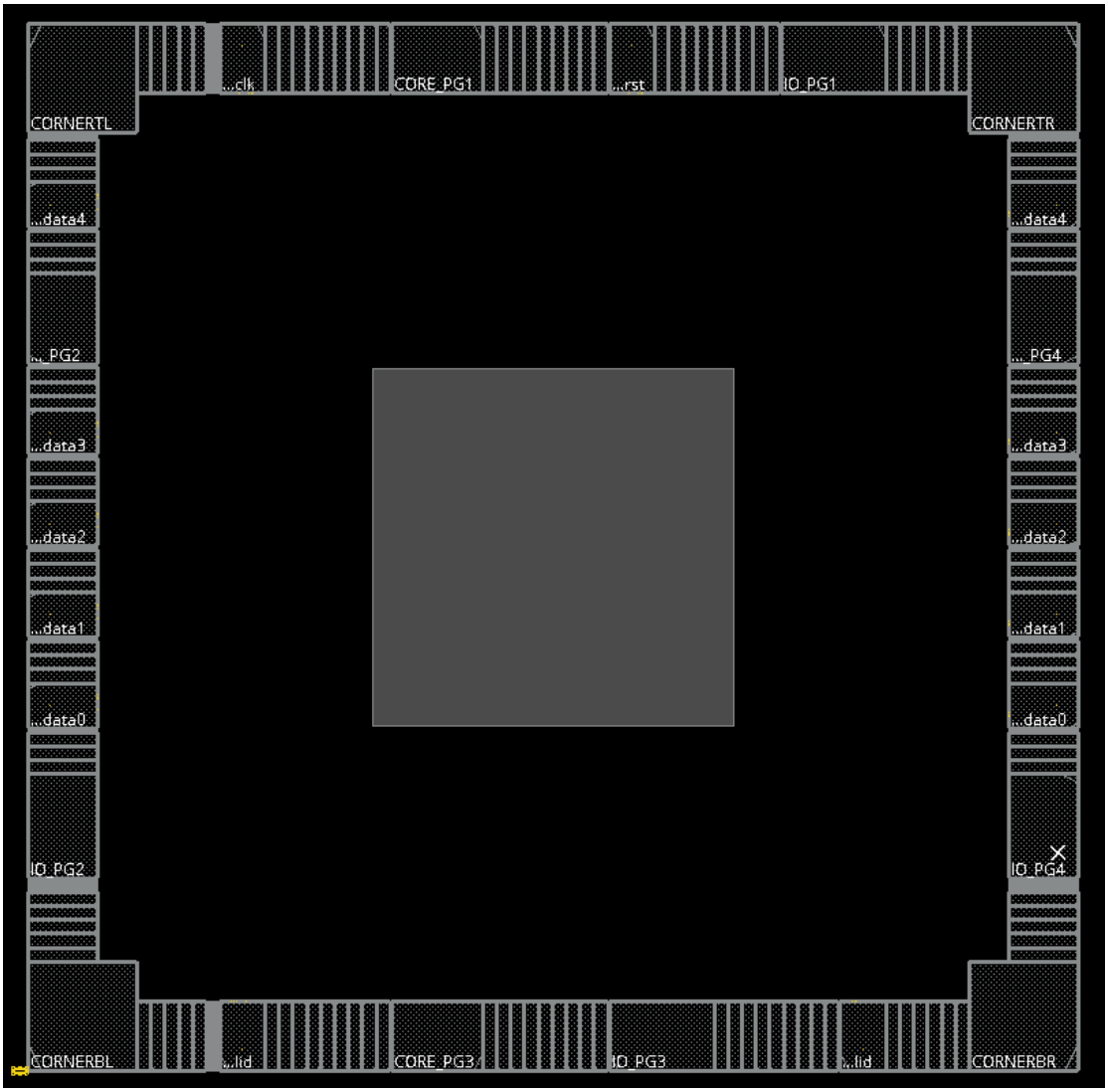


有確認 flip chip 可以擺上去並且繞線可以 RDL 繞線成功，原本我的版本為了求過，所以把晶片面積條大到 6*6 的 bumps 才可以繞

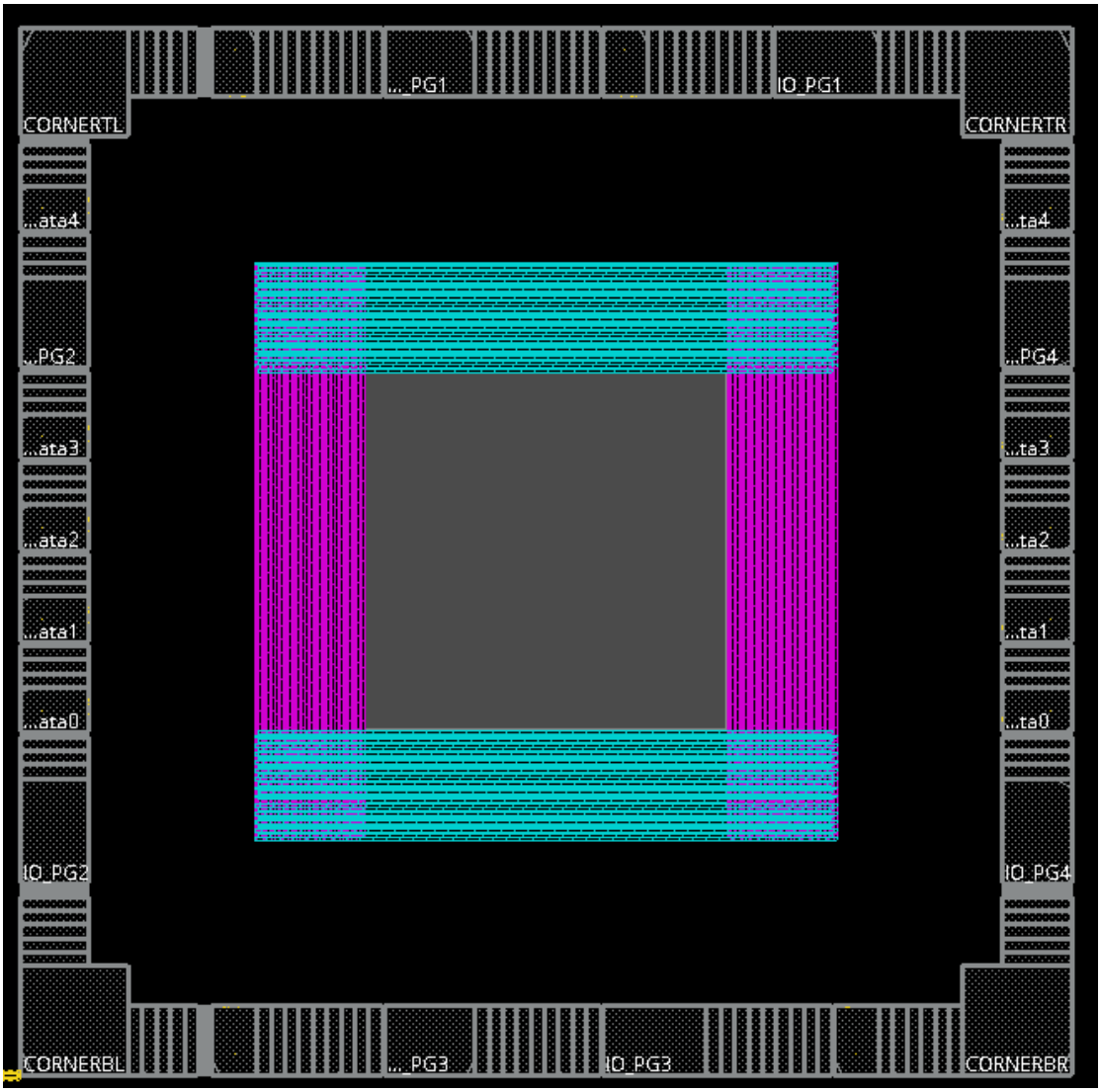
成功，但助教的 script 擺得很好，所以 5*5 的 bumps 就可以成功繞出來，底下為 RDL 繞線成功結果圖



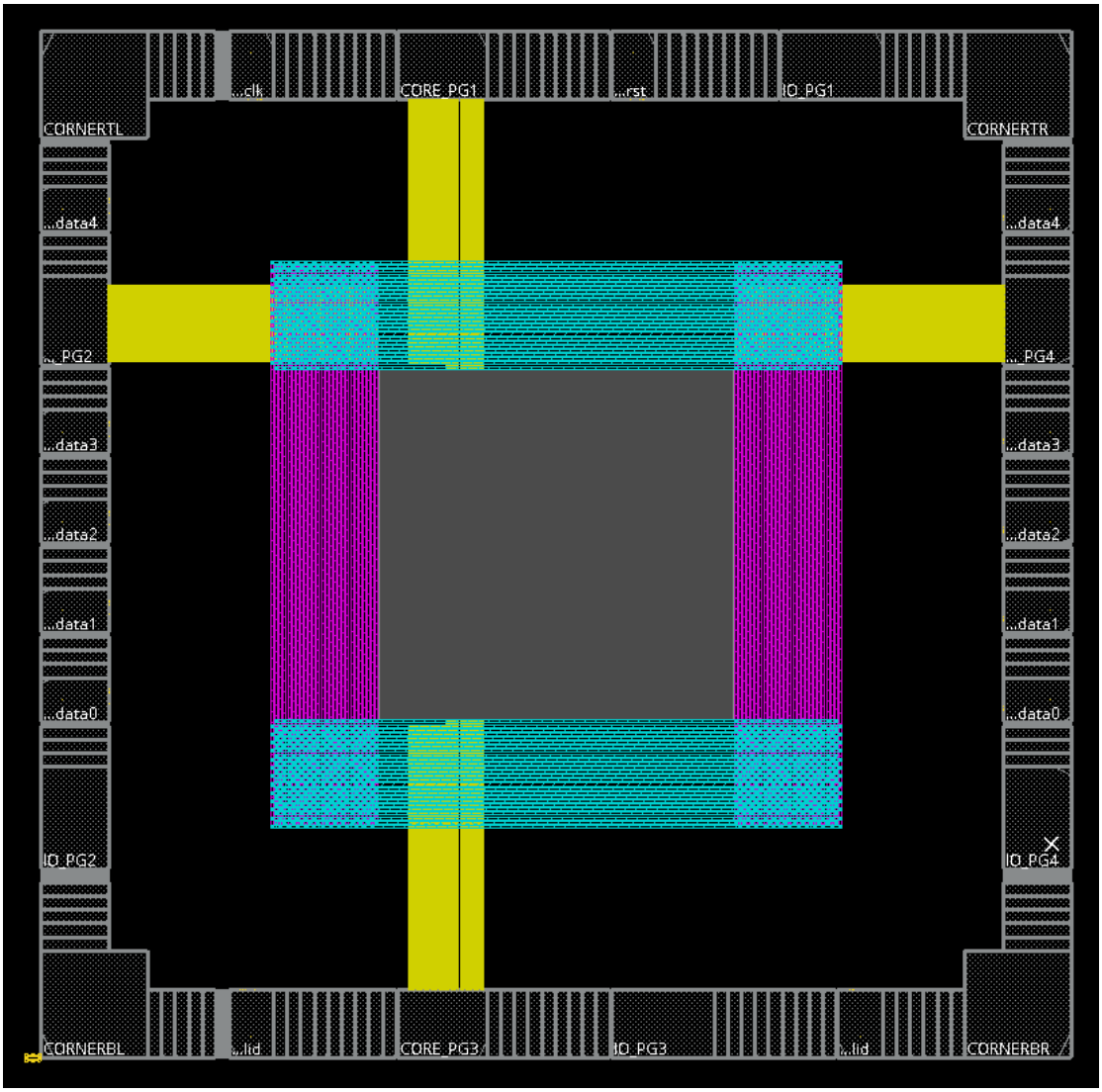
確認可以後再移除，並且最後加上 IO filler，以滿足實體上能夠製造晶片的規則



之後是開始進行 powerplan，先從 power ring 開始，為了降低 IR，所以會打很多層 metal 以降低電阻，讓外部電壓進來不會有太多壓降



之後是 power pad，主要是讓剛剛的 power ring 接上 IO pad 來讓他接到外部電源

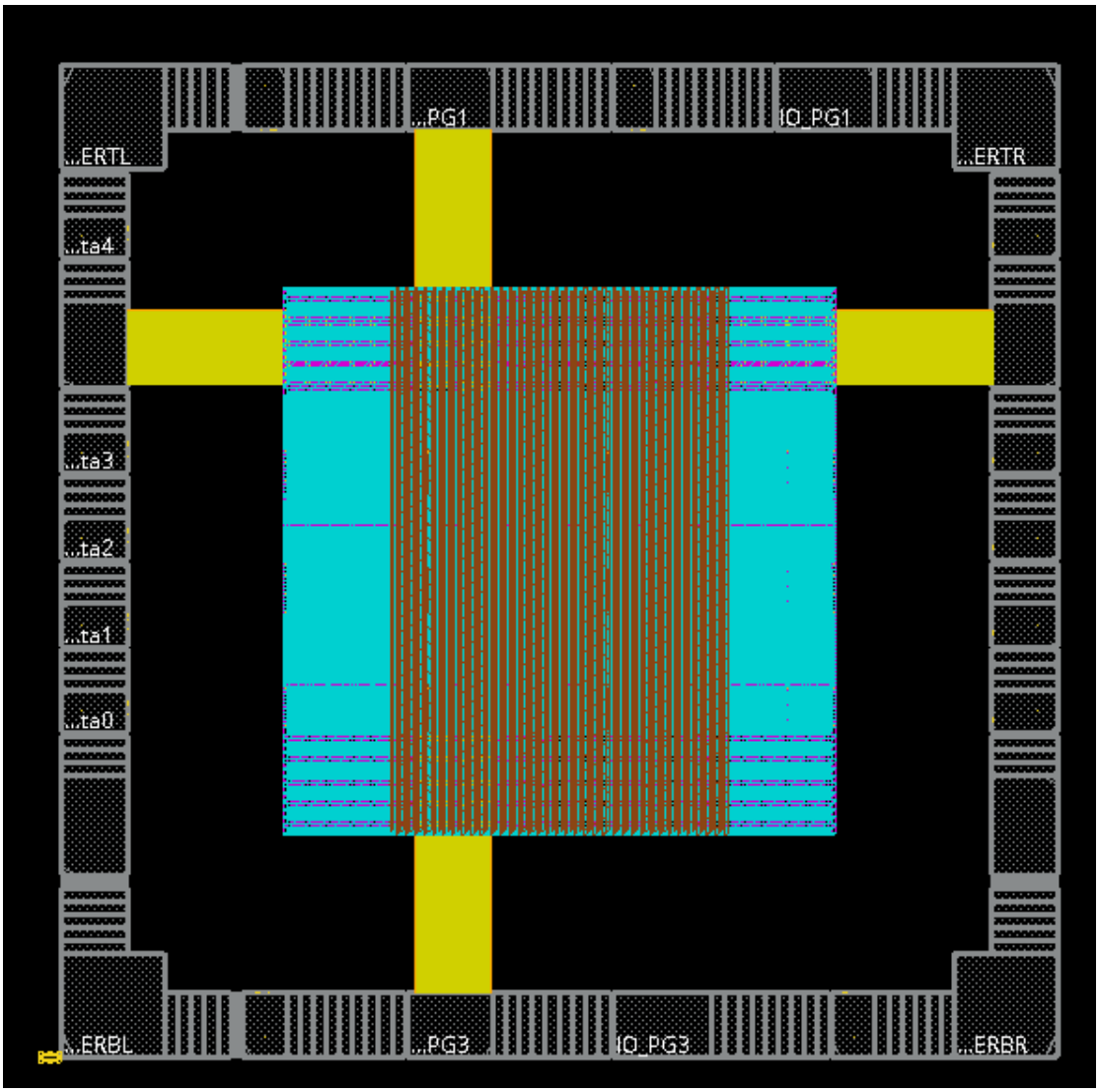


之後要初步確認到目前步驟下 DRC 沒有問題

```
VERIFY DRC ..... Sub-Area: {163.680 735.072 190.960 758.064} 735 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {190.960 735.072 218.240 758.064} 736 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {218.240 735.072 245.520 758.064} 737 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {245.520 735.072 272.800 758.064} 738 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {272.800 735.072 300.080 758.064} 739 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {300.080 735.072 327.360 758.064} 740 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {327.360 735.072 354.640 758.064} 741 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {354.640 735.072 381.920 758.064} 742 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {381.920 735.072 409.200 758.064} 743 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {409.200 735.072 436.480 758.064} 744 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {436.480 735.072 463.760 758.064} 745 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {463.760 735.072 491.040 758.064} 746 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {491.040 735.072 518.320 758.064} 747 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {518.320 735.072 545.600 758.064} 748 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {545.600 735.072 572.880 758.064} 749 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {572.880 735.072 600.160 758.064} 750 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {600.160 735.072 627.440 758.064} 751 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {627.440 735.072 654.720 758.064} 752 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {654.720 735.072 682.000 758.064} 753 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {682.000 735.072 709.280 758.064} 754 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {709.280 735.072 736.560 758.064} 755 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {736.560 735.072 761.580 758.064} 756 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {218.240 197.904 245.520 226.176} 205 of 756  Thread : 7
VERIFY DRC ..... Sub-Area: {218.240 565.440 245.520 593.712} 569 of 756  Thread : 3
VERIFY DRC ..... Sub-Area: {572.880 197.904 600.160 226.176} 218 of 756  Thread : 0
VERIFY DRC ..... Sub-Area: {190.960 593.712 218.240 621.984} 596 of 756  Thread : 0
VERIFY DRC ..... Sub-Area: {218.240 593.712 245.520 621.984} 597 of 756  Thread : 0
VERIFY DRC ..... Sub-Area: {245.520 593.712 272.800 621.984} 598 of 756  Thread : 0
VERIFY DRC ..... Sub-Area: {572.880 565.440 600.160 593.712} 582 of 756  Thread : 2
VERIFY DRC ..... Sub-Area: {572.880 593.712 600.160 621.984} 610 of 756  Thread : 0
VERIFY DRC ..... Sub-Area: {600.160 593.712 627.440 621.984} 611 of 756  Thread : 0
VERIFY DRC ..... Sub-Area: {518.320 197.904 545.600 226.176} 216 of 756  Thread : 4
VERIFY DRC ..... Sub-Area: {190.960 226.176 218.240 254.448} 232 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {518.320 565.440 545.600 593.712} 580 of 756  Thread : 6
VERIFY DRC ..... Sub-Area: {491.040 593.712 518.320 621.984} 607 of 756  Thread : 5
VERIFY DRC ..... Sub-Area: {545.600 593.712 572.880 621.984} 609 of 756  Thread : 4
VERIFY DRC ..... Sub-Area: {518.320 593.712 545.600 621.984} 608 of 756  Thread : 4
VERIFY DRC ..... Sub-Area: {163.680 537.168 190.960 565.440} 539 of 756  Thread : 1
VERIFY DRC ..... Sub-Area: {190.960 169.632 218.240 197.904} 176 of 756  Thread : 7
VERIFY DRC ..... Sub-Area: {572.880 537.168 600.160 565.440} 554 of 756  Thread : 2
VERIFY DRC ..... Sub-Area: {600.160 565.440 627.440 593.712} 583 of 756  Thread : 2
VERIFY DRC ..... Sub-Area: {218.240 537.168 245.520 565.440} 541 of 756  Thread : 3
VERIFY DRC ..... Sub-Area: {245.520 565.440 272.800 593.712} 570 of 756  Thread : 2
VERIFY DRC ..... Sub-Area: {518.320 537.168 545.600 565.440} 552 of 756  Thread : 6
VERIFY DRC ..... Sub-Area: {190.960 537.168 218.240 565.440} 540 of 756  Thread : 3
VERIFY DRC ..... Sub-Area: {545.600 537.168 572.880 565.440} 553 of 756  Thread : 6
VERIFY DRC ..... Thread : 2 finished.
VERIFY DRC ..... Thread : 7 finished.
VERIFY DRC ..... Sub-Area: {190.960 565.440 218.240 593.712} 568 of 756  Thread : 3
VERIFY DRC ..... Thread : 3 finished.
VERIFY DRC ..... Sub-Area: {545.600 565.440 572.880 593.712} 581 of 756  Thread : 6
VERIFY DRC ..... Thread : 6 finished.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:55.1  ELAPSED TIME: 11.00  MEM: 312.6M) ***
```

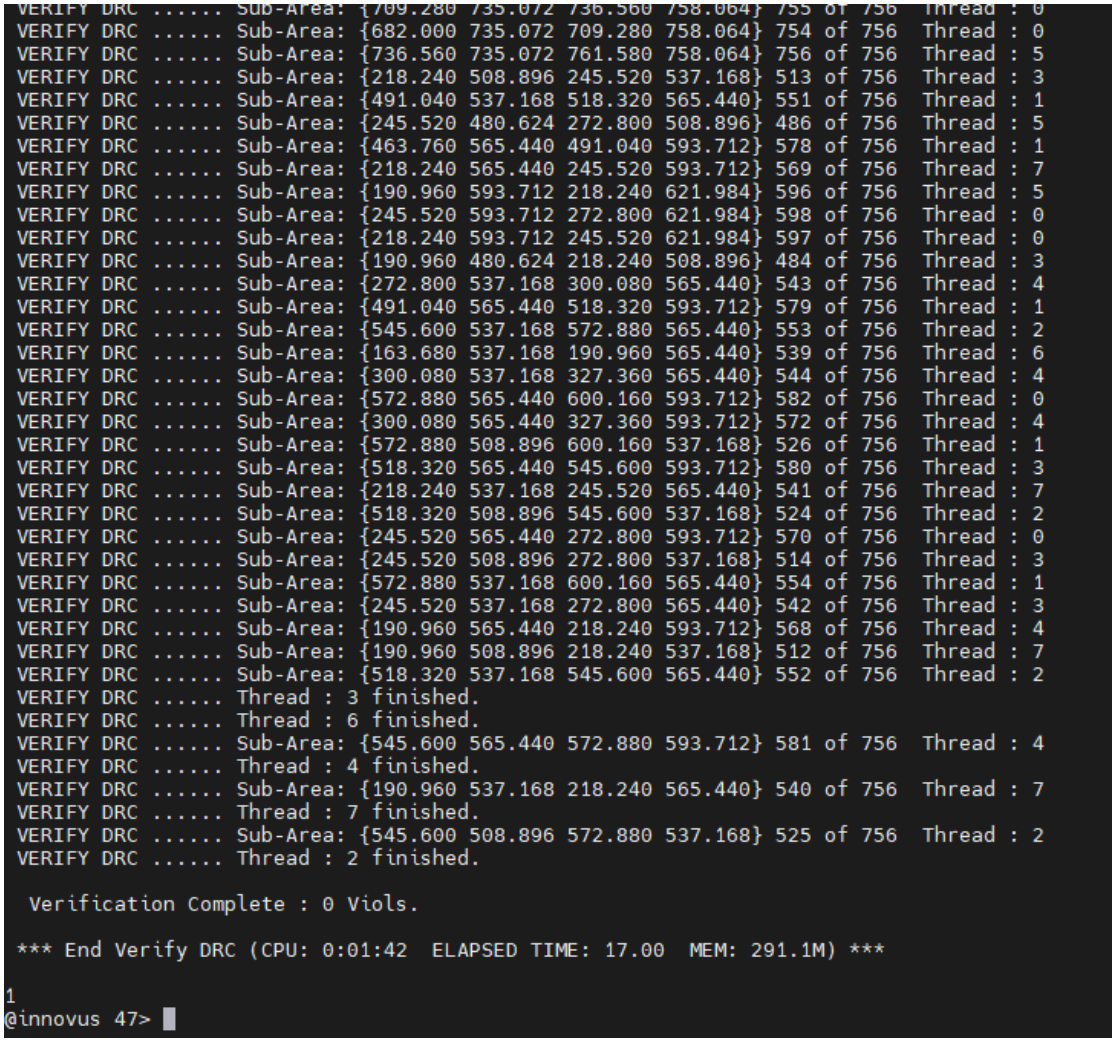
接著是 powerstripe，這部是讓剛剛從外部接到 powerring 的店員

在給晶片內部



這個之後要經過一連串修 DRC 的動作，但都助教給好的 script，

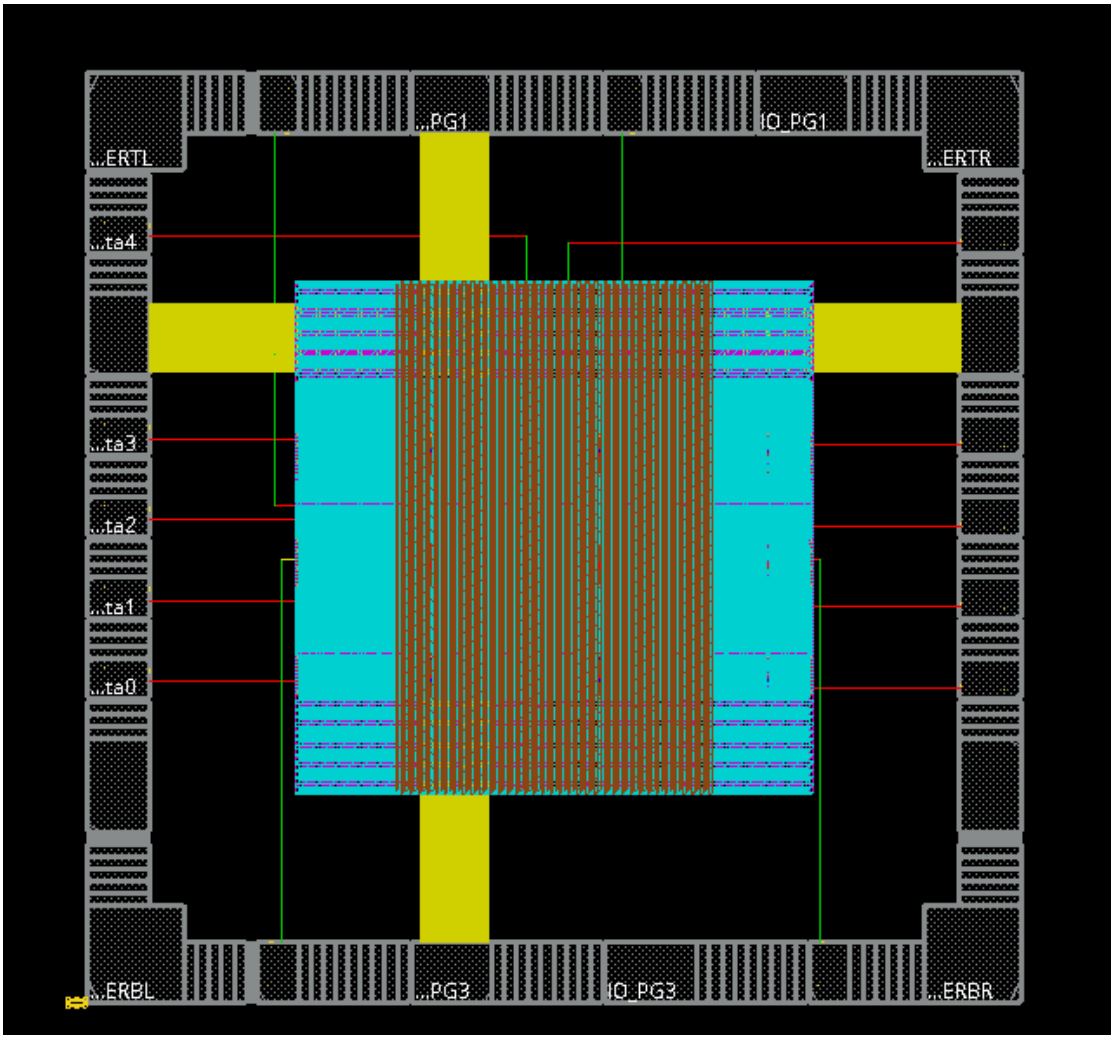
我放結果



Placement

Placement 第一步是加 endcap cell，避免切割動作破壞晶片本身，

之後該使擺 cell，底下維結果



Timing Report Before CTS

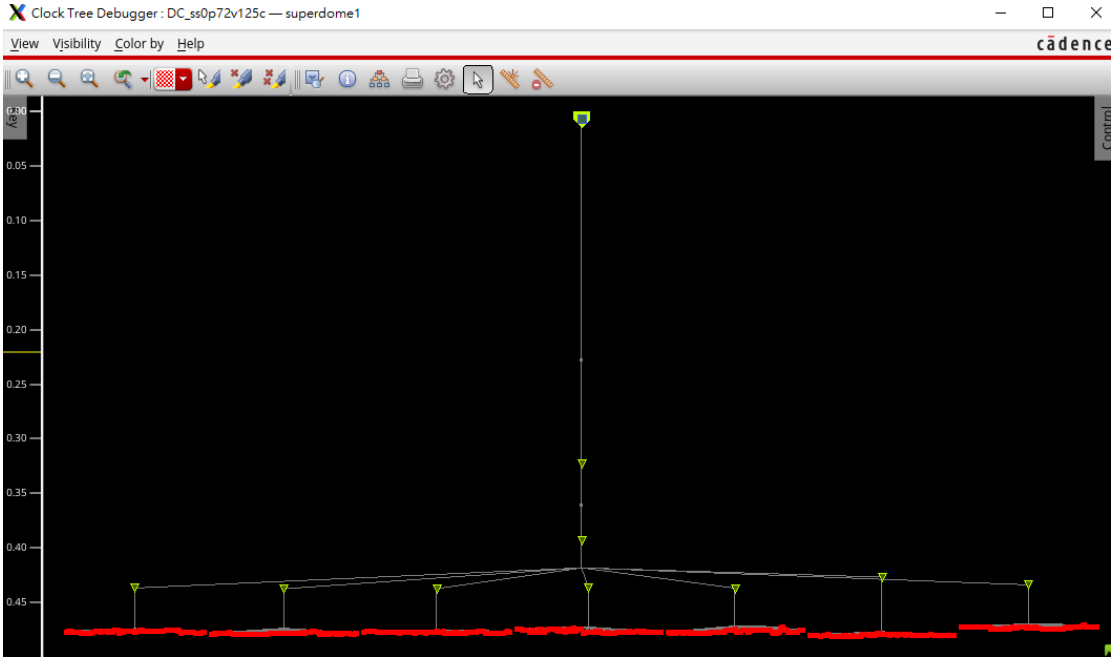
一開始擺時 place 完，timing 沒 meet

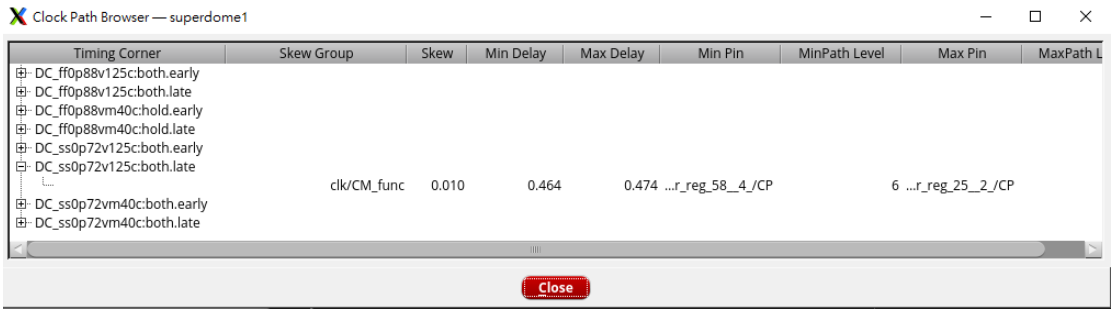
```
#############################################################################
# Design Stage: PreRoute
# Design Name: CHIP
# Design Mode: 16nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#############################################################################
Start delay calculation (fullDC) (8 T). (MEM=4301.62)
Total number of fetched objects 2971
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
Total number of fetched objects 2971
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
Total number of fetched objects 2971
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=4861.2 CPU=0:00:02.5 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=4682.73 CPU=0:00:04.2 REAL=0:00:02.0)
*** Done Building Timing Graph (cpu=0:00:05.1 real=0:00:03.0 totSessionCpu=0:10:57 mem=4690.7M)

------------------------------------------------------------------
         time_design Summary
------------------------------------------------------------------

Setup views included:
 AV_func_ss0p72v125c AV_func_ss0p72vm40c

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| -1.134  |  2.947  | -1.134  |   N/A   |   N/A   |  0.000  |
|           TNS (ns):|-497.157 |  0.000  |-497.157 |   N/A   |   N/A   |  0.000  |
|    Violating Paths:|   617   |    0    |   617   |   N/A   |   N/A   |    0    |
|          All Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |     11 (11)      |   -1.018   |     12 (12)      |
|   max_tran     |    11 (1960)     |   -7.182   |    18 (1967)     |
|   max_fanout   |      0 (0)       |     0      |      1 (1)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 2.138%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 7.46 sec
Total Real time: 5.0 sec
Total Memory Usage: 4401.417969 Mbytes
*** time_design #1 [finish] : cpu/real = 0:00:07.3/0:00:04.7 (1.6), totSession cpu/real = 0:10:57.9/0:20:10.9 (0.5), mem = 4401.4M
@innovus 52>
```

之後下指令 place_opt_design，來修 timing

```
------------------------------------------------------------------
         time_design Summary
------------------------------------------------------------------

Setup views included:
 AV_func_ss0p72v125c

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  2.945  |  3.169  |  2.945  |   N/A   |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |   N/A   |   N/A   |    0    |
|          All Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      7 (7)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 2.158%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 1.48 sec
Total Real time: 2.0 sec
Total Memory Usage: 5370.0 Mbytes
*** time_design #2 [finish] : cpu/real = 0:00:01.5/0:00:01.7 (0.9), totSession cpu/real = 0
@innovus 54>
```

CTS





Timing Report After CTS

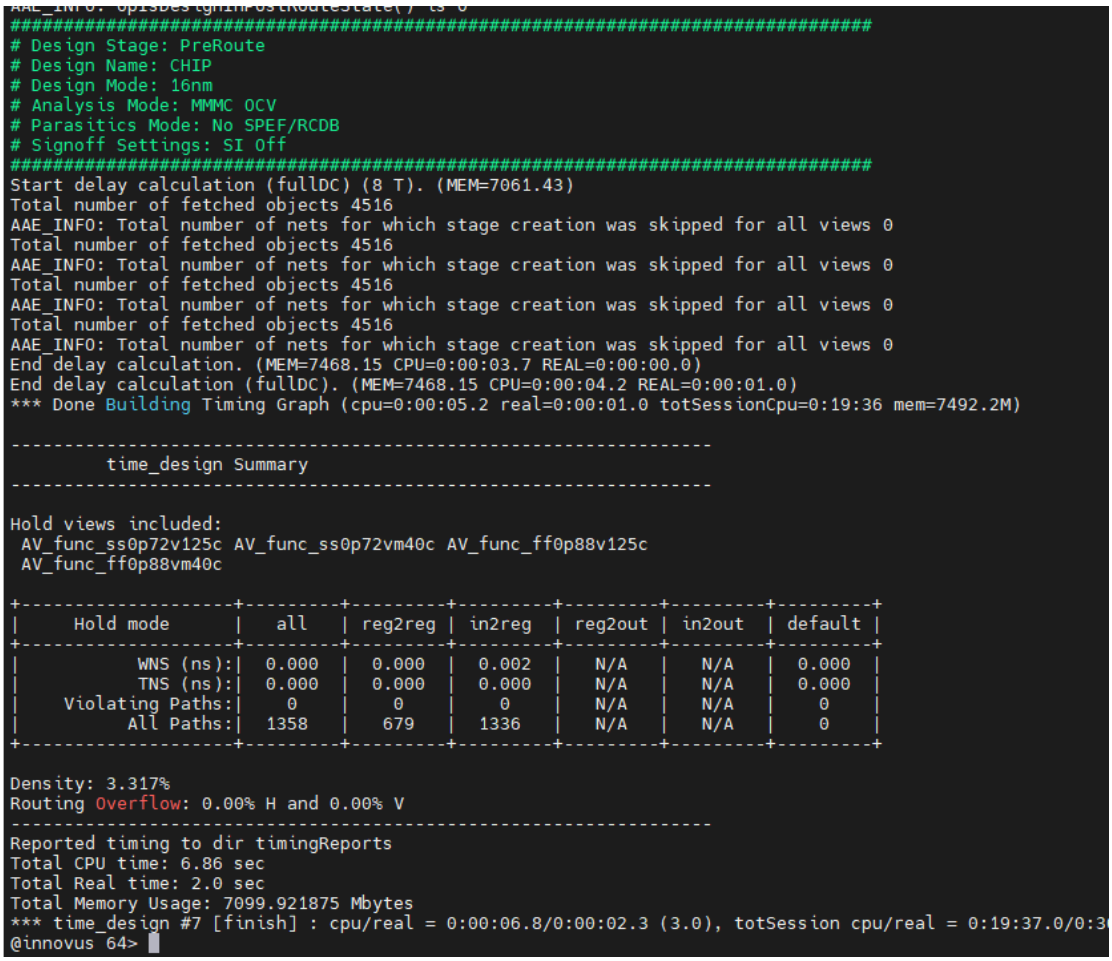
Setup time:

```
------------------------------------------------------------------
         time_design Summary
------------------------------------------------------------------

Setup views included:
 AV_func_ss0p72v125c

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  2.944  |  3.170  |  2.944  |   N/A   |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |   N/A   |   N/A   |    0    |
|          All Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      7 (7)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 2.158%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 3.7 sec
Total Real time: 2.0 sec
Total Memory Usage: 5418.328125 Mbytes
*** time_design #3 [finish] : cpu/real = 0:00:03.7/0:00:02.6 (1.4), totSession cpu/real = 0:
@innovus 57>
```

Hold time:

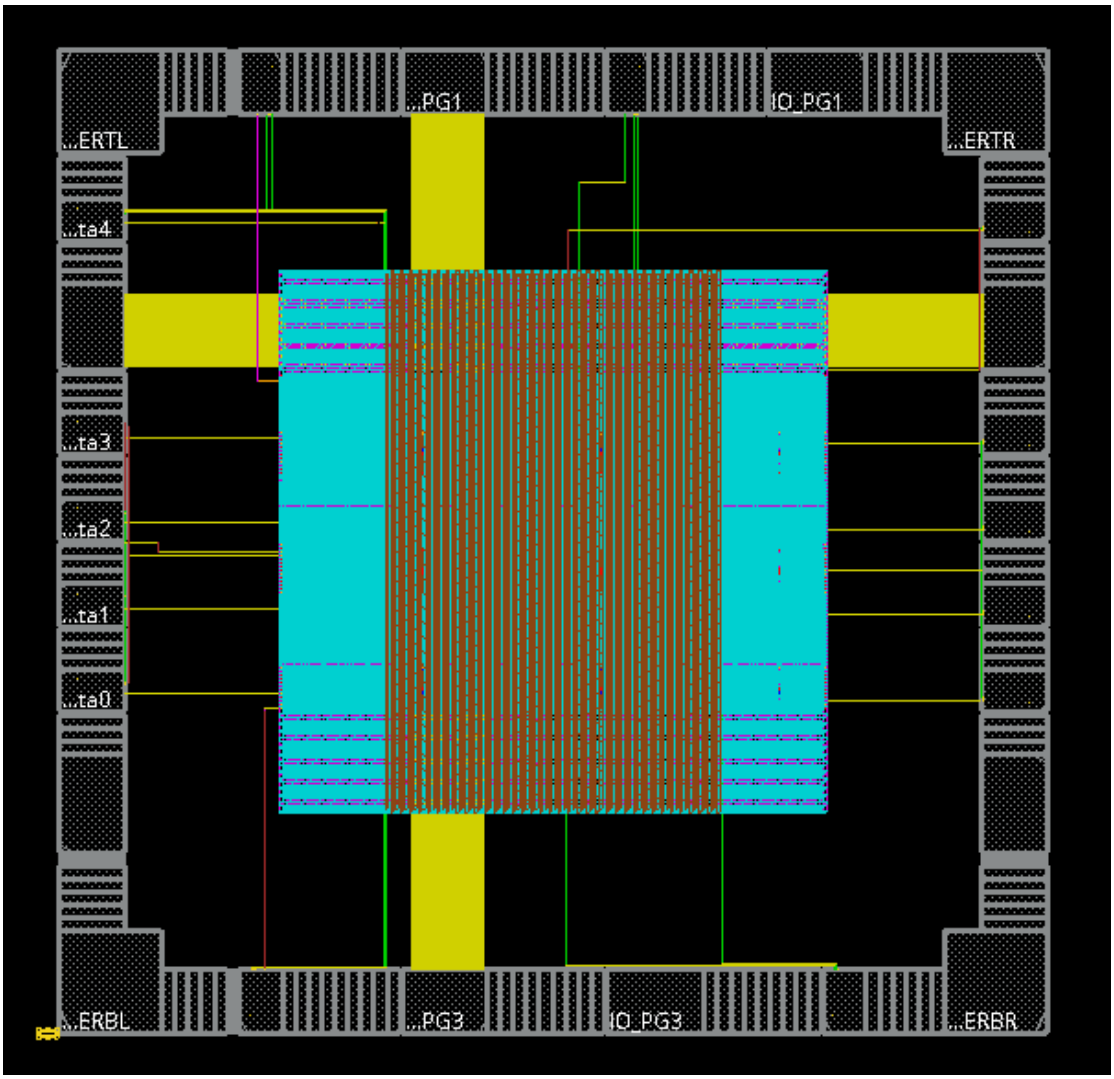
```
------------------------------------------------------------------
         time_design Summary
------------------------------------------------------------------

Hold views included:
 AV_func_ss0p72v125c AV_func_ss0p72vm40c AV_func_ff0p88v125c
 AV_func_ff0p88vm40c

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| -0.308  | -0.074  | -0.308  |   N/A   |   N/A   |  0.000  |
|           TNS (ns):|-215.183 | -44.757 |-213.876 |   N/A   |   N/A   |  0.000  |
|    Violating Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
|          All Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 2.151%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 5.6 sec
Total Real time: 2.0 sec
Total Memory Usage: 6585.085938 Mbytes
*** time_design #6 [finish] : cpu/real = 0:00:05.6/0:00:02.0 (2.8), totSession cpu/real =
@innovus 62>
```

一開始沒過後來下指令 opt_design -post_cts -hold

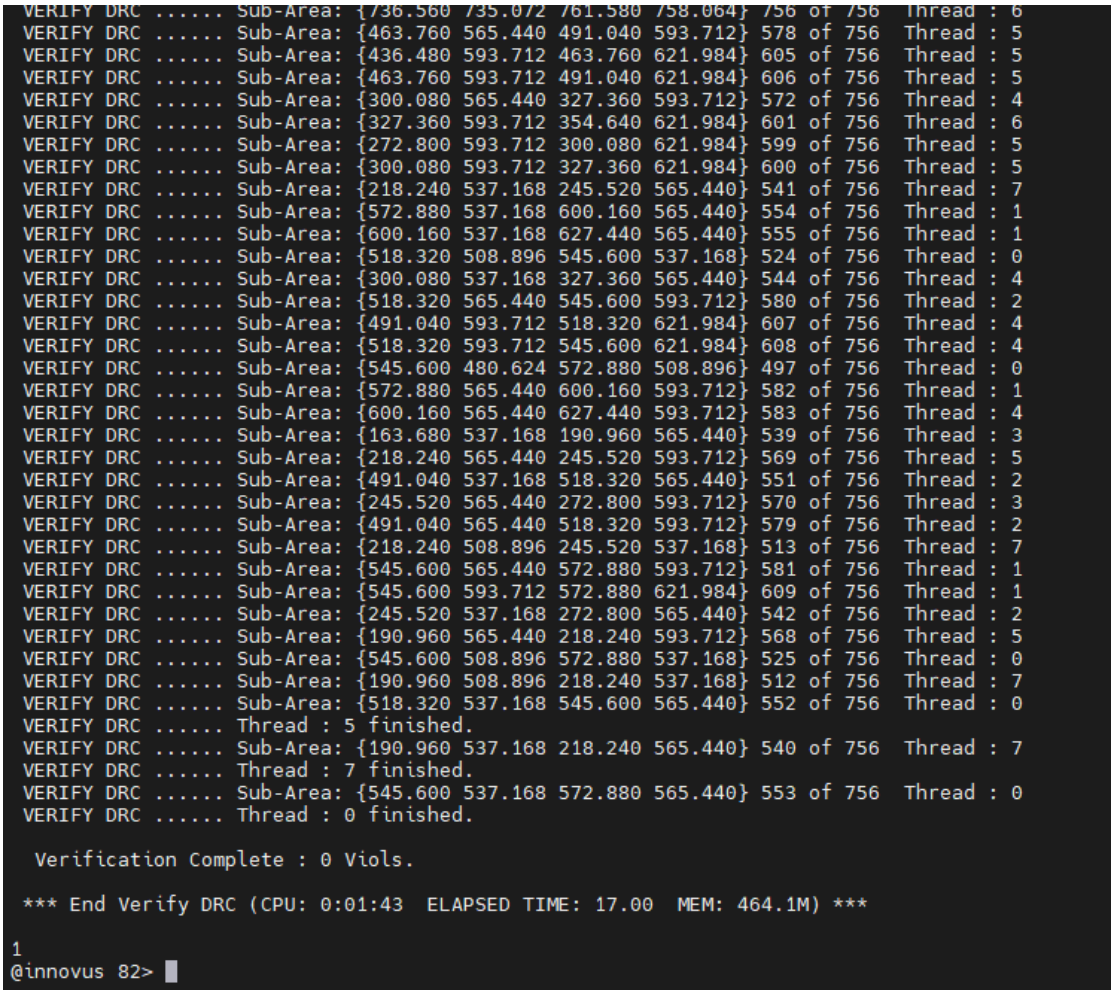


Routing

下指令 route design，來繞線，並且要確認 timing，底下為結果



之後就是下一堆指令修 DRC，結果有成功修好



Timing Report After Routing

Set up time:

```
Setup views included:
 AV_func_ss0p72v125c

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  1.970  |  2.715  |  1.970  |   N/A   |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |   N/A   |   N/A   |    0    |
|          All Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      7 (7)       |   -0.025   |      7 (7)       |
|   max_tran     |      0 (0)       |   0.000    |      7 (7)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 3.321%
---------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 30.53 sec
Total Real time: 15.0 sec
Total Memory Usage: 8483.5 Mbytes
Reset AAE Options
*** time_design #8 [finish] : cpu/real = 0:00:30.5/0:00:15.5 (2.0), totSession cpu/real
@innovus 70>
```

一開始沒過後來下指令，opt_design -post_route -setup -hold，就把 set up/hold time 都修好

```
---------------------------------------------------------------------
         time_design Summary
---------------------------------------------------------------------

Setup views included:
 AV_func_ss0p72v125c

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  2.419  |  2.704  |  2.419  |   N/A   |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |   N/A   |   N/A   |    0    |
|          All Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      7 (7)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 3.336%
---------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 1.97 sec
Total Real time: 2.0 sec
Total Memory Usage: 9428.070312 Mbytes
Reset AAE Options
*** time_design #10 [finish] : cpu/real = 0:00:02.0/0:00:01.9 (1.0), totSession cpu/real = 0:30:
@innovus 73>
@innovus 73>
```

Hold time:

```
------------------------------------------------------------------
        time_design Summary
------------------------------------------------------------------

Hold views included:
 AV_func_ss0p72v125c AV_func_ss0p72vm40c AV_func_ff0p88v125c
 AV_func_ff0p88vm40c

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| -0.003  | -0.003  |  0.376  |   N/A   |   N/A   |  0.000  |
|           TNS (ns):| -0.010  | -0.010  |  0.000  |   N/A   |   N/A   |  0.000  |
|    Violating Paths:|    8    |    8    |    0    |   N/A   |   N/A   |    0    |
|         All Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 3.321%
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 11.49 sec
Total Real time: 4.0 sec
Total Memory Usage: 8524.679688 Mbytes
Reset AAE Options
*** time_design #9 [finish] : cpu/real = 0:00:11.5/0:00:03.7 (3.1), totSession cpu/real = 0:27:40.1/0:45:15.9 (0.6), mem = 8524.7M
@innovus 71>
```

一開始沒過後來下指令，opt_design -post_route -setup -hold，就把

set up/hold time 都修好

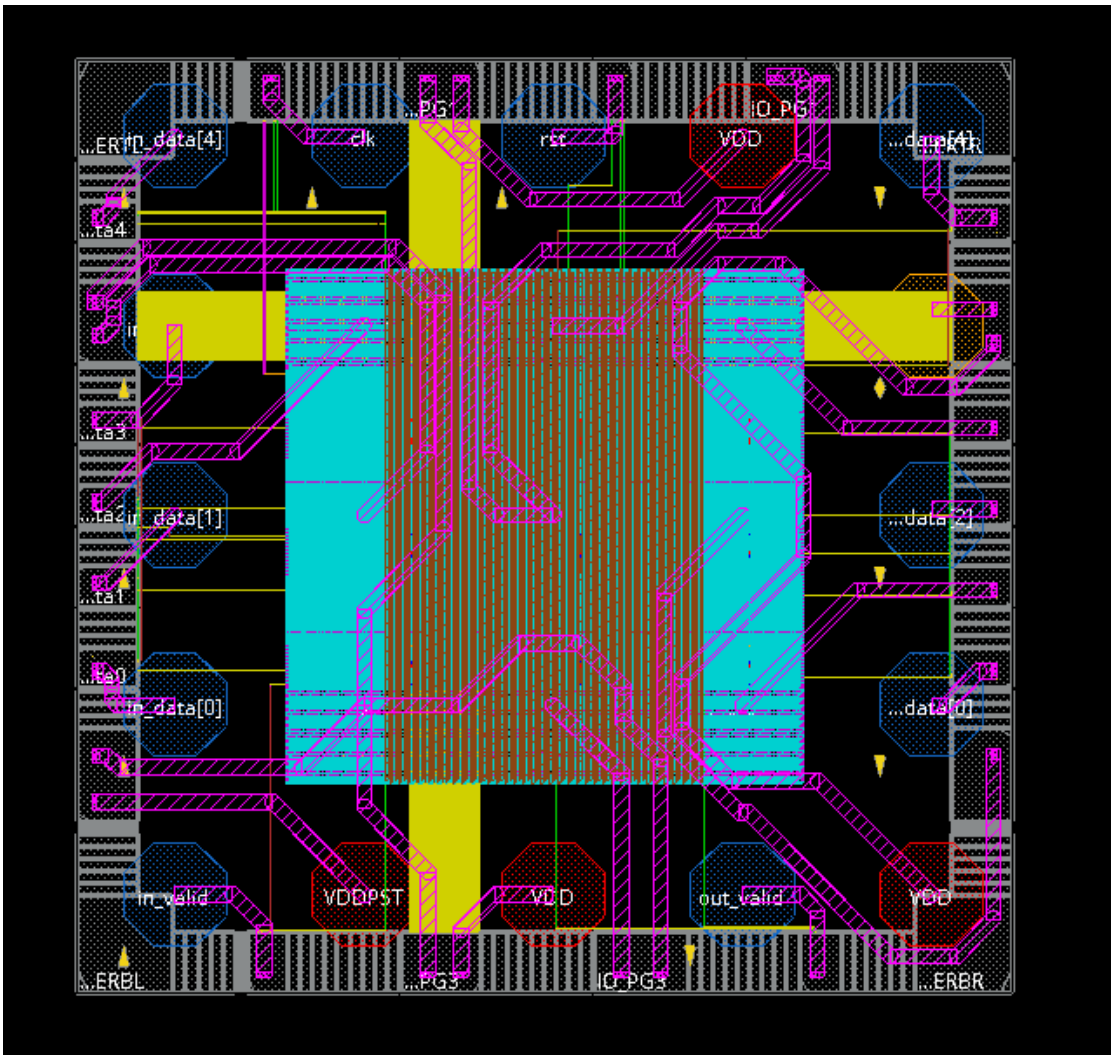
```
------------------------------------------------------------------
         time_design Summary
------------------------------------------------------------------

Hold views included:
 AV_func_ss0p72v125c AV_func_ss0p72vm40c AV_func_ff0p88v125c
 AV_func_ff0p88vm40c

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| -0.000  | -0.000  |  0.003  |   N/A   |   N/A   | -0.000  |
|           TNS (ns):| -0.000  |  0.000  |  0.000  |   N/A   |   N/A   |  0.000  |
|    Violating Paths:|    1    |    1    |    0    |   N/A   |   N/A   |    0    |
|         All Paths:|  1358   |   679   |  1336   |   N/A   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 3.336%
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 10.83 sec
Total Real time: 4.0 sec
Total Memory Usage: 10439.5 Mbytes
Reset AAE Options
*** time_design #13 [finish] : cpu/real = 0:00:10.8/0:00:03.8 (2.9), totSession cpu/real = 0
@innovus 77>
```

Create Bump

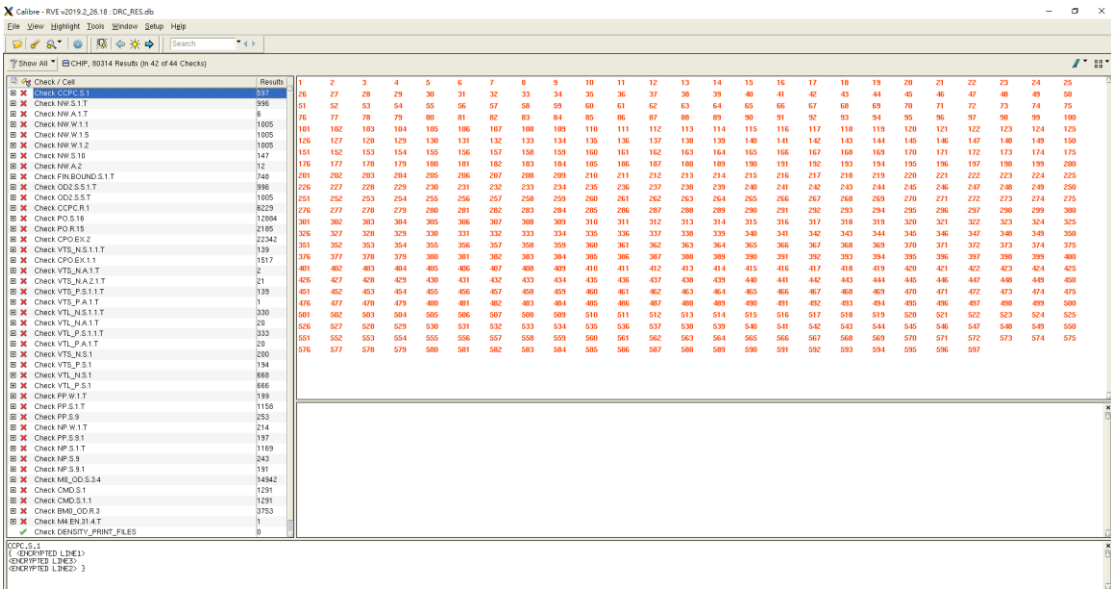
之後就照前面 floorplan 試擺過的 bump 擺法再擺回去

RDL Routing

之後就照前面 floorplan 試繞過的 RDL 繞法讓 tool 再繞一次

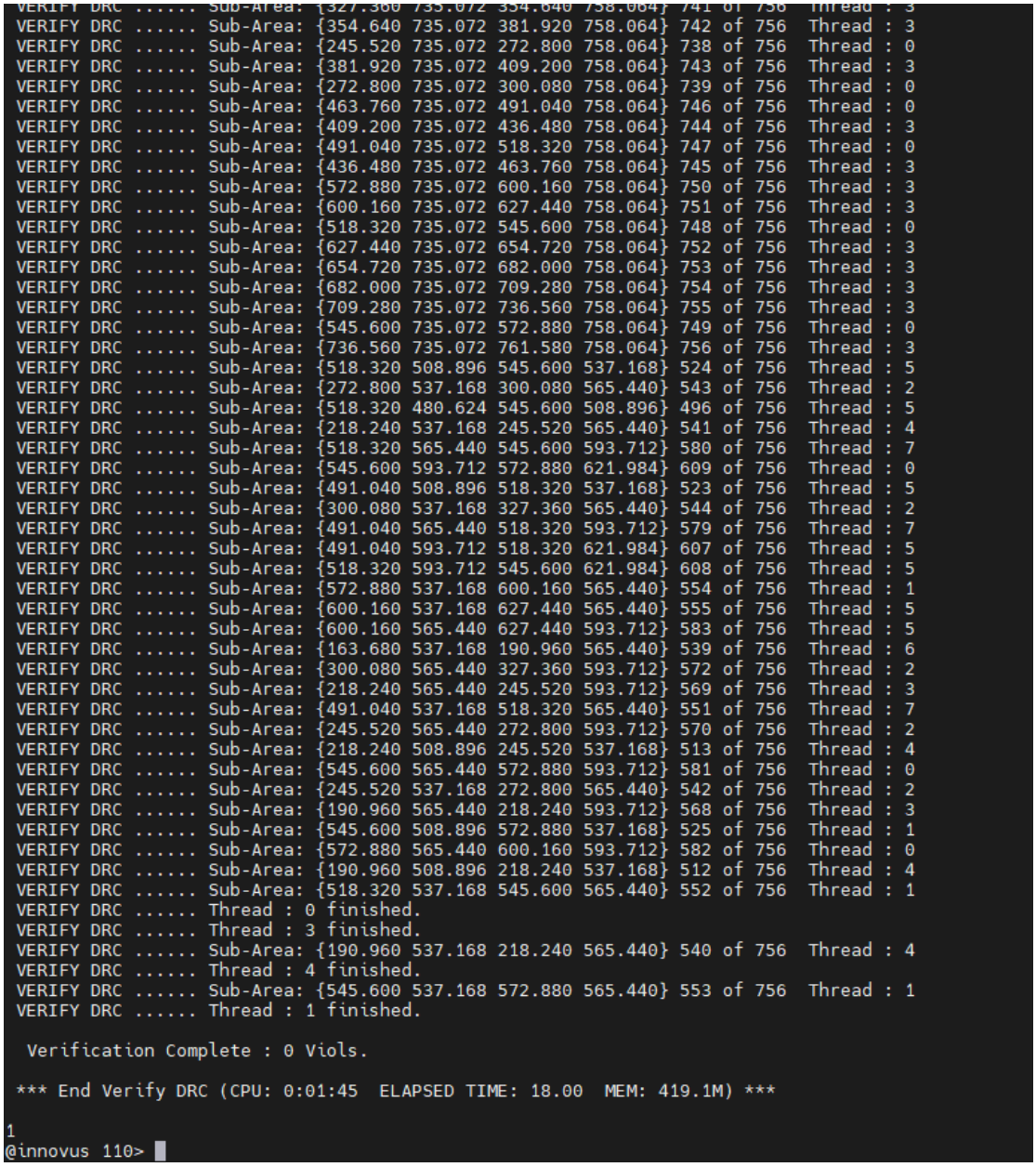


DRC Check



錯一狗票不知為啥，但剛剛繞完再 innovous 明明是 0 個，但開

calibre 出現一狗票，底下是 innovous 上的



LVS Check

LVS 出現了經典笑臉

```
                ##############################################
                ##                                          ##
                ##        C A L I B R E   S Y S T E M       ##
                ##                                          ##
                ##           L V S   R E P O R T            ##
                ##                                          ##
                ##############################################


REPORT FILE NAME:         output/lvs.rep
LAYOUT NAME:              layout.spi ('CHIP')
SOURCE NAME:              CHIP_inc.spi ('CHIP')
RULE FILE:                ./scr/runset.cmd
CREATION TIME:            Mon Jun 16 19:14:22 2025
CURRENT DIRECTORY:        /home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/hw13_Example/pr/verify/lvs
USER NAME:                hdlcs2590
CALIBRE VERSION:          v2019.2_26.18    Tue May 7 10:57:04 PDT 2019


                            OVERALL COMPARISON RESULTS


                       #       ##################       _   _
                      #        #                #       *   *
                  #   #        #     CORRECT    #         |
                   # #         #                #       \___/
                    #          ##################


  Warning:  Ambiguity points were found and resolved arbitrarily.

********************************************************************************************************************
                                      CELL  SUMMARY
********************************************************************************************************************

  Result         Layout                      Source
  -----------    -----------                 --------------
  CORRECT        CHIP                        CHIP


********************************************************************************************************************
                                      LVS PARAMETERS
********************************************************************************************************************

o LVS Setup:

    // LVS COMPONENT TYPE PROPERTY
    // LVS COMPONENT SUBTYPE PROPERTY
    // LVS PIN NAME PROPERTY
    LVS POWER NAME                          "VDD" "VDDPST" "AVDD" "DVDD"
    LVS GROUND NAME                         "VSS"
    LVS CELL SUPPLY                         NO
    LVS RECOGNIZE GATES                     NONE
    LVS IGNORE PORTS                        NO
    LVS CHECK PORT NAMES                    YES
    LVS IGNORE TRIVIAL NAMED PORTS          NO
    LVS BUILTIN DEVICE PIN SWAP             YES
    LVS ALL CAPACITOR PINS SWAPPABLE        YES
    LVS DISCARD PINS BY DEVICE              NO
```

7. 心得分享