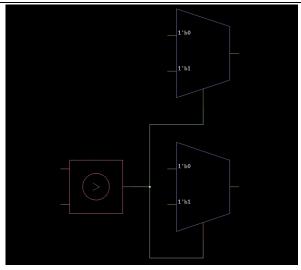
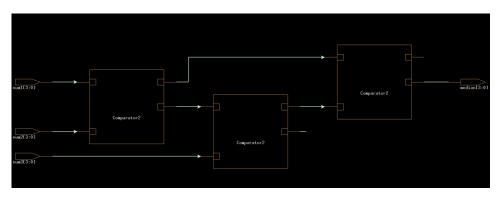
2025 Digital IC Design Homework 1

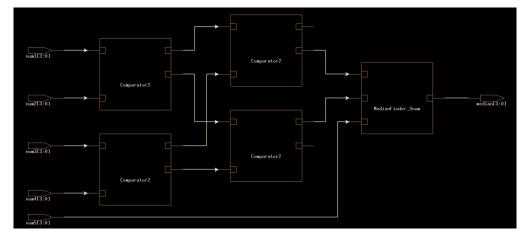
NAME		童品	綸							
Student ID	dent ID M16131111									
Functional Simulation Result										
Stage 1	P	ass	Stage 2	Pass	Stage 3	Pass	Stage 4	Pass		
Stage 1										
# Stagel: Comparator2 Pass !										
				Stag	ge 2					
# Stage2: MedianFinder_3num Pass !										
Stage 3										
# Stage3: MedianFinder_5num Pass !										
Stage 4										
# #			Sta	ge4: Median	Finder_7num	n Pass !				
Description of your design										
Stage1 之電路是照助教所給之電路圖時做出找輸入大小的電路,但我的控制										
訊號只用了一個比較器其實就可以完成,如下圖 schematic。										



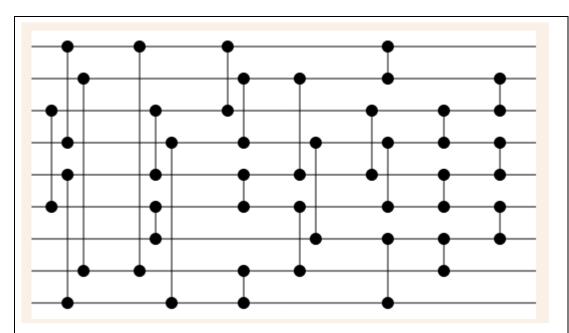
Stage2,则是完全照助教所給電路去 implement RTL code,底下我的 RTL code 之電路 schematic



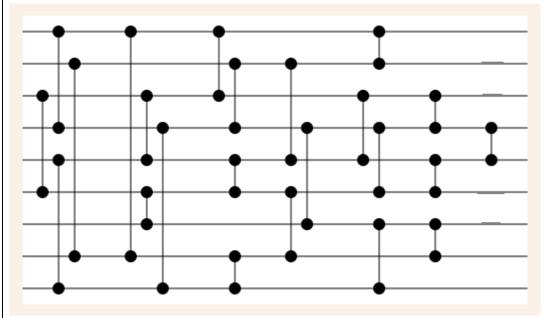
Stage3,也是完全照助教所給電路去 implement RTL code,底下我的 RTL code 之電路 schematic



Stage4,是照底下的7-input sort network 來進行改良,由於只要取中間值,所以最後一級的三個比較器實際上只需要一個就可以完成



改良後之 schematic 如下圖



而底下為我的 RTL code 之實際 schematic

