





2025 Digital IC Design Homework 3

NAME	童品綸			
Student ID	M16131111			
Simulation Result				
Functional simulation	Pass	Pre-Layout simulation	Pass	
P1		Please specify your clock width:16(ns)		
<div><div>Transcript</div><div><div>## FFT imag part on pattern 928 ~ 943, PASS!!</div><div>## FFT real part on pattern 944 ~ 959, PASS!!</div><div>## FFT imag part on pattern 944 ~ 959, PASS!!</div><div>## FFT real part on pattern 960 ~ 975, PASS!!</div><div>## FFT imag part on pattern 960 ~ 975, PASS!!</div><div>## FFT real part on pattern 976 ~ 991, PASS!!</div><div>## FFT imag part on pattern 976 ~ 991, PASS!!</div><div>## FFT real part on pattern 992 ~ 1007, PASS!!</div><div>## FFT imag part on pattern 992 ~ 1023, PASS!!</div><div>## FFT real part on pattern 1008 ~ 1023, PASS!!</div><div>## FFT imag part on pattern 1008 ~ 1023, PASS!!</div></div><div><div></div><div>Congratulations! All data have been generated successfully! Total use 1049 cycles to complete simulation.</div><div><div>** Note: \$finish : D:/Downloads/DIC_HW3/M16131111/file/testfixture.sv(213)</div><div>Time: 16000 ns Iteration: 0 Instance: /testfixture</div><div># 1</div><div>Break in Module testfixture at D:/Downloads/DIC_HW3/M16131111/file/testfixture.sv line 213</div></div></div></div> <div><div>Transcript</div><div><div>## FFT imag part on pattern 928 ~ 943, PASS!!</div><div>## FFT real part on pattern 944 ~ 959, PASS!!</div><div>## FFT imag part on pattern 944 ~ 959, PASS!!</div><div>## FFT real part on pattern 960 ~ 975, PASS!!</div><div>## FFT imag part on pattern 960 ~ 975, PASS!!</div><div>## FFT real part on pattern 976 ~ 991, PASS!!</div><div>## FFT imag part on pattern 976 ~ 991, PASS!!</div><div>## FFT real part on pattern 992 ~ 1007, PASS!!</div><div>## FFT imag part on pattern 992 ~ 1023, PASS!!</div><div>## FFT real part on pattern 1008 ~ 1023, PASS!!</div><div>## FFT imag part on pattern 1008 ~ 1023, PASS!!</div></div><div><div></div><div>Congratulations! All data have been generated successfully! Total use 1049 cycles to complete simulation.</div><div><div>** Note: \$finish : D:/Downloads/DIC_HW3/M16131111/file/testfixture.sv(213)</div><div>Time: 16000 ns Iteration: 0 Instance: /testfixture</div><div># 1</div><div>Break in Module testfixture at D:/Downloads/DIC_HW3/M16131111/file/testfixture.sv line 213</div></div></div></div>		P1		<div><div>Transcript</div><div><div>## FFT imag part on pattern 928 ~ 943, PASS!!</div><div>## FFT real part on pattern 944 ~ 959, PASS!!</div><div>## FFT imag part on pattern 944 ~ 959, PASS!!</div><div>## FFT real part on pattern 960 ~ 975, PASS!!</div><div>## FFT imag part on pattern 960 ~ 975, PASS!!</div><div>## FFT real part on pattern 976 ~ 991, PASS!!</div><div>## FFT imag part on pattern 976 ~ 991, PASS!!</div><div>## FFT real part on pattern 992 ~ 1007, PASS!!</div><div>## FFT imag part on pattern 992 ~ 1023, PASS!!</div><div>## FFT real part on pattern 1008 ~ 1023, PASS!!</div><div>## FFT imag part on pattern 1008 ~ 1023, PASS!!</div></div><div><div></div><div>Congratulations! All data have been generated successfully! Total use 1050 cycles to complete simulation.</div><div><div>** Note: \$finish : D:/Downloads/DIC_HW3/M16131111/file/testfixture.sv(213)</div><div>Time: 16009546 ps Iteration: 0 Instance: /testfixture</div><div># 1</div><div>Break in Module testfixture at D:/Downloads/DIC_HW3/M16131111/file/testfixture.sv line 213</div></div></div></div> <div><div>Transcript</div><div><div>## FFT imag part on pattern 928 ~ 943, PASS!!</div><div>## FFT real part on pattern 944 ~ 959, PASS!!</div><div>## FFT imag part on pattern 944 ~ 959, PASS!!</div><div>## FFT real part on pattern 960 ~ 975, PASS!!</div><div>## FFT imag part on pattern 960 ~ 975, PASS!!</div><div>## FFT real part on pattern 976 ~ 991, PASS!!</div><div>## FFT imag part on pattern 976 ~ 991, PASS!!</div><div>## FFT real part on pattern 992 ~ 1007, PASS!!</div><div>## FFT imag part on pattern 992 ~ 1023, PASS!!</div><div>## FFT real part on pattern 1008 ~ 1023, PASS!!</div><div>## FFT imag part on pattern 1008 ~ 1023, PASS!!</div></div><div><div></div><div>Congratulations! All data have been generated successfully! Total use 1050 cycles to complete simulation.</div><div><div>** Note: \$finish : D:/Downloads/DIC_HW3/M16131111/file/testfixture.sv(213)</div><div>Time: 16009546 ps Iteration: 0 Instance: /testfixture</div><div># 1</div><div>Break in Module testfixture at D:/Downloads/DIC_HW3/M16131111/file/testfixture.sv line 213</div></div></div></div>
Synthesis Result				
Total logic elements	1729			
Total memory bits	160			
Total registers	966			
Embedded multiplier 9-bit elements	8			

Compilation Report - FFT

Assignment Editor

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Flow Summary

<<Filter>>

Flow Status	Successful - Fri May 09 02:53:14 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	FFT
Top-level Entity Name	FFT
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	1,729 / 55,856 (3 %)
Total registers	966
Total pins	277 / 325 (85 %)
Total virtual pins	0
Total memory bits	160 / 2,396,160 (< 1 %)
Embedded Multiplier 9-bit elements	8 / 308 (3 %)
Total PLLs	0 / 4 (0 %)

Description of your design

我的設計主要就是拆 4 個 stage，一個 stage，一個蝴蝶單元來做，然後只有第二個 stage 會用到乘法器，我有自己對 twiddle factor 做化簡，把很多旋轉因子能變成乘負一或正一，然後因為要前一組到，才有辦法用蝴蝶算出下一級輸入，所以上面有移位暫存器，最後出來會做順序重排，以及累積每 16 筆輸出二次(實部跟虛部)，底下有架構圖

