

2025 Digital IC Design Homework 4

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ATCONV Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass
tb1:		tb1:	
			
tb2:		tb2:	
			
tb3:		tb3:	
			
System Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass

tb1:

```
Library Project Memory List sim
Transcript
# 0020 0040 0060 0080 0020 0010 0000 0000 0000 0050 00a0 0030 0030 0090 0170 0000 01a0 02a0 03b0 05a0
# 0090 00a0 00b0 00c0 00d0 00e0 00f0 0040 0090 0090 0000 0000 0000 00b0 0180 01b0 0000 02f0 03a0 00b0 05a0
# 0020 0000 0000 0090 00b0 0090 0070 00c0 0100 00e0 0110 0200 02f0 0210 0160 00a0 0530 0430 0500 04e0
# 0030 0070 0050 0070 00a0 0000 0000 0000 00e0 0090 0120 01f0 0010 0170 0560 0040 03a0 04e0 0580 0000
# 0000 0000 0000 0000 0050 0040 0040 0020 00a0 00b0 0040 0130 0000 0720 0000 02f0 02a0 0570 0000
#
#
# ----- S U M M A R Y -----
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at 41990 cycle
#
# ** Note: $finish : C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture.av(228)
# Time: 2099500 ns Iteration: 0 Instance: /testfixture
# 1
# Break in Module testfixture at C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture
V$M 11>
```

tb2:

```
Library Project Memory List sim
Transcript
# 0020 0000 0010 0000 0000 0000 0010 0040 0290 0000 0350 0040 0040 0020 04f0 00b0 0210 0470 0020 0050
# 0020 0010 0000 0000 0000 0000 0020 0150 0290 01a0 0020 0000 0010 04c0 0030 00b0 0470 0010 0020
# 0020 0000 0000 0000 0000 0000 0010 01a0 0190 0010 0000 0010 0470 0000 0050 0430 0010 0010
# 0020 0000 0000 0010 0010 0000 0010 0200 00a0 01a0 0090 0010 0000 0010 0420 0000 0000 0410 0010 0020
# 0010 0000 0000 0000 0010 0000 00a0 0250 0000 01c0 0030 0030 0020 0030 01f0 02c0 02f0 01b0 0010 0020
#
#
# ----- S U M M A R Y -----
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at 41990 cycle
#
# ** Note: $finish : C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture.av(228)
# Time: 2099500 ns Iteration: 0 Instance: /testfixture
# 1
# Break in Module testfixture at C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture
V$M 13>
```

tb3:

```
Library Project Memory List sim
Transcript
# 0100 0210 0210 01f0 0250 0230 0210 0290 02c0 0070 01f0 00a0 0110 0150 0190 0130 0170 0210 0170 01a0
# 00a0 0100 01a0 01a0 01c0 01c0 01e0 01a0 02a0 0290 0230 0290 0250 02a0 02a0 02a0 02a0 0220 0230 0210
# 0040 0040 0020 00a0 0010 0040 0020 0010 0050 0020 0000 0070 0030 0010 0030 0040 0000 0020 0020 0000
# 0000 0000 0000 0010 0020 0020 0000 0030 0030 0040 0040 0010 0020 0000 0040 0020 0010 0040 0020 00a0
# 0020 0030 0040 0000 0010 0050 0090 0010 0050 0020 0000 0000 0030 0010 0020 0010 0040 0020 0040 0030
#
#
# ----- S U M M A R Y -----
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at 41990 cycle
#
# ** Note: $finish : C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture.av(228)
# Time: 2099500 ns Iteration: 0 Instance: /testfixture
# 1
# Break in Module testfixture at C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture
V$M 15>
```

tb1:

```
Library Project Memory List sim
Transcript
# 0020 0040 0060 0080 0020 0010 0000 0000 0000 0050 00a0 0030 0030 0090 0170 0000 01a0 02a0 03b0 05a0
# 0090 00a0 00b0 00c0 00d0 00e0 00f0 0040 0090 0090 0000 0000 0000 00b0 0180 01b0 0000 02f0 03a0 00b0 05a0
# 0020 0000 0000 0090 00b0 0090 0070 00c0 0100 00e0 0110 0200 02f0 0210 0160 00a0 0530 0430 0500 04e0
# 0030 0070 0050 0070 00a0 0000 0000 0000 00e0 0090 0120 01f0 0010 0170 0560 0040 03a0 04e0 0580 0000
# 0000 0000 0000 0000 0050 0040 0040 0020 00a0 00b0 0040 0130 0000 0720 0000 02f0 02a0 0570 0000
#
#
# ----- S U M M A R Y -----
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at 41990 cycle
#
# ** Note: $finish : C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture.av(228)
# Time: 2099507735 ps Iteration: 0 Instance: /testfixture
# 1
# Break in Module testfixture at C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture
V$M 4>
```

tb2:

```
Library Project Memory List sim
Transcript
# 0020 0000 0010 0000 0000 0000 0010 0040 0290 0000 0350 0040 0040 0020 04f0 00b0 0210 0470 0020 0050
# 0020 0010 0000 0000 0000 0000 0020 0150 0290 0230 01a0 0020 0000 0010 04c0 0030 00b0 0470 0010 0020
# 0020 0000 0000 0000 0000 0000 0010 01a0 0190 0010 0000 0010 0470 0000 0050 0430 0010 0010
# 0020 0000 0000 0010 0010 0000 0010 0200 00a0 01a0 0090 0010 0000 0010 0420 0000 0000 0410 0010 0020
# 0010 0000 0000 0000 0010 0000 00a0 0250 0000 01c0 0030 0030 0020 0030 01f0 02c0 02f0 01b0 0010 0020
#
#
# ----- S U M M A R Y -----
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at 41990 cycle
#
# ** Note: $finish : C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture.av(228)
# Time: 2099507735 ps Iteration: 0 Instance: /testfixture
# 1
# Break in Module testfixture at C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture
V$M 6>
```

tb3:

```
Library Project Memory List sim
Transcript
# 0100 0210 0210 01f0 0250 0230 0210 0290 02c0 0070 01f0 00a0 0110 0150 0190 0130 0170 0210 0170 01a0
# 00a0 0100 01a0 01a0 01c0 01c0 01e0 01a0 02a0 0290 0230 0290 0250 02a0 02a0 02a0 02a0 0220 0230 0210
# 0040 0040 0020 00a0 0010 0040 0020 0010 0050 0020 0000 0070 0030 0010 0030 0040 0000 0020 0020 0000
# 0000 0000 0000 0010 0020 0020 0000 0030 0030 0040 0040 0010 0020 0000 0040 0020 0010 0040 0020 00a0
# 0020 0030 0040 0000 0010 0050 0090 0010 0050 0020 0000 0000 0030 0010 0020 0010 0040 0020 0040 0030
#
#
# ----- S U M M A R Y -----
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at 41990 cycle
#
# ** Note: $finish : C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture.av(228)
# Time: 2099507735 ps Iteration: 0 Instance: /testfixture
# 1
# Break in Module testfixture at C:/Users/t/Downloads/System-20250525T1811282-1-001/System/testfixture
V$M 8>
```

ATCONV Synthesis Result

Total logic elements	223
Total memory bits	0
Total registers	86
Embedded multiplier 9-bit elements	2
Total Cycle used	41990

Compilation Report - ATCONV	
Table of Contents	Flow Summary
<ul style="list-style-type: none"> Flow Summary Flow Settings Flow Non-Default Global Settings Flow Elapsed Time Flow OS Summary Flow Log Analysis & Synthesis Fitter Assembler Timing Analyzer EDA Netlist Writer Flow Messages Flow Suppressed Messages 	<p><<Filter>></p> <p>Flow Status: Successful - Mon May 26 04:03:03 2025</p> <p>Quartus Prime Version: 20.1.1 Build 720 11/11/2020 SJ Lite Edition</p> <p>Revision Name: ATCONV</p> <p>Top-level Entity Name: ATCONV</p> <p>Family: Cyclone IV E</p> <p>Device: EP4CE55F23A7</p> <p>Timing Models: Final</p> <p>Total logic elements: 223 / 55,856 (< 1 %)</p> <p>Total registers: 86</p> <p>Total pins: 124 / 325 (38 %)</p> <p>Total virtual pins: 0</p> <p>Total memory bits: 0 / 2,396,160 (0 %)</p> <p>Embedded Multiplier 9-bit elements: 2 / 308 (< 1 %)</p> <p>Total PLLs: 0 / 4 (0 %)</p>

System Synthesis Result

Total logic elements	240
Total memory bits	0
Total registers	86
Embedded multiplier 9-bit elements	2
Total Cycle used	41990

Compilation Report - top	
Table of Contents	Flow Summary
<ul style="list-style-type: none"> Flow Summary Flow Settings Flow Non-Default Global Settings Flow Elapsed Time Flow OS Summary Flow Log Analysis & Synthesis Fitter Assembler Timing Analyzer EDA Netlist Writer Flow Messages Flow Suppressed Messages 	<p><<Filter>></p> <p>Flow Status: Successful - Mon May 26 02:48:41 2025</p> <p>Quartus Prime Version: 20.1.1 Build 720 11/11/2020 SJ Lite Edition</p> <p>Revision Name: top</p> <p>Top-level Entity Name: top</p> <p>Family: Cyclone IV E</p> <p>Device: EP4CE55F23A7</p> <p>Timing Models: Final</p> <p>Total logic elements: 240 / 55,856 (< 1 %)</p> <p>Total registers: 86</p> <p>Total pins: 124 / 325 (38 %)</p> <p>Total virtual pins: 0</p> <p>Total memory bits: 0 / 2,396,160 (0 %)</p> <p>Embedded Multiplier 9-bit elements: 2 / 308 (< 1 %)</p> <p>Total PLLs: 0 / 4 (0 %)</p>

Description of your design

基本上因為在 moodle 上助教說 bus 沒有規定 protocol，然後因為本次作業只有一個 master，所以我是讓 master 決定跟誰通訊，等於是 bridge 只是連線，我自己設計因為考量到 bus 的 bandwidth 所以是用一個乘加器來做卷積，然後我算卷積的順序剛好是 max_pool 的四個，因此每四次剛好也把 max_pool 結果算出，就不用再去重讀 layer0，所以變成說我的 SRAM 就只要被寫入，不會有讀取的動作，因此設計上是讓 master 要寫入 data 直接 broadcast 給 slave_1 跟 slave_2，地址也是直接 broadcast 給 slave_0 跟 slave_1 還有 slave_2，但寫入致能只有當 ID 對到會拉高，然後 ROM 的讀取致能直接給高，然後 master 讀資料因為只要讀 slave_0 的，所以直接把 ROM 資料接給 master 的讀通道就可。