2025 Digital IC Design Homework 5

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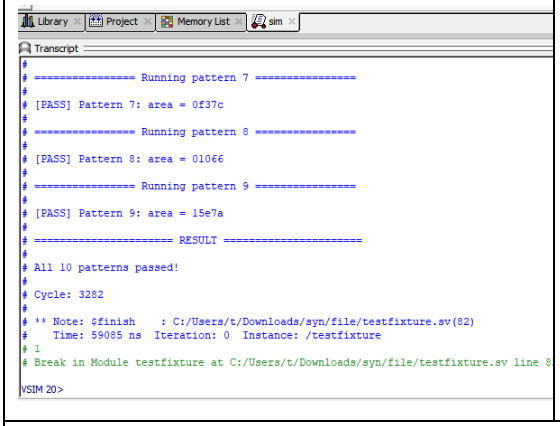
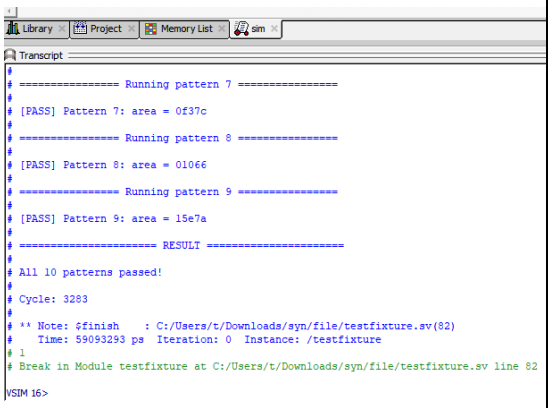
Simulation Result

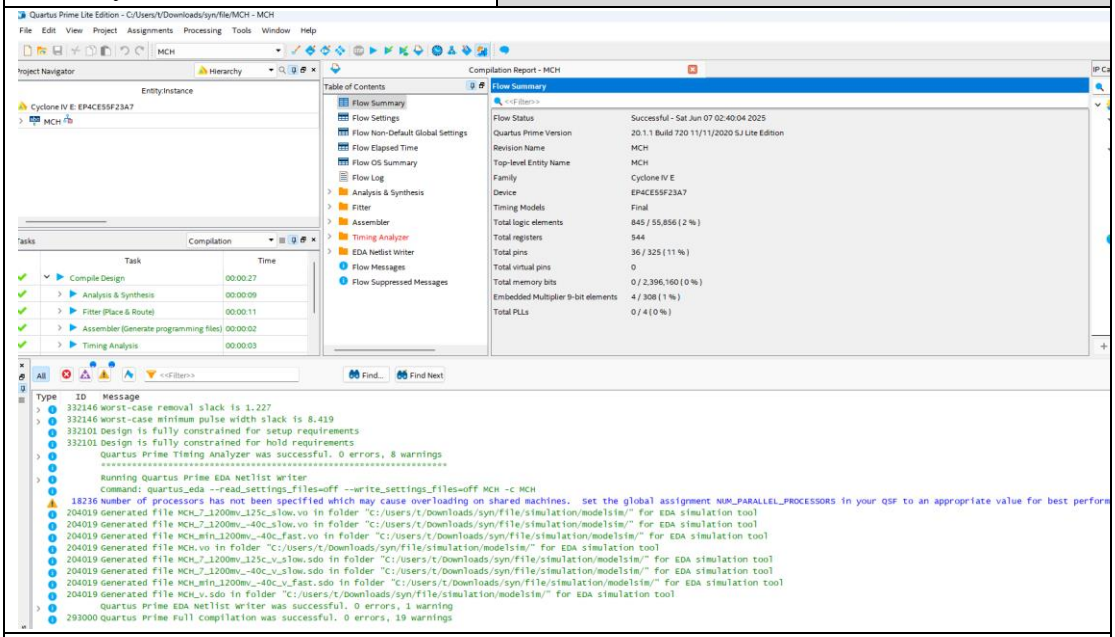
Functional simulation	Pass/Fail	Pre-Layout simulation	Pass/Fail





Synthesis Result

Total logic elements	845
Total memory bits	0
Total registers	544
Embedded multiplier 9-bit elements	4
Clock period (ns)	18
Total Cycle used	3283



Description of your design

我是用 gift wrapping algo，基本上收完資料就用狀態機迭代，邊做同時編算面積。