Run Length Encoding ₹

電路設計與後端

Digital-Based Design Flow

流程實作

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1. 電路功能介紹與應用:

此次電路是 RLE,是一種可變長度編碼,可以讓資料有大量 0時,大幅降低資料 symbol 數量,再會出現大量 0的場景,如人工智慧模型中經過 ReLU 運算或權重剪枝後,資料會出現大量的 0,因此可以在傳回 DRAM 時可以經過編碼,從 DRAM 讀出來後再進行解碼,如此一來可以大幅降低與 DRAM 傳輸之資料量。

電路功能驗證:

RTL SIM TEST=0:

RTL SIM TEST=1:

RTL SIM TEST=2:

RTL SIM TEST=3:

```
out: 1, type:
out: 1, type:
out: 7, type:
out: 4, type:
out: 5, type:
out: 9, type:
out: 1, type:
out: 13, type:
out: 10, type:
out: 5, type:
out: 5, type:
out: 3, type:
out: 5, type:
out: 23, type:
out: 23, type:
out: 3, type:
out: 3, type:
out: 1, type:
                         70, correct_answer:
70, correct_answer:
71, correct_answer:
72, correct_answer:
73, correct_answer:
74, correct_answer:
                                                                                                                                                                                                                                                                                                        PASS
PASS
                                                                                                                                                                                                                                                               level,
                                                                                                                                                                                                                                                                level,
                          75, correct_answer:
76, correct_answer:
                                                                                                                                                                                                                                                                                                        PASS
PASS
                       76, correct_answer: 1,
77, correct_answer: 13,
78, correct_answer: 10,
80, correct_answer: 5,
81, correct_answer: 23,
82, correct_answer: 3,
                                                                                                                                                                                                                                                                                                        PASS
PASS
               80, correct_answer: 5, out: 5, type: level, 81, correct_answer: 23, out: 23, type: run, 82, correct_answer: 3, out: 3, type: level, 83, correct_answer: 1, out: 1, type: term, 84, correct_answer: 11, out: 11, type: run, 85, correct_answer: 2, out: 2, type: run, 87, correct_answer: 3, out: 3, type: level, 88, correct_answer: 31, out: 31, type: run, 89, correct_answer: 31, out: 31, type: run, 89, correct_answer: 1, out: 1, type: level, 90, correct_answer: 31, out: 31, type: run, 92, correct_answer: 31, out: 31, type: run, 92, correct_answer: 31, out: 3, type: level, 93, correct_answer: 3, out: 3, type: run, 94, correct_answer: 3, out: 3, type: level, 95, correct_answer: 3, out: 3, type: level, 95, correct_answer: 30, out: 1, type: level, 97, correct_answer: 10, out: 10, type: level, 99, correct_answer: 10, out: 10, type: run, 100, correct_answer: 5, out: 5, type: level, 101, correct_answer: 1, out: 1, type: run, 102, correct_answer: 1, out: 1, type: level, 102, correct_answer: 21, out: 21, type: run, 103, correct_answer: 12, out: 12, type: level, 104, correct_answer: 12, out: 12, type: term, 105, correct_answer: 8, out: 8, type: run, 105, correct_answer: 10, out: 10, type: term, 105, correct_answer: 8, out: 8, type: run, 105, correct_answer: 10, out: 10, type: term, 105, correct_answer: 1
                                                                                                                                                                                                                                                                                                        PASS
PASS
                                                                                                                                                                                                                                                                                                        PASS
PASS
                                                                                                                                                                                                                                                                                                        PASS
PASS
                                                                                                                                                                                                                                                                                                        PASS
PASS
                                                                                                                                                                                                                                                                                                        PASS
PASS
                                                                                                                                                                                                                                                                   term, PASS
run, PASS
                                                                                                                             *********
                                                   |\/\/|
                                                                                                                                                                                                                                                                                                                            **
                                                         (0)(0)
                                                                                                                             **
                                                                                                                                                                           Congratulations !!
                                                                                                                                                                                                                                                                                                                            **
                                                                                                                                                                           Simulation PASS!!!
                                                                                                                                                                                                                                                                                                                            **
                                                                                                                              ********
  $finish called from file "/home/user1/hdlcs25/hdlcs2590/LAB13_FUCK/hw13_Example/sim/top_tb.sv", line 115.
$finish at simulation time 500000
VCS Simulation Report
Time: 5000000 ps
VCS Stmutation
Time: 5000000 ps
CPU Time: 0.240 seconds; Data structure size: 0.0Mb
Mon Jun 16 16:10:36 2025
CPU time: .305 seconds to compile + .275 seconds to elab + .190 seconds to link + .259 seconds in simulation
```

RTL SIM TEST=4

POST SYN SIM TEST=0

```
## 29, COTTECT_ANNUME 12, Out 12, 1 type: Level, PASS
# 71, COTTECT_ANNUME 12, Out 12, 1 type: Level, PASS
# 71, COTTECT_ANNUME 12, Out 12, 1 type: Level, PASS
# 72, COTTECT_ANNUME 11, Out 11, 1 type: Level, PASS
# 73, COTTECT_ANNUME 11, Out 11, 1 type: Level, PASS
# 75, COTTECT_ANNUME 11, Out 11, 1 type: Level, PASS
# 76, COTTECT_ANNUME 11, Out 11, 1 type: Level, PASS
# 77, COTTECT_ANNUME 11, Out 11, 1 type: Level, PASS
# 77, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 77, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 77, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 77, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 77, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 77, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16, 1 type: Level, PASS
# 78, COTTECT_ANNUME 12, Out 16
```

POST_SYN_SIM TEST=1

```
## 77, correct_manwer: 20, out: 20, type: run, PASS
# 78, correct_manwer: 25, out: 26, type: run, PASS
# 79, correct_manwer: 25, out: 26, type: run, PASS
# 81, correct_manwer: 19, out: 19, type: level, PASS
# 81, correct_manwer: 19, out: 19, type: level, PASS
# 81, correct_manwer: 19, out: 10, type: level, PASS
# 82, correct_manwer: 10, out: 10, type: level, PASS
# 83, correct_manwer: 10, out: 10, type: level, PASS
# 84, correct_manwer: 10, out: 10, type: level, PASS
# 85, correct_manwer: 1, out: 1, type: level, PASS
# 86, correct_manwer: 1, out: 1, type: level, PASS
# 88, correct_manwer: 1, out: 1, type: level, PASS
# 88, correct_manwer: 1, out: 11, type: run, PASS
# 88, correct_manwer: 1, out: 11, type: run, PASS
# 88, correct_manwer: 1, out: 11, type: run, PASS
# 88, correct_manwer: 1, out: 1, type: run, PASS
# 89, correct_manwer: 2, out: 2, type: level, PASS
# 91, correct_manwer: 3, out: 3, type: level, PASS
# 92, correct_manwer: 0, out: 0, type: level, PASS
# 93, correct_manwer: 1, out: 1, type: level, PASS
# 93, correct_manwer: 1, out: 1, type: level, PASS
# 94, correct_manwer: 1, out: 1, type: level, PASS
# 95, correct_manwer: 1, out: 1, type: level, PASS
# 96, correct_manwer: 1, out: 1, type: level, PASS
# 97, correct_manwer: 10, out: 10, type: level, PASS
# 98, correct_manwer: 10, out: 10, type: level, PASS
# 99, correct_manwer: 10, out: 10, type: level, PASS
# 99, correct_manwer: 10, out: 10, type: level, PASS
# 99, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, correct_manwer: 10, out: 10, type: level, PASS
# 100, co
```

POST SYN SIM TEST=2

```
# 62, correct_answer: 1, out: 1, type: term, PASS
# 63, correct_answer: 16, out: 16, type: run, PASS
# 64, correct_answer: 5, out: 5, type: term, PASS
# 65, correct_answer: 5, out: 5, type: run, PASS
# 65, correct_answer: 3, out: 3, type: level, PASS
# 67, correct_answer: 3, out: 3, type: level, PASS
# 67, correct_answer: 10, out: 11, type: run, PASS
# 68, correct_answer: 10, out: 1, type: term, PASS
# 70, correct_answer: 8, out: 8, type: run, PASS
# 71, correct_answer: 8, out: 8, type: run, PASS
# 72, correct_answer: 8, out: 8, type: run, PASS
# 73, correct_answer: 4, out: 4, type: level, PASS
# 74, correct_answer: 4, out: 2, type: level, PASS
# 74, correct_answer: 8, out: 8, type: level, PASS
# 75, correct_answer: 9, out: 0, type: run, PASS
# 76, correct_answer: 0, out: 0, type: run, PASS
# 77, correct_answer: 0, out: 0, type: run, PASS
# 78, correct_answer: 0, out: 0, type: run, PASS
# 78, correct_answer: 0, out: 0, type: run, PASS
# 78, correct_answer: 0, out: 0, type: run, PASS
# 78, correct_answer: 0, out: 0, type: run, PASS
# 78, correct_answer: 0, out: 0, type: run, PASS
# 88, correct_answer: 0, out: 0, type: run, PASS
# 88, correct_answer: 0, out: 0, type: run, PASS
# 88, correct_answer: 0, out: 0, type: run, PASS
# 88, correct_answer: 0, out: 0, type: run, PASS
# 88, correct_answer: 0, out: 0, type: run, PASS
# 88, correct_answer: 0, out: 0, type: run, PASS
# 88, correct_answer: 0, out: 0, type: run, PASS
# 89, correct_answer: 0, out: 0, type: run, PASS
# 89, correct_answer: 0, out: 0, type: run, PASS
# 89, correct_answer: 0, out: 0, type: run, PASS
# 89, correct_answer: 0, out: 0, type: run, PASS
# 89, correct_answer: 0, out: 0, type: run, PASS
# 89, correct_answer: 0, out: 0, type: run, PASS
# 89, correct_answer: 0, out: 0, type: run, PASS
# 89, correct_answer: 0, out: 0, type: run, PASS
# 99, correct_answer: 0, out: 0, type: run, PASS
# 99, correct_answer: 0, out: 0, type: run, PASS
# 99, correct_answer: 0, out: 0, type: run, PASS
# 99, correct_answer: 0, out: 0, type: run, PASS
# 99, correct_answe
```

POST SYN SIM TEST=3

```
# 73, correct_answer: 2, out: 2, type: rum, PASS # 75, correct_answer: 1, out: 1, type: terem, PASS # 75, correct_answer: 1, out: 1, type: terem, PASS # 77, correct_answer: 3, out: 3, type: level, PASS # 77, correct_answer: 3, out: 3, type: rum, PASS # 78, correct_answer: 3, out: 3, type: rum, PASS # 79, correct_answer: 3, out: 3, type: rum, PASS # 80, correct_answer: 5, out: 3, type: rum, PASS # 81, correct_answer: 3, out: 3, type: rum, PASS # 81, correct_answer: 3, out: 3, type: rum, PASS # 82, correct_answer: 1, out: 1, type: rum, PASS # 83, correct_answer: 1, out: 1, type: rum, PASS # 83, correct_answer: 4, out: 4, type: rum, PASS # 85, correct_answer: 4, out: 4, type: rum, PASS # 88, correct_answer: 3, out: 3, type: rum, PASS # 88, correct_answer: 3, out: 3, type: rum, PASS # 88, correct_answer: 3, out: 3, type: rum, PASS # 88, correct_answer: 4, out: 1, type: rum, PASS # 89, correct_answer: 4, out: 1, type: rum, PASS # 89, correct_answer: 0, out: 0, type: level, PASS # 89, correct_answer: 0, out: 0, type: level, PASS # 89, correct_answer: 0, out: 1, type: rum, PASS # 99, correct_answer: 0, out: 1, type: term, PASS # 99, correct_answer: 0, out: 1, type: rum, PASS # 93, correct_answer: 0, out: 3, type: rum, PASS # 93, correct_answer: 0, out: 0, type: rum, PASS # 94, correct_answer: 0, out: 0, type: rum, PASS # 95, correct_answer: 0, out: 0, type: rum, PASS # 95, correct_answer: 0, out: 0, type: rum, PASS # 96, correct_answer: 1, out: 1, type: rum, PASS # 99, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_answer: 1, out: 1, type: rum, PASS # 103, correct_a
```

POST SYN SIM TEST=4

```
type:
type:
type:
type:
             57, correct_answer: 4, out: 58, correct_answer: 31, out: 59, correct_answer: 0, out: 60, correct_answer: 1, out: 61, correct_answer: 14, out:
                                                                                                                                           run,
level,
                                                                                                                                           run,
level,
             62, correct_answer:
63, correct_answer:
64, correct_answer:
        65, correct answer: 5, out:
66, correct answer: 31, out:
66, correct answer: 0, out:
67, correct answer: 7, out:
68, correct answer: 5, out:
70, correct answer: 1, out:
71, correct answer: 4, out:
72, correct answer: 20, out:
73, correct answer: 24, out:
74, correct answer: 24, out:
75, correct answer: 10, out:
76, correct answer: 1, out:
77, correct answer: 5, out:
78, correct answer: 5, out:
78, correct answer: 2, out:
                                                                                                                                          level,
                                                                                                                       type:
type:
                                                                                                                                            term,
run,
                                                                                                                      type:
type:
type:
type:
                                                                                                                    type: run,
type: level,
type: run,
type: run,
type: level
                                                                                                                       type:
                                                                                                                                            term,
run,
            77, correct_answer: 5, out: 5, type: 78, correct_answer: 2, out: 2, type: 79, correct_answer: 31, out: 31, type: 80, correct_answer: 0, out: 0, type: 81, correct_answer: 6, out: 6, type: 82, correct_answer: 3, out: 3, type: 83, correct_answer: 1, out: 1, type: 84, correct_answer: 30, out: 30, type:
                                                                                                                                         level,
run,
level,
                                                                                                                                         run,
level,
                                                                                                                                                                PASS
PASS
                                                                                                                                               term, PASS
run, PASS
                                 (0)(0)
                                                                                       Congratulations !!
                                                                                          Simulation PASS!!!
```

POST LAYOUT SUM TEST=0

```
# 75, correct_answer: 11, out: 11, type: level, PASS
# 76, correct_answer: 1, out: 1, type: term, PASS
# 77, correct_answer: 0, out: 0, type: run, PASS
# 77, correct_answer: 5, out: 5, type: level, PASS
# 77, correct_answer: 5, out: 5, type: level, PASS
# 80, correct_answer: 1, out: 1, type: level, PASS
# 81, correct_answer: 1, out: 1, type: level, PASS
# 82, correct_answer: 1, out: 1, type: term, PASS
# 83, correct_answer: 1, out: 1, type: term, PASS
# 83, correct_answer: 1, out: 1, type: level, PASS
# 83, correct_answer: 1, out: 1, type: run, PASS
# 85, correct_answer: 1, out: 1, type: level, PASS
# 86, correct_answer: 24, out: 24, type: run, PASS
# 87, correct_answer: 4, out: 8, type: level, PASS
# 88, correct_answer: 4, out: 4, type: level, PASS
# 89, correct_answer: 4, out: 4, type: level, PASS
# 90, correct_answer: 4, out: 4, type: level, PASS
# 91, correct_answer: 1, out: 1, type: level, PASS
# 92, correct_answer: 1, out: 1, type: level, PASS
# 93, correct_answer: 1, out: 1, type: level, PASS
# 94, correct_answer: 1, out: 1, type: level, PASS
# 95, correct_answer: 1, out: 1, type: level, PASS
# 96, correct_answer: 1, out: 1, type: level, PASS
# 97, correct_answer: 1, out: 1, type: level, PASS
# 96, correct_answer: 1, out: 1, type: level, PASS
# 97, correct_answer: 1, out: 1, type: level, PASS
# 96, correct_answer: 0, out: 0, type: level, PASS
# 97, correct_answer: 0, out: 0, type: level, PASS
# 99, correct_answer: 0, out: 0, type: level, PASS
# 99, correct_answer: 0, out: 0, type: level, PASS
# 101, correct_answer: 0, out: 0, type: level, PASS
# 102, correct_answer: 0, out: 0, type: level, PASS
# 103, correct_answer: 0, out: 0, type: level, PASS
# 104, correct_answer: 0, out: 0, type: level, PASS
# 105, correct_answer: 0, out: 0, type: level, PASS
# 106, correct_answer: 0, out: 0, type: level, PASS
# 107, correct_answer: 0, out: 0, type: level, PASS
# 108, correct_answer: 0, out: 0, type: level, PASS
# 109, correct_answer: 0, out: 0, type: level, PASS
# 109, correct_answer: 0, out: 0, type: level, PASS
#
```

POST_LAYOUT_SUM TEST=1

```
# 81, correct_answer: 19, out: 19, type: run, PASS
# 81, correct_answer: 3, out: 3, type: level, PASS
# 82, correct_answer: 1, out: 1, type: term, PASS
# 83, correct_answer: 6, out: 6, type: run, PASS
# 85, correct_answer: 10, out: 10, type: run, PASS
# 85, correct_answer: 10, out: 10, type: level, PASS
# 86, correct_answer: 10, out: 11, type: run, PASS
# 88, correct_answer: 11, out: 11, type: run, PASS
# 89, correct_answer: 2, out: 2, type: level, PASS
# 89, correct_answer: 3, out: 3, type: run, PASS
# 89, correct_answer: 3, out: 3, type: run, PASS
# 91, correct_answer: 3, out: 3, type: run, PASS
# 92, correct_answer: 1, out: 1, type: term, PASS
# 92, correct_answer: 1, out: 1, type: level, PASS
# 93, correct_answer: 1, out: 1, type: level, PASS
# 94, correct_answer: 14, out: 14, type: level, PASS
# 95, correct_answer: 14, out: 14, type: level, PASS
# 96, correct_answer: 14, out: 14, type: level, PASS
# 97, correct_answer: 14, out: 14, type: level, PASS
# 98, correct_answer: 14, out: 14, type: level, PASS
# 99, correct_answer: 14, out: 14, type: level, PASS
# 100, correct_answer: 10, out: 11, type: level, PASS
# 101, correct_answer: 10, out: 11, type: level, PASS
# 102, correct_answer: 10, out: 11, type: level, PASS
# 103, correct_answer: 10, out: 11, type: level, PASS
# 104, correct_answer: 10, out: 11, type: level, PASS
# 105, correct_answer: 10, out: 11, type: level, PASS
# 106, correct_answer: 10, out: 11, type: level, PASS
# 107, correct_answer: 10, out: 11, type: level, PASS
# 108, correct_answer: 10, out: 11, type: level, PASS
# 109, correct_answer: 10, out: 11, type: level, PASS
# 100, correct_answer: 10, out: 11, type: level, PASS
# 101, correct_answer: 10, out: 11, type: level, PASS
# 102, correct_answer: 10, out: 11, type: level, PASS
# 103, correct_answer: 10, out: 11, type: level, PASS
# 104, correct_answer: 10, out: 11, type: level, PASS
# 105, correct_answer: 10, out: 11, type: level, PASS
# 107, correct_answer: 10, out: 11, type: level, PASS
# 109, correct_answer: 10, out: 11, type: level, PASS
```

POST LAYOUT SUM TEST=2

```
### 0.00 | Context_answer: 0.0 | Out: 0.10 | Out: 0.10 |
### 0.1 | Correct_answer: 1.0 | Out: 0.10 | Out: 0.10 |
### 0.2 | Correct_answer: 1.0 | Out: 1.0 | Out: 1.0 | Out: 1.0 |
### 0.3 | Correct_answer: 1.0 | Out: 1.0 | Out: 1.0 | Out: 1.0 |
### 0.3 | Correct_answer: 3.0 | Out: 3.10 | Out: 1.0 | Out: 1.0 |
### 0.5 | Correct_answer: 3.0 | Out: 3.10 | Out: 1.0 | Out: 1.0 |
### 0.5 | Correct_answer: 3.0 | Out: 3.10 | Out: 3.10 | Out: 3.10 |
### 0.6 | Correct_answer: 3.0 | Out: 4.10 | Out: 3.10 | Out: 3.10 |
### 0.7 | Out: 4.0 | Out: 4.10 |
### 0.7 | Correct_answer: 6.0 | Out: 6.10 | Out: 4.10 | Out: 4
```

POST LAYOUT SUM TEST=3

```
# 75, correct_answer: 9, out: 9, type: level, PASS
# 76, correct_answer: 1, out: 1, type: term, PASS
# 77, correct_answer: 13, out: 31, type: run, PASS
# 77, correct_answer: 13, out: 31, type: run, PASS
# 78, correct_answer: 10, out: 10, type: run, PASS
# 88, correct_answer: 10, out: 10, type: run, PASS
# 88, correct_answer: 20, out: 20, type: run, PASS
# 81, correct_answer: 10, out: 10, type: run, PASS
# 82, correct_answer: 10, out: 10, type: term, PASS
# 83, correct_answer: 10, out: 10, type: term, PASS
# 83, correct_answer: 10, out: 10, type: term, PASS
# 85, correct_answer: 11, out: 11, type: term, PASS
# 86, correct_answer: 20, out: 20, type: level, PASS
# 87, correct_answer: 31, out: 31, type: level, PASS
# 88, correct_answer: 31, out: 31, type: level, PASS
# 89, correct_answer: 31, out: 31, type: level, PASS
# 89, correct_answer: 31, out: 31, type: run, PASS
# 89, correct_answer: 0, out: 0, type: level, PASS
# 89, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 91, correct_answer: 0, out: 0, type: level, PASS
# 92, correct_answer: 0, out: 0, type: level, PASS
# 93, correct_answer: 0, out: 0, type: level, PASS
# 94, correct_answer: 0, out: 0, type: level, PASS
# 95, correct_answer: 0, out: 0, type: level, PASS
# 96, correct_answer: 0, out: 0, type: level, PASS
# 97, correct_answer: 0, out: 0, type: level, PASS
# 98, correct_answer: 0, out: 0, type: level, PASS
# 99, correct_answer: 0, out: 0, type: level, PASS
# 99, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 1, type: term, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level, PASS
# 90, correct_answer: 0, out: 0, type: level,
```

POST LAYOUT SUM TEST=4

```
# 50, correct_mswer: 0, out: 0, type: level, PASS
# 51, correct_mswer: 1, out: 1, type: run, PASS
# 52, correct_mswer: 10, out: 10, type: run, PASS
# 53, correct_mswer: 10, out: 10, type: run, PASS
# 53, correct_mswer: 10, out: 10, type: run, PASS
# 54, correct_mswer: 10, out: 10, type: run, PASS
# 55, correct_mswer: 10, out: 10, type: run, PASS
# 55, correct_mswer: 10, out: 10, type: run, PASS
# 57, correct_mswer: 4, out: 4, type: run, PASS
# 57, correct_mswer: 4, out: 4, type: run, PASS
# 59, correct_mswer: 0, out: 0, type: run, PASS
# 59, correct_mswer: 1, out: 1, type: run, PASS
# 60, correct_mswer: 1, out: 1, type: run, PASS
# 63, correct_mswer: 1, out: 1, type: run, PASS
# 64, correct_mswer: 8, out: 8, type: run, PASS
# 65, correct_mswer: 8, out: 8, type: run, PASS
# 66, correct_mswer: 9, out: 0, type: level, PASS
# 66, correct_mswer: 0, out: 0, type: level, PASS
# 67, correct_mswer: 0, out: 0, type: level, PASS
# 68, correct_mswer: 0, out: 0, type: level, PASS
# 69, correct_mswer: 0, out: 1, type: term, PASS
# 69, correct_mswer: 0, out: 1, type: term, PASS
# 70, correct_mswer: 1, out: 1, type: term, PASS
# 71, correct_mswer: 1, out: 1, type: term, PASS
# 72, correct_mswer: 1, out: 1, type: term, PASS
# 73, correct_mswer: 1, out: 1, type: term, PASS
# 74, correct_mswer: 2, out: 2, type: run, PASS
# 77, correct_mswer: 3, out: 3, type: run, PASS
# 77, correct_mswer: 2, out: 2, type: level, PASS
# 78, correct_mswer: 3, out: 1, type: term, PASS
# 78, correct_mswer: 3, out: 1, type: term, PASS
# 79, correct_mswer: 3, out: 1, type: term, PASS
# 79, correct_mswer: 3, out: 1, type: term, PASS
# 79, correct_mswer: 3, out: 1, type: term, PASS
# 79, correct_mswer: 3, out: 1, type: term, PASS
# 79, correct_mswer: 3, out: 1, type: term, PASS
# 79, correct_mswer: 3, out: 1, type: term, PASS
# 79, correct_mswer: 3, out: 1, type: term, PASS
# 79, correct_mswer: 3, out: 1, type: term, PASS
# 84, correct_mswer: 3, out: 1, type: term, PASS
# 85, correct_mswer: 3, out: 1, type: term, PASS
# 86, correct_mswer: 3, out: 1, type
```

2. IN/OUT Pin/Port 宣告:

```
module CHIP (
    input clk,
    input rst,
    input [4:0] in_data,
    input in_valid,
    output [4:0] out_data,
    output out_valid
);
```

```
PDCDG_V ipad_clk (.C(clk_core), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(clk));
PDCDG_V ipad_rst (.C(rst_core), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(rst));
PDCDG_H ipad_indata0 (.C(in_data_core[0]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[0])
PDCDG_H ipad_indata1 (.C(in_data_core[1]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[1]))
PDCDG_H ipad_indata2 (.C(in_data_core[2]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[2]))
PDCDG_H ipad_indata3 (.C(in_data_core[3]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[3]))
PDCDG_H ipad_indata4 (.C(in_data_core[4]), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_data[4]))
PDCDG_V ipad_in_valid (.C(in_valid_core), .I(1'b0), .IE(1'b1), .OEN(1'b1), .PAD(in_valid));
PDCDG_V opad_out_valid (.C(), .I(out_valid_core), .IE(1'b0), .OEN(1'b0), .PAD(out_valid));
PDCDG_H opad_odata0 (.C(), .I(out_data_core[0]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[0]));
PDCDG_H opad_odata1 (.C(), .I(out_data_core[1]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[1]));
PDCDG_H opad_odata2 (.C(), .I(out_data_core[2]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[2]));
PDCDG_H opad_odata3 (.C(), .I(out_data_core[3]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[3]));
PDCDG_H opad_odata4 (.C(), .I(out_data_core[4]), .IE(1'b0), .OEN(1'b0), .PAD(out_data[4]));
```

3. Design Compiler

```
Design constraint
set clk period 4.0
create clock -name clk -period $clk period [get ports clk]
set dont touch network
                              [all clocks]
set fix hold
                               [all clocks]
                       0.1 [all clocks]
set clock uncertainty
set clock latency
                        0.5
                            [all clocks]
set input transition
                      0.2
                           [all inputs]
set clock transition
                      0.1
                            [all clocks]
                              [all clocks]
set ideal network
set dont touch [get cells ipad *]
set dont touch [get cells opad *]
set operating conditions -min library
N16ADFP StdCellff0p88v125c -min ff0p88v125c \
                             -max library
N16ADFP StdCellss0p72vm40c -max ss0p72vm40c
```

set dont use N16ADFP StdCellss0p72vm40c/TIEHBWP16P90

set dont use N16ADFP StdCellss0p72vm40c/TIEHBWP16P90LVT

```
set dont use N16ADFP StdCellss0p72vm40c/TIEHBWP20P90
set dont use N16ADFP StdCellss0p72vm40c/TIEHBWP20P90LVT
set dont use N16ADFP StdCellss0p72vm40c/TIELBWP16P90
set dont use N16ADFP StdCellss0p72vm40c/TIELBWP16P90LVT
set dont use N16ADFP StdCellss0p72vm40c/TIELBWP20P90
set dont use N16ADFP StdCellss0p72vm40c/TIELBWP20P90LVT
N16ADFP StdCellff0p88vm40c/TIEHBWP16P90LVT
N16ADFP StdCellff0p88vm40c/TIEHBWP20P90LVT
N16ADFP StdCellff0p88vm40c/TIELBWP16P90LVT
N16ADFP StdCellff0p88vm40c/TIELBWP20P90LVT
set dont use N16ADFP StdCellff0p88v125c/TIEHBWP16P90
set dont use N16ADFP StdCellff0p88v125c/TIEHBWP16P90LVT
set dont use N16ADFP StdCellff0p88v125c/TIEHBWP20P90
set dont use N16ADFP StdCellff0p88v125c/TIEHBWP20P90LVT
set dont use N16ADFP StdCellff0p88v125c/TIELBWP16P90
set dont use N16ADFP StdCellff0p88v125c/TIELBWP16P90LVT
set dont use N16ADFP StdCellff0p88v125c/TIELBWP20P90
set dont use N16ADFP StdCellff0p88v125c/TIELBWP20P90LVT
set input max clk
                  [expr {double(round(1000*$clk period *
0.6))/1000
set input min clk
                 [expr {double(round(1000*$clk period *
(0.0)
                  [expr {double(round(1000*$clk period *
set output max clk
0.1))/1000
set output min clk
                 [expr {double(round(1000*$clk period *
(0.0)
set load [load of
"N16ADFP StdIOss0p72v1p62v125c/PDCDG H/PAD"]
[all outputs]
set load [load of
"N16ADFP StdIOss0p72v1p62v125c/PDCDG V/PAD"]
[all outputs]
set driving cell-library N16ADFP StdIOss0p72v1p62v125c -
```

lib cell PDCDG H -pin {C} [all inputs]

Area report

```
area.log
  2 **************
 3 Report : area
4 Design : CHIP
 5 Version: P-2019.03-SP1-1
6 Date : Mon Jun 16 16:49:10 2025
 9 Library(s) Used:
10
          N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/II
N16ADFP_StdI0ss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package/Collateral:
11
12
13
14 Number of ports:
15 Number of nets:
16 Number of cells:
17 Number of combinational cells:
18 Number of sequential cells:
19 Number of macros/black boxes:
20 Number of buf/inv:
21 Number of references:
                                                                      56
                                                                    4060
                                                                    4000
                                                                    3302
                                                                     679
                                                                    1117
21 Number of references:
23 Combinational area:
                                                        1283.091861
24 Buf/Inv area:
                                                          635.610239
25 Noncombinational area:
                                                          774.593308
26 Macro/Black Box area:
                                                       23102.004639
27 Net Interconnect area:
                                               undefined (Wire load has zero net area)
28
29 Total cell area:
                                                       25159.689808
30 Total area:
                                               undefined
31 1
```

Power report

Timing report

Set up:

```
*************
Report : timing -path full
               -delay max
               -max_paths 1
               -sort_by group
Design : CHIP
Version: P-2019.03-SP1-1
Date : Mon Jun 16 16:49:14 2025
Operating Conditions: ss0p72vm40c Library: N16ADFP_StdCellss0p72vm40c Wire Load Model Mode: segmented
    Startpoint: top/out_counter_reg_2
   (rising edge-triggered flip-flop clocked by clk)
Endpoint: top/OUT_buffer_reg_127__0_
(rising edge-triggered flip-flop clocked by clk)
    Path Group: clk
   Path Type: max
   Des/Clust/Port Wire Load Model Li
                                                                          Library
   CHIP ZeroWireload N16ADFP_StdCellssOp72vm40c
top ZeroWireload N16ADFP_StdCellssOp72vm40c
top_DW01_inc_1 ZeroWireload N16ADFP_StdCellssOp72vm40c
                                                                                                            Incr
    clock clk (rise edge)
   clock CIK (rise edge)
clock network delay (ideal)
top/out_counter_reg_2_/CP (DFCNQD2BWP16P90LVT)
top/out_counter_reg_2_/Q (DFCNQD2BWP16P90LVT)
top/U721/Z (DEL025D1BWP20P90)
top/U2799/ZN (XNR2D1BWP16P90LVT)
top/U763/Z (AN4D2BWP16P90LVT)
                                                                                                            0.50
                                                                                                      0.00
0.06
                                                                                                                                0.50 r
0.56 f
                                                                                                           0.05
                                                                                                                                0.61 f
                                                                                                           0.03
                                                                                                                                0.64 r
   top/U763/Z (AN4D2BWP16P90LVT)
top/U1656/ZN (IOA21D1BWP16P90LVT)
top/U1436/ZN (OAI21D1BWP16P90LVT)
top/U1435/ZN (AOI22D1BWP16P90LVT)
top/U1453/ZN (ND2D1BWP16P90LVT)
top/U1368/ZN (IND2D1BWP16P90LVT)
top/U1326/ZN (ND2D1BWP16P90LVT)
top/U1391/ZN (IOAI21D1BWP16P90LVT)
top/U1390/Z (BUFFD1BWP16P90LVT)
top/U1270/ZN (ND3D1BWP16P90LVT)
top/U1271/ZN (CKND1BWP16P90LVT)
top/U1271/ZN (OAI22D1BWP16P90LVT)
top/U1002/ZN (OAI22D1BWP16P90LVT)
top/U796/ZN (CKND1BWP16P90LVT)
top/U796/ZN (CKND1BWP16P90LVT)
top/U1600/Z (AN2D1BWP16P90LVT)
top/U1600/Z (AN2D1BWP16P90LVT)
                                                                                                           0.02
                                                                                                                                0.66 r
                                                                                                           0.01
                                                                                                                                0.67 r
0.68 f
                                                                                                           0.01
                                                                                                                                0.69 r
                                                                                                            0.01
                                                                                                                                0.71 f
                                                                                                            0.02
                                                                                                                                 0.73 f
                                                                                                           0.01
                                                                                                                                0.74 r
0.75 f
                                                                                                                                0.78 f
                                                                                                            0.03
                                                                                                                                0.79
                                                                                                            0.01
                                                                                                                                0.79 r
0.81 f
                                                                                                            0.02
                                                                                                           0.03
                                                                                                                                0.84 r
0.86 f
                                                                                                            0.02
                                                                                                                                0.88 r
                                                                                                                                0.90 r
0.91 f
                                                                                                            0.02
    top/U1475/ZN (AOI22D1BWP16P90LVT)
top/U1597/ZN (IOA21D1BWP16P90LVT)
top/U63/Z (DELO50D1BWP20P90)
                                                                                                            0.01
                                                                                                                                0.91 r
1.00 r
                                                                                                           0.01
    top/OUT_buffer_reg_127__0_/D (DFCNQD2BWP16P90LVT)
                                                                                                           0.00
                                                                                                                                 1.00 r
    data arrival time
                                                                                                                                 1.00
                                                                                                           4.00
0.50
   clock clk (rise edge)
clock network delay (ideal)
                                                                                                                                4.00
                                                                                                                                4.50
                                                                                                                                4.40
    clock uncertainty
                                                                                                          -0.10
   top/OUT_buffer_reg_127__0_/CP (DFCNQD2BWP16P90LVT) library setup time data required time
                                                                                                           0.00
                                                                                                                                4.40 r
                                                                                                                                4.40
                                                                                                                                4.40
                                                                                                                                4.40
    data reguired time
    data arrival time
                                                                                                                              -1.00
                 3.40
    slack (MET)
```

Hold time:

Report : timing -path full -delay min -max_paths 1

Operating Conditions: ff0p88v125c Library: N16ADFP_StdCellff0p88v125c Wire Load Model Mode: segmented

Des/Clust/Port Wire Load Model

Library

Path Group: clk Path Type: min

Des/Clust/Port	Wire Load Model	Library		
CHIP top	ZeroWireload ZeroWireload	N16ADFP_StdC N16ADFP_StdC		
Point			Incr	Path
top/current_state top/U1494/ZN (CKN top/U15/ZN (CKNR2 top/U18/Z (CKBD1B top/U17/Z (CKBD1B top/U16/Z (CKBD1B top/U12/ZN (INVD1 top/U13/ZN (INVD1	ay (ideal) _reg_1_/CP (DFCNQD2BWF _reg_1_/Q (DFCNQD2BWP) D1BWP16P90LVT) D1BWP20P90) WP16P90LVT) WP16P90LVT) WP16P90LVT) BWP16P90LVT) BWP16P90LVT) BWP16P90LVT) /D (DFCNQD2BWP16P90LVT)	6P90LVT)	0.00 0.50 0.00 0.06 0.01 0.02 0.01 0.01 0.01 0.00 0.00	0.00 0.50 0.50 r 0.56 f 0.57 r 0.59 f 0.60 f 0.61 f 0.62 f 0.62 r 0.63 f 0.63 f
clock clk (rise e clock network del clock uncertainty top/out_valid_reg library hold time data required tim	ay (ideal) / /CP (DFCNQD2BWP16P90LV :	T)	0.00 0.50 0.10 0.00 0.03	0.00 0.50 0.60 0.60 r 0.63 0.63
data required tim data arrival time				0.63 -0.63
slack (MET)				0.00

4. Post-Synthesis Timing/Power Report :

Primetime report

Set up time violation path:

```
max_timing_violati...
1 **************
2 Report : timing
    -path_type full
    -delay_type max
-slack_lesser_than 0.00
5
    -max_paths 20
    -sort_by slack
7
8 Design : CHIP
9 Version: P-2019.03-SP5-1
        : Mon Jun 16 17:04:31 2025
11 ***************
12
13 No paths with slack less than 0.00.
14
15 1
16
```

Hold time violation path:

```
min_timing_violatio...
1 *************
2 Report : timing
   -path_type full
   -delay_type min
   -slack_lesser_than 0.00
5
   -max_paths 20
   -sort_by slack
8 Design : CHIP
9 Version: P-2019.03-SP5-1
       : Mon Jun 16 17:04:31 2025
10 Date
11 **************
12
13 No paths with slack less than 0.00.
```

Primepower report

根據 pattern 0 的 toggle 情形之 power 計算:

```
************
Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date : Mon Jun 16 17:15:56 2025
************
  Attributes
      i - Including register clock pin internal power

    User defined power group

                       Internal Switching Leakage
                                                       Total
Power Group
                                            Power
                                                      Power (
                                                                   %) Attrs
                       Power Power
                    3.915e-04
                                    0.0000
                                              0.0000 3.915e-04 (72.86%) i
clock network
                       1.359e-06 2.748e-07 5.172e-07 2.151e-06 ( 0.40%) 7.066e-06 8.083e-06 4.740e-07 1.562e-05 ( 2.91%)
register
combinational
                       0.0000 0.0000 0.0000 0.0000 (0.00%)
sequential
                       0.0000 0.0000 0.0000 0.0000 (0.00%)
7.799e-05 4.705e-05 3.024e-06 1.281e-04 (23.83%)
memory
io_pad
black_box
                          0.0000
                                    0.0000
                                              0.0000 0.0000 (0.00%)
  Net Switching Power = 5.541e-05
                                    (10.31%)
  Cell Internal Power = 4.780e-04
                                    (88.94\%)
  Cell Leakage Power = 4.015e-06
                                    (0.75\%)
Total Power
                      = 5.374e-04 (100.00%)
```

根據 pattern 1 的 toggle 情形之 power 計算:

```
***********
Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date : Mon Jun 16 17:18:17 2025
***********
  Attributes

    Including register clock pin internal power
    User defined power group

                                 Internal Switching Leakage
                                                                               Total
                                                                                                   %) Attrs
Power Group
                                 Power
                                                Power
                                                               Power
                                                                               Power
                                 3.916e-04 0.0000 0.0000 3.916e-04 (71.26%) i
1.409e-06 2.866e-07 5.161e-07 2.212e-06 (0.40%)
7.427e-06 8.544e-06 4.733e-07 1.644e-05 (2.99%)
0.0000 0.0000 0.0000 0.0000 (0.00%)
0.0000 0.0000 0.0000 0.0000 (0.00%)
8.904e-05 4.721e-05 2.999e-06 1.393e-04 (25.34%)
                         3.916e-04
clock_network
register
combinational
sequential
io_pad
black_box
                                      0.0000
                                                   0.0000
                                                                  0.0000
                                                                                0.0000 (0.00%)
  Net Switching Power = 5.605e-05
Cell Internal Power = 4.894e-04
Cell Leakage Power = 3.988e-06
                                                    (10.20\%)
                                                    (89.07%)
                                                    (0.73\%)
Total Power
                               = 5.495e-04 (100.00%)
```

根據 pattern 2 的 toggle 情形之 power 計算:

```
***********
Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date : Mon Jun 16 17:19:27 2025
   Attributes
       i – Including register clock pin internal power u – User defined power group
                           Internal Switching Leakage
Power Group
                                                   Power
                          Power Power
                                                                Power
                                                                       ( %) Attrs
clock_network 3.916e-04
                                          0.0000
                                                     0.0000 3.916e-04 (72.44%) i
                         1.286e-06 2.623e-07 5.088e-07 2.057e-06 ( 0.38%) 6.447e-06 6.865e-06 4.749e-07 1.379e-05 ( 2.55%)
register
combinational
                           0.0000 0.0000 0.0000 0.0000 (0.00%)
sequential
                                          0.0000
                           0.0000 0.0000 0.0000 0.0000 (0.00%)
8.300e-05 4.713e-05 3.010e-06 1.331e-04 (24.63%)
                                                     0.0000
memory
io_pad
black_box
                              0.0000 0.0000
                                                     0.0000 0.0000 (0.00%)
  Net Switching Power = 5.425e-05
Cell Internal Power = 4.824e-04
Cell Leakage Power = 3.993e-06
                                         (10.04\%)
                                           (89.23\%)
                                          (0.74\%)
Total Power
                          = 5.406e-04 (100.00%)
```

根據 pattern 3 的 toggle 情形之 power 計算:

```
**********
```

Report : Averaged Power Design : CHIP

Version: P-2019.03-SP5-1

Date : Mon Jun 16 17:24:34 2025

Attributes

i - Including register clock pin internal power

u - User defined power group

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
clock_network register combinational sequential memory io_pad black_box	1.333e-06 6.869e-06 0.0000 0.0000	0.0000 4.712e-05	5.108e-07 4.748e-07 0.0000 0.0000	2.116e-06 1.491e-05 0.0000 0.0000 1.326e-04	(0.39%) (2.75%) (0.00%) (0.00%)	i
Net Switching Power Cell Internal Power Cell Leakage Power Total Power	= 4.823e-0	4 (89.11) 6 (0.74)	(x) (x)			

根據 pattern 4 的 toggle 情形之 power 計算:

```
**********
 Report : Averaged Power
Design : CHIP
Version: P-2019.03-SP5-1
Date : Mon Jun 16 17:26:46 2025
 ************
      Attributes
                i – Including register clock pin internal power u – User defined power group
                                                                Internal Switching Leakage
                                                                                                                                                  Total
                                                                                                                    Power
 Power Group
                                                             Power Power
                                                                                                                                               Power ( %) Attrs

        clock_network
        3.917e-04
        0.0000
        0.0000
        3.917e-04
        (73.50%)

        register
        1.201e-06
        2.463e-07
        5.033e-07
        1.951e-06
        (0.37%)

        combinational
        5.794e-06
        5.869e-06
        4.760e-07
        1.214e-05
        (2.28%)

        sequential
        0.0000
        0.0000
        0.0000
        0.0000
        (0.0000)
        (0.0000)

        memory
        0.0000
        0.0000
        0.0000
        0.0000
        0.0000
        (0.0000)

        io_pad
        7.705e-05
        4.704e-05
        3.048e-06
        1.271e-04
        (23.86%)

        black_box
        0.0000
        0.0000
        0.0000
        0.0000
        0.0000

                                                                                                 0.0000 0.0000 3.917e-04 (73.50%) i
      Net Switching Power = 5.315e-05 (9.97%)
Cell Internal Power = 4.757e-04 (89.27%)
Cell Leakage Power = 4.027e-06 (0.76%)
Total Power
                                                        = 5.329e-04 (100.00%)
```

5. DFT 驗證與分析:

DFT Coverage

Uncollapsed Stuck Fault Summary Report							
fault class	code	#faults					
Detected Possibly detected Undetectable ATPG untestable Not detected	DT PT UD AU ND	35359 7 29 15 0					
total faults test coverage		35410 99.95%					
Pattern Summary Report							
#internal patterns #basic_scan patterns		1255 1255					
	- 25 (k J)	2500 (LAD42					

Area/Power before inserting DFT

Area:

```
area.log
    2 *********************
    3 Report : area
4 Design : CHIP
    5 Version: P-2019.03-SP1-1
    6 Date
                        : Mon Jun 16 16:49:10 2025
    7 **************
    9 Library(s) Used:
  10
                  N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/II
N16ADFP_StdI0ss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package/Collateral:
  12
  13
  14 Number of ports:
15 Number of nets:
16 Number of cells:
                                                                                                                        56
                                                                                                                   4060
                                                                                                                   4000
   17 Number of combinational cells:
                                                                                                                   3302
  17 Number of combinational cells:
18 Number of sequential cells:
19 Number of macros/black boxes:
20 Number of buf/inv:
21 Number of references:
                                                                                                                     679
                                                                                                                        14
                                                                                                                   1117
  23 Combinational area:
                                                                                                 1283.091861
  24 Buf/Inv area:
25 Noncombinational area:
                                                                                                   635.610239
774.593308
  26 Macro/Black Box area:
                                                                                              23102.004639
  27 Net Interconnect area:
                                                                                undefined (Wire load has zero net area)
  29 Total cell area:
                                                                                              25159.689808
                                                                                 undefined
  30 Total area:
 31 1
Power:
Loading db file '/usr/cad/CBDK/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIo/NLDM/N16ADFP_StdIossOp72v1p62v125c.db' Loading db file '/usr/cad/CBDK/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/N16ADFP_StdCellssOp72vm4Oc.db' Information: Propagating switching activity (low effort zero delay simulation). (PWR-6) Warning: Design has unannotated primary inputs. (PWR-415)

Warning: Design has unannotated sequential cell outputs. (PWR-415)
 ***********
Report: power
-analysis_effort low
Design: CHIP
Version: P-2019.03-SP1-1
Date: Mon Jun 16 16:49:14 2025
Library(s) Used:
      N16ADFP_StdCellssOp72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/N16ADFP_StdCellssOp72vm40c.db)
N16ADFP_StdIOssOp72vlp62vl25c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM/N16ADFP_StdIOssOp72vlp62vl25c.db)
Operating Conditions: ss0p72vm40c Library: N16ADFP_StdCe11ss0p72vm40c Wire Load Model Mode: segmented
Design Wire Load Model
                     ZeroWireload
ZeroWireload
) ZeroWireload
ZeroWireload
                                                             N16ADFP_StdCellss0p72vm40c
N16ADFP_StdCellss0p72vm40c
N16ADFP_StdCellss0p72vm40c
N16ADFP_StdCellss0p72vm40c
top
top_DW01_inc_0
top_DW01_inc_1
Global Operating Voltage = 0.72
Power-specific unit information :
Voltage Units = IV
Capacitance Units = 1.000000pf
Time Units = Ins
Dynamic Power Units = ImW
Leakage Power Units = InW
   Cell Internal Power = 504.4058 uW (88%)
Net Switching Power = 69.0963 uW (12%)
Total Dynamic Power = 573.5021 uW (100%)
Cell Leakage Power = 4.0422 uW
                         Internal
Power
0.1033
0.0000
0.0000
0.0000
0.3941
0.0000
0.0000
                                                  Switching
Power
5.5631e-02
                                                                             Leakage
Power
3.1768e+03
Power Group
                                                                                                                        ( % ) Attrs
                                                                                                              0.1621
0.0000
0.0000
0.0000
io_pad
                                                                                                                             28.06%)
0.00%)
0.00%)
0.00%)

        io_pad
        0.1033

        memory
        0.0000

        black_box
        0.0000

        clock_network
        0.0000

        register
        0.3941

        sequential
        0.0000

        combinational
        7.0098e-03

                                                 0.0000
0.0000
0.0000
3.2542e-04
                                                                              0.0000
0.0000
0.0000
419.7646
                                                                                                              0.3949 \\ 0.0000
                                                  0.0000
1.3140e-02
                                                                                0.0000
445.6599
                                                                                                        2.0596e-02
                                                                                                  0.5775 mW
Total 0.5044 mW
                                                 6.9096e-02 mW
                                                                            4.0422e+03 nW
```

Area:

```
area.log
 1
 2 ********************
3 Report : area
4 Design : CHIP
 5 Version: P-2019.03-SP1-1
 6 Date : Mon Jun 16 16:53:01 2025
 7 **************
9 Information: Updating design information... (UID-85)
10 Library(s) Used:
11
       N16ADFP_StdCellss0p72vm40c (File: /usr/cad/CBDK/Executable_Package/(N16ADFP_StdIOss0p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package)
12
13
14
15 Number of ports:
16 Number of nets:
                                                      66
                                                    4927
17 Number of cells:
                                                    4858
18 Number of combinational cells:
19 Number of sequential cells:
                                                    4160
                                                     679
20 Number of macros/black boxes:
                                                      14
21 Number of buf/inv:
22 Number of references:
                                                    2619
24 Combinational area:
                                           2020.930578
25 Buf/Inv area:
                                           1423.059843
26 Noncombinational area:
                                             915.183327
27 Macro/Black Box area:
                                          23102.004639
28 Net Interconnect area:
                                    undefined (Wire load has zero net area)
30 Total cell area:
                                          26038.118544
                                    undefined
31 Total area:
```

Power:

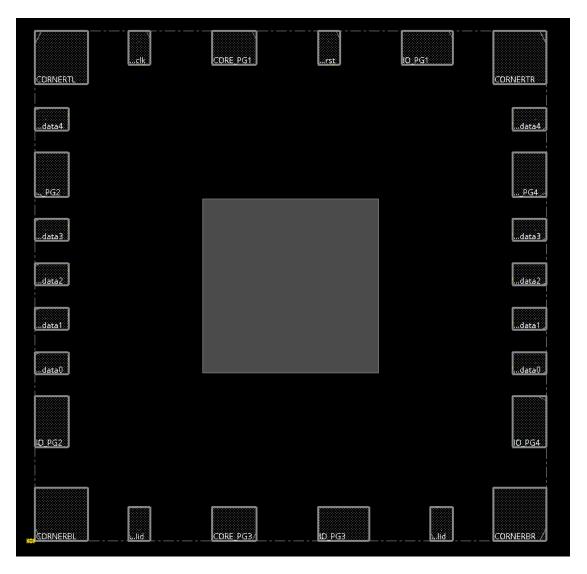
```
N16ADFP_StdCellss@p72vm4@c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/N16ADFP_StdCellss@p72vm4@c.db)
N16ADFP_StdIOss@p72v1p62v125c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM/N16ADFP_StdIOss@p72v1p62v125c.db)
 Operating Conditions: ss0p72vm40c Library: N16ADFP_StdCellss0p72vm40c
Wire Load Model Mode: segmented
 Design Wire Load Model
                                                                                       Library
CHIP
top_test_1
top_DW01_inc_0
top_DW01_inc_1
                                               ZeroWireload
ZeroWireload
ZeroWireload
ZeroWireload
                                                                                       N16ADFP_StdCellss0p72vm40c
N16ADFP_StdCellss0p72vm40c
N16ADFP_StdCellss0p72vm40c
N16ADFP_StdCellss0p72vm40c
Global Operating Voltage = 0.72
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000pf
Time Units = 1ns
Dynamic Power Units = 1mW
Leakage Power Units = 1nW
    Cell Internal Power = 482.5706 uW (86%)
Net Switching Power = 75.9865 uW (14%)
Total Dynamic Power = 558.5571 uW (100%)
Cell Leakage Power = 3.9787 uW
                                                                     Switching
Power
                                   Internal
Power
                                                                                                              Leakage
Power
                                                                                                                                                          Total
Power
                                                                    5.4254e-02
0.0000
0.0000
0.0000
4.693e-04
0.0000
2.1262e-02
                                                                                                            Power

3.1266e+03
0.0000
0.0000
0.0000
154.8525
0.0000
697.2756
io_pad 3.4391e-02
memory 0.0000
black_box 0.0000
clock_network 0.0000
register 0.4217
sequential 0.0000
combinational 2.6490e-02
                               3.4391e-02
0.0000
                                                                                                                                                  9.1772e-02 ( 16.31%)
0.0000 ( 0.00%)
0.0000 ( 0.00%)
0.0000 ( 0.00%)
0.4223 ( 75.07%)
0.0000 ( 0.00%)
4.8450e-02 ( 8.61%)
                                      0.4826 mW 7.5986e-02 mW 3.9787e+03 nW
                                                                                                                                                          0.5625 mW
```

6. APR 實作演練與 LVS 成果:

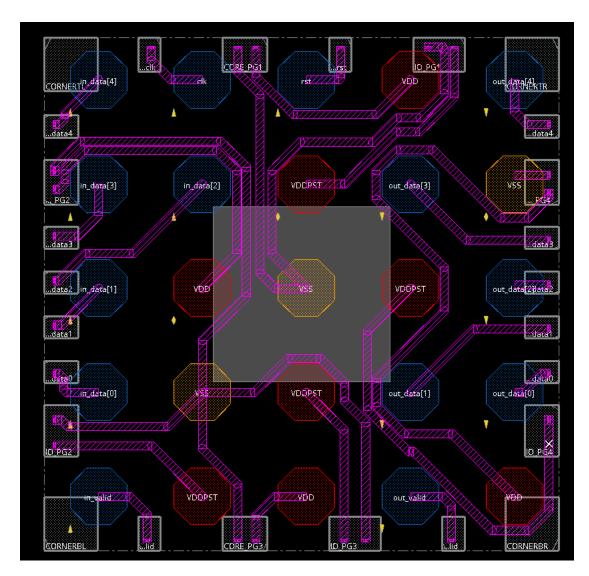
Floorplan

要先擺 IO 然後對齊 FinGrid,並且先看看這樣的擺法以及晶片大小 IO 能不能藉由 bump 出去

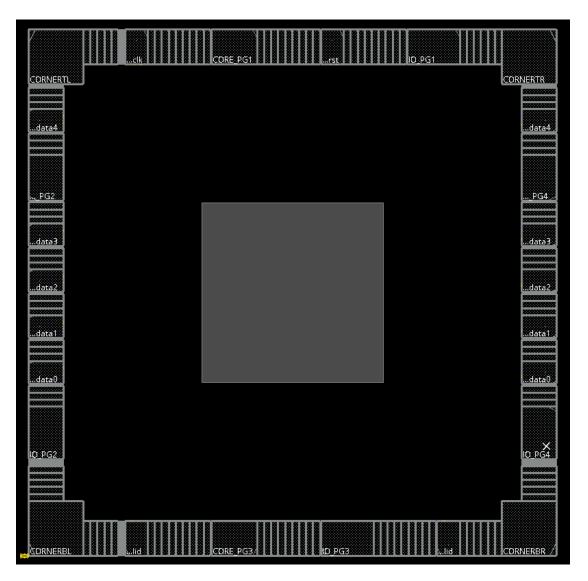


有確認 flip chip 可以擺上去並且繞線可以 RDL 繞線成功,原本我的版本為了求過,所以把晶片面積條大到 6*6 的 bumps 才可以繞

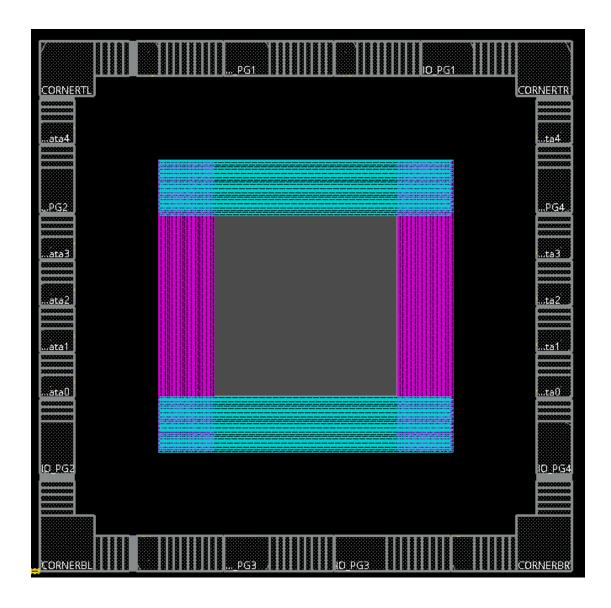
成功,但助教的 script 擺得很好,所以 5*5 的 bumps 就可以成功 繞出來,底下為 RDL 繞線成功結果圖



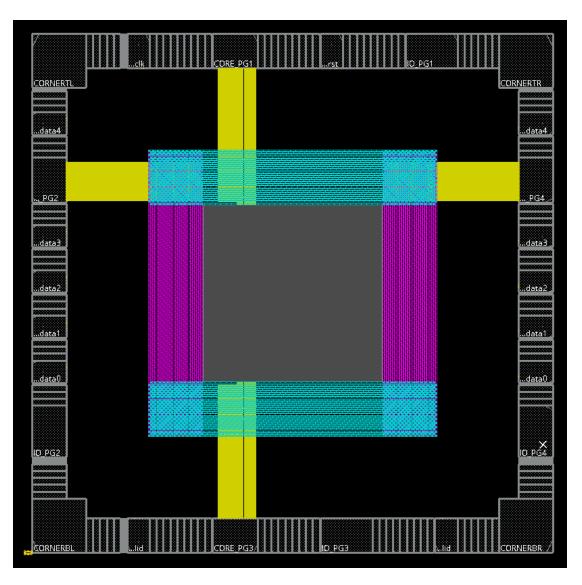
確認可以後再移除,並且最後加上 IO filler,以滿足實體上能夠 製造晶片的規則



之後是開始進行 powerplan,先從 power ring 開始,為了降低 IR,所以會打很多層 metal 以降低電阻,讓外部電壓進來不會有 太多壓降



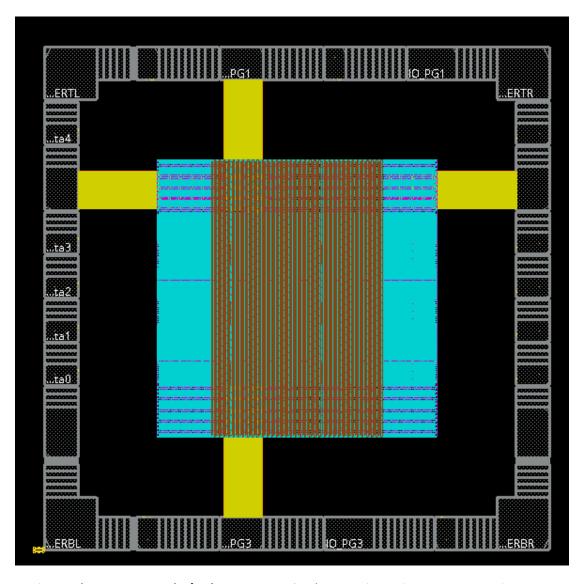
之後是 power pad, 主要是讓剛剛的 power ring 接上 IO pad 來讓 他接到外部電源



之後要初步確認到目前步驟下 DRC 沒有問題

```
VERIFY DRC
                                                                             735 of
736 of
                     Sub-Area:
                                  {163.680 735.072 190.960 758.064}
{190.960 735.072 218.240 758.064}
                                                                                            Thread
                                             735.072 218.240
735.072 245.520
VERTEY DRC
                      Sub-Area:
                                                                                     756
                                                                                            Thread
VERIFY DRC
                                                                             737 of
                     Sub-Area:
                                   {218.240
                                                                 758.064}
                                                                                     756
                                                                                            Thread
                                             735.072 272.800
                                                                 758.064}
VERIFY DRC
                     Sub-Area:
                                   {245.520
                                                                             738
                                                                                 of
                                                                                     756
                                                                                            Thread
                                                                 758.064}
758.064}
                                             735.072 300.080
                                                                                 of
VERIFY DRC
                      Sub-Area:
                                   {272.800
                                                                             739
                                                                                     756
                                                                                            Thread
VERIFY DRC
                      Sub-Area:
                                   {300.080
                                             735.072
                                                       327.360
                                                                             740
                                                                                 of
                                                                                            Thread
                                                                 758.064}
758.064}
VERIFY DRC
                                             735.072
                                                                             741 of
                     Sub-Area:
                                   {327.360
                                                       354.640
                                                                                     756
                                                                                            Thread
VERIFY DRC
                                             735.072
                                                                                 of
                     Sub-Area:
                                   {354.640
                                                       381.920
                                                                             742
                                                                                     756
                                                                                            Thread
                                                                 758.064}
758.064}
                                                                             743 of
VERIFY DRC
                                   {381.920
                                             735.072 409.200
                     Sub-Area:
                                                                                     756
                                                                                            Thread
                                                                             744 of
745 of
VERIFY DRC
                      Sub-Area:
                                   {409.200
                                             735.072 436.480
                                                                                            Thread
                                             735.072 463.760
735.072 491.040
                                                                 758.064}
758.064}
VERIFY DRC
                     Sub-Area:
                                   {436.480
                                                                                     756
                                                                                            Thread
VERIFY DRC
                                                                             746 of
747 of
                     Sub-Area:
                                   {463.760
                                                                                            Thread
                                                                 758.064}
758.064}
VERIFY DRC
                     Sub-Area:
                                   {491.040
                                             735.072 518.320
                                                                                     756
                                                                                            Thread
                                             735.072 545.600
735.072 572.880
735.072 600.160
                     Sub-Area:
VERIFY DRC
                                   {518.320
                                                                             748
                                                                                 of
                                                                                            Thread
                                                                 758.064}
758.064}
VERIFY DRC
                                   {545.600
                                                                             749 of
                                                                                     756
                     Sub-Area:
                                                                                            Thread
                                                                             750 of
751 of
VERIFY DRC
                     Sub-Area:
                                   {572.880
                                                                                            Thread
                                                                 758.064}
758.064}
VERIFY DRC
                     Sub-Area:
                                   {600.160
                                             735.072 627.440
                                                                                            Thread
                                  {627.440
{654.720
                                             735.072 654.720
735.072 682.000
735.072 709.280
VERIFY DRC
                     Sub-Area:
                                                                                 of
                                                                                            Thread
VERIFY DRC
                                                                 758.064}
758.064}
                                                                             753 of
                                                                                     756
                     Sub-Area:
                                                                                            Thread
                                                                             754 of
755 of
VERIFY DRC
                     Sub-Area:
                                   {682.000
                                                                                            Thread
                                                                 758.064}
758.064}
VERIFY DRC
                     Sub-Area:
                                   {709.280
                                             735.072
                                                       736.560
                                                                                            Thread
                                  {736.560
{218.240
VERIFY DRC
                     Sub-Area:
                                              735.072
                                                       761.580
                                                                             756
                                                                                            Thread
                                             197.904
565.440
                                                                                     756
VERIFY DRC
                     Sub-Area:
                                                       245.520
                                                                 226.176}
                                                                             205 of
                                                                                            Thread
                                                                 593.712
VERIFY DRC
                     Sub-Area:
                                   {218.240
                                                       245.520
                                                                             569
                                                                                 of
                                                                                            Thread
                                  {572.880
{190.960
                                                                 226.176]
621.984]
VERIFY DRC
                     Sub-Area:
                                             197.904 600.160
                                                                                            Thread
VERIFY DRC
                     Sub-Area:
                                              593.712
                                                       218.240
                                                                             596
                                                                                            Thread
                                                       245.520 621.984
272.800 621.984
VERIFY DRC
                     Sub-Area:
                                   {218.240
                                             593.712
                                                                             597
                                                                                     756
VERIFY DRC
                     Sub-Area:
                                   {245.520
                                             593.712
                                                                             598
                                                                                 of
                                                                                            Thread
                                                                 593.712
621.984
VERIFY DRC
                     Sub-Area:
                                   {572.880
                                             565.440 600.160
                                                                             582 of
VERIFY DRC
                     Sub-Area:
                                   {572.880
                                             593.712
                                                       600.160
                                                                             610
                                                                                 of
                                                                                            Thread
VERIFY DRC
                     Sub-Area:
                                   {600.160
                                             593.712
                                                       627.440 621.984}
VERIFY DRC
                     Sub-Area:
                                   {518.320
                                              197.904
                                                       545.600
                                                                 226.176
                                                                            216
                                                                                 of
                                                                                            Thread
             ..... Sub-Area:
VERIFY DRC
                                   {190.960
                                             226.176
                                                       218.240
                                                                 254.448}
VERIFY DRC
                     Sub-Area:
                                   {518.320
                                             565.440
                                                       545.600
                                                                 593.712
                                                                             580
                                                                                 of
                                                                                            Thread
                                                                 621.984
621.984
VERIFY DRC
             ..... Sub-Area:
                                   {491.040
                                             593.712
                                                       518.320
                                                                             607 of
                                                                                            Thread
VERIFY DRC
              ..... Sub-Area:
                                   {545.600
                                             593.712
                                                       572.880
                                                                             609
                                                                                 of
                                                                                            Thread
             ..... Sub-Area:
                                                                 621.984
VERIFY DRC
                                   {518.320
                                             593.712
                                                       545.600
                                                                                            Thread
VERIFY DRC
                     Sub-Area:
                                   {163.680
                                             537.168
                                                       190.960
                                                                 565.440
                                                                             539
                                                                                 of
                                                                                            Thread
                                                                 197.904]
565.440]
VERIFY DRC
             ..... Sub-Area:
                                   {190.960
                                             169.632
                                                       218.240
                                                                                            Thread
VERIFY DRC
              ...... Sub-Area:
                                             537.168
                                                       600.160
                                                                             554
                                   {572.880
                                                                                 of
                                                                                            Thread
             ..... Sub-Area:
VERIFY DRC
                                   {600.160 565.440
                                                       627.440
                                                                 593.712
                                                                             583
                                                                                 of
                                                                                            Thread
                     Sub-Area: {248.240 537.168 245.520 Sub-Area: {245.520 565.440 272.800 Sub-Area: {518.320 537.168 545.600 Sub-Area: {190.960 537.168 218.240 Sub-Area: {545.600 537.168 572.880
VERIFY DRC
                                                                 565.440
                                                                             541 of
                                                                                            Thread
VERIFY DRC
             ..... Sub-Area:
                                                                 593.712}
                                                                             570
                                                                                 of
                                                                                            Thread
VERIFY DRC
              ..... Sub-Area:
                                                                 565.440}
                                                                                 of
                                                                                     756
                                                                                            Thread
             ..... Sub-Area:
VERIFY DRC
                                                                 565.440}
                                                                                 of
                                                                                            Thread
VERIFY DRC
                                                                 565.440}
                                                                            553
                                                                                            Thread
                     Thread : 2 finished
Thread : 7 finished
VERIFY DRC
VERIFY DRC
                      Sub-Area: {190.960 565.440 218.240 593.712} 568 of 756
VERIFY DRC
                                                                                            Thread: 3
                     Thread : 3 finished.
Sub-Area: {545.600 565.440 572.880 593.712} 581 of 756
VERIFY DRC
VERIFY DRC
                                                                                            Thread: 6
VERIFY DRC ..... Thread : 6 finished.
 Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:55.1 ELAPSED TIME: 11.00 MEM: 312.6M) ***
```

接著是 powerstripe, 這部是讓剛剛從外部接到 powerring 的店員 在給晶片內部



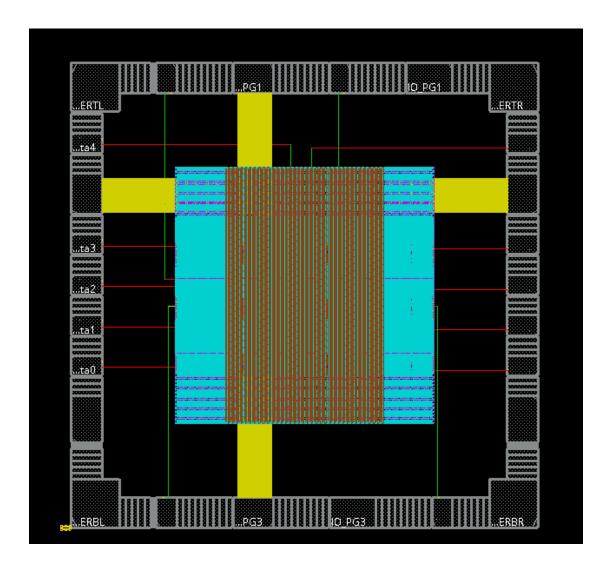
這個之後要經過一連串修 DRC 的動作,但都助教給好的 script, 我放結果

```
{682.000
                                                                           754 of
 VERIFY DRC
                                             735.072 709.280
                                                                758.064}
                                                                                    756
                      Sub-Area:
                                                                                          Thread
                                                       761.580
                                                                                    756
 VERIFY DRC
                      Sub-Area:
                                   {736.560
                                             735.072
                                                                 758.064}
                                                                                          Thread
                                   218.240
                                             508.896 245.520
                                                                537.168}
 VERIFY DRC
                      Sub-Area:
                                                                                    756
                                                                                          Thread
 VERIFY DRC
                                   {491.040
                                             537.168
                                                      518.320
                                                                565.440}
                      Sub-Area:
                                                                                          Thread
 VERIFY DRC
                                   {245.520
                                             480.624
                                                      272.800
                                                                508.896}
                      Sub-Area:
                                                                                          Thread
                                   {463.760
                                                                593.712}
593.712}
 VERIFY DRC
                                             565.440 491.040
                                                                                of
                      Sub-Area:
                                                                                    756
                                                                                          Thread
                                             565.440 245.520
 VERIFY DRC
                                   218.240
                      Sub-Area:
                                                                                    756
                                                                                          Thread
 VERIFY DRC
                                   [190.960
                                             593.712
                                                      218.240
                                                                621.984}
                                                                           596
                                                                                of
                                                                                    756
                      Sub-Area:
                                                                                          Thread
 VERIFY DRC
                                   245.520
                                             593.712 272.800
                      Sub-Area:
                                                                621.984}
                                                                           598
                                                                                          Thread
                                                                621.984}
508.896}
 VERIFY DRC
                                   {218.240
                                             593.712 245.520
                                                                                of
                                                                                    756
                      Sub-Area:
                                                                           597
                                                                                          Thread
                                                                                                     Θ
 VERIFY DRC
                                   {190.960 480.624 218.240
                      Sub-Area:
                                                                           484
                                                                                    756
                                                                                          Thread
 VERIFY DRC
                                                                565.440}
                                                                           543
                                                                                of
                      Sub-Area:
                                   {272.800 537.168 300.080
                                                                                    756
                                                                                          Thread
 VERIFY DRC
                                   {491.040
                                             565.440
                                                                593.712]
                      Sub-Area:
                                                      518.320
                                                                           579
                                                                                    756
                                                                                          Thread
VERIFY DRC
VERIFY DRC
                                   {545.600
                                             537.168 572.880
537.168 190.960
                                                                565.440}
565.440}
                                                                                    756
                      Sub-Area:
                                                                                          Thread
                                   {163.680
                                                                           539
                      Sub-Area:
                                                                                    756
                                                                                          Thread
                                             537.168 327.360
565.440 600.160
                                                                565.440}
593.712}
 VERIFY DRC
                      Sub-Area:
                                   {300.080
                                                                                          Thread
                      Sub-Area:
 VERIFY DRC
                                   {572.880
                                                                           582
                                                                                          Thread
                                             565.440 327.360
508.896 600.160
                                                                593.712]
537.168]
 VERIFY DRC
                      Sub-Area:
                                   (300.080
                                             565.440
                                                                                          Thread
                      Sub-Area:
 VERIFY DRC
                                   {572.880
                                                                                          Thread
                                             565.440 545.600
 VERIFY DRC
                                   {518.320
                      Sub-Area:
                                                                593.712}
                                                                                          Thread
 VERIFY DRC
                      Sub-Area:
                                   {218.240
                                             537.168
                                                      245.520
                                                                565.440}
                                                                           541
                                                                                    756
                                                                                          Thread
                                                                537.168}
593.712}
                                                      545.600
 VERIFY DRC
                      Sub-Area:
                                   {518.320
                                             508.896
                                                                           524
                                                                                    756
                                                                                          Thread
                                   {245.520
 VERIFY DRC
                      Sub-Area:
                                             565.440 272.800
                                                                           570
                                                                                    756
                                                                                of
                                                                                          Thread
                                   {245.520
 VERIFY DRC
                      Sub-Area:
                                             508.896 272.800
                                                                537.168}
                                                                           514
                                                                                of
                                                                                    756
                                                                                          Thread
                                  {572.880 537.168 600.160 {245.520 537.168 272.800
 VERIFY DRC
                                                                565.440}
565.440}
                                                                           554
                                                                                of
                                                                                    756
                      Sub-Area:
                                                                                          Thread
 VERIFY DRC
                      Sub-Area:
                                                                           542
                                                                                of
                                                                                    756
                                                                                          Thread
                      Sub-Area: {190.960 565.440 218.240 593.712}
Sub-Area: {190.960 508.896 218.240 537.168}
Sub-Area: {518.320 537.168 545.600 565.440}
 VERIFY DRC
                                                                           568
                                                                                of
                                                                                    756
                                                                                          Thread
                                                                                                     4
VERIFY DRC
VERIFY DRC
                                                                                of
                                                                           512
                                                                                    756
                                                                                          Thread
                                                                           552
                                                                                          Thread
                      Thread : 3 finished.
Thread : 6 finished.
 VERIFY DRC
 VERIFY DRC
                      Sub-Area: {545.600 565.440 572.880 593.712} 581 of 756
 VERIFY DRC
                                                                                          Thread: 4
                      Thread: 4 finished.
 VERIFY DRC
                      Sub-Area: {190.960 537.168 218.240 565.440} 540 of 756
 VERIFY DRC
                                                                                          Thread: 7
                      Thread: 7 finished.
Sub-Area: {545.600 508.896 572.880 537.168} 525 of 756
 VERIFY DRC
 VERIFY DRC
                                                                                          Thread: 2
 VERIFY DRC
              ..... Thread : 2 finished.
 Verification Complete: 0 Viols.
 *** End Verify DRC (CPU: 0:01:42 ELAPSED TIME: 17.00 MEM: 291.1M) ***
@innovus 47>
```

Placement

Placement 第一步是加 endcap cell,避免切割動作破壞晶片本身,

之後該使擺 cell,底下維結果



Timing Report Before CTS

一開始擺時 place 完,timing 沒 meet

```
time_design Summary
 etup views included:
AV_func_ss0p72v125c AV_func_ss0p72vm40c
        Setup mode
                                           | reg2reg | in2reg
                                                                       | reg2out | in2out
                                                                                                      default
      WNS (ns):| -1.134
TNS (ns):|-497.157
Violating Paths:| 617
All Paths:| 1358
                                                                                                       0.000
0.000
                           Nr nets(terms)
                                                                        Nr nets(terms)
                                                    Worst Vio
                              11 (11)
11 (1960)
0 (0)
0 (0)
                                                                           12 (12)
18 (1967)
1 (1)
0 (0)
Density: 2.138%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 7.46 sec
Total Real time: 5.0 sec
Total Real time: 5.0 sec
Total Memory Usage: 4401.417969 Mbytes
*** time_design #1 [finish] : cpu/real = 0:00:07.3/0:00:04.7 (1.6), totSession cpu/real = 0:10:57.9/0:20:10.9 (0.5), mem = 4401.4M
```

之後下指令 place opt design,來修 timing

```
time_design Summary
Setup views included:
AV_func_ss0p72v125c
                                    all
        Setup mode
                                             | reg2reg | in2reg
                                                                            reg2out |
                                                                                           in2out
                                                                                                         default
                 WNS (ns):|
TNS (ns):|
                                  2.945
0.000
                                                                               N/A
                                                 3.169
                                                               2.945
                                                                                              N/A
                                                                                                           0.000
                                                 0.000
                                                               0.000
                                                                                              N/A
                                                                               N/A
                                                                                                           0.000
       Violating Paths:
All Paths:
                                     Θ
                                                   Θ
                                                                  Θ
                                                                               N/A
                                                                                              N/A
                                                                1336
                                                  679
                                   1358
                                                                               N/A
                                                                                              N/A
                                                                                                              Θ
                                              Real
                                                                                  Total
       DRVs
                             Nr nets(terms)
                                                      Worst Vio
                                                                           Nr nets(terms)
                                  0 (0)
0 (0)
0 (0)
0 (0)
                                                                                0 (0)
7 (7)
0 (0)
0 (0)
                                                          0.000
     max_cap
     max_tran
max_fanout
max_length
                                                          0.000
Density: 2.158%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 1.48 sec
Total Real time: 2.0 sec
Total Memory Usage: 5370.0 Mbytes

*** time_design #2 [finish] : cpu/real = 0:00:01.5/0:00:01.7 (0.9), totSession cpu/real = 0
@innovus 54>
```

CTS X Clock Tree Debugger: DC_si0p72v125c — superdome1 - □ X yew Visibility Color by Help - cā de n.ce - cā

Close

Timing Report After CTS

Setup time:

```
time_design Summary
Setup views included:
  AV_func_ss0p72v125c
         Setup mode
                                        all
                                                                                                                     default
                                                     reg2reg |
                                                                     in2reg
                                                                                     reg2out
                                                                                                      in2out
                    WNS (ns):
                                                       3.170
                                                                       2.944
                                                                                        N/A
                                                                                                        N/A
                                                                                                                       0.000
                                                                                        N/A
N/A
                                                                                                        N/A
N/A
                   TNS (ns):
                                      0.000
                                                       0.000
                                                                       0.000
                                                                                                                       0.000
        Violating Paths:
All Paths:
                                                   Real
                                                                                           Total
        DRVs
                                Nr nets(terms)
                                                          | Worst Vio
                                                                                   Nr nets(terms)
                                      0 (0)
0 (0)
0 (0)
0 (0)
                                                                                         0 (0)
7 (7)
0 (0)
0 (0)
      max cap
                                                                0.000
      max_tran
max_fanout
max_length
                                                                0.000
                                                                   Θ
Density: 2.158%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports

Total CPU time: 3.7 sec

Total Real time: 2.0 sec

Total Memory Usage: 5418.328125 Mbytes

*** time_design #3 [finish] : cpu/real = 0:00:03.7/0:00:02.6 (1.4), totSession cpu/real = 0:00:03.7/0:00:02.6 (1.4),
```

Hold time:

```
time_design Summary
Hold views included:
 AV_func_ss0p72v125c AV_func_ss0p72vm40c AV_func_ff0p88v125c
AV_func_ff0p88vm40c
        Hold mode
                                  all
                                             reg2reg | in2reg | reg2out
                                                                                       in2out
                                                                                                     default |
                              -0.308
                                              -0.074
                WNS (ns):|
                                                           -0.308
                                                                            N/A
                                                                                          N/A
                                                                                                      0.000
                TNS (ns): |-215.183
ing Paths: | 1358
                                              -44.757
                                                           -213.876
                                                                            N/A
                                                                                          N/A
                                                                                                      0.000
       Violating Paths:
All Paths:
                                                679
                                                             1336
                                                                                          N/A
                                                                            N/A
                                 1358
                                                679
                                                             1336
                                                                                          N/A
                                                                                                         0
Density: 2.151%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 5.6 sec
Total Real time: 2.0 sec
Total Memory Usage: 6585.085938 Mbytes
*** time_design #6 [finish] : cpu/real = 0:00:05.6/0:00:02.0 (2.8), totSession cpu/real :
@innovus 62>
```

```
Design Name: CHIP
Design Mode: 16nm
Analysis Mode: MMMC OCV
Parasitics Mode: No SPEF/RCDB
Signoff Settings: SI Off
time_design Summary
Hold views included:
AV_func_ss0p72v125c AV_func_ss0p72vm40c AV_func_ff0p88v125c
AV_func_ff0p88vm40c
                               all | reg2reg |
                                                                                            default |
       Hold mode
                                                      in2reg | reg2out |
                                                                               in2out
      WNS (ns):|
TNS (ns):|
Violating Paths:|
All Paths:|
                              0.000
                                          0.000
                                                       0.002
                                                                     N/A
                                                                                             0.000
                                                                     N/A
N/A
N/A
                                                                                  N/A
N/A
N/A
                              0.000
                                          0.000
                                                       0.000
                                                                                             0.000
                                                                                               Θ
Θ
                              1358
Density: 3.317%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 6.86 sec

Total Real time: 2.0 sec

Total Real time: 2.0 sec

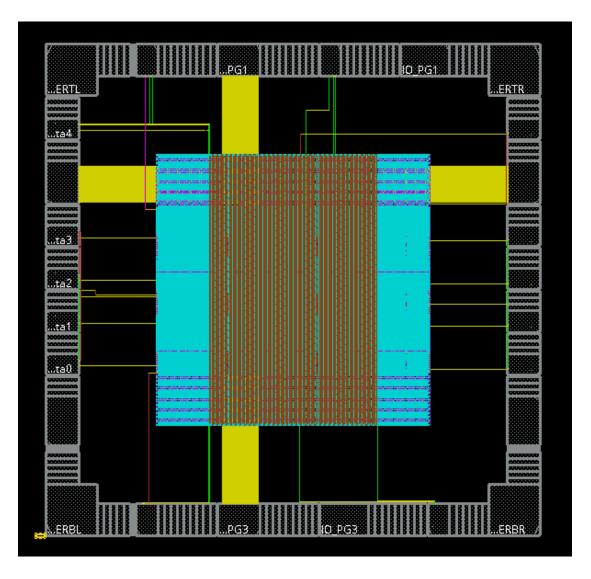
Total Memory Usage: 7099.921875 Mbytes

*** time_design #7 [finish] : cpu/real = 0:00:06.8/0:00:02.3 (3.0), totSession cpu/real = 0:19:37.0/0:30

@innovus 64>
```

Routing

下指令 route design,來繞線,並且要確認 timing,底下為結果



之後就是下一堆指令修 DRC, 結果有成功修好

```
VERIFY DRC
                         Sub-Area:
                                      463.760
                                                 565.440
                                                           491.040
                                                                      593.712
 VERIFY DRC
                         Sub-Area:
                                      436.480
                                                 593.712
                                                            463.760
                                                                      621.984
                                                                                                  Thread
                                                           491.040 621.984}
327.360 593.712}
 VERIFY DRC
                         Sub-Area:
                                      463.760
                                                 593.712
                                                                                                  Thread
 VERIFY DRC
                        Sub-Area:
                                       300.080
                                                 565.440
                                                                                  572
                                                                                                  Thread
                                                            354.640 621.984}
300.080 621.984}
 VERIFY DRC
                         Sub-Area:
                                       [327.360
                                                 593.712
                                                                                  601
                                                                                           756
                                                                                                  Thread
 VERIFY DRC
                         Sub-Area:
                                      272.800
                                                 593.712
                                                                                  599
                                                                                           756
                                                                                                  Thread
                                                 593.712
537.168
                                                            327.360
245.520
                                                                      621.984}
565.440}
 VERIFY DRC
                         Sub-Area:
                                      {300.080
                                                                                  600
                                                                                           756
                                                                                                  Thread
 VERIFY
          DRC
                        Sub-Area:
                                      {218.240
                                                                                  541
                                                                                                  Thread
                                      {572.880
{600.160
                                                 537.168
537.168
                                                                      565.440}
565.440}
 VERIFY DRC
                        Sub-Area:
                                                            600.160
                                                                                  554
                                                                                           756
                                                                                                  Thread
 VERIFY DRC
                        Sub-Area:
                                                            627.440
                                                                                  555
                                                                                       of
                                                                                           756
                                                                                                  Thread
                                                 508.896
537.168
                                                                      537.168}
565.440}
 VERIFY DRC
                        Sub-Area:
                                      {518.320
                                                            545.600
                                                                                  524 of
                                                                                           756
                                                                                                  Thread
 VERIFY DRC
                        Sub-Area:
                                      {300.080
                                                            327.360
                                                                                  544 of
                                                                                                  Thread
                                                 565.440
                                                                      593.712}
621.984}
                                                                                  580 of
                                                                                           756
 VERIFY DRC
                        Sub-Area:
                                      {518.320
                                                           545.600
                                                                                                  Thread
                                                 593.712
593.712
                                                           518.320
545.600
 VERIFY DRC
                        Sub-Area:
                                      {491.040
                                                                                  607 of
                                                                                                  Thread
                                      {518.320
{545.600
                                                                      621.984}
508.896}
                                                                                  608 of
 VERIFY DRC
                                                                                           756
                        Sub-Area:
                                                                                                  Thread
                                                                                  497 of
582 of
 VERIFY DRC
                                                            572.880
                        Sub-Area:
                                                 480.624
                                                                                                  Thread
                                     {572.880
{600.160
 VERIFY DRC
VERIFY DRC
                                                 565.440 600.160
565.440 627.440
                                                                      593.712}
593.712}
                                                                                           756
                        Sub-Area:
                                                                                                  Thread
                                                                                  583 of
                                                                                           756
                        Sub-Area:
                                                                                                  Thread
                                                           190.960
245.520
518.320
                                      {163.680 537.168
{218.240 565.440
                                                                                  539 of
 VERIFY DRC
                                                                                           756
                        Sub-Area:
                                                                      565.440}
                                                                                                  Thread
                                                                                  569 of
551 of
570 of
 VERIFY DRC
                                     {218.240
{491.040
{245.520
                                                                      593.712}
565.440}
                        Sub-Area:
                                                                                           756
                                                                                                  Thread
                                     {491.040 537.168 518.320
{245.520 565.440 272.800
{491.040 565.440 518.320
{218.240 508.896 245.520
 VERIFY DRC
VERIFY DRC
VERIFY DRC
                                                                                           756
                                                                                                  Thread
                        Sub-Area:
                                                                                           756
756
                                                                      593.712
                        Sub-Area:
                                                                                                  Thread
              593.712
                                                                                  579 of
                                                                                                  Thread
                        Sub-Area:
 VERIFY DRC
                                                                                                  Thread
 VERIFY DRC
VERIFY DRC
VERIFY DRC
VERIFY DRC
                                                                                                  Thread
                                                                                                  Thread
                                                                                                  Thread
                                                                                                  Thread
 VERIFY DRC
VERIFY DRC
VERIFY DRC
VERIFY DRC
                                                                                                  Thread
                                                                                                              Θ
                                                                                                  Thread
                                                                                                  Thread
                                                                                                             Θ
                                                                                                 Thread: 7
 VERIFY DRC
 VERIFY DRC
 VERIFY DRC
                                                                                                 Thread: 0
 VERIFY DRC
  Verification Complete: 0 Viols.
 *** End Verify DRC (CPU: 0:01:43 ELAPSED TIME: 17.00 MEM: 464.1M) ***
@innovus 82>
```

Timing Report After Routing

Set up time:

```
Setup views included:
 AV_func_ss0p72v125c
        Setup mode
                                  all
                                             reg2reg |
                                                           in2reg |
                                                                        reg2out |
                                                                                      in2out
                                                                                                   default
                WNS (ns):|
TNS (ns):|
                                                                           N/A
N/A
N/A
                                                                                        N/A
N/A
N/A
                                 1.970
                                              2.715
                                                            1.970
                                                                                                     0.000
                                 0.000
                                              0.000
                                                            0.000
                                                                                                     0.000
       Violating Paths:
All Paths:
                                   Θ
                                                               0
                                                679
                                                            1336
                                 1358
                                                                           N/A
                                                                                        N/A
                                                                                                       0
                                                                              Total
                                           Real
      DRVs
                           Nr nets(terms)
                                                 | Worst Vio
                                                                      Nr nets(terms)
                                7 (7)
0 (0)
0 (0)
0 (0)
                                                                            7 (7)
7 (7)
0 (0)
                                                       -0.025
     max_cap
     max_tran
max_fanout
max_length
                                                      0.000
                                                                            0 (0)
                                                         Θ
Density: 3.321%
Reported timing to dir timingReports
Total CPU time: 30.53 sec
Total Real time: 15.0 sec
Total Memory Usage: 8483.5 Mbytes
Reset AAE Options
*** time_design #8 [finish] : cpu/real = 0:00:30.5/0:00:15.5 (2.0), totSession cpu/real
@innovus 70>
```

一開始沒過後來下指令,opt_design -post_route -setup -hold,就把 set up/hold time 都修好

```
time_design Summary
Setup views included:
 AV_func_ss0p72v125c
                                  all
                                                           in2reg
                                                                                                    default
        Setup mode
                                             reg2reg
                                                                        reg2out
                                                                                       in2out
                WNS (ns):|
TNS (ns):|
                                 2.419
                                                                           N/A
N/A
                                                                                         N/A
N/A
N/A
                                               2.704
                                                            2.419
                                                                                                      0.000
                                 0.000
                                               0.000
                                                            0.000
                                                                                                      0.000
       Violating Paths:
All Paths:
                                                0
679
                                 1358
                                                            1336
                                                                                         N/A
                                                                                                        Θ
                                            Real
                                                                              Total
       DRVs
                                                    Worst Vio
                           Nr nets(terms)
                                                                       Nr nets(terms)
                                0 (0)
0 (0)
0 (0)
0 (0)
                                                                            0 (0)
7 (7)
0 (0)
0 (0)
     max_cap
                                                       0.000
     max_tran
max_fanout
max_length
                                                       0.000
                                                         0
                                                         Θ
Density: 3.336%
Reported timing to dir timingReports
Total CPU time: 1.97 sec
Total Real time: 2.0 sec
Total Memory Usage: 9428.070312 Mbytes
Reset AAE Options
*** time design #10 [finish] : cpu/real = 0:00:02.0/0:00:01.9 (1.0), totSession cpu/real = 0:30:
@innovus 73>
@innovus 73>
```

Hold time:

```
time_design Summary

Hold views included:
AV func ss0p72v125c AV_func_ss0p72vm40c AV_func_ff0p88v125c
AV_func_ff0p88vm40c

Hold mode | all | reg2reg | in2reg | reg2out | in2out | default |

WNS (ns): | -0.003 | -0.003 | 0.376 | N/A | N/A | 0.000 |

TNS (ns): | -0.010 | -0.010 | 0.000 | N/A | N/A | 0.000 |

Violating Paths: | 8 | 8 | 0 | N/A | N/A | 0 |

All Paths: | 1358 | 679 | 1336 | N/A | N/A | 0 |

Density: 3.321%

Reported timing to dir timingReports
Total CPU time: 11.49 sec
Total Real time: 4.0 sec
Total Real time: 4.0 sec
Total Memory Usage: 8524.679688 Mbytes
Reset AAE Options
*** time design #9 [finish] : cpu/real = 0:00:11.5/0:00:03.7 (3.1), totSession cpu/real = 0:27:40.1/0:45:15.9 (0.6), mem = 8524.7M @innovus 71>
```

一開始沒過後來下指令,opt_design -post_route -setup -hold,就把 set up/hold time 都修好

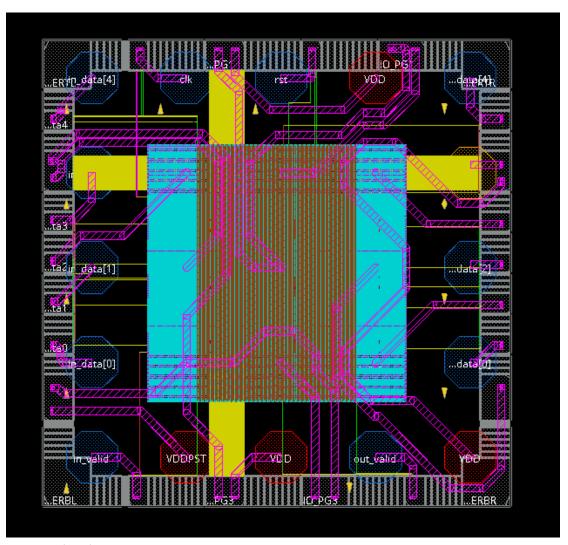
```
time_design Summary
Hold views included:
AV_func_ss0p72v125c AV_func_ss0p72vm40c AV_func_ff0p88v125c
AV_func_ff0p88vm40c
        Hold mode
                                    all
                                             | reg2reg | in2reg
                                                                                           in2out
                                                                                                        | default
                 WNS (ns):|
TNS (ns):|
                                 -0.000
                                                -0.000
                                                                0.003
                                                                                N/A
                                                                                                          -0.000
                                                                                N/A
N/A
                                                                                              N/A
N/A
                                 -0.000
                                                 0.000
                                                                0.000
                                                                                                           0.000
       Violating Paths:
All Paths:
                                  1358
                                                  679
                                                                1336
                                                                                N/A
                                                                                                              0
Density: 3.336%
Reported timing to dir timingReports
Total CPU time: 10.83 sec
Total Real time: 4.0 sec
Total Memory Usage: 10439.5 Mbytes
Reset AAE Options
*** time_design #13 [finish] : cpu/real = 0:00:10.8/0:00:03.8 (2.9), totSession cpu/real = 0
@innovus 77> |
```

Create Bump

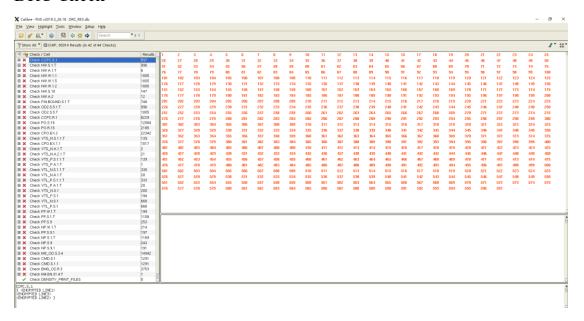
之後就照前面 floorplan 試擺過的 bump 擺法再擺回去

RDL Routing

之後就照前面 floorplan 試繞過的 RDL 繞法讓 tool 再繞一次



DRC Check



錯一狗票不知為啥,但剛剛繞完再 innovous 明明是 0 個,但開

calibre 出現一狗票,底下是 innovous 上的

```
VERIFY DRC
VERIFY DRC
VERIFY DRC
                                                                 {354.640 735.072 381.920 758.064}
{245.520 735.072 272.800 758.064}
{381.920 735.072 409.200 758.064}
                                                                                                                                            742 of 756
738 of 756
743 of 756
739 of 756
746 of 756
747 of 756
747 of 756
750 of 756
751 of 756
752 of 756
753 of 756
754 of 756
754 of 756
755 of 756
754 of 756
754 of 756
524 of 756
523 of 756
524 of 756
523 of 756
524 of 756
523 of 756
524 of 756
527 of 756
529 of 756
                                          Sub-Area:
                                                                                                                                                                                            0
                                          Sub-Area:
                                                                                                                                                                        Thread
Sub-Area:
                                                                                                                                                                        Thread
                                                                                                                                                                                            3
                                                                 272.800 735.072 300.080
{463.760 735.072 491.040
{409.200 735.072 436.480
{491.040 735.072 518.320
{436.480 735.072 463.760
  VERIFY DRC
VERIFY DRC
                                                                                                                        758.064}
758.064}
                                          Sub-Area:
                                                                                                                                                                        Thread
                          ..... Sub-Area:
     Verification Complete: 0 Viols.
   *** End Verify DRC (CPU: 0:01:45 ELAPSED TIME: 18.00 MEM: 419.1M) ***
@innovus 110>
```

LVS Check

LVS 出現了經典笑臉

```
REPORT FILE NAME:
LAYOUT NAME:
SOURCE NAME:
RULE FILE:
CREATION TIME:
CURRENT DIRECTORY:
USER NAME:
CALIBRE VERSION:
                                        output/lvs.rep
layout.spi ('CHIP')
CHIP_inc.spi ('CHIP')
,/scr/runset.cmd
Mon Jun 16 19:14:22 2025
/home/userl/hdlcs25/hdlcs2590/LAB13_FUCK/hw13_Example/pr/verify/lvs
hdlcs2590
v2019.2_26.18 Tue May 7 10:57:04 PDT 2019
                                                 OVERALL COMPARISON RESULTS
                                                    Warning: Ambiguity points were found and resolved arbitrarily.
  CELL SUMMARY
   Result Layout
                          CHIP
   CORRECT
                                                                          CHIP
 LVS PARAMETERS
 o LVS Setup:
    LVS SETUP:

// LVS COMPONENT TYPE PROPERTY
// LVS COMPONENT SUBTYPE PROPERTY
// LVS PIN NAME PROPERTY
// LVS PIN NAME PROPERTY
LVS PROBLEN NAME
LVS GROUND NAME
LVS GROUND NAME
LVS CELL SUPPLY
LVS RECORD NAMES
LVS TIANORE PORTS
LVS TIANORE PORTS
LVS LONGRE PORTS
LVS LONGRE PORTS
LVS LONGRE TRIVIAL NAMED PORTS
LVS BULL TIAN DEVICE PIN SWAP
LVS BULL CAPACITOR PINS SWAPPABLE
LVS DISCARD PINS BY DEVICE
                                                                 "VDD" "VDDPST" "AVDD" "DVDD"

"VSS"
NO
NONE
NO
YES
VS
YES
NO
YES
NO
YES
NO
```

7. 心得分享