2025 Digital IC Design Homework 3

NAME	童品綸
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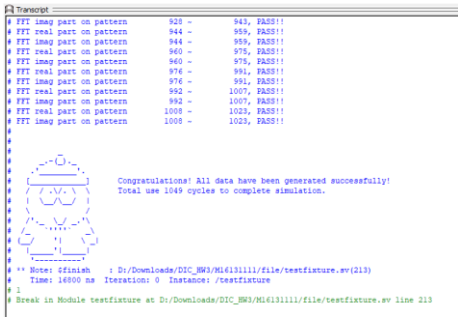
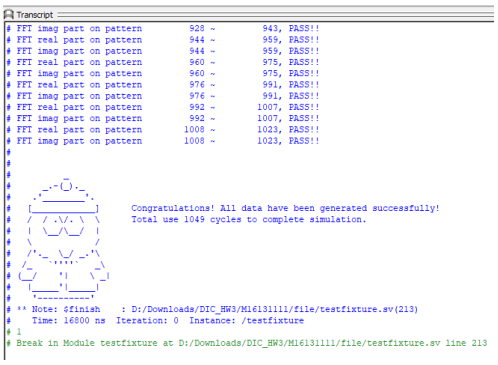
Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass

P1

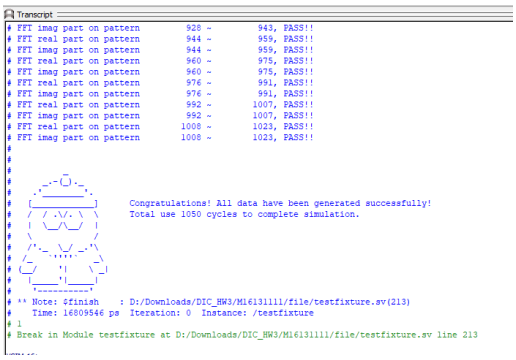


P2

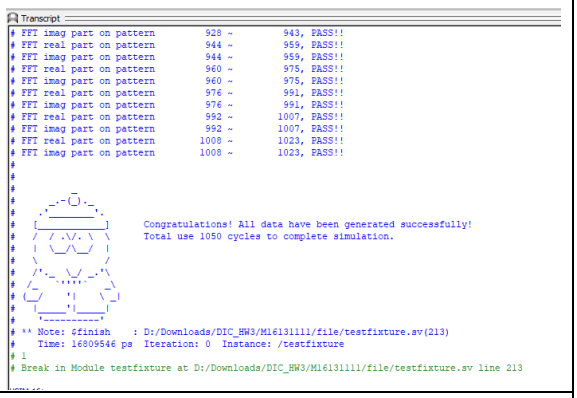


Please specify your clock width:16(ns)

P1

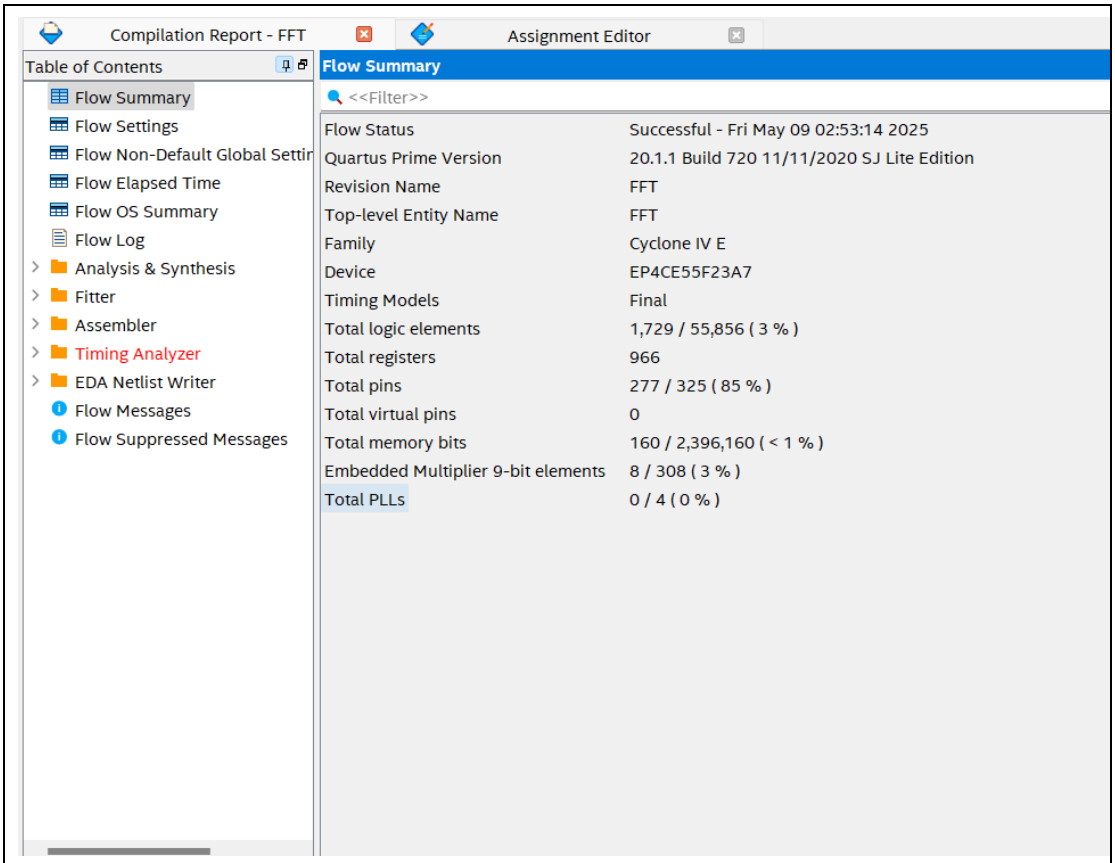


P2



Synthesis Result

Total logic elements	1729
Total memory bits	160
Total registers	966
Embedded multiplier 9-bit elements	8



Description of your design

我的設計主要就是拆 4 個 stage，一個 stage，一個蝴蝶單元來做，然後只有第二個 stage 會用到乘法器，我有自己對 twiddle factor 做化簡，把很多旋轉因子能變成乘負一或正一，然後因為要前一組到，才有辦法用蝴蝶算出下一級輸入，所以上面有移位暫存器，最後出來會做順序重排，以及累積每 16 筆輸出二次(實部跟虛部)，底下有架構圖