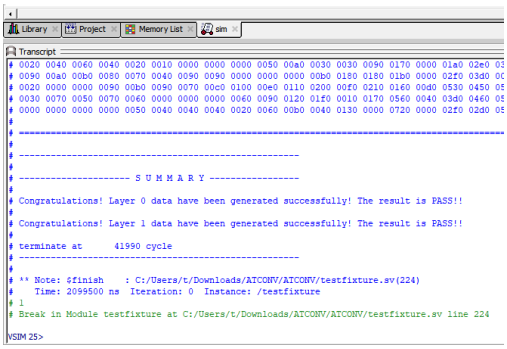
2025 Digital IC Design Homework 4

NAME	童品綸
Student ID	M16131111

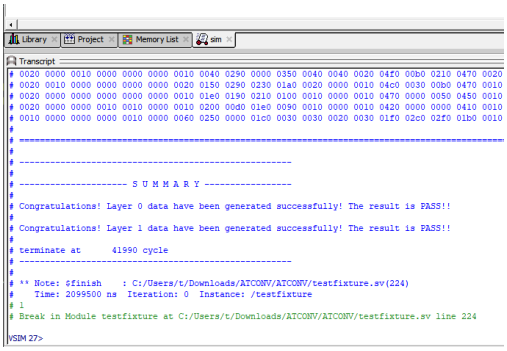
ATCONV Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass

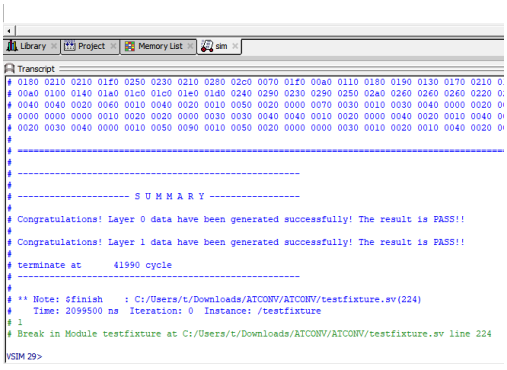
tb1:



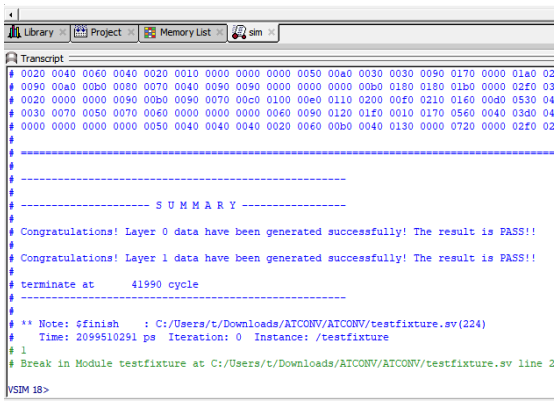
tb2:



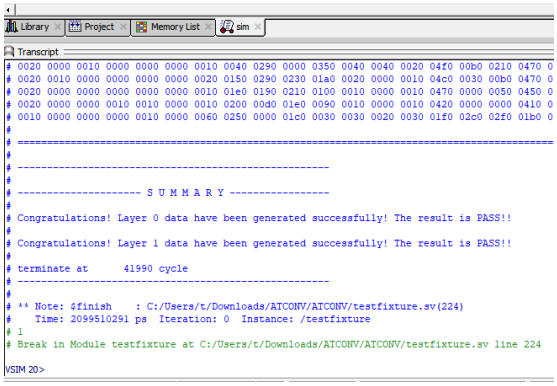
tb3:



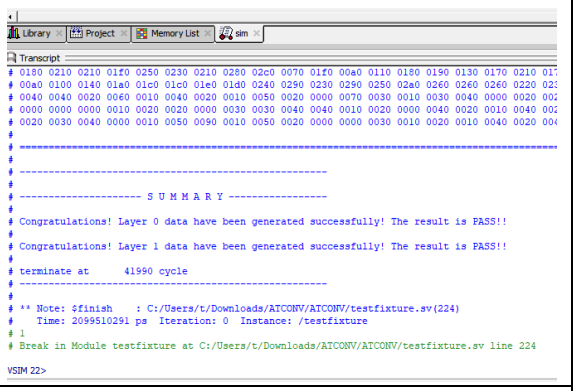
tb1:



tb2:



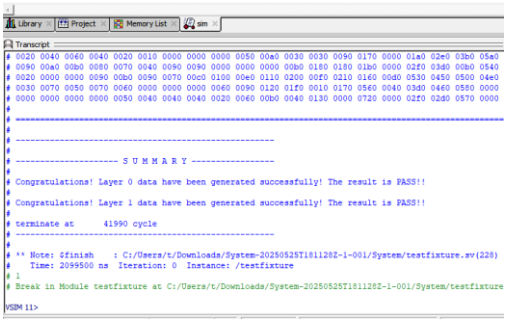
tb3:



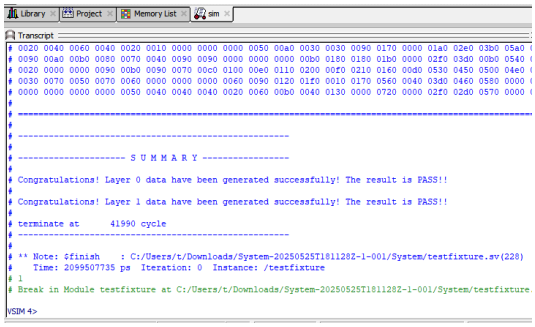
System Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass

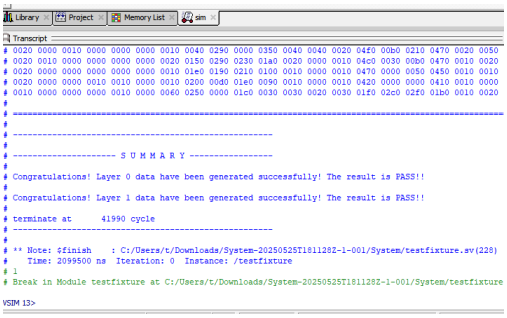
tb1:



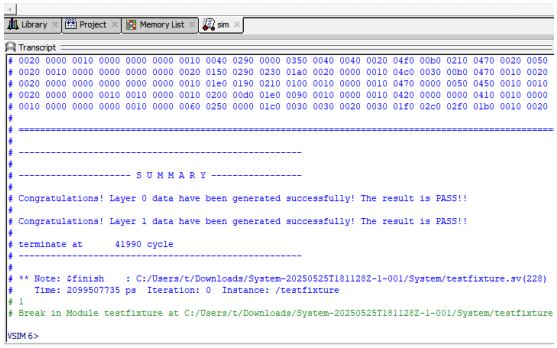
tb1:



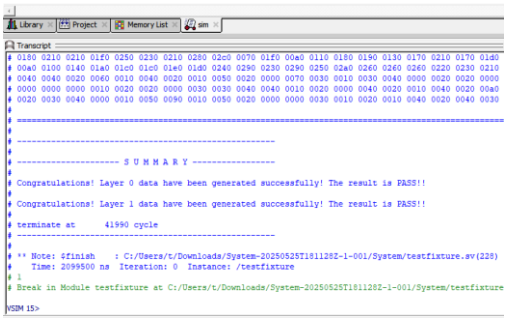
tb2:



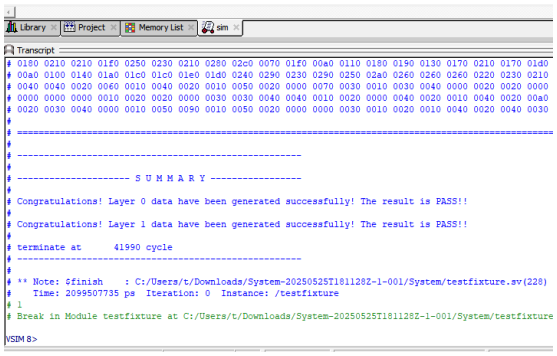
tb2:



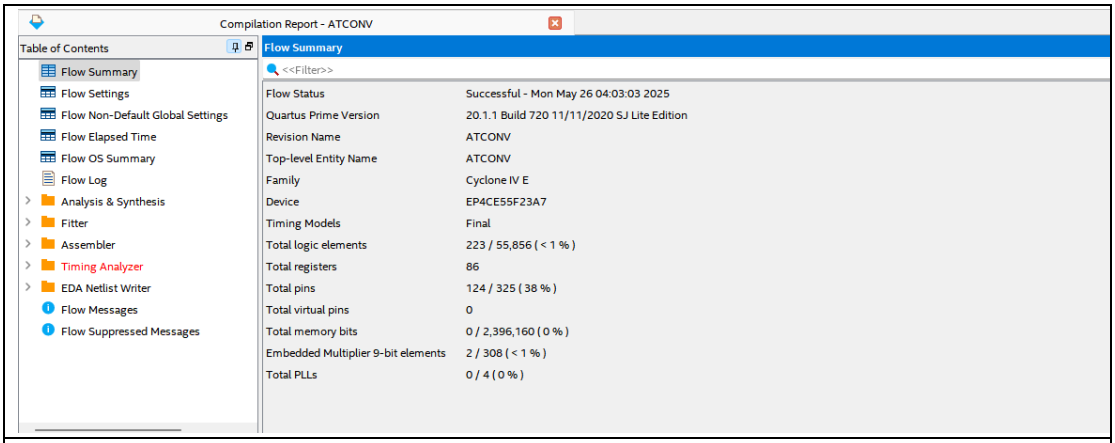
tb3:



tb3:

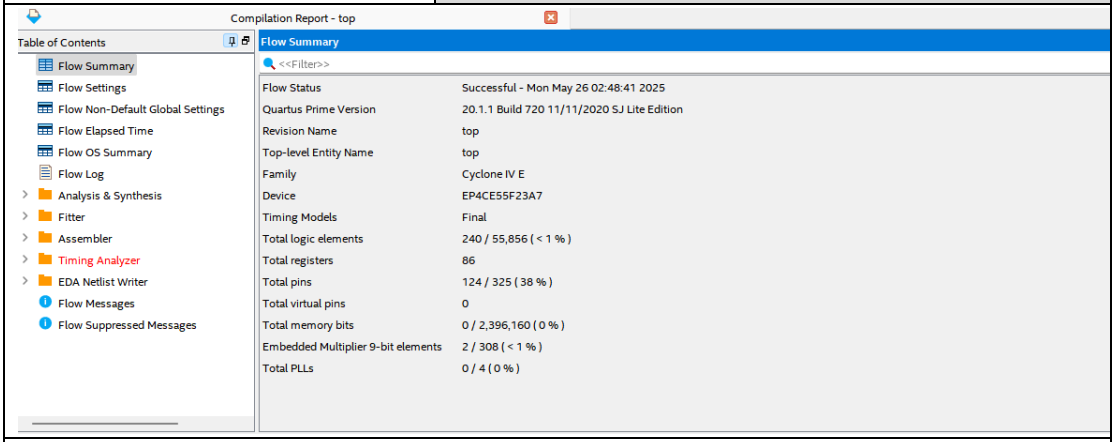


ATCONV Synthesis Result	
Total logic elements	223
Total memory bits	0
Total registers	86
Embedded multiplier 9-bit elements	2
Total Cycle used	41990



System Synthesis Result

Total logic elements	240
Total memory bits	0
Total registers	86
Embedded multiplier 9-bit elements	2
Total Cycle used	41990



Description of your design

基本上因為在 moodle 上助教說 bus 沒有規定 protocol，然後因為本次作業只有一個 master，所以我是讓 master 決定跟誰通訊，等於是 bridge 只是連線，我自己設計因為考量到 bus 的 bandwidth 所以是用一個乘加器來做卷積，然後我算卷積的順序剛好是 max_pool 的四個，因此每四次剛好也把 max_pool 結果算出，就不用再去重讀 layer0，所以變成說我的 SRAM 就只要被寫入，不會有讀取的動作，因此設計上是讓 master 要寫入 data 直接 broadcast 給 slave_1 跟 slave_2，地址也是直接 broadcast 給 slave_0 跟 slave_1 還有 slave_2，但寫入致能只有當 ID 對到會拉高，然後 ROM 的讀取致能直接給高，然後 master 讀資料因為只要讀 slave_0 的，所以直接把 ROM 資料接給 master 的讀通道就可。