Lab 8: I²C
(Inter-Integrated Circuit Bus)

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Outline

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- Hardware Description
  - I/O Information
  - System Information
- Simulation Result
- Criteria
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  - Deadline
  - Commands in Makefile
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Introduction

- Inter-integrated Circuit:
  - 讓嵌入式系統與周邊低速裝置溝通所發展的傳輸介面
  - 傳輸時由一個Master端與一個或多個Slave端完成

Introduction

- SCL:

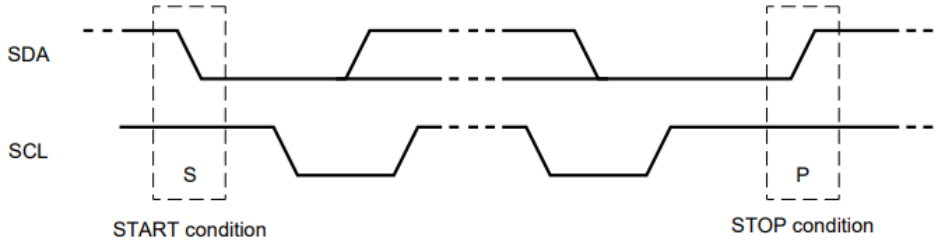
  Serial Clock Line, holds Clock signal (單向, Master to Slave)

- SDA:

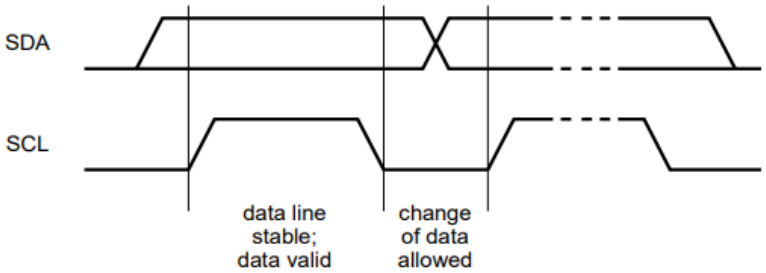
  Serial Data Line, holds Data or address signal (雙向)

Introduction

- I²C Operation
  - Start/Stop Condition
    - Start Condition: SCL=High時，SDA為negedge
    - Stop Condition: SCL=High時，SDA為posedge



  - SCL和SDA關係



    - 在SCL為0時，SDA可以改變資料
    - 在SCL為1時，SDA不能改變資料

    總結來說，在SCL拉起來前，SDA (Data) 要提前準備好

Introduction

- ACK/NACK
  - transmitter在傳輸byte時(這次的lab都是byte傳輸)，會主控SDA通道，在每個posedge SCL時傳送一個bit的資料；在第九個posedge SCL時，receiver主控SDA通道，進行ACK/NACK，ACK=1'b0, NACK=1'b1。
  - 承上，在write device, address, data時，master是transmitter，而slave是receiver；read data時，slave是transmitter，而master是receiver。
  - 以下為NACK的情況:
    1. No receiver is present on the bus with the transmitted address so there is no device to respond with an acknowledge.
    2. The receiver is unable to receive or transmit because it is performing some real-time function and is not ready to start communication with the controller.
    3. During the transfer, the receiver gets data or commands that it does not understand.
    4. During the transfer, the receiver cannot receive any more data bytes.
    5. **A controller-receiver must signal the end of the transfer to the target transmitter. (在這次lab，你會在波形上觀察到master會NACK給slave，中斷read data。)**

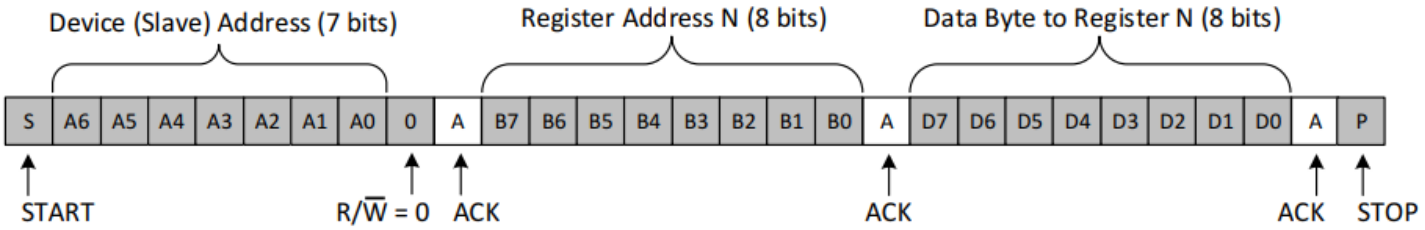
Introduction

Write Mode

Master Controls SDA Line

Slave Controls SDA Line

Write to One Register in a Device

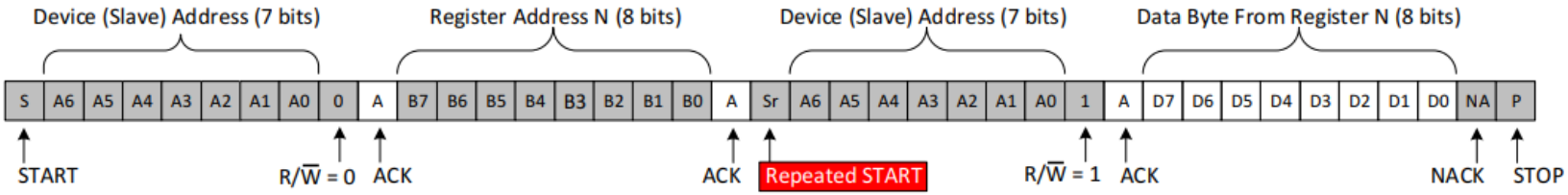


Read Mode

Master Controls SDA Line

Slave Controls SDA Line

Read From One Register in a Device



Hardware Description

■ I/O Information (i2c_slave.v)

Signal	I/O	Width	Description
clk	I	1	Clock signal
rst_n	I	1	系統重置訊號，為 active low
scl	I	1	i2c serial clock line
sda_i	I	1	i2c serial data line input (from master)
i2c_din	I	8	從 reg_bank 讀取的資料
sda_o	O	1	i2c serial data line output (from slave)
sda_o_en	O	1	i2c serial data line output enable (from slave)
wr	O	1	write enable = 1， 寫資料進reg_bank
rd	O	1	read enable = 1， 從reg_bank讀資料
i2c_addr	O	8	從reg_bank讀寫資料的address
i2c_dout	O	8	寫入 reg_bank 的資料

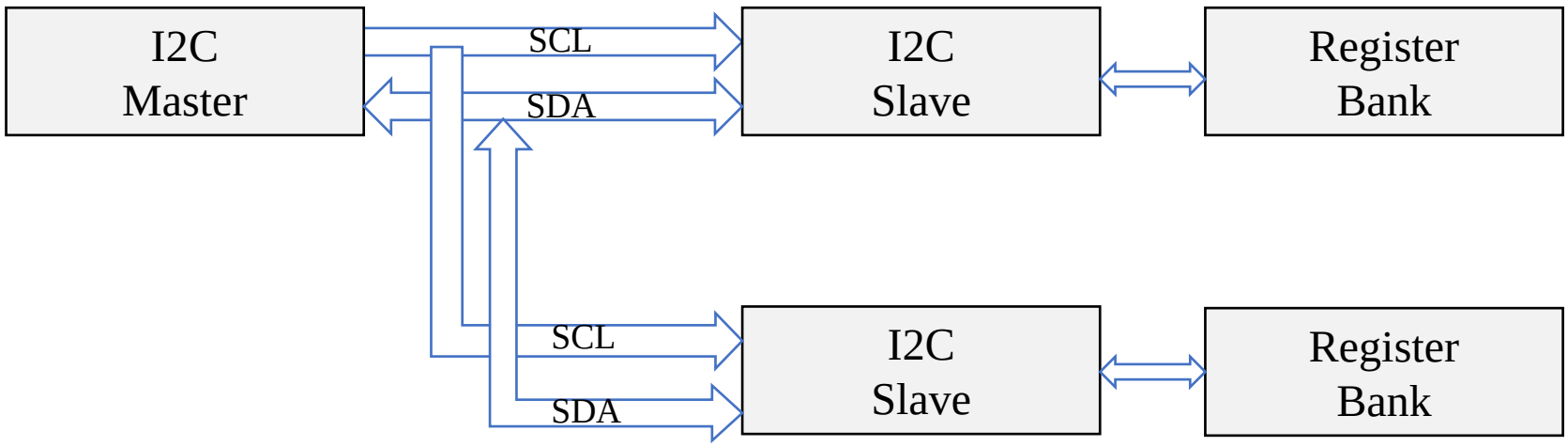
Hardware Description

■ I/O Information (host_reg_bank.v)

Signal	I/O	Width	Description
clk	I	1	Clock signal
rst_n	I	1	系統重置訊號，為 active low
wr	I	1	write enable = 1， 寫資料進reg_bank
rd	I	1	read enable = 1， 從reg_bank讀資料
i2c_addr	I	8	從reg_bank讀寫資料的address
i2c_dout	I	8	寫入 reg_bank 的資料
i2c_din	O	8	從 reg_bank 讀取的資料

Hardware Description

■ System Information



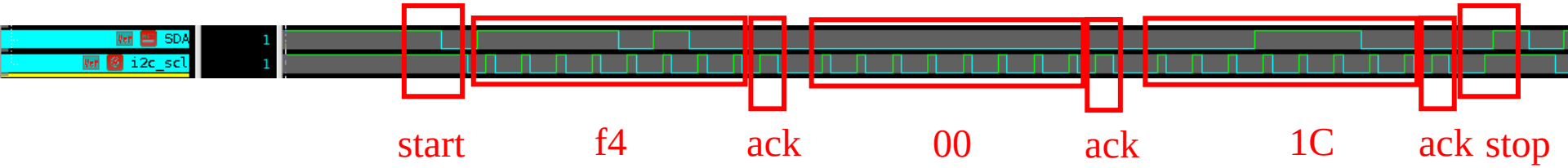
slave分別有其對應的address，相對應的slave必須負責ack給master。
address分別為7‘b111_1101和7’b111_1010，請自行分配。

Simulation Result

■ Write Mode

```
....Set value:1c to address:0........
device ID=f4 ack
sub addr =00 ack
write =1c ack
```

如果有not ack，需要修正



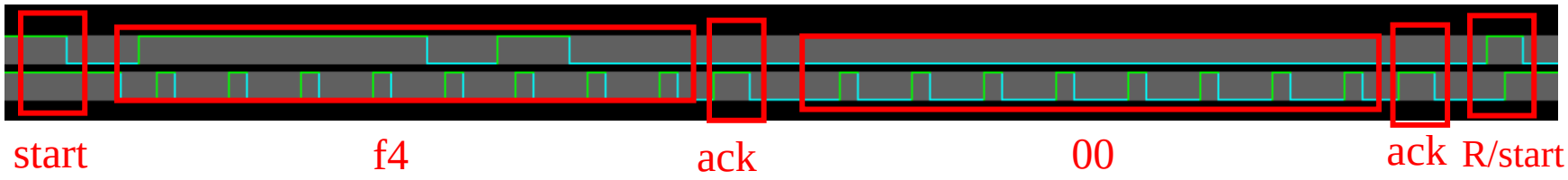
Simulation Result

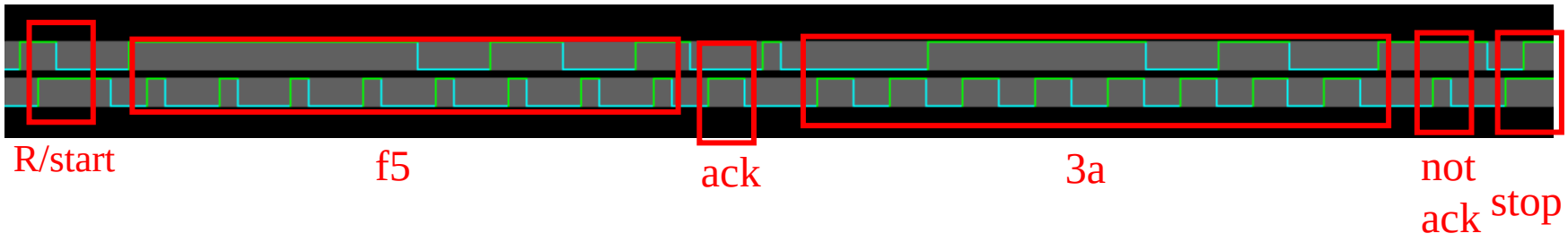
■ Read Mode

```
....Read data from address 0.......
device ID=f4 ack
sub addr =00 ack
device ID=f5 ack
read BYTE=3a
Master get data = 3a
Master not ack
....i2c read ok!!.....
```

如果有not ack，需要修正

必須為read ok才算成功





Criteria

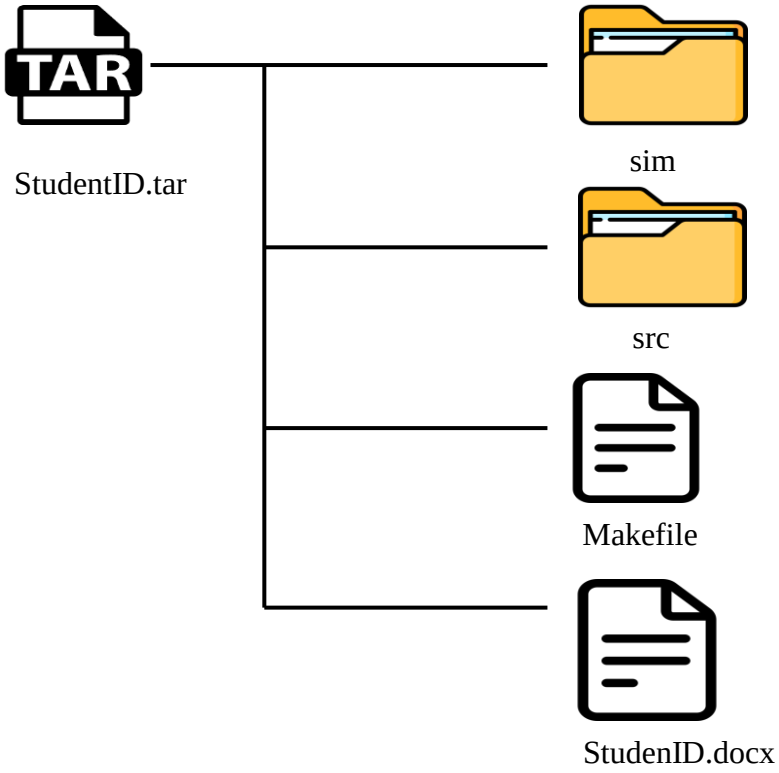
- Grading Policy (100%)
  - terminal結果和波形均正確 (100%)

Criteria

- Requirement & File Format
  - 請打開nWave，點選SDA和i2c_scl兩個訊號，並擷取Read/Write Mode下的波形，請如Simulation Result那邊的方式表示出來，終端機的結果只要擷取波形對應的片段即可，並且放到word裡。

Criteria

- Requirement & File Format



Criteria

- Deadline: 2025/05/20 (Tue) 14:00
  - Late submissions will receive a partial score as follow:
    - 1 day late -> 80 %
    - 2 day late -> 50 %
    - 3 day late -> 20 %
    - Over 3 days late - > 0 %

Criteria

- Commands in Makefile

Situation	Command
RTL simulation	make vcs
Dump Waveform (no array)	make vcs WV=1
Dump Waveform (with array)	make vcs WV=2
Launch nWave	make wave
Delete waveform files	make clean
Compress homework to tar format	make tar

Reference

- https://www.ti.com/lit/an/slva704/slva704.pdf
- https://www.nxp.com/docs/en/user-guide/UM10204.pdf