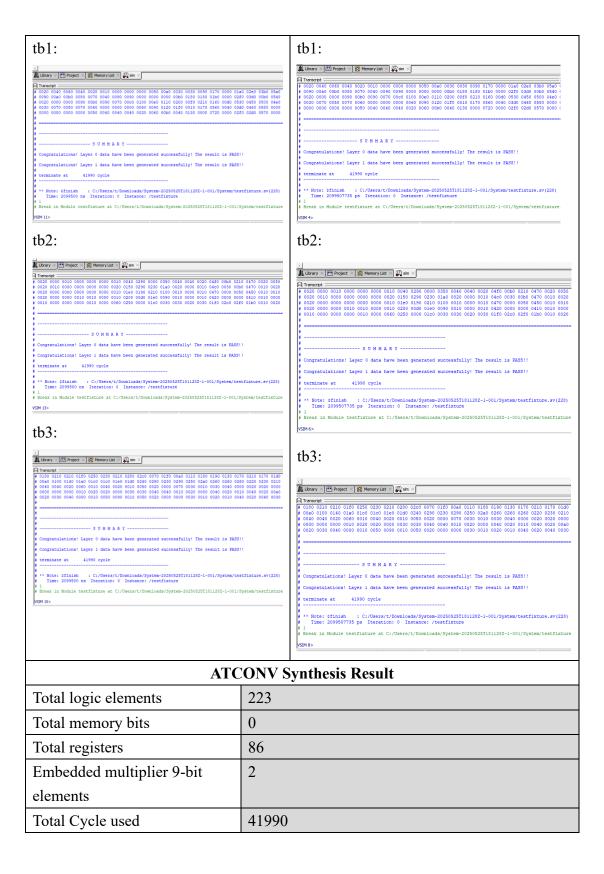
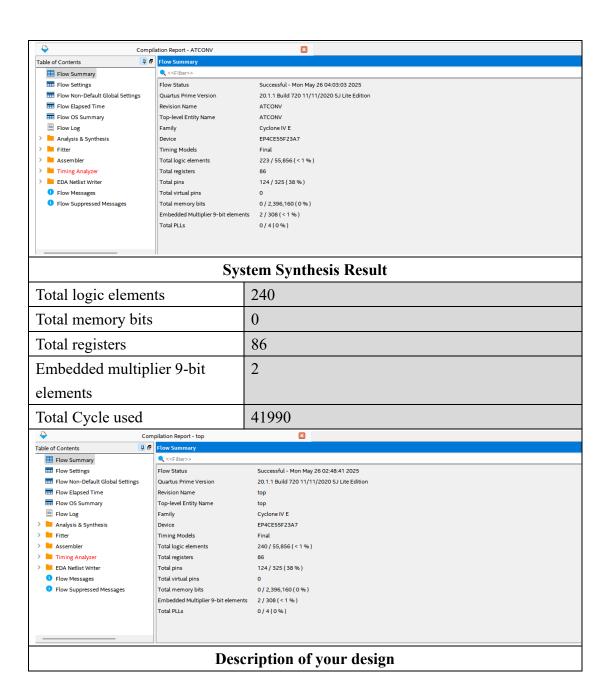
2025 Digital IC Design Homework 4

NAME	童品綸			
Student ID	M16131111			
ATCONV Simulation Result				
Functional		Pass	Pre-Layout	D
simulation			simulation	Pass
tb1:			tb1:	
# Congratulations! Layer 0 data Congratulations! Layer 0 data Congratulations Layer 0 data Congratulations Layer 1 data Transcopt Market Market Market Congratulations Layer 1 data ** Note: Sfinish C.7/Ber Time: 2095500 ns Tereatis Reak in Module testfixture Congratulations Layer 0 data Congratulations Layer 1 data	0 0000 0000 0 0 0000 0 0 0000 0 0 0 0	000 0050 0000 0010 0010 0010 0110 0100 0110 0200 01 000 0000 0	### SUBMERS STATE STATE	Particle Successfully! The result is PASS!! ATCONY/ATCONY/testfixture.sv(224) Ince: /testfixture Downloads/ATCONY/ATCONY/testfixture.sv line 2 Downloads/ATCONY/ATCONY/Testfixture.sv line 2 Downloads/ATCONY/ATCONY/Testfixture.sv line 2 Downloads/ATCONY/ATCONY/Testfixture.sv line 2 Downloads/ATCONY/Testfixture.sv line 2 Downloads/ATCONY/Testfixture.sv line 2 Downloads/ATCONY/Testfixture.sv line 3 Downloads/ATCONY/Testfixture.sv line 224 Downloads/ATCONY/Testfixture.sv line 3 Downloads/ATCONY/Testfix
			# Break in Module testfixture at C:/Users/t/Downloads/ATCONV/ATCONV/testfixture.sv line 224 VSDM 22>	
System Simulation Result				
Functiona	1	Pass	Pre-Layout	Pass
simulation	1		simulation	





基本上因為在 moodle 上助教說 bus 沒有規定 protocol,然後因為本次作業只有一個 master,所以我是讓 master 決定跟誰通訊,等於是 bridge 只是連線,我自己設計因為考量到 bus 的 bandwidth 所以是用一個乘加器來做卷積,然後我算卷積的順序剛好是 max_pool 的四個,因此每四次剛好也把 max_pool 結果算出,就不用再去重讀 layer0,所以變成說我的 SRAM 就只要被寫入,不會有讀取的動作,因此設計上是讓 master 要寫入 data 直接 broadcast 給 slave_1 跟 slave_2,地址也是直接 broadcast 給 slave_0 跟 slave_1 還有 slave_2,但寫入致能只有當 ID 對到會拉高,然後 ROM 的讀取致能直接給高,然後 master 讀資料因為只要讀 slave_0 的,所以直接把 ROM 資料接給 master 的讀通道就可。