Quick Start for VHDL Simulations using ModelSim

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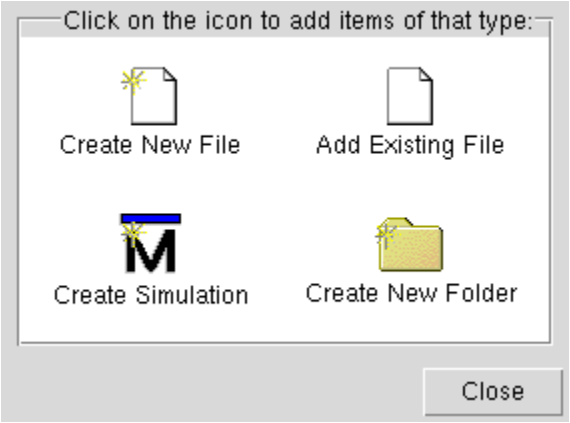
In the following, quick instructions are given to do a VHDL simulation using ModelSim. For more information use the ModelSim totorial manual. A restricted student version of ModelSim can be freely downloaded from the web pages of Mentor Graphics.

1. How to launch ModelSim:
   a) If you are working on the Linux PC's at HuCE-microLab, you can directly launch ModelSim from the icon menus, no preparation is necessary. In the Ubuntu **Menu** select **HuCE-microLab** and choose **HuCE-microLab – Mentor**. As an alternative, you can also launch ModelSim in a terminal window by typing the command **vsim**.
   b) If you are using your own Linux labptop with no local ModelSim installation, you can run ModelSim remotely on our server "xena":
      - open a terminal window and prepare your window for remote display by typing: **xhost +xena.bfh.ch**
      - login to xena: **ssh -X <yourname>@xena.bfh.ch**
      - copy the file **modlsim.ini** into your home directory
      - now you are ready to launch ModelSim by typing the **vsim** command into the terminal window.
2. How to simulate with ModelSim:
   a) First create a new project .
   b) Load your VHDL design files in the order from bottom up (lowest level first, …, testbench last) by the Add



   c) Compile your design and correct any syntax errors if present: **Compile → Compile All**
   d) You could interactively type waveform and stimuli commands into the console window of ModelSim in a script language. At the end of the session, all comands are stored in a local file called "transcript". As you might need several trial simulations until it runs, copy your "transcript" commands (and thus your complete test bench by manual editing the file) into a simulation macro file called **<your_design>.do** and launch it with **do <macro-file>** in the simulation console next time you launch the simulation.
   e) Start the simulation: **Simulate → Start Simulation …**
   In the appearing *Start Simulation* window select the **work** directory and then choose you top level testbench, close with **ok**. A new window with an empty simulation graph appeass.
   f) Now you can either graphically choose the signals you want to be visible for the simulation, or you make the selection textually. In case you want to see internal signals, like for example a *state* signal, then we have to choose them textually in the *sim* window by typing the command: **add wave /UUT/I_2/state** or something similar depending on your signal and hierarchy names. Add all necessary internal signal names for better debugging your design. You can run the simulation either graphically or textually (**run 5000000**). Be aware that the time units are by default ps.

g) When the simulation is finished, you can exit ModelSim and a new transcript file is generated showing your all your script commands. In case you want to use all action you have defined in this last simulation, then just copy the new transcript file (it might be in your home directory or your simulation directory, depending on how you launched ModelSim) to your **<your_design>.do** file. But be aware that you have to edit the simulation file **<your_design>.do** and at least remove the very last **quit** command, and mybe others as well.

h) To repeat the simulation, launch again ModelSim and directly run your new **<your_design>.do** script by typing do <your_design>.do into the Transcript window. In case you have changed your VHDL files, you need to re-compile it before running the script. Your simulation might look something similar as shown below (after fitting the screen to show the complete simulation):