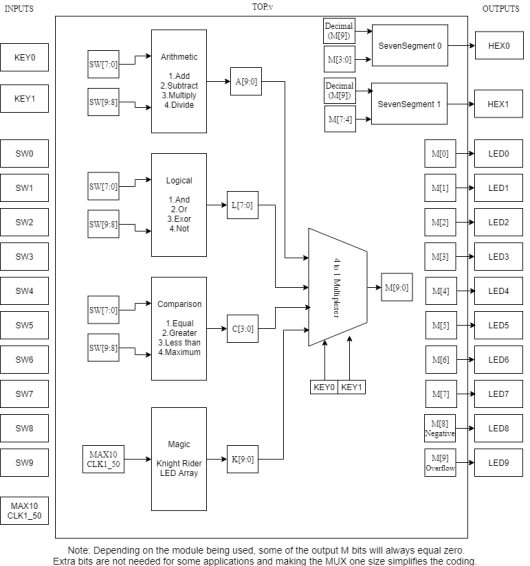
VHDL 4-bit Computer

Synthesis from PLT Class work

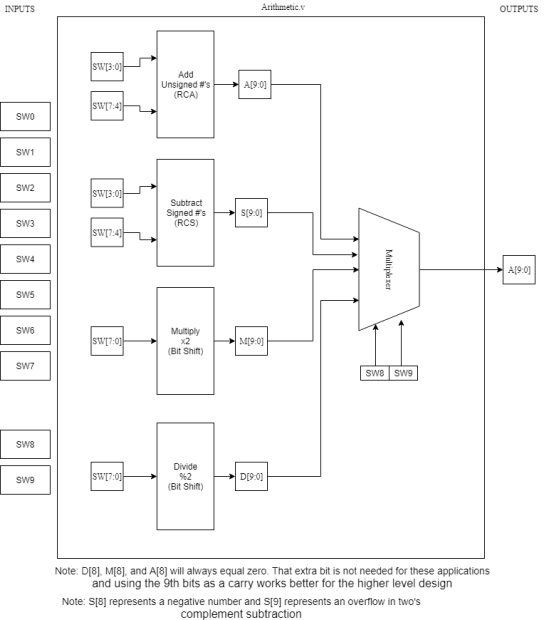
Revision 04

# Introduction

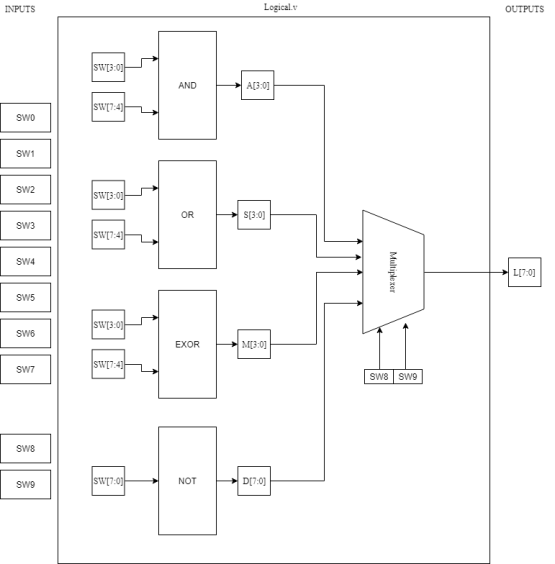
Using the tutorial from University of Colorado [1], we implement a 4-bit computer in VHDL. The overall system diagram is shown here, which relates to the top level entity, ‘computer\_4bit’. The system is implemented in VHDL on a DE10 Lite FPGA.



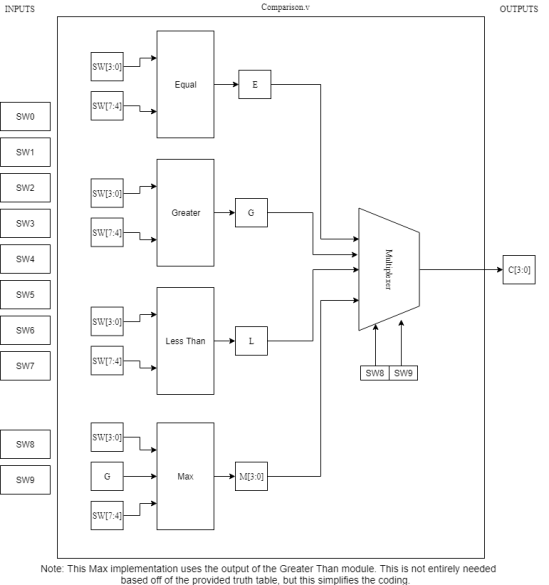
*Figure 1: The overall 4-bit computer with I/O of DE10 Lite*  [1]



*Figure 2: The structure of Arithmetic block with I/O of DE10 Lite*  [1]



*Figure 3: The structure of Logic block with I/O of DE10 Lite*  [1]



*Figure 4: The structure of Comparison block with I/O of DE10 Lite*  [1]

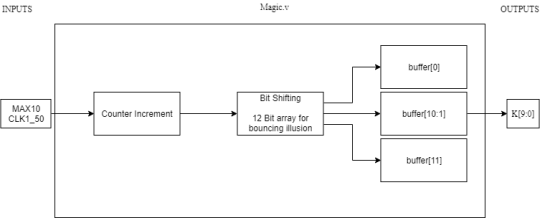


Figure 5: The structure of Magic block with I/O of DE10 Lite [1]

The system consisted of four activities: Arithmetic, Logic, Comparison and Magic (display). Key 0 and Key 1, the push buttons, set the activity to use and SW9 and SW8 set the individual operation within that activity.

For example, Setting Key0=1 and Key1=0 chooses the comparator. Setting SW9=0 SW8=0 chooses the equals operation on the comparator. The two 4-bit numbers SW3,2,10 and SW7,6,5,4 are compared for equal. The LEDs show the output result.

# Quartus Implementation

A new project was created called computer\_4bit with a top level entity of computer\_4bit. All the VHDL files in the project were added in the new project wizard (Add files). The 10M50DAF484C7G FPGA was chosen.

The project was compiled up with no errors.

The pins were assigned to the inputs and outputs shown in Figure 1.

A screenshot of a computer

Description automatically generated

A screenshot of a computer

Description automatically generated

The device was then programmed and tested using the different activities and operations.

# References (web only)

https://ryanzumbrunnen.wordpress.com/2018/03/04/4-bit-fpga-cpu/